

October 19, 2011

ELEN-474: Analog VLSI  
**Course Projects**

Preliminary report: Due on November 19, 2010. **It must be submitted electronically**

Final report: Due on December 7, 2010. **It must be submitted electronically**

10 minute Power Point presentation: December 12, 2010 9:10-10AM

**Policies:**

Project teams can consist of 1-3 students.

- Specifications and background. (5%)
- Search of existing solutions; use IEEExplore. (10%)
- Justify and define your architecture. (20%)
- Design and simulate your building blocks. (30%)
- Comparison of results (hand calculations and SPICE and/or spectre). (10%)
- Show the final results that proof your theory. (15%)
- Conclusions. (10%)

**Pay attention to all sections!**

After the project report exceeds 10 pages, usually the report size is inversely proportional to the quality of the results. Cover all the aforementioned issues, but please do not expend time discussing trivial or irrelevant stuff. In no more than 8 pages (you may have more pages due to the simulation results) you should be able to explain your work and be able to convince the instructor about the suitability of your approach. Please be clear and concise.

## Here is a list of potential projects, but feel free to suggest topics.

### Project #1. (High speed data converters)

Design a first-order switched-capacitor sample/hold and amplifier with closed-loop gain of 2 intended for pipeline ADCs. The sampling frequency will be 100 MHz, while the settling accuracy has to be better than 0.1%. The OTA must satisfy the following specifications:  $A_V > 50\text{dB}$ ,  $GBW > 250\text{ MHz}$  (to be confirmed), open-loop phase margin  $> 45$  degrees, in-band input referred noise level  $< 50\text{ uV}$ , and slew-rate  $> 250\text{ V/usec}$ . Use supply voltages of  $\pm 1.5$  Volts.

### Project #2 (Audio-Video applications, high-resolution (Sigma-Delta Modulators) data converters, high-performance filters).

Design a first order switched-capacitor filter with a unity gain frequency of 4 MHz and dc-gain of 0 dB. Probe the stability and the precision of the integrator. Use a clock frequency of 40 MHz. The amplifier must satisfy the following specifications:

$A_V > 80\text{ dB}$ ,  $GBW$  must be enough to achieve a settling error  $< 0.01\%$  within the integrating period, open-loop phase margin  $> 48$  degrees, input referred noise level  $< 50\text{ uV}$ , and output voltage swing  $> \pm 0.6\text{ V}$ . Use supply voltages of  $\pm 1.5$  Volts.

### Project #3 (Extremely high-frequency applications, Wireless, Continuous-time filters).

Design a second order LP-BP OTA\_C filter. The resonant/center frequency must be 100 MHz, quality factor of 10, pass-band gain = 0 dB. The basic integrator must also satisfy the following requirements: DC gain  $> 40\text{ dB}$ , excess phase at 100 MHz  $< 2$  degrees, input referred noise level  $< 100\text{ uV}$ . The maximum input signal amplitude is 100 mV, and the THD  $< -50\text{ dB}$ . Use supply voltages of  $\pm 1.5$  Volts.

### Project #4 (Extremely high-frequency applications, Wireless, optical fiber, read channel, instrumentation).

Design a variable gain amplifier such that the voltage gain can be varied in more than one decade (1-10). The -3 dB bandwidth must be greater than 200 MHz, and linearity better than 1%; minimize both power consumption and silicon area. Use supply voltages of  $\pm 1.5$  Volts.

### Project #5 (Instrumentation).

Design an operational amplifier similar to the 741.  $A_V \geq 106\text{dB}$ ,  $GBW = 1.2\text{ Mhz}$ , slew-rate  $> 1\text{ uV/sec}$  for a load capacitor of 10pF, output swing  $> \pm 0.6$  volts. Use supply voltages of  $\pm 1.5$  Volts; explore the possibility of using class AB output stage.

### Project #6 (Optical fiber communications, transimpedance amplifiers).

Design a low-noise preamplifier for a photodiode that produces an ac current in the range of 0.1-5 microamps; photodiode's output impedance is modeled by a 0.25 pF capacitor. The frequency response must be larger than 1 GHz, and the trans-impedance gain = 60 dB; phase response should be linear; check your group delay. The output impedance of the preamplifier should be less than 200 ohms. Use supply voltages of  $\pm 1.5$  Volts.

### Project #7 (Line drivers for Flat panel devices)

Design a 3 V rail to rail amplifier ( $v_{out}$  should cover  $> 90\%$  of the supply range). Load capacitor varies from 5-150 pF, and static current consumption must be less than 1 uA. This is a nice and challenging problem; stability is the main issue, especially because the huge load variation. Other design parameters will be discussed later. Use supply voltages of  $\pm 1.5$  Volts.

### Project #8 (High-Q Switched-capacitor filter: High frequency applications, IF filters).

Design a second-order bandpass switched-capacitor filter with a center frequency of 10 MHz and peak gain of 0 dB. Use a clock frequency of 64 MHz. The OTA must satisfy the following specifications:  $A_V > 50\text{ dB}$ ,  $GBW > 100\text{ MHz}$ , open-loop phase margin  $> 45$  degrees, input referred noise level  $< 50\text{ uV}$ . Use supply voltages of  $\pm 1.5$  Volts.

### Project #9. (Medical instrumentation and continuous-time filters)

Design a fully-programmable continuous-time bandpass filter with low-frequency corner from 0.5 Hz up to 10 Hz and the high frequency corner adjustable from 1-50 Hz. The SNR for the filter has to be better than 50 dB. Use supply voltages of  $\pm 1.5$  Volts.

**Project #10. (RF circuits)**

Design a fast high gain multistage amplifier for data communication applications. Gain must be  $> 20\text{dB}$ , for an overall load capacitor of  $1\text{ pF}$ ; frequency bandwidth must be better than  $1\text{ GHz}$ ; compensate for differential DC offsets; low frequency corner must be smaller than  $1\text{ MHz}$ . Minimize power consumption.

**Project #11. (Biomedical interface)**

Design a first order low-pass sigma delta ADC with  $>60\text{ dB SNR}$  for glucose meters. Specifications and architecture will be discussed with the instructor. Overall static power consumption must be  $< 1\mu\text{W}$ .

**Project #12. (Power Management)**

Design a capacitor-less linear regulator. Specifications and architecture have to be discussed with the instructor. Overall ground power must be  $< 10\mu\text{W}$  in standby condition and settling time  $< 1\mu\text{sec}$ .

**Your project suggestions are more than welcome!**