ECEN 474: (Analog) VLSI Circuit Design

Fall 2011 MWF 9:10-10:00, ZACH 223B http://www.ece.tamu.edu/~hoyos/ecen474.html

Instructor:	Sebastian Hoyos
Office:	315-D WERC
Office Hours:	MW 10:30-12:00
Phone:	862-4253
E-mail:	hoyos@ece.tamu.edu

Prerequisite: ECEN 326

Textbook: Design of Analog CMOS Integrated Circuits, B. Razavi, McGraw-Hill, 2001.

References:

- 1. *Analysis and Design of Analog Integrated Circuits*, P. Gray, R. Meyer, P. Hurst, and S. Lewis, John Wiley and Sons, 4th Edition, 2003.
- 2. Technical Papers

Class Notes: Posted on the web and will hand out hard copies in class

Objectives: At the end of this course, students be able to

- 1. To discuss basic transistor models and layout techniques for design and characterization of analog integrated circuits.
- 2. To study the most important building blocks in CMOS technologies and understand their advantages and limitations.
- 3. To design basic analog IC circuits considering practical parameters.
- 4. To use the IC design tools, especially Cadence, Spectre, Spice, and Matlab.
- 5. We expect to design and fabricate some projects at the end of the semester.

Grading: • Ex

- Exams
 - Three Midterm Exams (20% each)
 - Closed book
 - One double sided 8.5x11 note sheet allowed

60%

- No make-up exams except for university excused absences
- No Final Exam
- Homework 10%
 - You are encouraged to work together with your colleagues on the homework. However, each student must turn in an independent write-up.
 - Due at beginning of class
 - No late homework will be graded
- Laboratory
- Final Project 10%
 - o Report and PowerPoint presentation required

20%

Grading Policy*:

Letter Grade	x = Your Average
А	$x \ge 90.00$
В	$89.99 \ge x \ge 80.00$
С	$79.99 \ge x \ge 70.00$
D	$69.99 \ge x \ge 60.00$
F	$59.99 \ge x$

*This is the lowest grade that you are guaranteed for your raw average, x. Depending on the relative performance of the class, your grade **MAY** be adjusted higher. **Undergraduate and graduate students'** performance will be judged independently.

Outline

- I. Introduction and MOS models
 - Basis of CMOS Technology
 - Basic equations for the MOS transistor
 - Model level 3
 - Second order effects
 - SPICE parameters
 - Technology characterization
- II. CMOS Technologies and Layouts
 - CMOS technology
 - CMOS Layout and Design Rules
 - Layout considerations (transistors, capacitors, resistors and inductors)
 - Latch-up considerations
 - Advanced technologies: design examples
- III. Current Mirrors and Differential Pairs
 - Basic amplifier
 - Ideal and Basic current mirror
 - Basic amplifiers using current mirrors (design considerations, and evaluation techniques)
 - High-output impedance current mirrors
 - High dc gain amplifiers (cascode, folded-cascode, triple cascode, and regulated cascode)
 - Current mirror characterization techniques (DC and AC)
 - Differential pair
 - Frequency response
 - Noise considerations
 - Class AB amplifiers
 - Design examples

IV. Voltage References and Differential Pairs (* most of this material is taken from Gray's book)

- Supply independent current sources (*)
- Bootstrap Biasing (*)
- Temperature coefficient (*)
- Bandgap references (*)

- Differential Pair (large signal characteristics)
- Differential Pair (small signal characteristics)
- Frequency response (dc gain, poles and zeros)
- Node impedances, low-frequency and high-frequency poles
- Design examples
- V. OTA Design
 - First stage
 - DC considerations
 - AC considerations
 - Noise considerations: Output and input referred noise
 - Global design strategy
 - Three Current Mirror OTA
 - Cascode output stages
 - Telescopic amplifier
 - Folded-cascode OTA
 - OTA characterization

VI. Design of a Miller OPAMP

- First stage
- Output stage
- DC considerations
- Stability considerations
- Settling time and slew-rate
- DC offset and PSRR
- Noise considerations
- Design strategy

VII. Advanced Techniques

- Enhanced output stages
- Fully-differential structures
- Common-mode feedback: limitations and design techniques
- Phase compensation techniques
- Linear OTAs: Continuous-time circuits
- Linearization techniques: IM3 and Source degeneration
- Tuning techniques
- Design examples

Preliminary Schedule*

Торіс		Week
I.	Introduction and MOS models	Weels 1.4
II.	CMOS Technologies and Layouts	Week 1-4
	Review Session	Sep. 28
	1 st Exam	Sep. 30
III.	Current Mirrors and Differential Pairs	
IV.	Voltage References and Differential Pairs	Week 5-9
V.	OTA Design (Part 1)	
	Review Session	Nov. 2
	2 nd Exam	Nov. 4
VI.	OTA Design (Part 2)	
VII.	Miller OpAmp Design	Week 10-14
VIII.	Advanced Topics	
	Review Session	Nov. 30
	3 rd Exam	Dec. 2
	Project Report Due	Dec. 7
	Project Presentation	Dec. 12

*Exam dates are approximate and subject to change with reasonable notice.

Laboratory safety guidelines will be distributed at the beginning of the semester, they are to be reviewed, filled out, and turned back to the department.

Americans with Disabilities Act (ADA) Policy Statement:

The Americans with Disabilities Act (ADA) is a federal anti-discrimination statute that provides comprehensive civil rights protection for persons with disabilities. Among other things, this legislation requires that all students with disabilities be guaranteed a learning environment that provides for reasonable accommodation of their disabilities. If you believe you have a disability requiring an accommodation, please contact the Department of Student Life, Services for Students with Disabilities, in Room 126 of the Koldus Building or call 845-1637.

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Honor Council Rules and Procedures: http://www.tamu.edu/aggiehonor

Build the Hell Outta Analog VLSI Circuits!

