

ECEN-610: Mixed-Signal Interfaces

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Assignment # 4

1. A 200mV rms value sinusoidal signal is applied to an ideal 12 bits ADC. The full range peak-to-peak voltage of the ADC is 1.2V.
 - a. Find the SNR of the ADC output.
 - b. Now the input sinusoidal is full range but comes with an additive Gaussian noise with standard deviation of 0.5 V. What is the SNR of the input signal? What is the SNR of the ADC output bits?
 - c. Repeat b assuming that the noise added to the sinewave is uniformly distributed with peak-to-peak value of 1V.
2. Assume that an ADC uses an oversampling factor $K=fs/(2B)$, where fs is the sampling rate and B is the signal bandwidth. Then $K=1$ is Nyquist rate and $K>1$ means oversampling. The quantization noise variance is $\sigma_e^2=\Delta^2/12$ as we defined in class for the additive noise model. As you may recall also, this noise is uniformly distributed and white, i.e. is flat in the frequency range $[0 fs/2]$. Then the noise power spectral density will be σ_e^2/fs , so the integral in the range $[-fs/2 fs/2]$ is σ_e^2 . Now assume that a perfect low-pass filter is used that selects the signal bandwidth B and rejects all the out of band noise. Find an expression for the output SNR of this oversampled ADC+low-pass filter combination.
3. A 3-bit D/A converter were designed for an ideal LSB level of 100 mV. The following output voltages levels were measured for the real D/A for three codes 000 to 111 respectively: -0.01V 0.105V 0.195V 0.28V 0.37V 0.48V 0.6V 0.75V
 - a. Find the offset & full-scale error in units of LSBs
 - b. Find the end-point ideal & actual gain in LSB/code and compute the gain error in LSB/code
 - c. Find the end point corrected codes and compute DNL & INL for all the codes.
 - d. What is the maximum DNL and INL?

Hint: I suggest you take a look at the following article in case of you have questions for this problem:
<http://focus.ti.com/lit/an/slaa013/slaa013.pdf#search=%22understanding%20data%20converters%20%22>
4. A ramp histogram is used to characterize a 4-bit ADC, the following vector is found:
283 115 85 101 122 170 75 146 125 60 95 95 115 40 120 242
I suggest you do this in Matlab:
 - a.) Calculate the DNL and INL
 - b.) What are the peak DNL and INL values?
 - c.) Is this ADC monotonic?

Hint: Recall that you use as a reference the straight line that connects the end points of the transfer function provided by the histogram. This is needed to eliminate offset errors and full scale errors. There is a trivial way to eliminate these errors. How?

5. The end point DNL for a 3-bit ADC is measured to be:
DNL: 0 -0.5 0 +0.5 -1 +0.5 +0.5 0 (all numbers in terms of LSB)
 The ADC exhibits offset and full-scale error:

Offset error = +0.5LSB

Full scale error = +0.5LSB

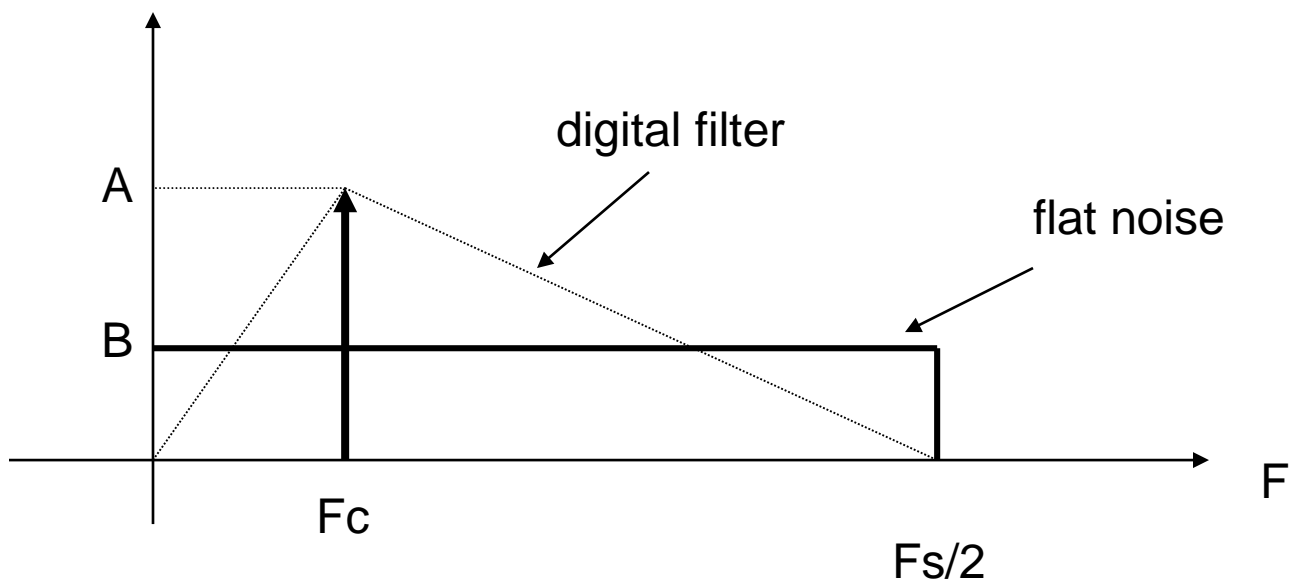
- a) Find the INL for this ADC
- b) Draw the transfer curve of this ADC.

6. A tone at frequency F_c is sampled at frequency F_s and quantized with N bits. The resulting quantization noise is white (flat in frequency, see the figure).

- a. (5%) What is the peak (full scale) signal to quantization noise ratio SQNR(dB)?
- b. (25%) Assume that an L point DFT of the sampled tone is calculated and plotted in a linear scale. Assume that resultant noise floor is perfectly flat. From the range $[0 \pi]$ of the DFT plot, the linear SNQR is calculated as the power of the sinewave frequency bin divided by the power of all the other bins. What is the height difference in dB between the sinewave frequency bin and the noise floor?
- c. (5%) What are necessary conditions in the previous problem for the DFT noise to be flat? Are these conditions sufficient for the noise to be completely flat?
- d. (25%) The digital filter shown in the figure is used to filter out the signal from the quantization noise. What is the SNR at the output of the filter?

7.

Amplitude



Consider the preamplifier/latch topology below.

- Please explain the circuit dynamics for Φ_1 and $\overline{\Phi_1}$. Clearly indicate the region of operation of the transistors (i.e., OFF, triode, saturation)
- Find an expression of the input vs the output that takes into account the gains and the positive regeneration of the circuit.
- Explain the advantages and disadvantages between dynamic and static latches?
- Is this latch a static, dynamic or a semi-dynamic latch? Why?

