ELEN 689:Special Topics
Advanced Mixed-Signal Interfaces

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Texas A&M University
Analog and Mixed Signal Group

Administrative

- Instructor: S. Hoyos, 315D WERC, hoyos@ece.tamu.edu.
- TA: Srikanth Pentakota #14, 114 WERC .
- Website: www.ee.tamu.edu/~hoyos. All lecture notes and handouts will be posted here.
- Time & Place: TR 3:55 PM to 5:10 PM ENPH 213
- Office Hour: TR 11:00 AM to 12:00PM.

Prerequisites

- Signal processing background:
  - **Digital and Statistical Signal Processing**
- Analog circuit design background:
  - **Analog Integrated-Circuit Design**
- Digital circuit design background:
  - Basic gate-level logic design knowledge is enough.

Course Materials

- Textbook: No textbook required.
- References reserved at the Library:
  1. **IEEE Transactions Journals and Conferences Papers**
  2. **Analog MOS Integrated Circuits for Signal Processing**, Wiley, 1986
     by Gregorian and Temes.
  2. **Principles of Data Conversion System Design**, IEEE Press, 1995
     by Razavi.
  3. **CMOS Integrated A/D and D/A Converters**, Kluwer, 2003
     by van de Plassche.
  4. **Delta-Sigma Data Converters: Theory, Design, and Simulation**, Wiley, 1996
     by Norsworthy, Schreier, and Temes.
  5. **Analysis and Design of Analog Integrated Circuits**, 4th Ed., Wiley, 2001
     by Gray, Hurst, Lewis, and Meyer.
- Readings: Will be posted on the course website.

CAD Tools

- Class accounts.

  For questions, contact Manager: Wayne Matous 25 ZEC
- CAD Tools required:
  - **MATLAB, Simulink**
    Mixed-domain behavioral modeling, analog/digital filter synthesis, and etc.
  - **Cadence:** GUI suite for design entry, layout, waveform display, and etc.
    - **Spectre RF**
      SPICE-type analyses: .dc, .ac, .xf, .noise, .tran, and etc.
      Additional capabilities: pss, pac, pxf, pnoise, pdisto to analyze large-signal nonlinear circuits (e.g., switched-capacitor circuits, RF circuits).
    - **Eldo**: For transient noise analysis.

Grading

- Homeworks: 15% Biweekly
- Lab: 10%
- Project 1: 15%
- Midterm : 20% In class.
- Final Project: 20% Assigned after midterm.
- Proj. Presentation: In class.
- Final Exam: 20% University schedule

Grading Policy: Discussion with classmates is encouraged but projects that are alike won't receive credit.

Course Outline

1. Transmitters (Nyquist rate DACs, Oversampled DACs, Mixers, Filtering)
2. Receivers (LNAs, Mixers, Antialiasing Filters, Nyquist rate ADCs, Oversampled ADCs)
3. Digitally Assisted Transceivers (Calibration Techniques)
4. Applications on Communication Standards (BlueTooth, GSM, EDGE, WIMAX, UWB)
5. Software Defined Radios
6. Cognitive Radios

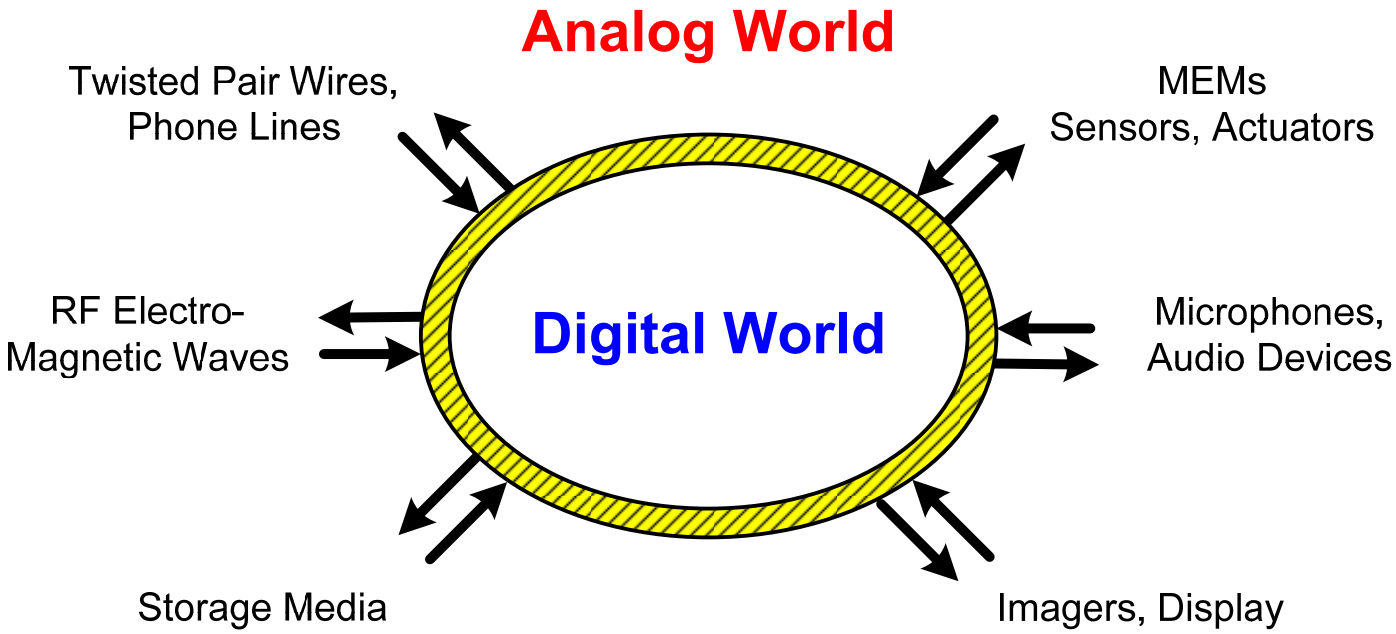
Methodology

- Every lecture will cover a group of papers plus some of the fundamental concepts needed to understand the contributions in the referred papers.

- The papers will be selected from the latest contributions to the state of the art. One of the main goals will be to understand which issues are addressed and why the previous topologies or techniques failed to tackle that issue.

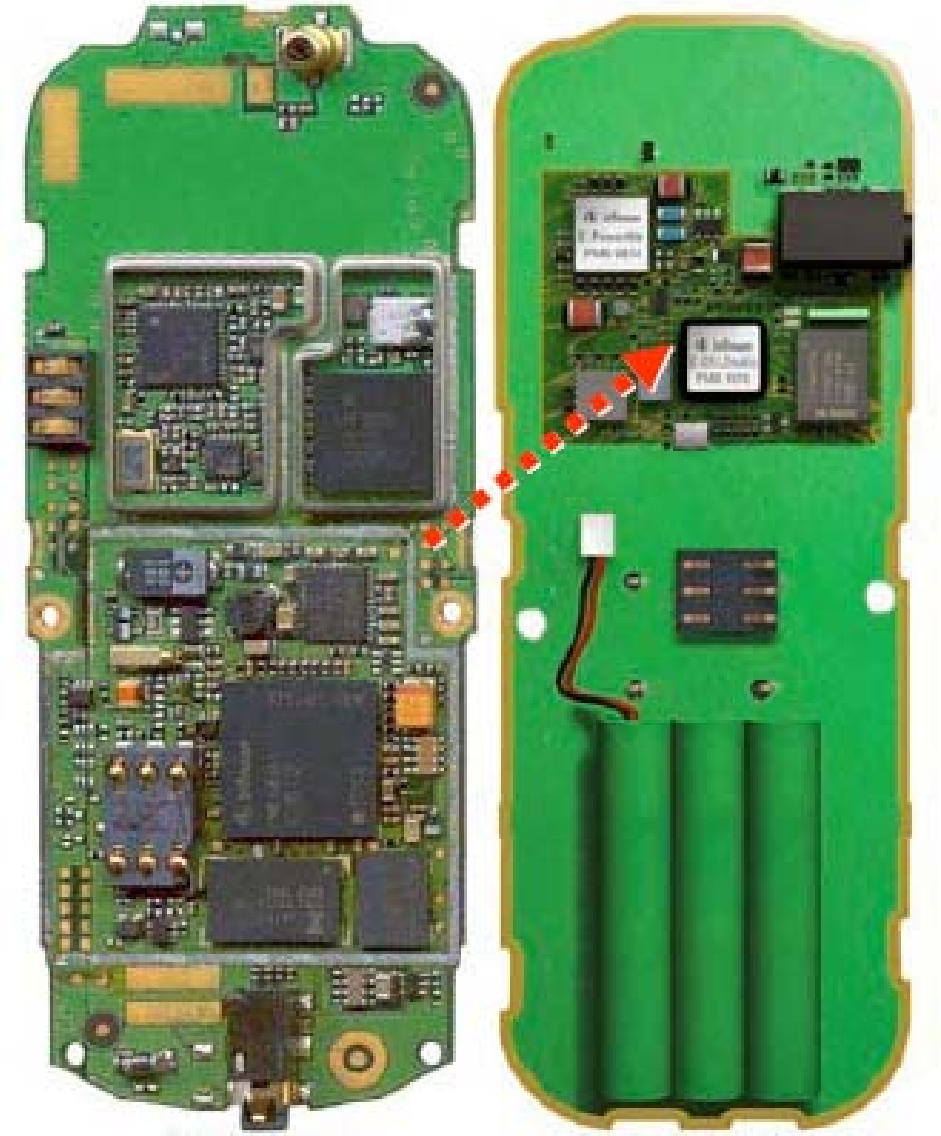
- The students will be encouraged to investigate new and improved techniques.

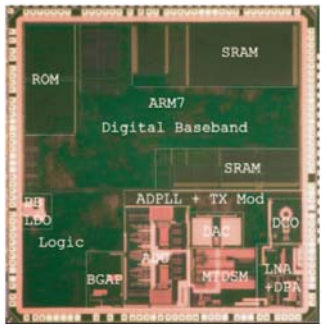
Why Mixed-Signal Interface?



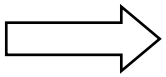
- Nature is analog, not digital.
- Mixed-Signal interface's role is "translator".

Why CMOS?





- TI Bluetooth SoC 2005 ~ 7 mm²
- Just 20% of SoC is RF/analog. Rest is digital logic and memory.

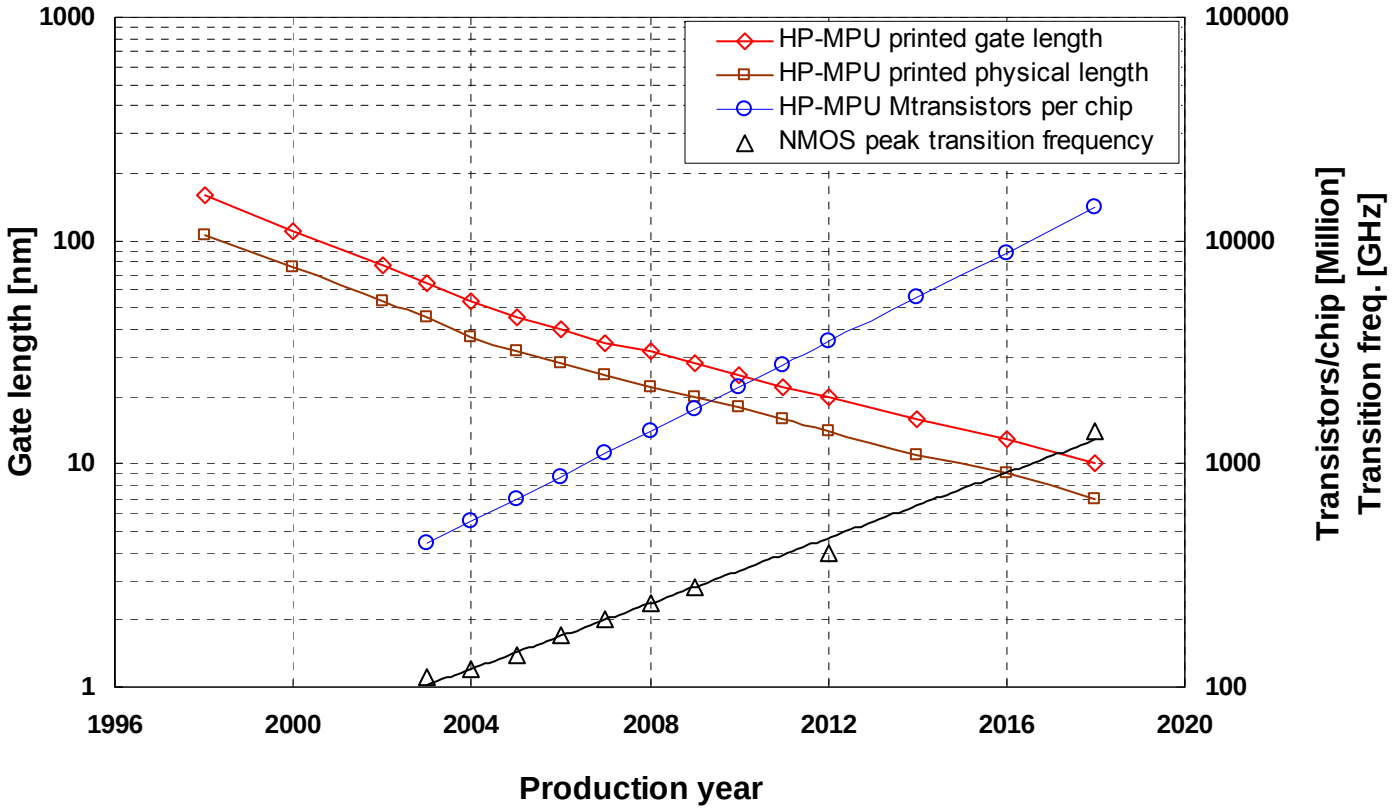


Desired features:
- Low cost
- Low power
- High integration
- Single chip radio

Digital Signal Processing

- Noise immunity, robustness.
- Unlimited precision or accuracy.
- Flexibility, programmability, and scalability.
- Electronic design automation (EDA) tools widely available and successful.
- Benefiting from **Moore's law** – "The number of transistors on a chip doubles every 18 months," *IEDM*, 1975.
  - Cost/function drops 29% every year.
  - That's 30X in 10 years.

2004 ITRS Silicon Technology Trend



Ref: ITRS website http://public.itrs.net/

Analog Signal Processing

- Sensitive to noise – SNR (signal-to-noise ratio).
- Subject to device nonlinearities – THD (total harmonic distortion).
- Sensitive to device mismatch and process variations.
- Difficult to design, simulate, layout, test, and debug.
- Inevitable, often limits the overall system performance.
- Scaling scenario:
  - Enjoyed scaling until ~0.35-μm technology node.
  - High-speed, low-resolution ADCs keep benefiting.
  - High SNR design difficult to scale with low supplies (≤ 3.3V).

Example1: Communication Transmitter

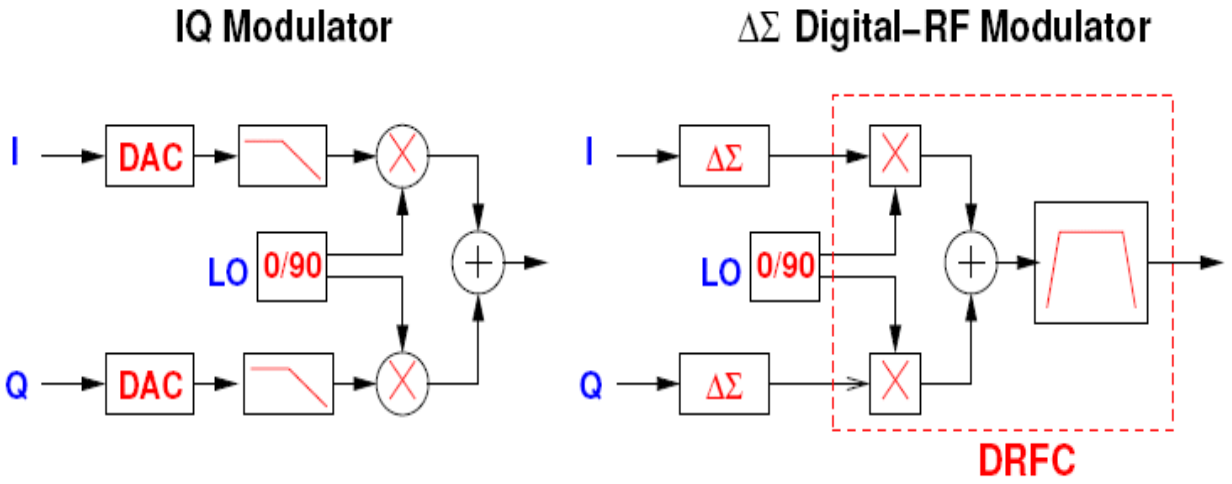
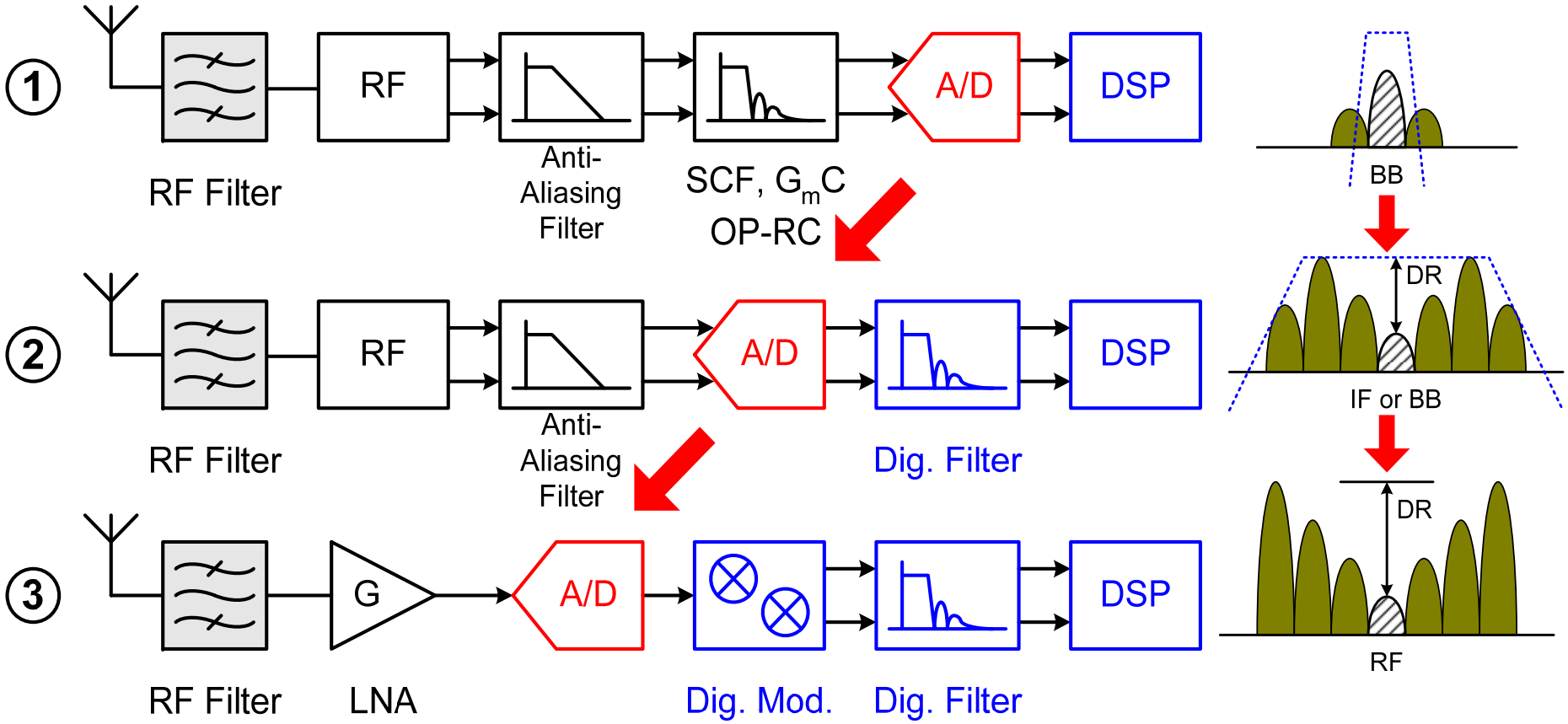


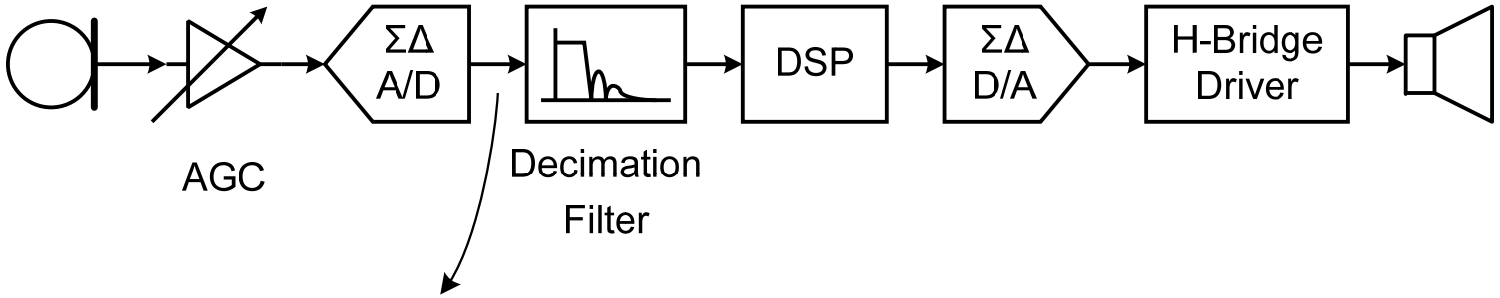
Fig. 1. Conventional and Proposed Modulator Architectures

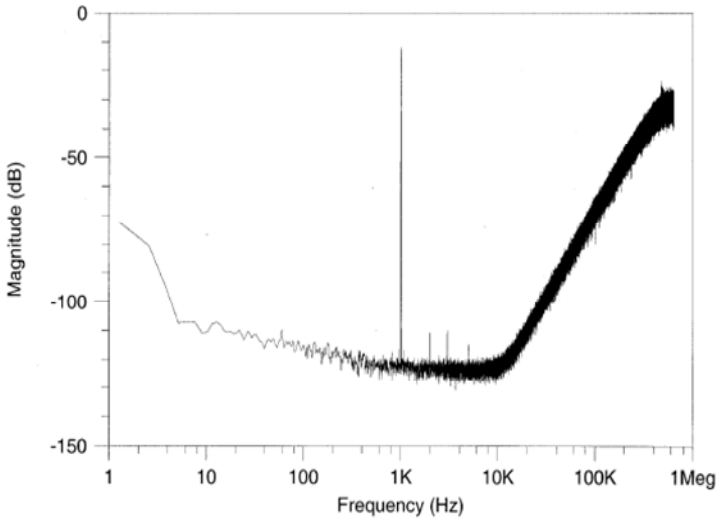
A. Jerng, and C. G. Sodini, “Wideband ΔΣ Digital-RF Modulator for High Data Rate Transmitters”.

Example 2: Communication Receiver



Example 3: Mixed-Signal Hearing Aid

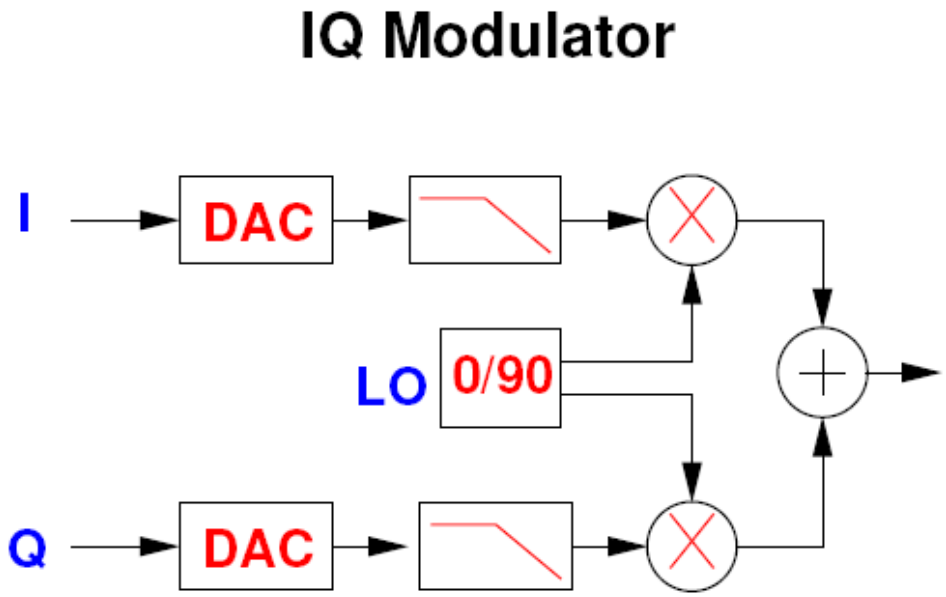




Ref: D. G. Gata, "A 1.1-V 270-μA mixed-signal hearing aid chip," *JSSC*, pp. 1670-8, Dec. 2002.

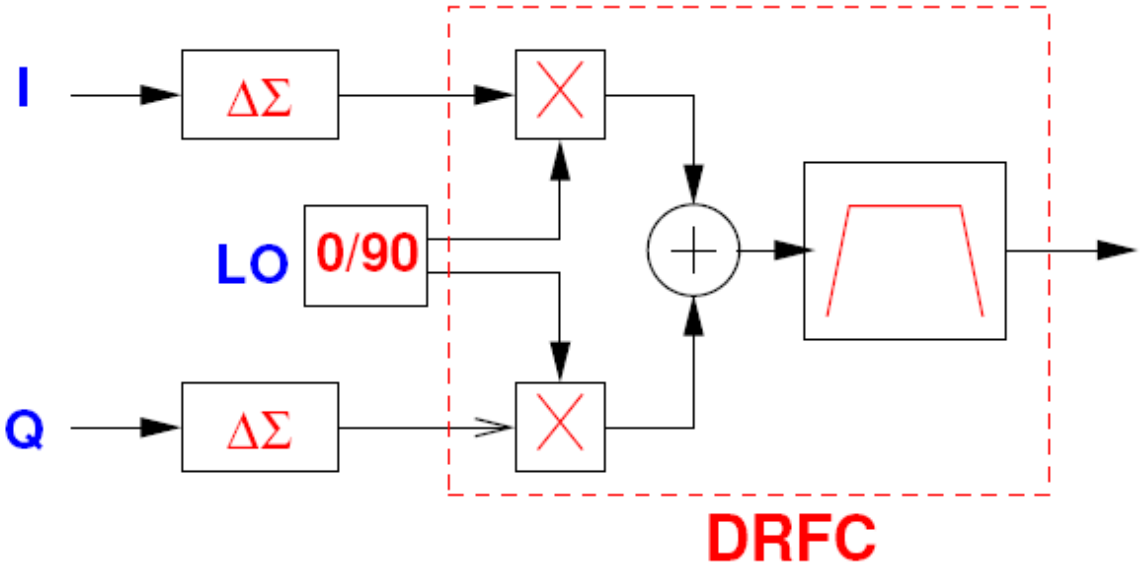
ΣΔ Modulator and Transmitter

Conventional IQ Modulator



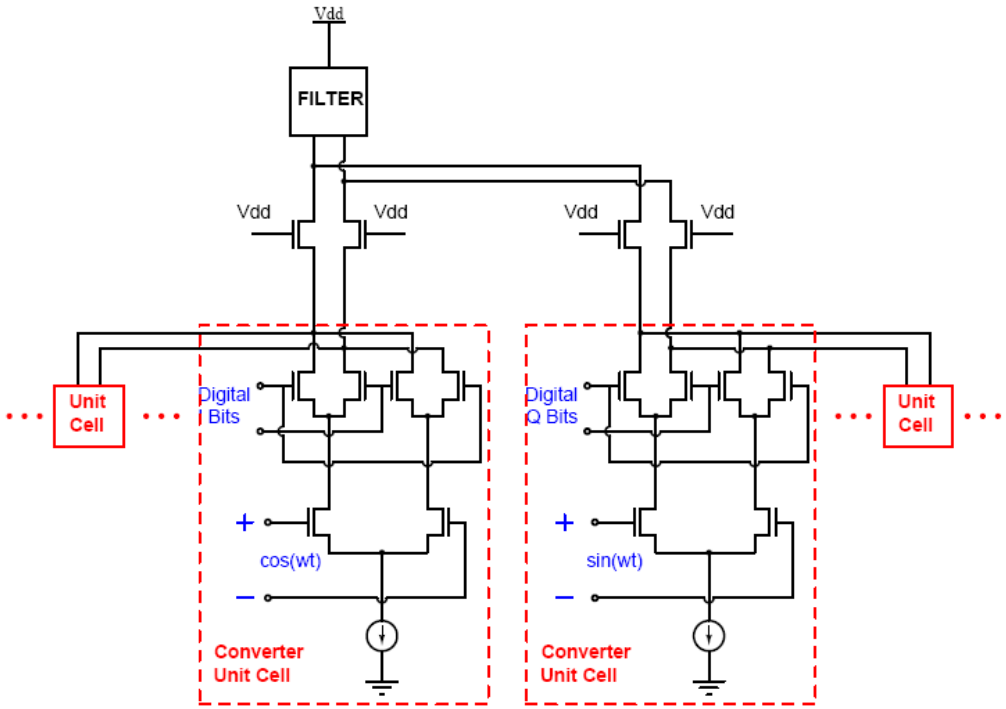
- DAC, analog filter and analog mixer. DAC and analog filter more difficult to design as bandwidth and number of bits increase.
- Problems: Timing errors, non-linear capacitances, IQ mismatches, DC offsets cause modulator image and LO leakage signals.
- Problem: Transmission of spurs outside signal band which are difficult to filter out at RF frequencies. Clock images and quantization noise is upconverted. Need better filtering that just sinc of zero-order-hold.

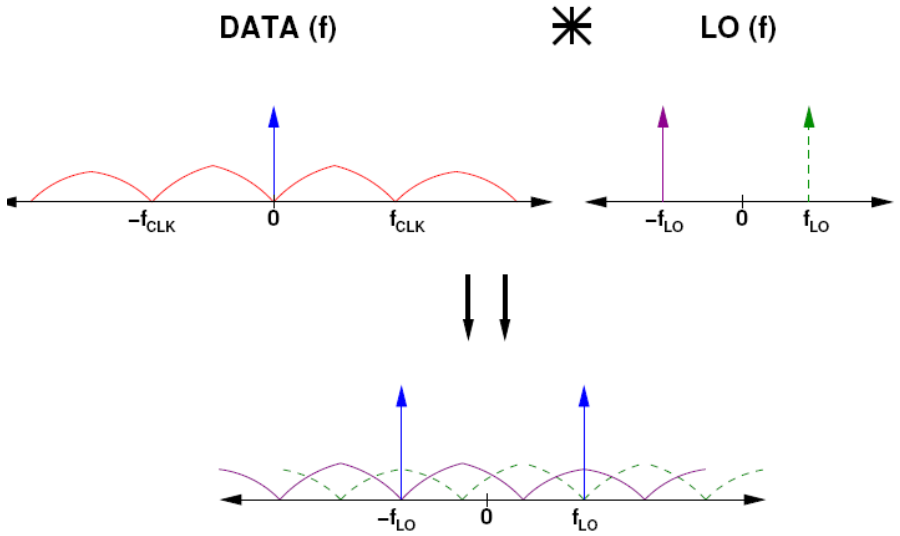
ΣΔ Digital-RF Modulator



- Oversampling IQ ΣΔ Modulators.
- DRFC is Digital RF converter which combines the functionality of the DAC and mixer.

Quadrature Digital-RF Converter

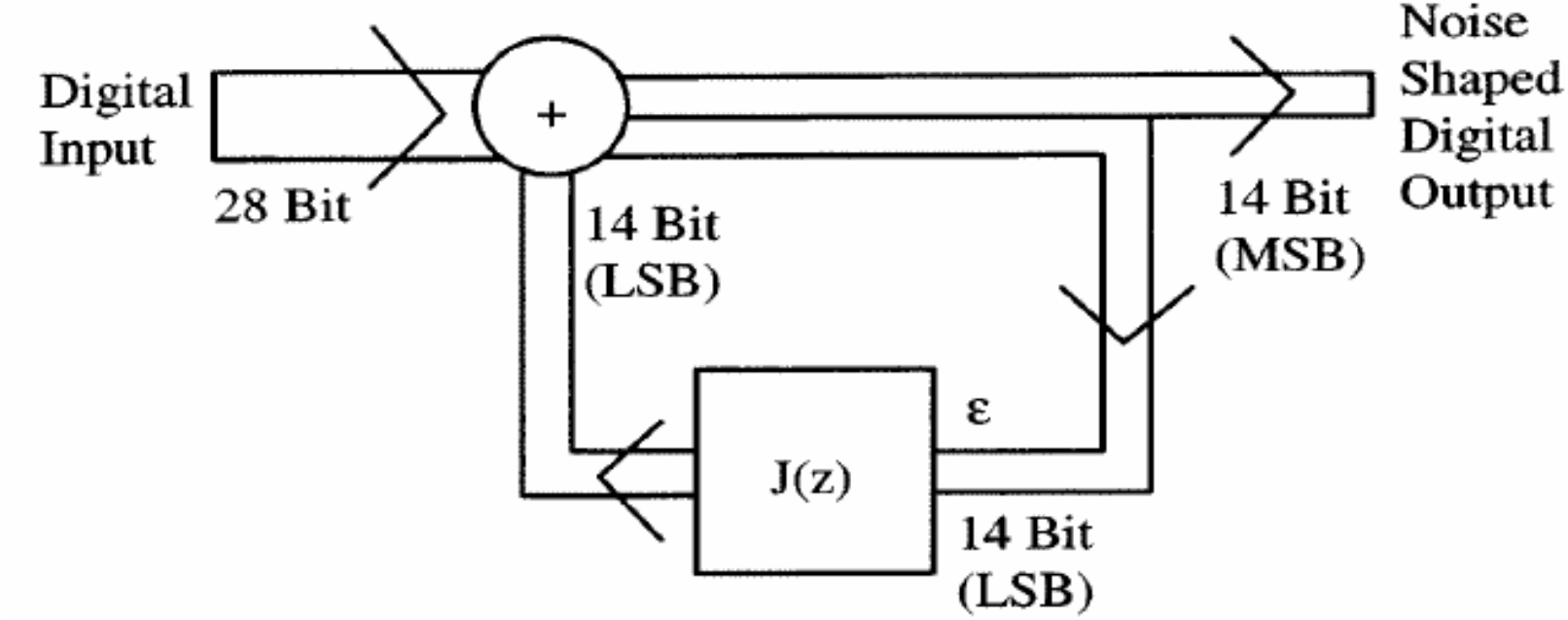




- In every cell a LO signal drives differential pairs with current sink. Modulated current is multiplied by digital bits. Common cascode devices isolate output from switches.
- $f_{LO} = \frac{n * f_{clk}}{2},\ n = 1,2,3$ to avoid aliasing of quantization noise.
- $f_{LO} = n * f_{clk},\ n = 1,2,3$ to avoid leaking of shaped ΣΔ quantization noise.

A. Jerng, C.G. Sodini, "A wideband ΔΣ Digital-RF Modulator for High Data Rate Transmitters"

Noise Shaping in ΣΔ DACs

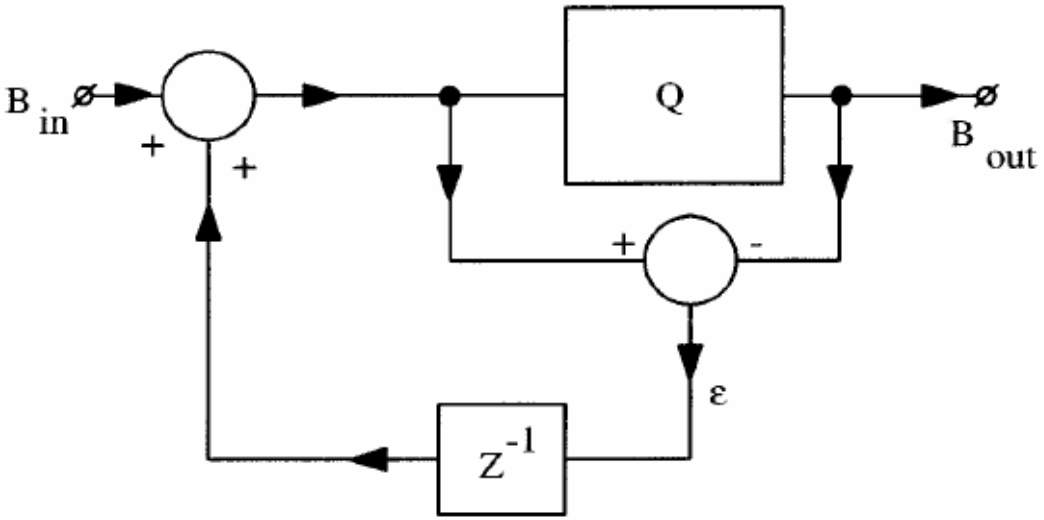


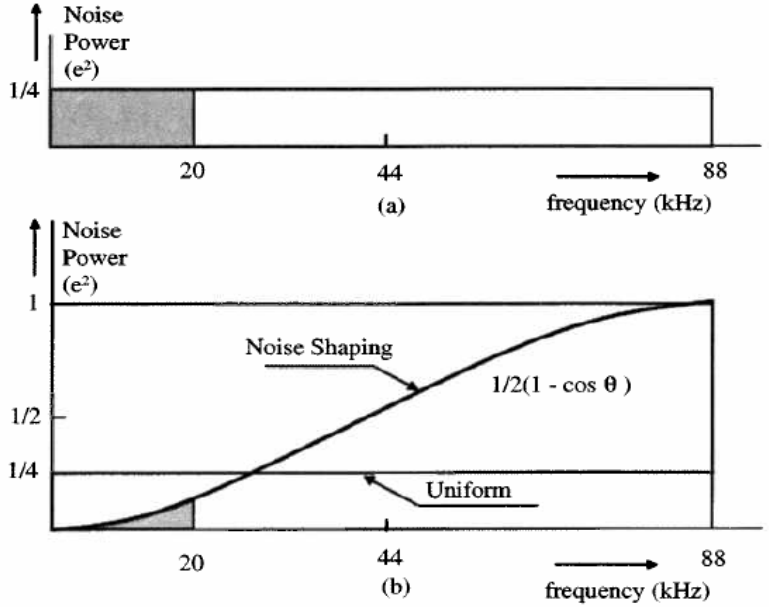
$$B_{in}(z) + \varepsilon(z)\,J(z) = B_{out}(z) + \varepsilon(z)$$

$$\frac{B_{out}(z)}{B_{in}(z)} = 1 - \frac{\varepsilon(z)}{B_{in}(z)}\left(1 - J(z)\right)$$

$$\varepsilon(z)\left(1 - J(z)\right)$$ Noise Transfer Function

First Order Noise Shaper





$$B_{out}(z) = B_{in}(z) - \varepsilon(z)\left(1 - z^{-1}\right)$$

$$e_{tot}^2 = \frac{\theta_1}{\pi}\int_0^{\theta_1} \varepsilon^2 \left|1 - z^{-1}\right|^2 d\theta \quad \theta_1 = \frac{2\pi f_b}{f_s}$$

$$\left|1 - z^{-1}\right|^2 = 2\left(1 - \cos\theta\right)$$

$$e_{tot}^2 = \frac{\theta_1}{\pi} 2\left(\theta_1 - \sin\theta_1\right)\varepsilon^2$$

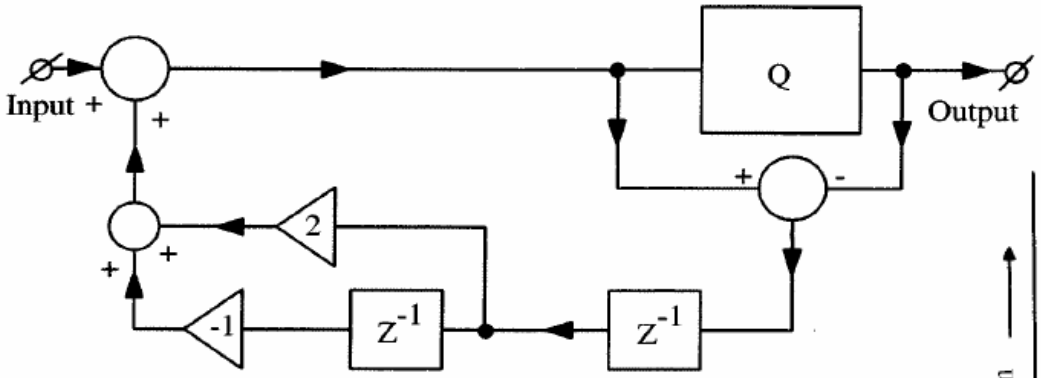
Without Noise Shaping

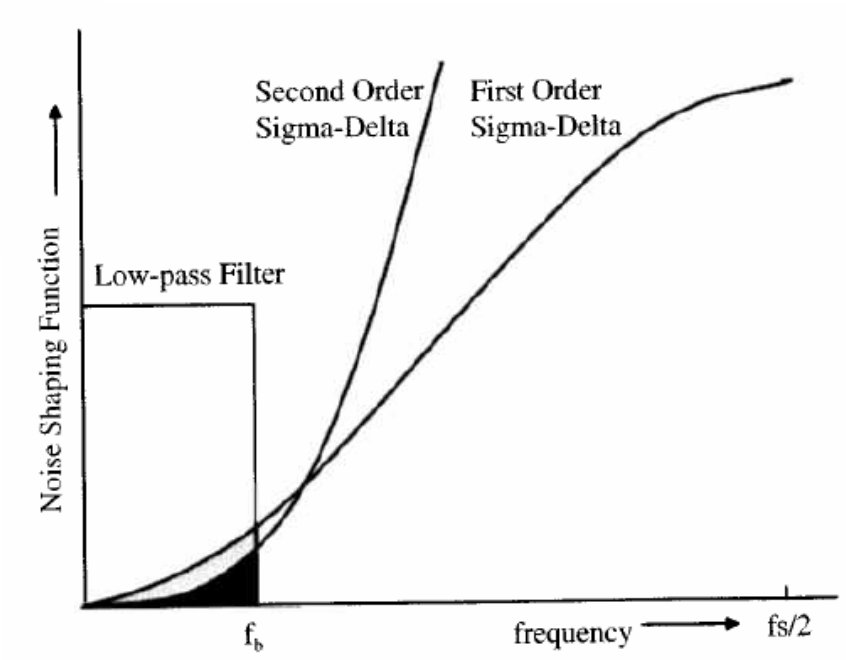
$$e_{uniform}^2 = \varepsilon^2 \int_0^{\theta_1} d\theta = \varepsilon^2 \theta_1$$

Dynamic Range Improvement

$$DR_{improvement} = \frac{e_{uniform}}{e_{tot}} = \left(\frac{2\theta_1}{\pi}\left(1 - \frac{\sin\theta_1}{\theta_1}\right)\right)^{-1/2}$$

Second Order Noise Shaper





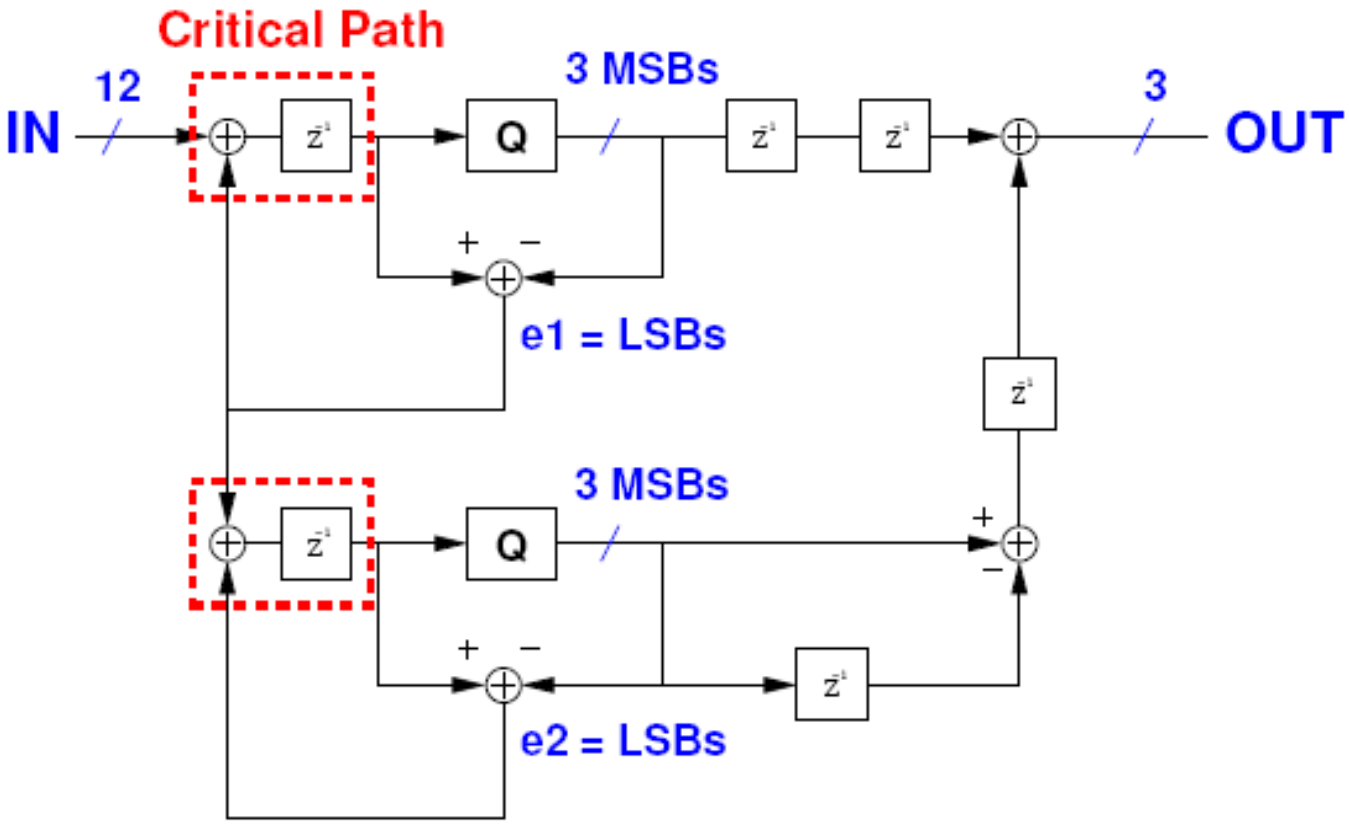
Noise Shaping:

$$1 - J(z) = (1 - z^{-1})^2$$

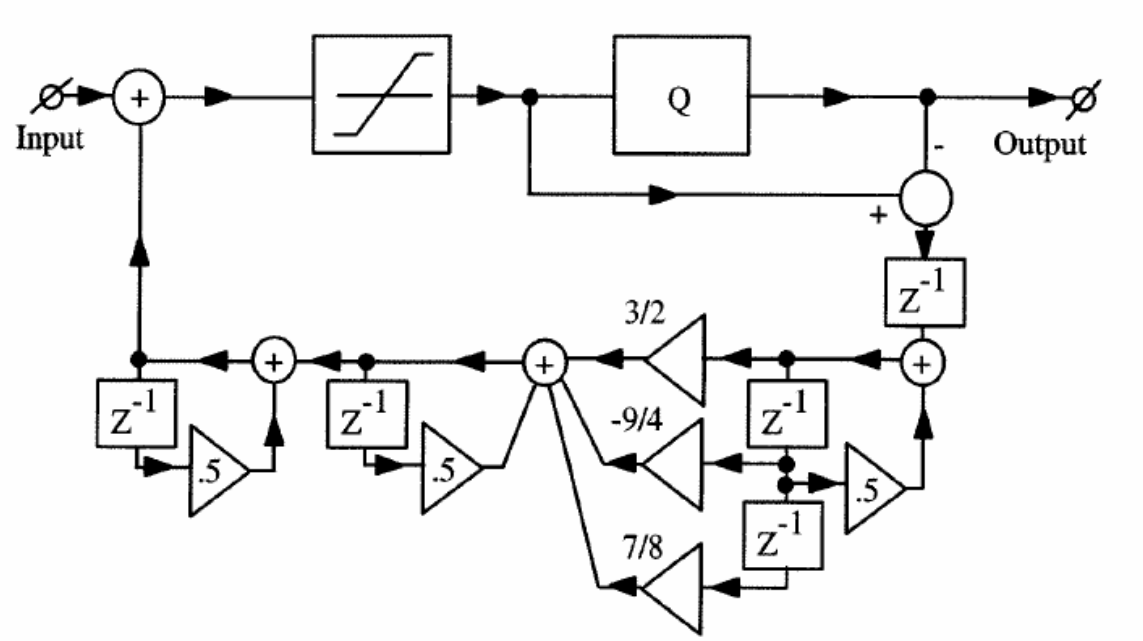
Dynamic Range Improvement:

$$DR_{improvement} = \frac{e_{uniform}}{e_{tot}} = \left(\frac{1}{\pi} \left(6\theta_1 + 2\sin\theta_1 \cos\theta_1 - 8\sin\theta_1 \right) \right)^{-1/2}$$

Second Order MASH Error Feedback Topology



Third Order Noise Shaper



Case 1: Output Bits larger than 1

Noise Shaping:

$$1 - J(z) = (1 - z^{-1})^3$$

Dynamic Range Improvement:

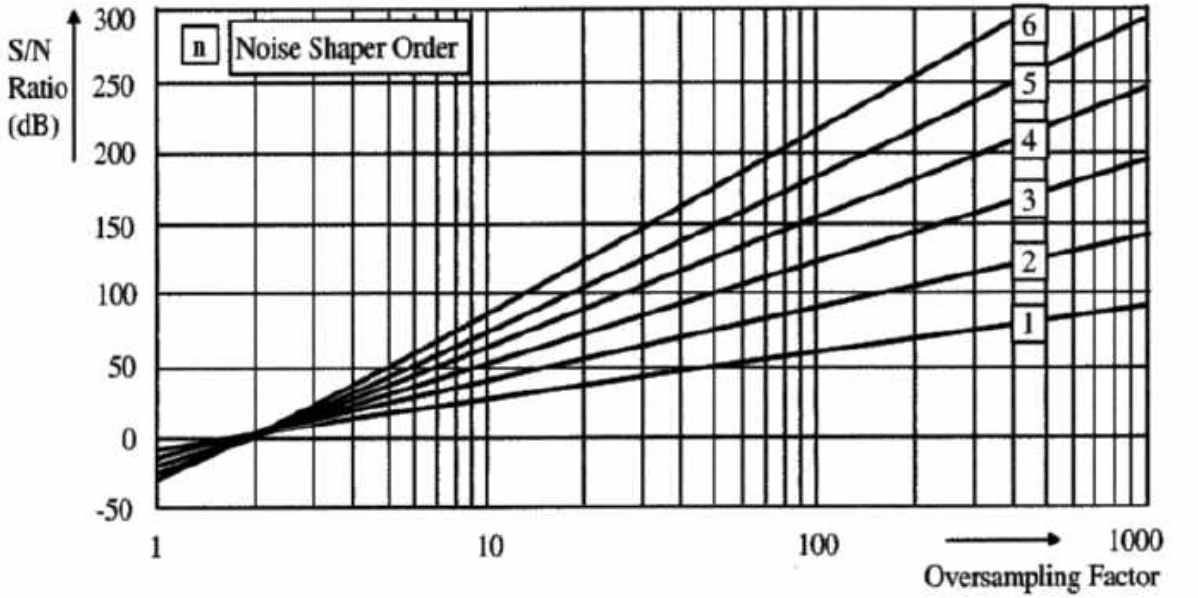
$$DR_{impr.} = \left(\frac{1}{\pi} \left(20\theta_1 - 30\sin\theta_1 + 6\sin 2\theta_1 - 2/3 \sin 3\theta_1 \right) \right)^{-1/2}$$

Case 2: Just 1 output bit

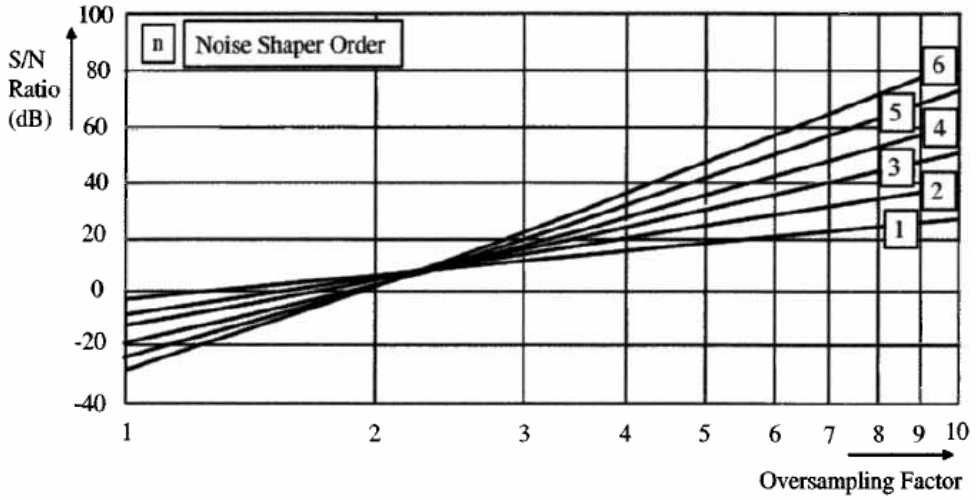
Noise Shaping:

$$1 - J(z) \left(= \frac{1 - z^{-1}}{1 - az^{-1}} \right)^3$$

Noise Shaping Improvements



- Assume ideal digital filtering



Co-Design ΣΔ NTF and BPF

$$Q_{ind} = \omega L/R, \text{ and } \omega_0^2 = 1/LC, \text{ then}$$

$$Q_{ind} \geq \frac{f_{LO}}{BW} \Rightarrow f_{LO} \leq Q_{ind} * BW$$

$$f_{clk} = OSR * BW, \quad f_{LO} = n * f_{clk}$$

$$OSR \leq \frac{Q_{ind}}{n}$$

- Q_{ind} ~ 10-25 depending on top metal resistance and distance to substrate.
- OSR ~ 10-16, 2nd order and 1 bit SNR=40 dB. Higher order increases the SNR but also increases the slope of the out of band quantization noise which need to be filtered out by the BPF. Low order, multi-bit ΣΔ modulator is a better option.

TABLE I
SIMULATED ΔΣ SNR WITH OSR=13

Loop Filter Order	Quantizer Bits	SNR	Matching Requirements (σ)	RF Filtering Requirements
2^{nd}	1	37 dB	None	Difficult
4^{th}	1	47 dB	None	Very Difficult
3^{rd} (1-2 MASH)	1	50 dB	$\sim 0.5\%$	Very Difficult
2^{nd}	3	52 dB	$\sim 1\%$	Moderate

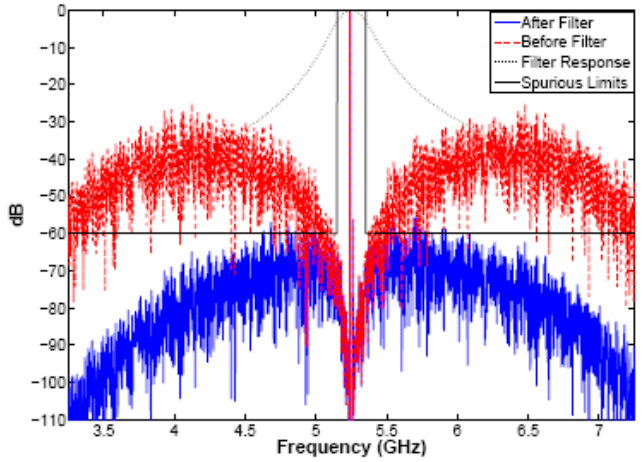


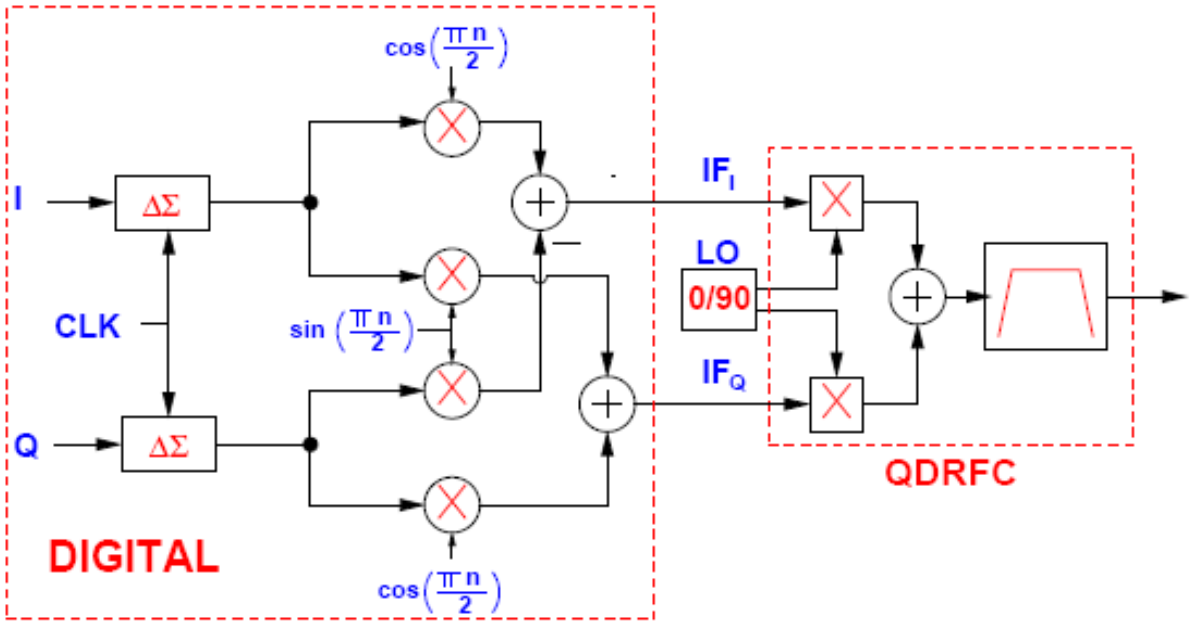
Fig. 4. RF Output Spectrum using 2nd order, 3-bit ΔΣ Modulator

What is the problem with going multi-bit ?

Quadrature Digital IF

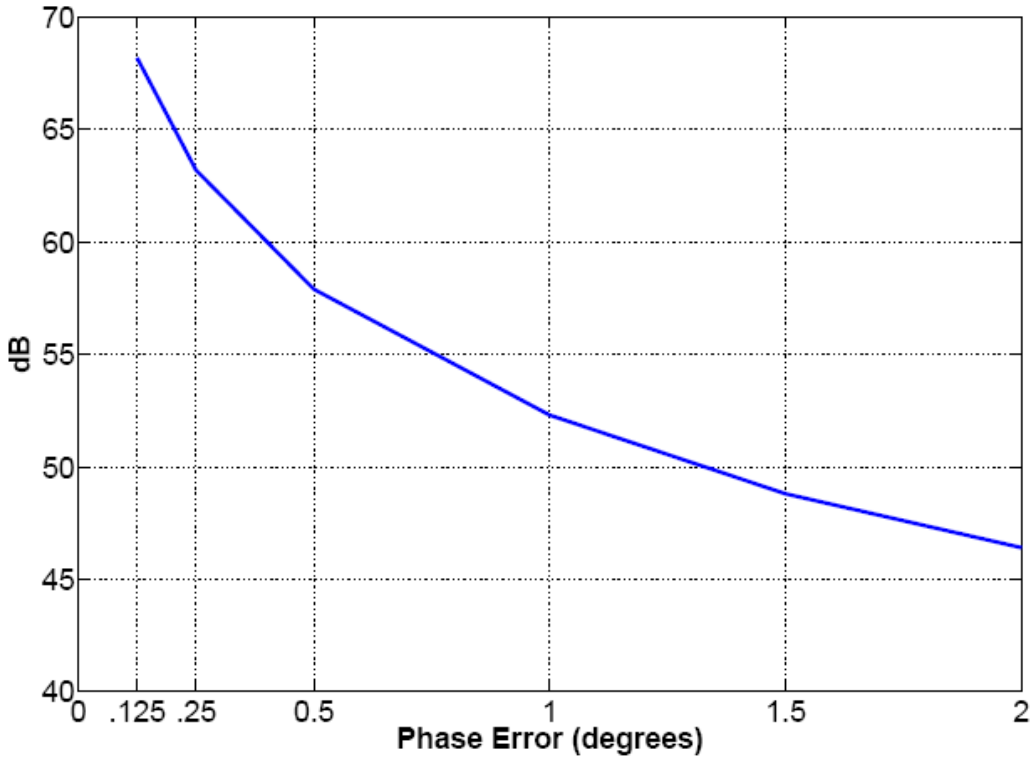
- ΣΔ modulator can be degraded by spurs coming from LO leakage and quadrature LO phase mismatches.
- A potential solution is digitally up-convert the ΣΔ signal before the RF modulation. LO and image spurs from the digital-RF converter will be separated from the RF output by f_{IF} and $2f_{IF}$.

- Conventional IF upconversion of $f_{IF}=f_{clk}/4$ would be convenient because digital cosine and sines only have values 1, -1, 0. However there is aliasing of shaped quantization noise from fclk/2.
- Quadrature IF upconversion solves the problem.

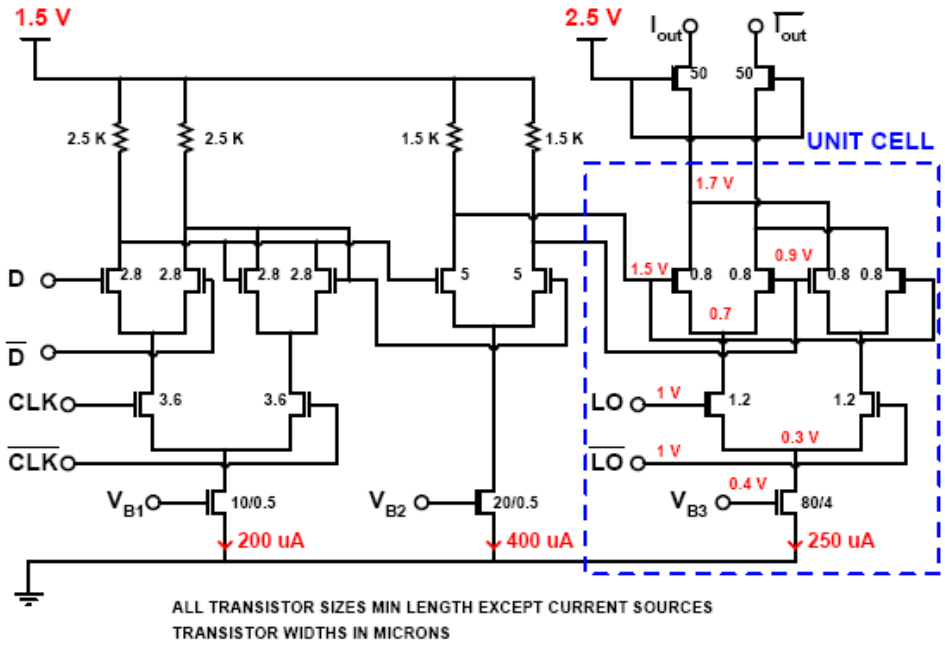


LO phase sensitivity of Quadrature Digital IF

- SNR vs. LO Phase Error for Quadrature Digital-IF.
- SNR for a 2nd order, 3 bit ΣΔ modulator.



Mismatches in the Digital-RF Converter

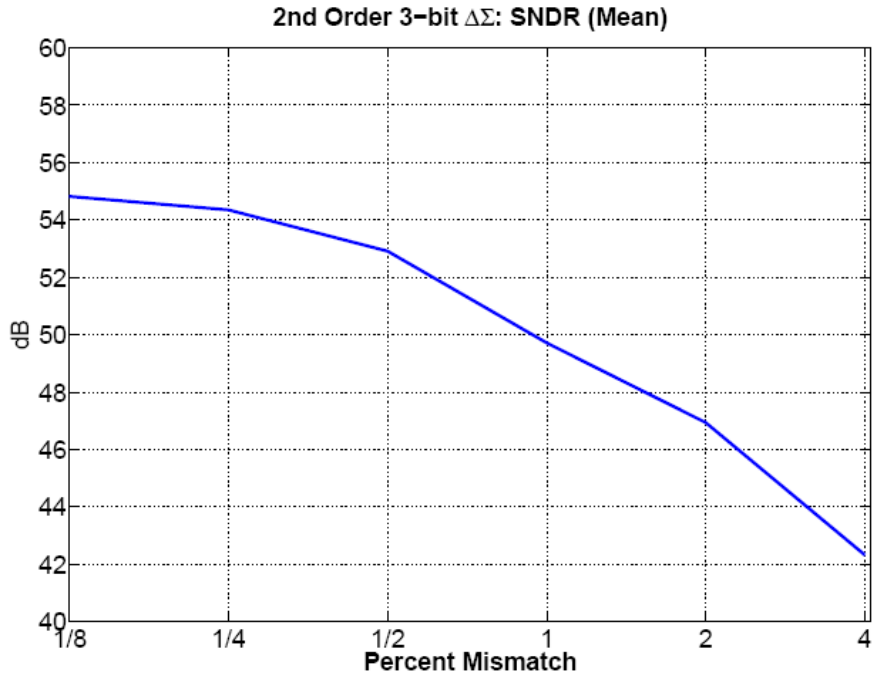


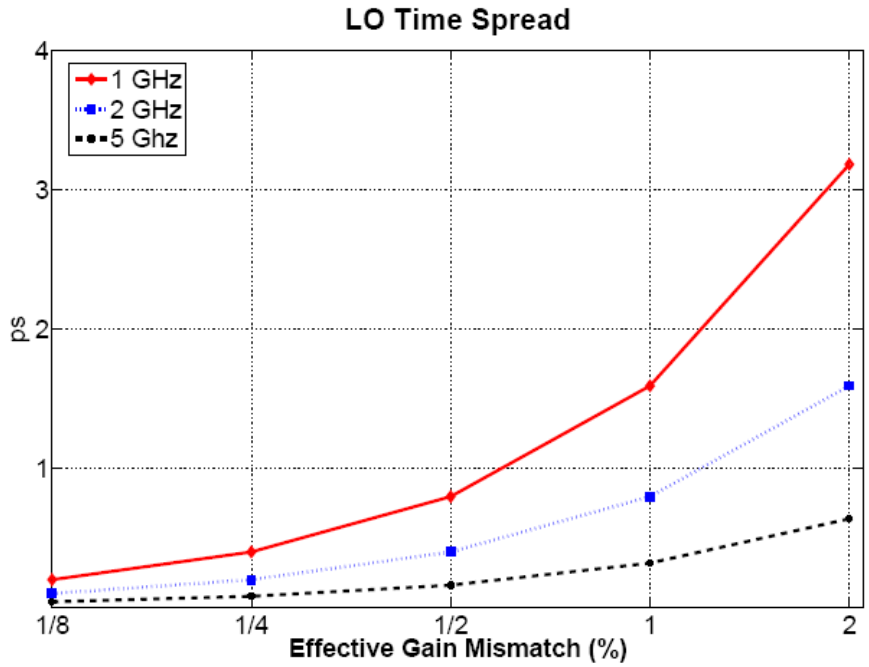
- Small phase mismatches in the LO can be modeled as gain mismatches

$$\sin(\omega t + \phi_{mismatches}) = \sin(\omega t) + \phi_{mismatches}\cos(\omega t)$$

- The DAC has 3 bits which can be implemented with 7 unit elements cells. Mismatches between the cells will degrade performance as well.

Mismatches in the Digital-RF Converter (Cont..)





- A matching better that 1 % needed for SNDR > 50 dB.
- For a 5 GHz LO, the timing spread needs to be better than 250 fs for a 1% mismatch.

HW 1

1. Explain why and prove that a discrete signal is periodic with period F_{CLK}.
2. Prove that a real valued signal has an even spectrum. Explain the symmetry differences between discrete-time and continuous-time signals.
3. Prove that multiplication of time domain signals produces convolution of the signals frequency domain. Prove the dual property as well. Explain the differences for this property between discrete-time and continuous-time signals.
4. Derive the noise shaping transfer function of the MASH DAC architecture. Find an expression for the dynamic range improvement vs. OSR. Please provide a plot.

Lab 1

- 1. Using simulink implement a 2nd order, 3 bit ΣΔ with IF digital modulation. Consider the following specifications:
  - $f_{IF} = f_{CLK}/4$
  - $f_{LO} = f_{RF} \pm f_{IF} = f_{RF} \pm f_{CLK}/4$ (use upper-sideband mixing)
  - f_{RF}=5.25 GHz, f_{CLK}=2.625 GHz, f_{LO}=4.6 GHz.
  - Simulate the full system and get plots of the spectrum at baseband, IF and RF. Play special attention to the impact of the second harmonic of the LO to the overall noise contribution to the RF signal band. Use a 4th order Bessel filter at 5.25 GHz.
- 2. Repeat the simulations for the following choice of frequencies: f_{CLK}=2.625 GHz, f_{IF}=600 MHz and f_{LO}=4.65 GHz. Note that f_{LO} is not longer a multiple f_{CLK}, then some aliasing of quantization noise will appear in the RF signal band. The only attenuation is provided by the sinc response of the zero-order-hold.
- 3. Repeat the simulations for finite rise and fall times (75 ps) of the clock signal. Please derive the new response of the zero-order-hold circuit. Characterize and simulate the improvement of the new filter response. What is the attenuation of the sinc response and the new response at $2f_{RF}$?

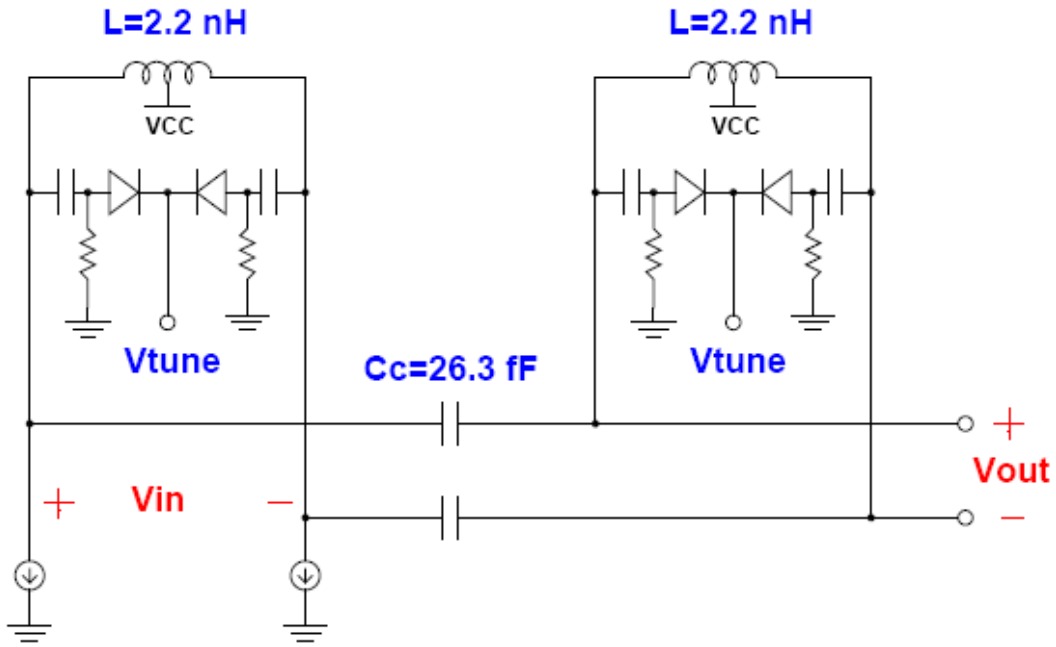
Lab 1 (Cont..)

- Provide signal spectrum plots and SNDRs for the output of the ΣΔ modulator and the RF output for the following cases:
  - $\mathbf{f}_{IN} = \mathbf{f}_{CLK}/8$.
  - $\mathbf{f}_{IN}$ = 1 MHz

For the SNDR calculation use the whole signal spectrum first and then assume an ideal filter of $\mathbf{f}_{CLK}/20$ for the ΣΔ output and a filter of 500 MHz for the RF output. Explain the differences in the results. Why for $\mathbf{f}_{IN} = \mathbf{f}_{CLK}/8$ there is so much harmonic distortion?

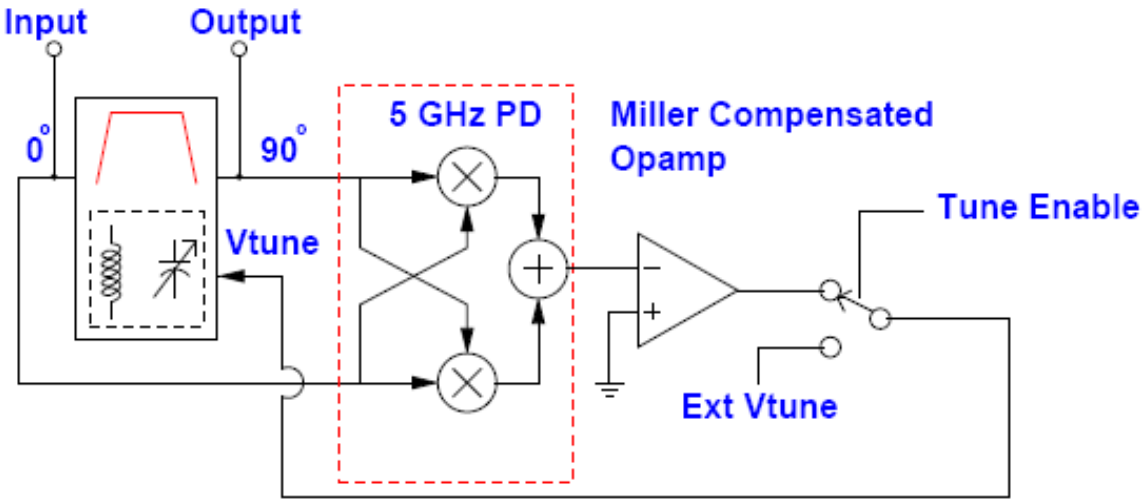
- Modified your simulink model to include the following inaccuracies in the 3 bit DAC. Assume that the LSB level is 100 mV and the following output voltage levels are measured from 000 to 111 (-0.01, 0.105, 0.195, 0.28, 0.37, 0.48, 0.6, 0.75) V.
- Find the offset & full scale errors in LSBs, the gain error using the LS method. Find the corrected codes and compute the DNL & INL.
- Repeat all your simulations with the nonideal DAC and provide the new plots and SNDRs.

RF Bandpass Reconstruction Filter



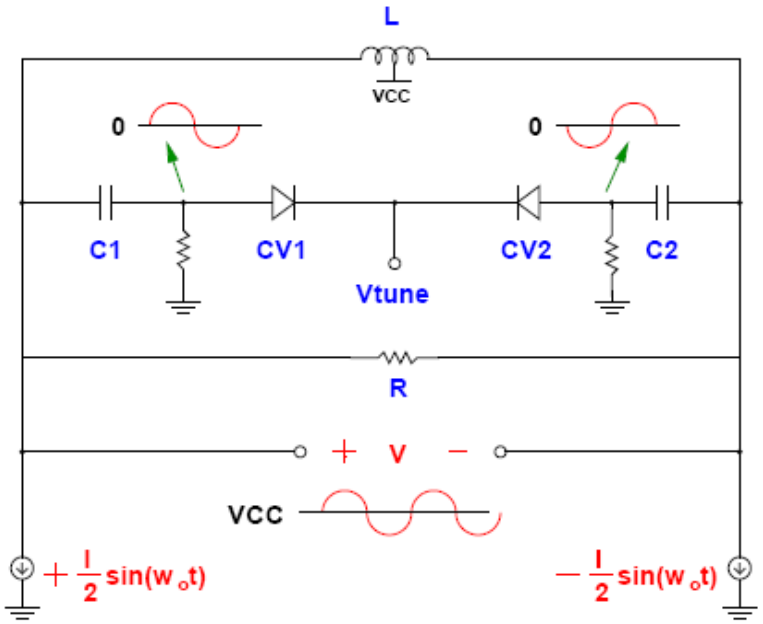
- 4th order Bessel bandpass filter with 260 MHz of bandwidth at 5.25 GHz.
- It a shunt LC resonator. The normalized resonator quality factor $q_0 = \frac{\Delta f}{f_m} Q_o$
- Then, $Q = \frac{f_m}{\Delta f} q_o = \frac{5.25e9}{260e6}(1.297) = 26.2$
- Tunability with PN junction varactors in the resonator load capacitance.

Tuning Loop Block Diagram



- A 90º phase difference between the phase detector inputs is achieved by the feedback loop.
- The phase detector can be 2 Gilbert-cell multipliers with cross-couple connections to cancel DC offsets produced by mismatches.

Distortion vs. Tunability



- Nonlinearity of the varactor:

$$C(V) = C_0 + C_1 V + C_2 V^2 + C_3 V^3 + ...$$

- The I-V relation in the tank:

$$I = V \cdot Y = V\left(\frac{1}{R} + j\omega C(V) - \frac{j}{\omega L}\right)$$

- Intermodulations: IM3 products produce non-linearity at $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$.

- Only even powers in C(V) matter since it a differential implementation.

$$I = \left(A\sin(\omega_1 t) + A\sin(\omega_2)\right) \cdot \left(\frac{1}{R} - \frac{j}{\omega_o L} + j\omega_o C_o + j\omega_o C_2 \left(A\sin(\omega_1 t) + A\sin(\omega_2)\right)^2\right)$$

$$I = \frac{A}{R}\sin(\omega_1 t) + \frac{A}{R}\sin(\omega_2 t) + \frac{3}{4} j\omega_o C_2 A^3 \left(\sin(2\omega_1 - \omega_2)t + \sin(2\omega_2 - \omega_1)t\right)$$

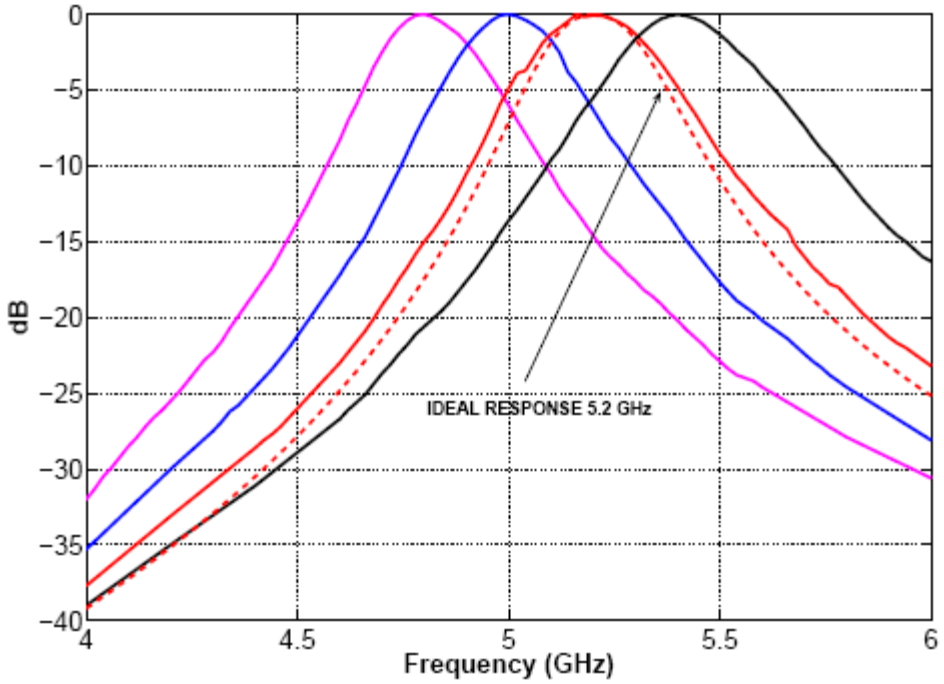
$$IM3(dBc) = 20\log 10\left(\frac{3\omega_o C_2 R A^2}{4}\right)$$

- Trade-off: higher R, worse IM3 but better Q.

Filter Testing Results

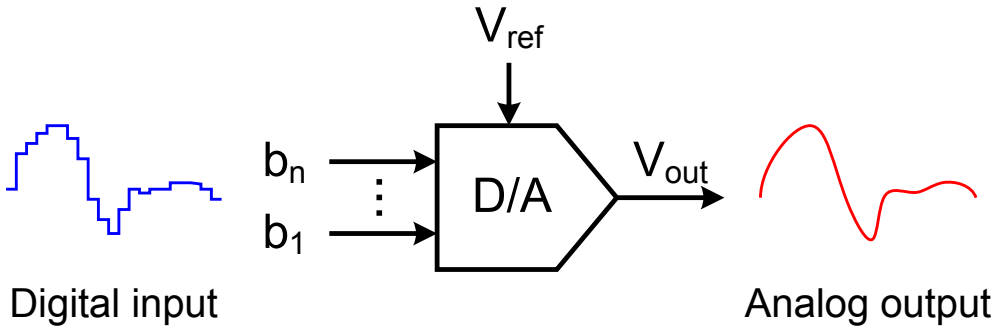
$$IM3(dBc) = 20\log 10\left(\frac{3\omega_o C_2 R A^2}{4}\right)$$

- Higher C_2 also worsens the linearity. The varactor can be operated in amore linear region if fixed switch capacitors are use to increase the tunability. This can lead to a full bank of digitally switchable caps, which requires a digital tuning loop.



DAC Architectures

D/A Converter Transfer Characteristic

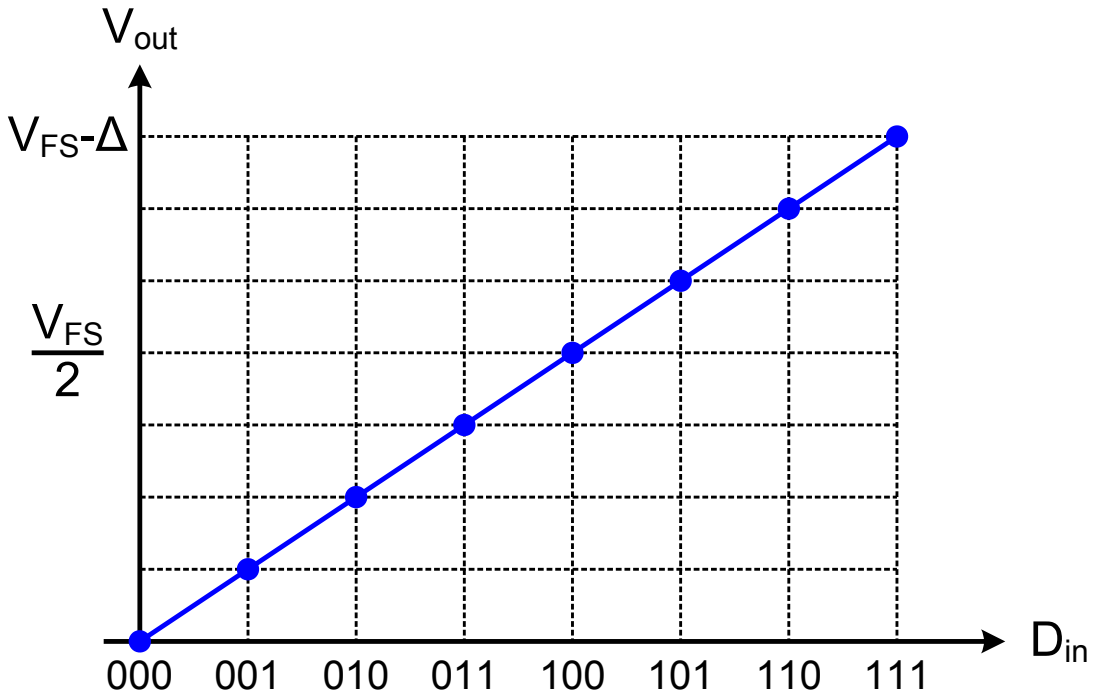


$$V_{out} = V_{FS} \cdot \sum_{i=1}^{N} \frac{b_i}{2^i} = \Delta \cdot \sum_{i=1}^{N} b_i \cdot 2^{N-i}$$

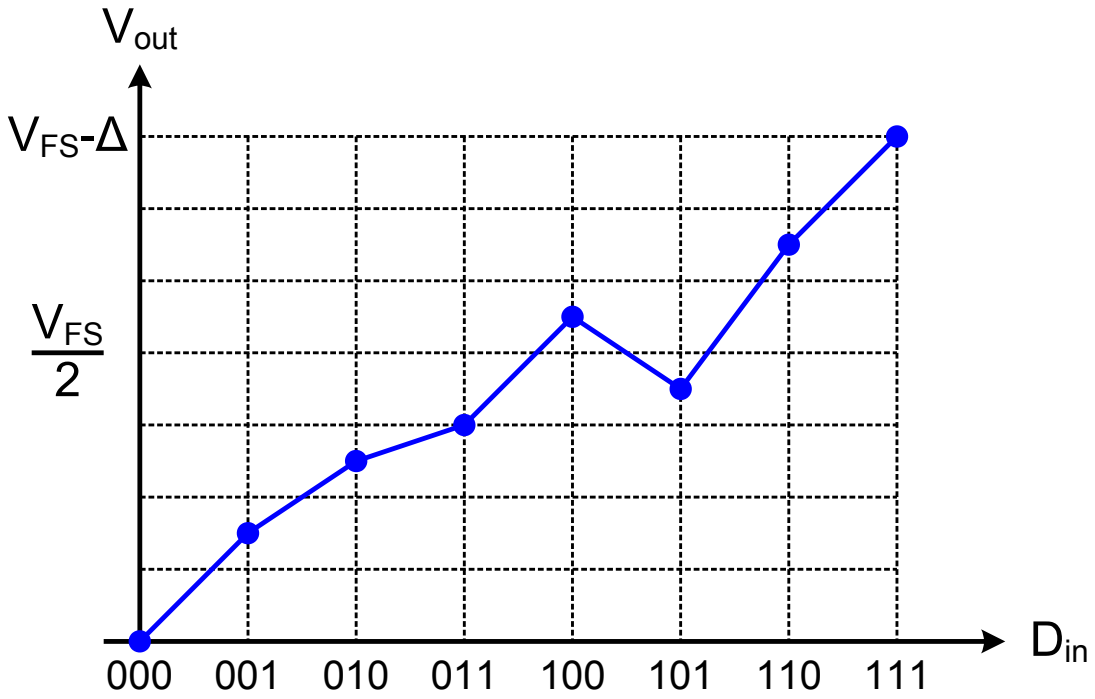
- N = # of bits
- V_{FS} = Full-scale input
- $\Delta = V_{FS}/2^N$ = 1LSB
- b_i = 0 or 1
- Multiplication

Note: V_{out} (b_i = 1, for all i) = $V_{FS} - \Delta = V_{FS}(1-2^{-N}) \neq V_{FS}$

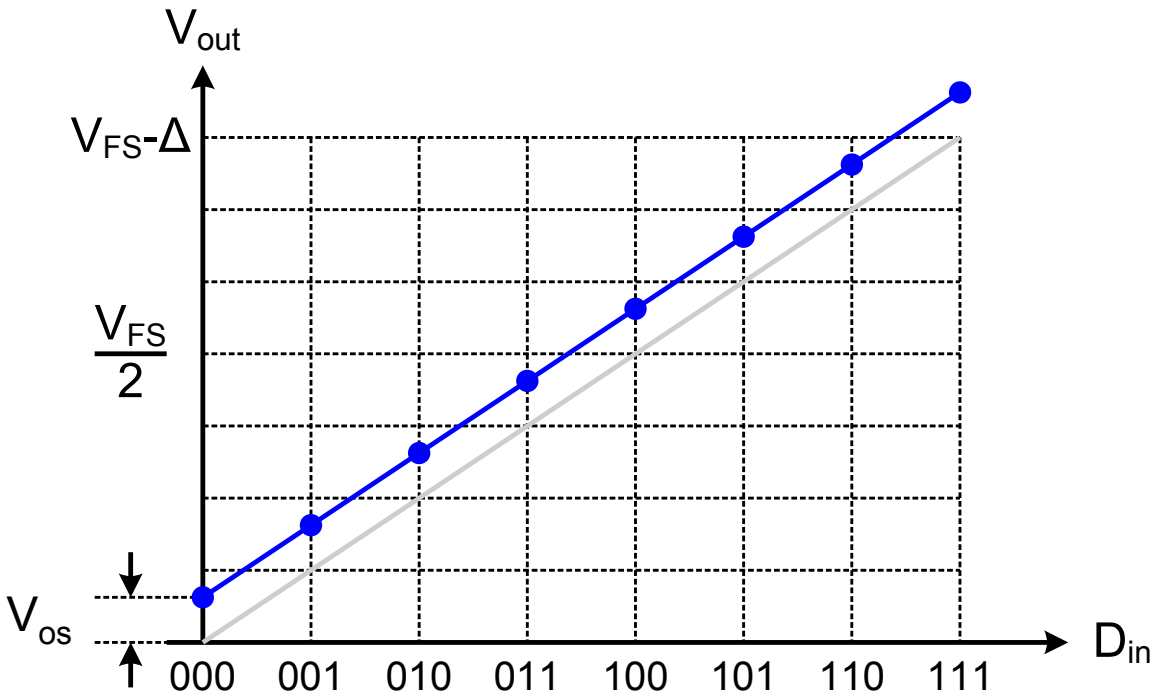
Ideal DAC Transfer Characteristic



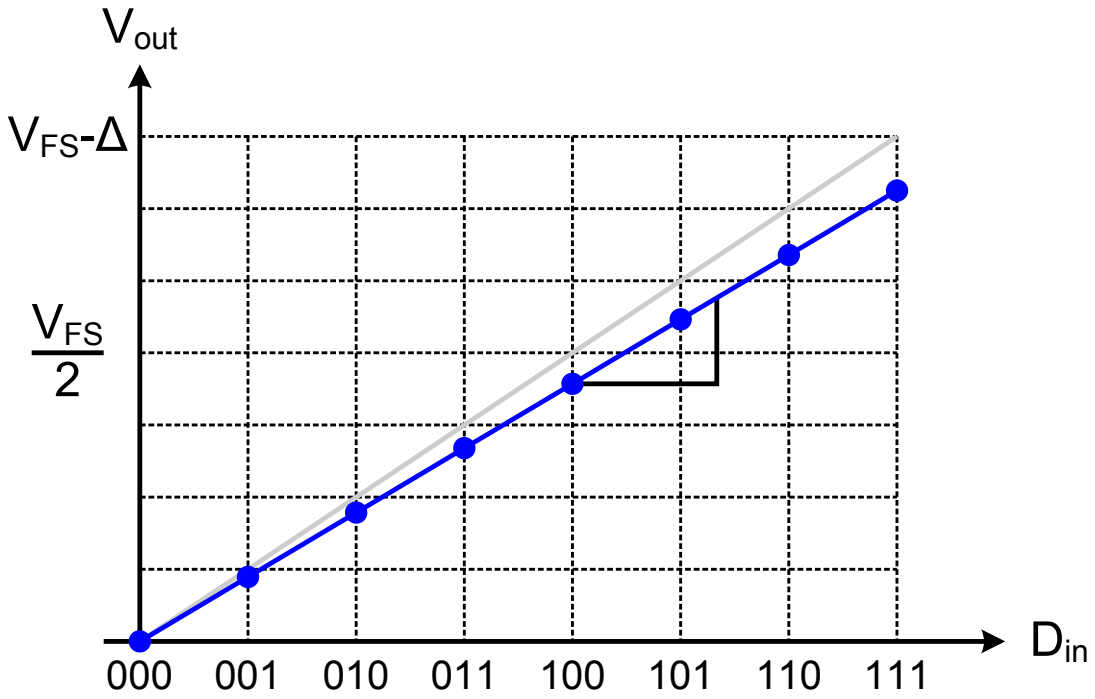
Monotonicity



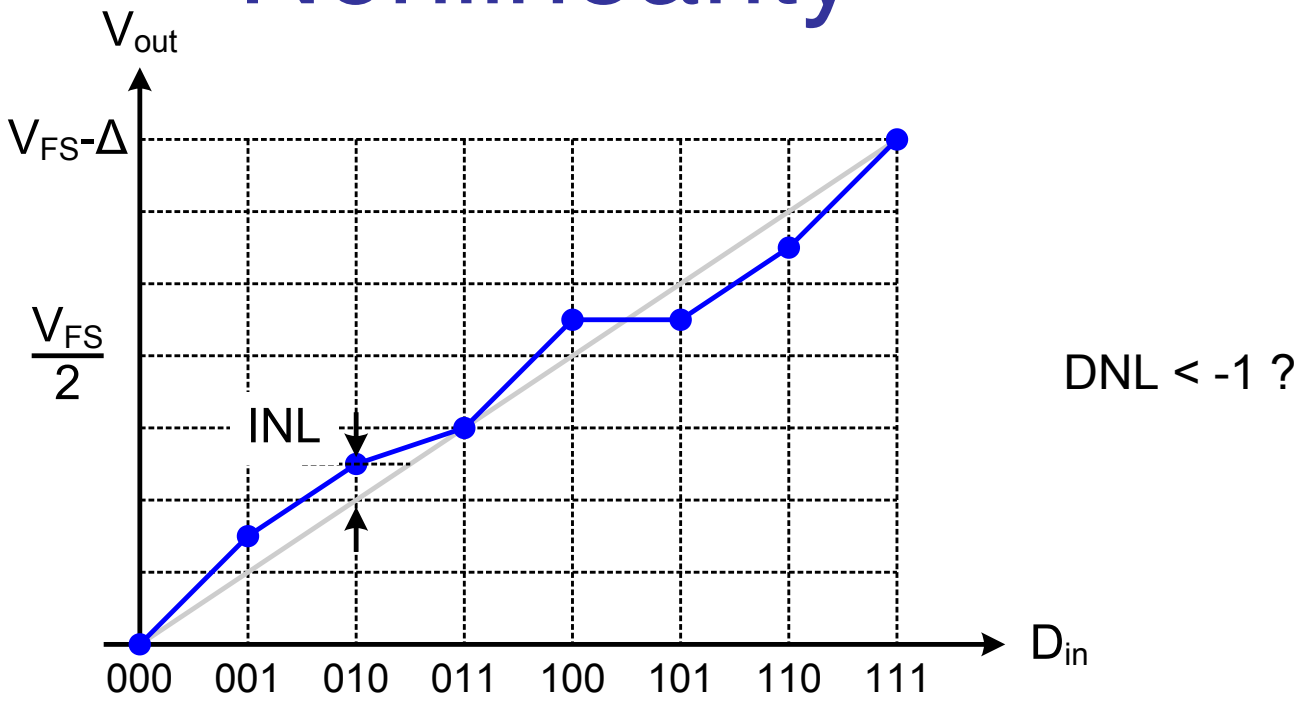
Offset



Gain Error

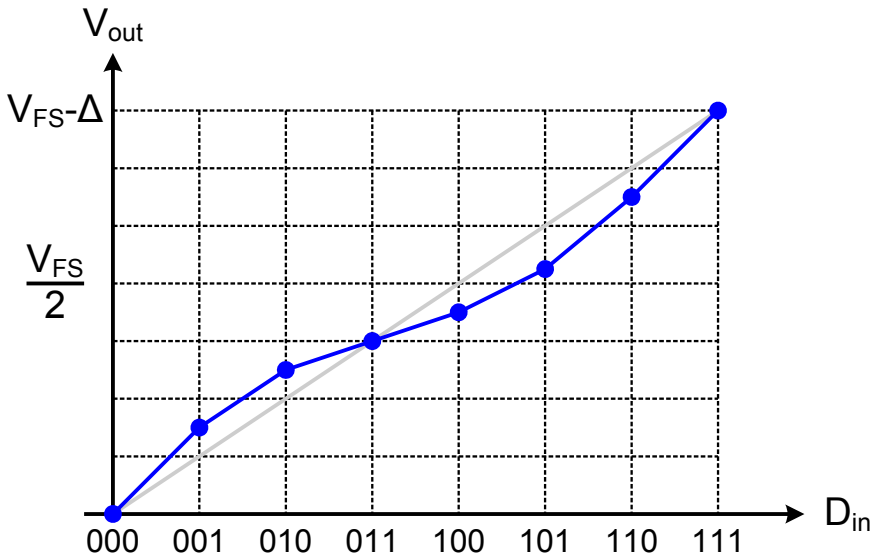


Differential and Integral Nonlinearity

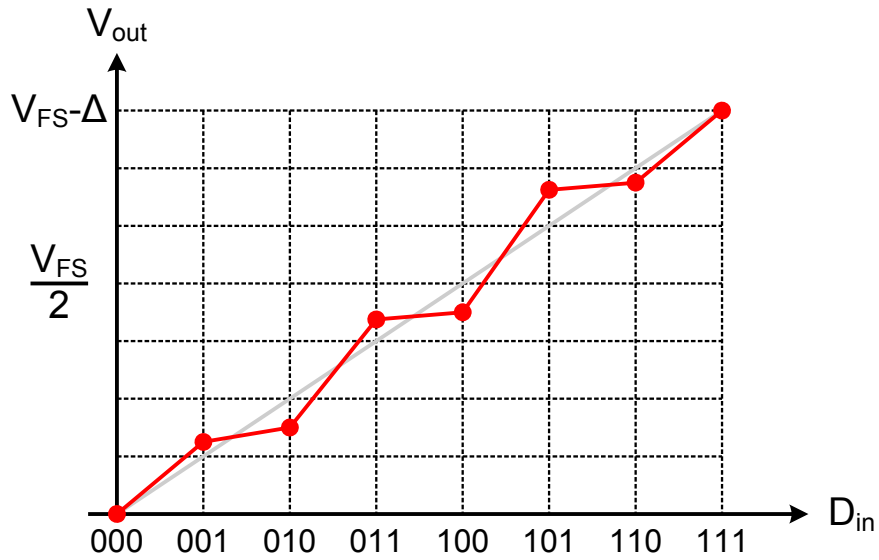


- DNL = deviation of an output step from 1 LSB (= $\Delta = V_{FS}/2^N$)
- INL = deviation of the output from the ideal transfer characteristic

DNL and INL



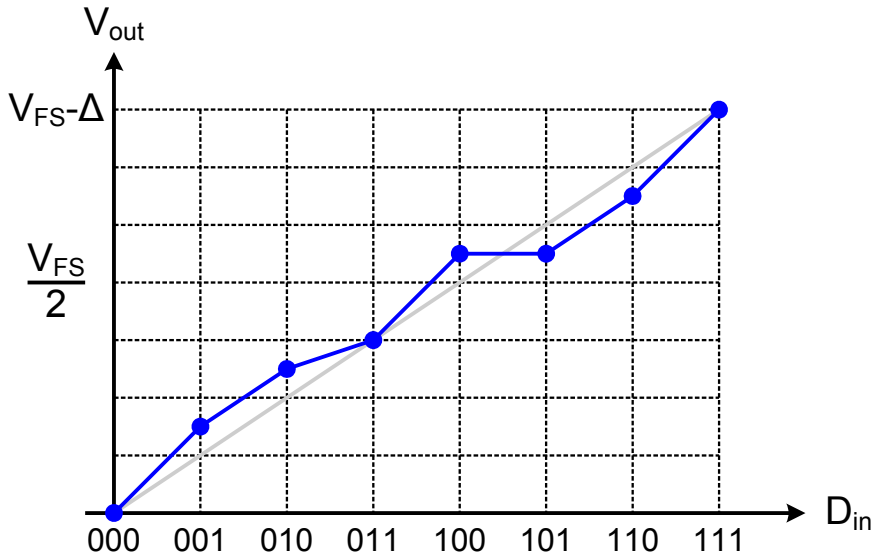
Smooth



Noisy

- DNL measures the incremental (local) nonlinearity.
- INL measures the cumulative (global) nonlinearity.

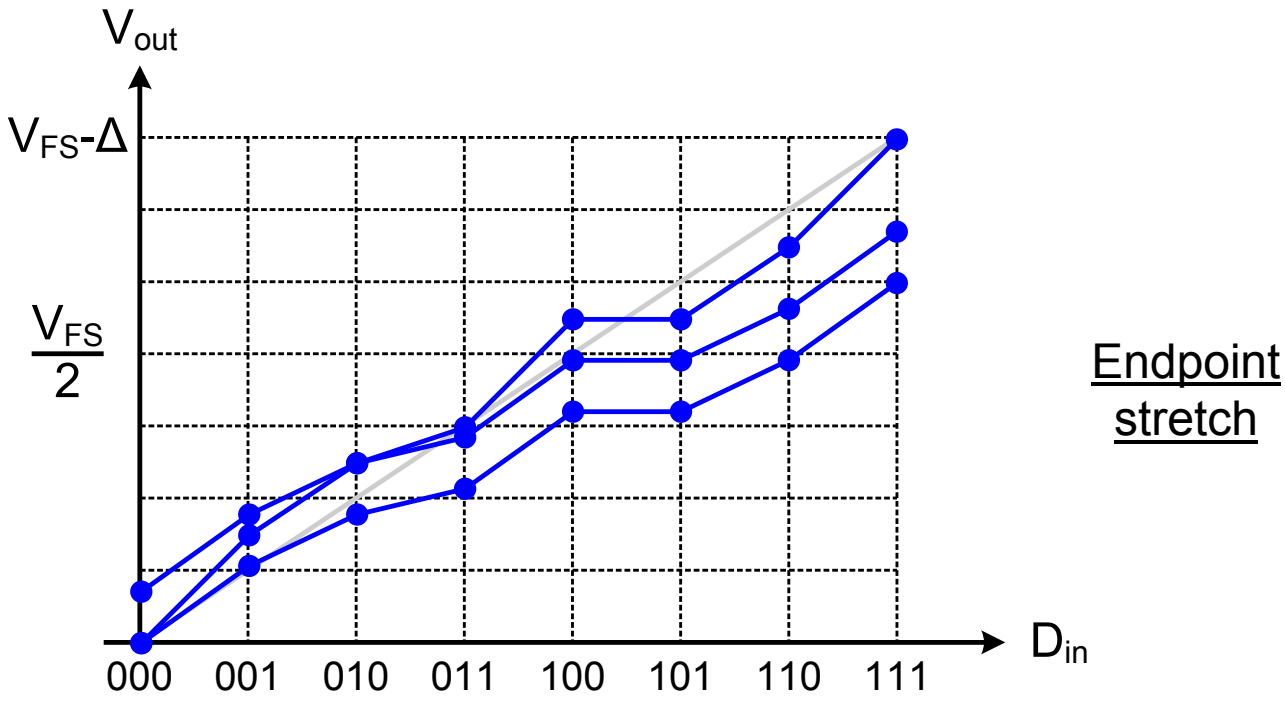
DNL and INL



$$INL_i = \sum_{j=0}^{i} DNL_j$$

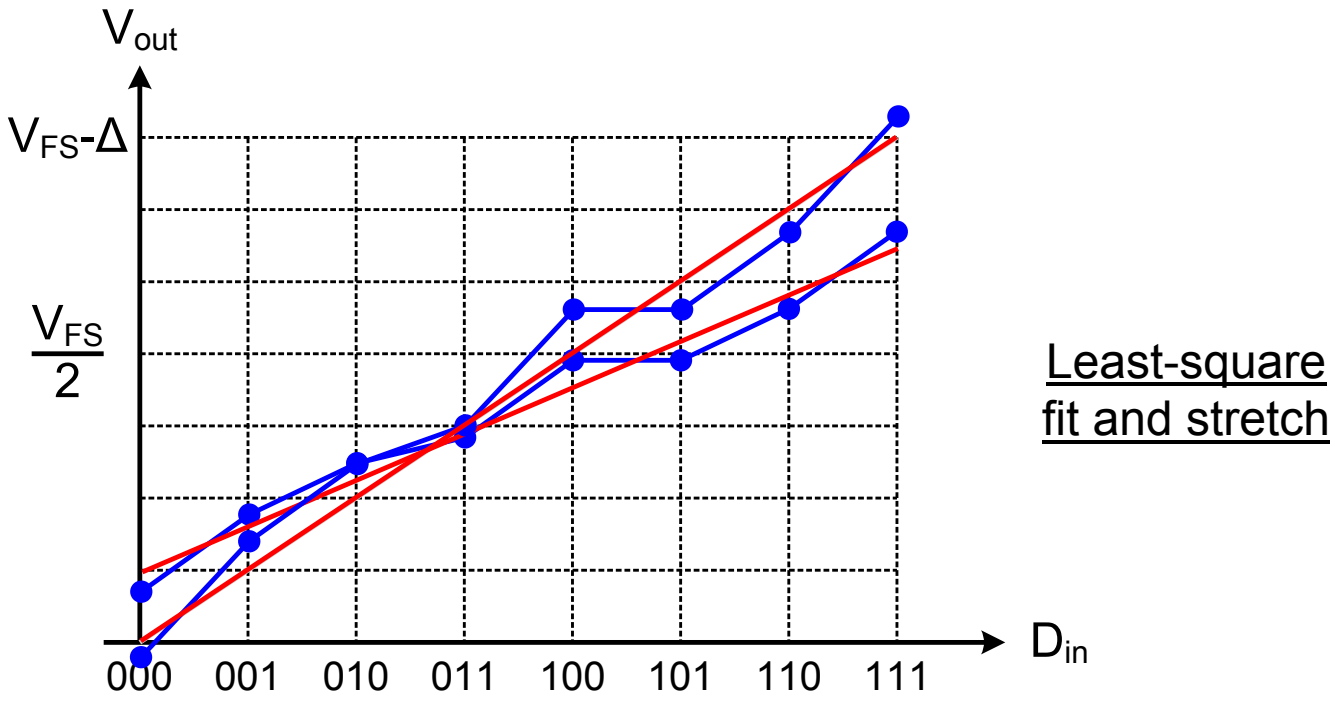
INL = cumulative sum of DNL

Measure DNL and INL (Method I)



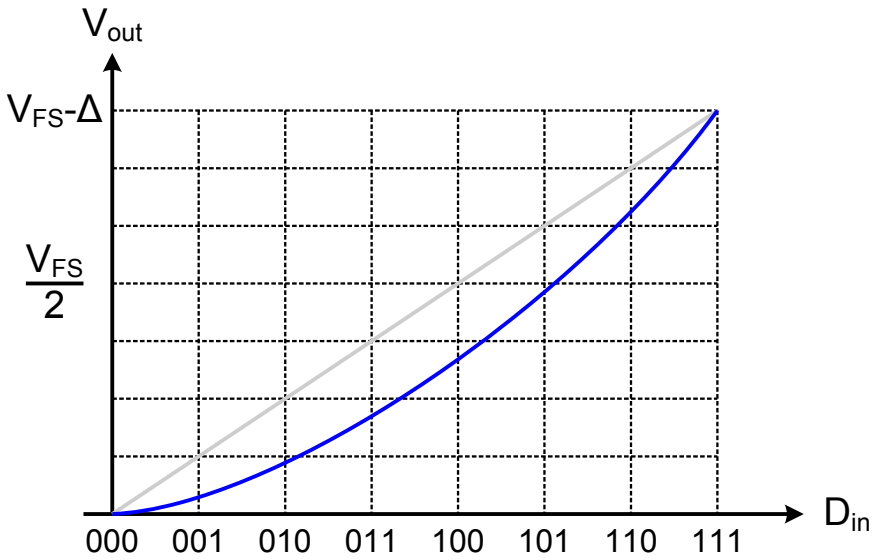
Endpoints of the transfer characteristic are always at 0 and V_{FS}-Δ.

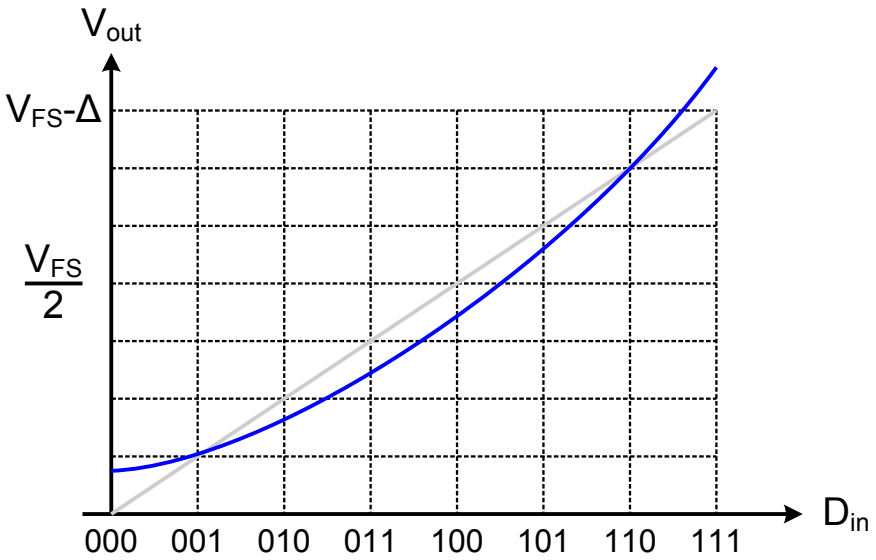
Measure DNL and INL (Method II)



Endpoints of the transfer characteristic may not be at 0 and V_{FS}-Δ.

Measure DNL and INL





Method I (endpoint stretch)

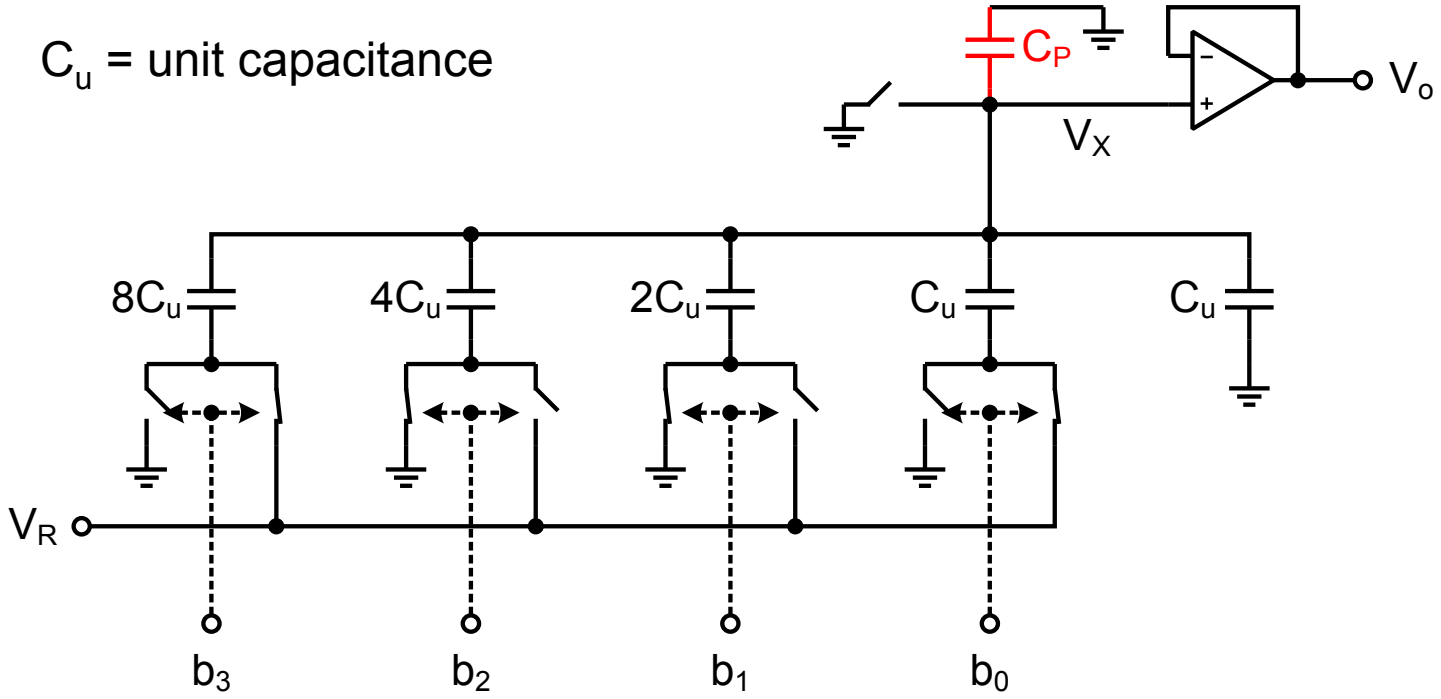
$\Sigma(INL) \neq 0$

Method II (LS fit & stretch)

$\Sigma(INL) = 0$

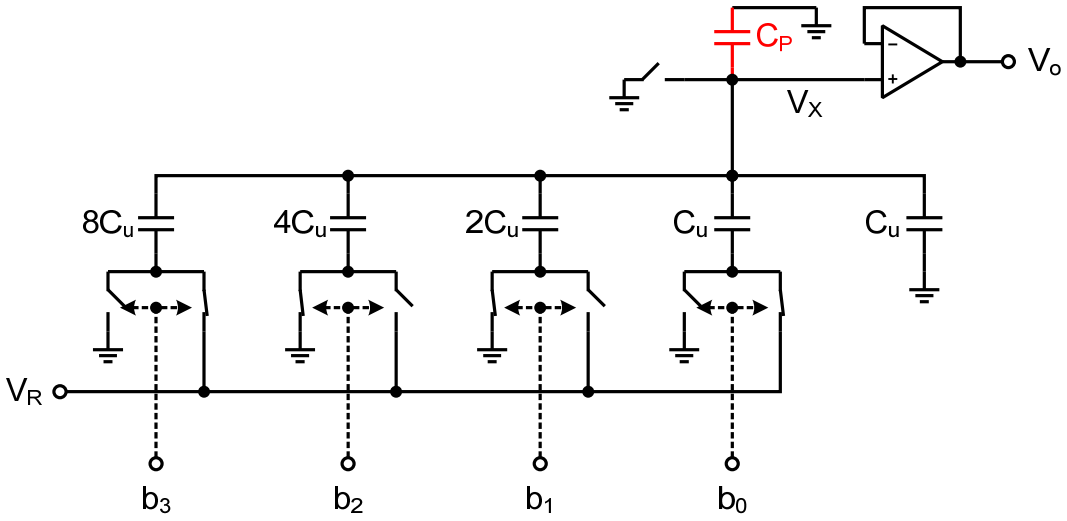
Binary-Weighted DAC

Binary-Weighted CR DAC



- Binary-weighted capacitor array → most efficient architecture
- Bottom plate @ V_R with $b_j = 1$ and @ GND with $b_j = 0$

Binary-Weighted CR DAC



$$V_o = \left(\frac{\sum_{j=1}^{N} b_{N-j} \cdot 2^{N-j} C_u}{C_p + C_u + \sum_{j=1}^{N} 2^{N-j} C_u} \right) \cdot V_R$$

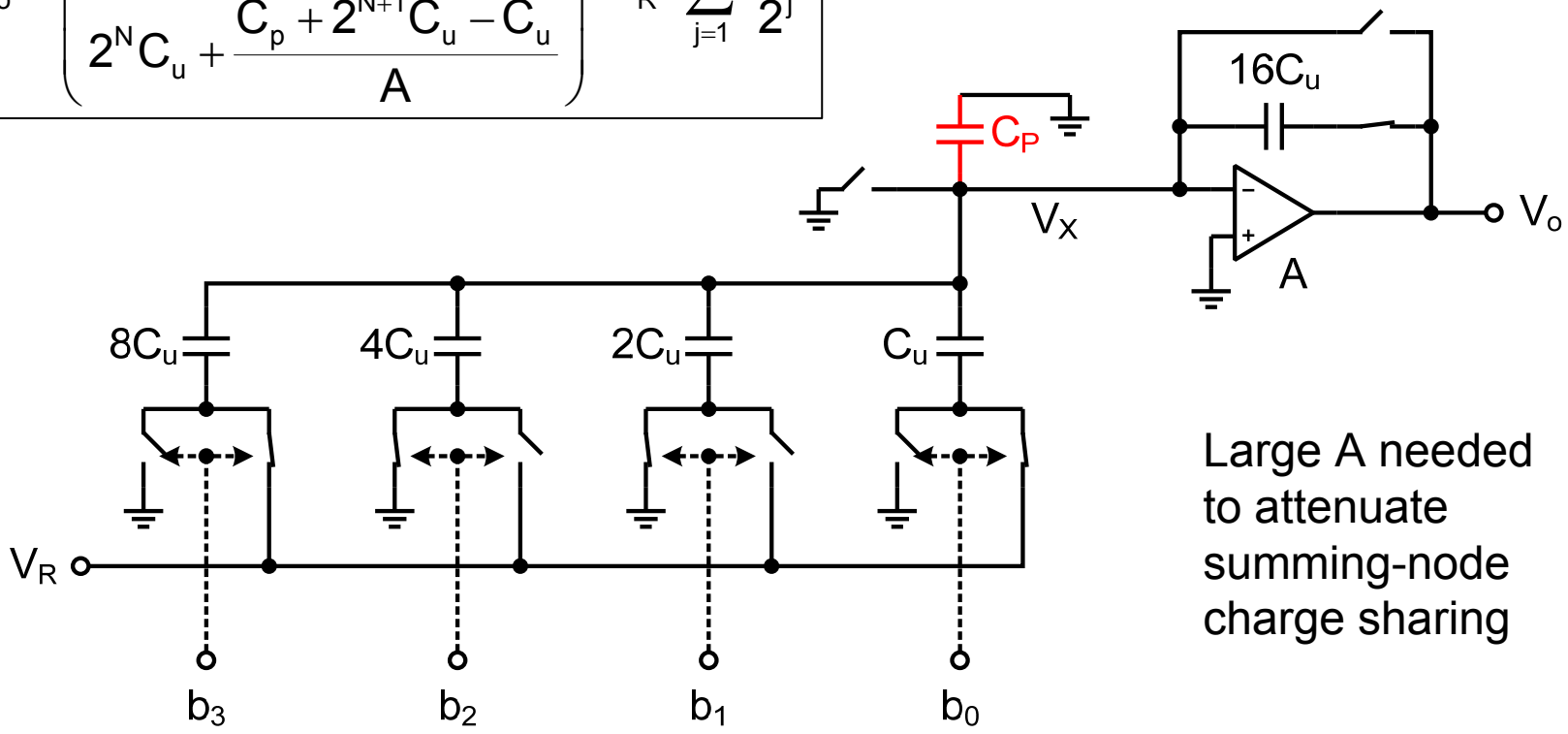
$$= \left(\frac{\sum_{j=1}^{N} b_{N-j} \cdot 2^{N-j} C_u}{C_p + 2^N C_u} \right) \cdot V_R$$

$$\boxed{V_o = \left(\frac{2^N C_u}{C_p + 2^N C_u} \right) \cdot V_R \cdot \sum_{j=1}^{N} \frac{b_{N-j}}{2^j}}$$

- $C_p \rightarrow$ gain error (nonlinearity if C_p is nonlinear)
- INL and DNL limited by capacitor array mismatch

Stray-Insensitive CR DAC

$$V_o = \left(\frac{2^N C_u}{2^N C_u + \frac{C_p + 2^{N+1} C_u - C_u}{A}} \right) \cdot V_R \cdot \sum_{j=1}^{N} \frac{b_{N-j}}{2^j}$$



Large A needed to attenuate summing-node charge sharing

MSB Transition

Code 0111

$$V_o(0111) = \left(\frac{C_1 + C_2 + C_3}{C_p + C + \sum_{j=1}^{4} 2^{4-j} C} \right) \cdot V_R$$

Code 1000

$$V_o(1000) = \left(\frac{C_4}{C_p + C + \sum_{j=1}^{4} 2^{4-j} C} \right) \cdot V_R$$

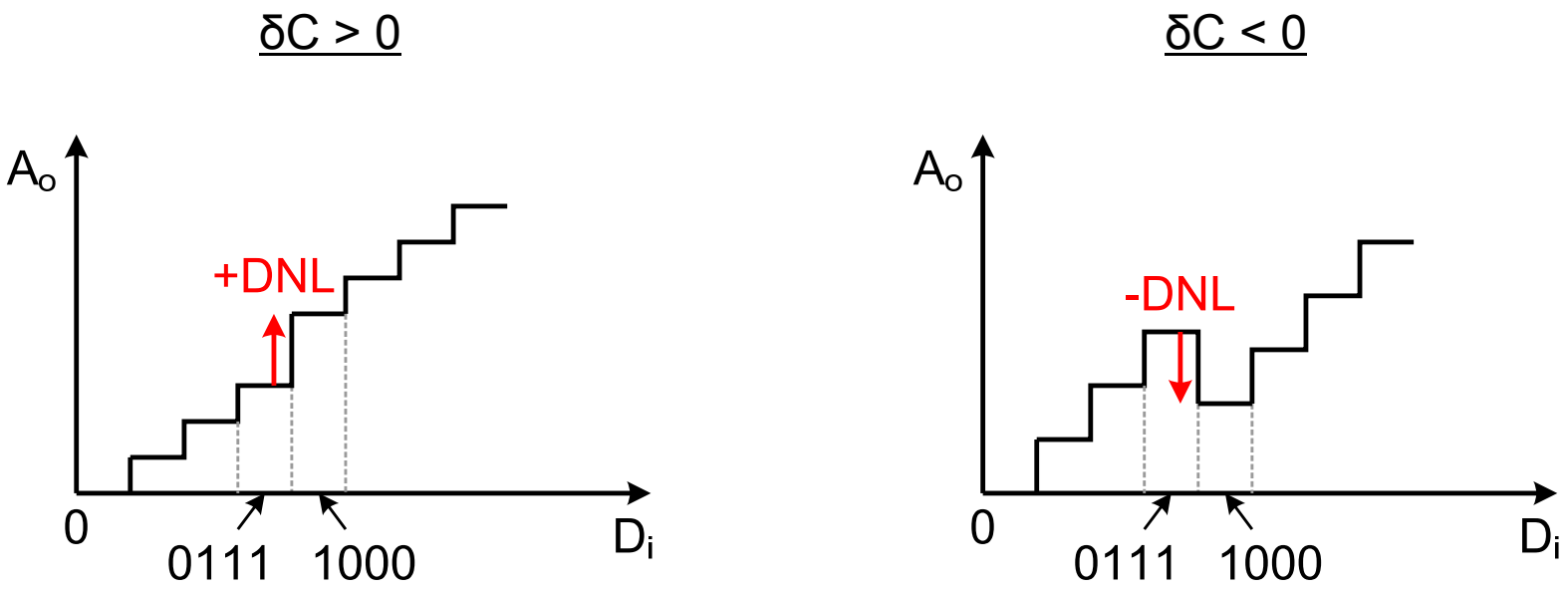
$$\text{Assume : } C_4 - (C_1 + C_2 + C_3) = C_u + \delta C,$$

$$\text{DNL} = [V_o(1000) - V_o(0111) - 1\text{LSB}]/1\text{LSB}$$

$$= \frac{\delta C}{\sum C} \Big/ \frac{C_u}{\sum C} = \delta C / C_u$$

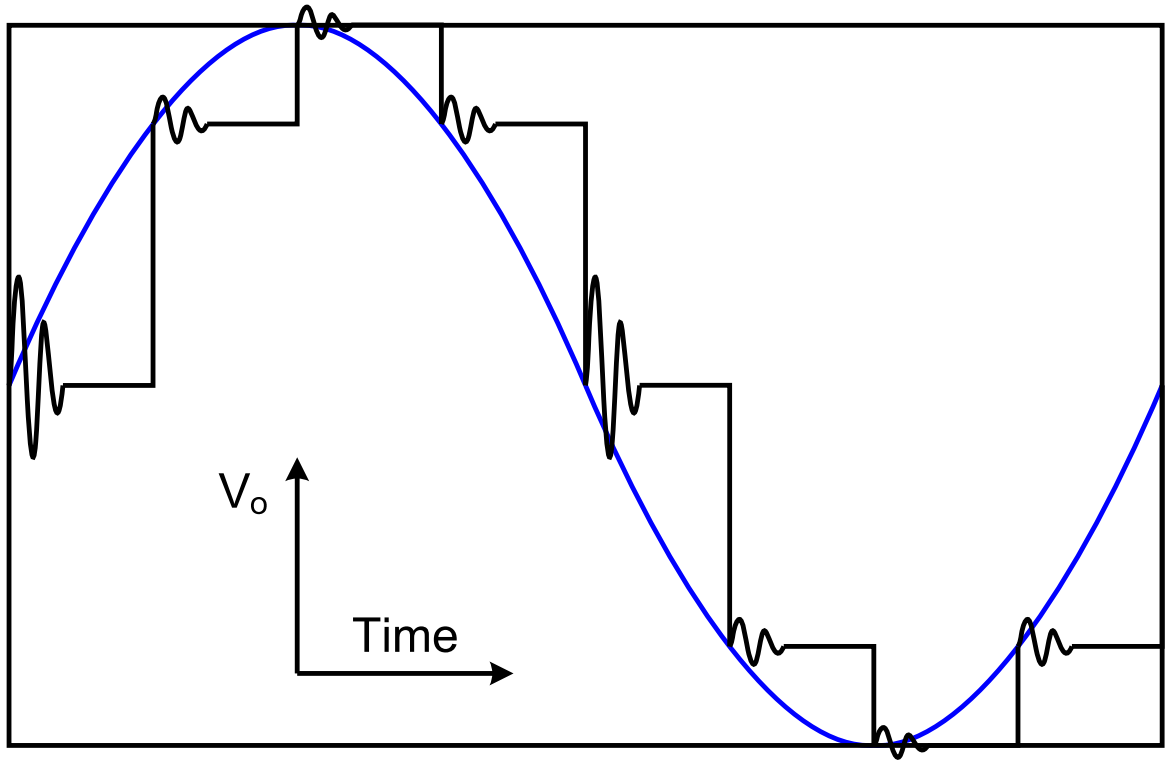
Largest DNL error occurs at the midpoint where MSB transitions, determined by the mismatch between the MSB capacitor and the rest of the array.

Midpoint DNL



- δC > 0 results in positive DNL.
- δC < 0 results in negative DNL or even nonmonotonicity.

Output Glitches



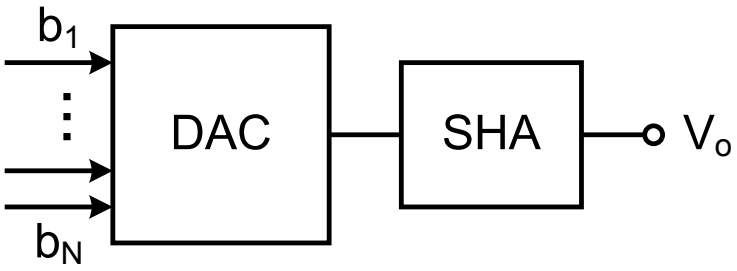
- Cause: Signal and clock skew in circuits
- Especially severe at MSB transition where all bits are switching –

  0111…111 →

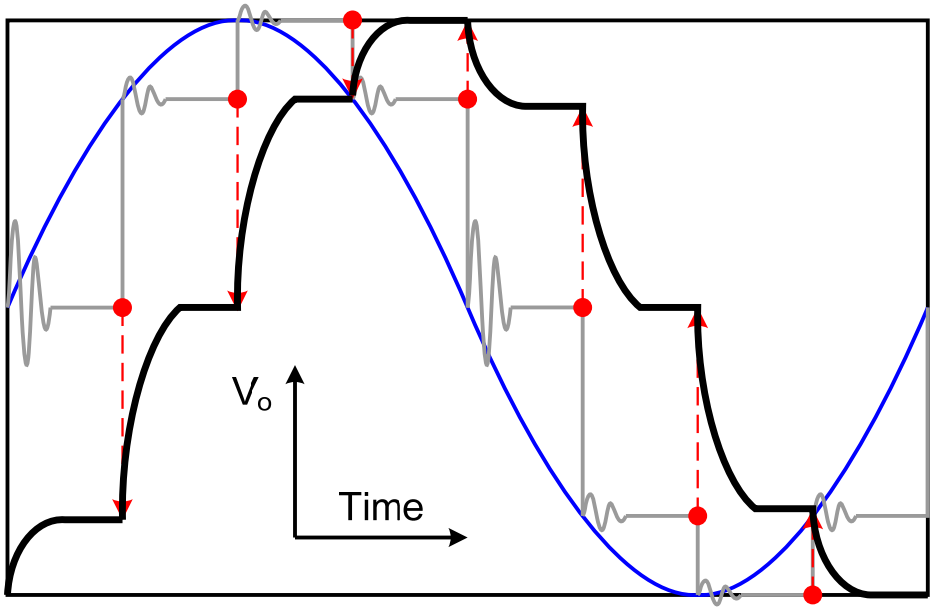
  1000…000

- Glitches cause waveform distortion, spurs and elevated noise floors.
- High-speed DAC output is often followed by a de-glitching SHA.

De-Glitching SHA

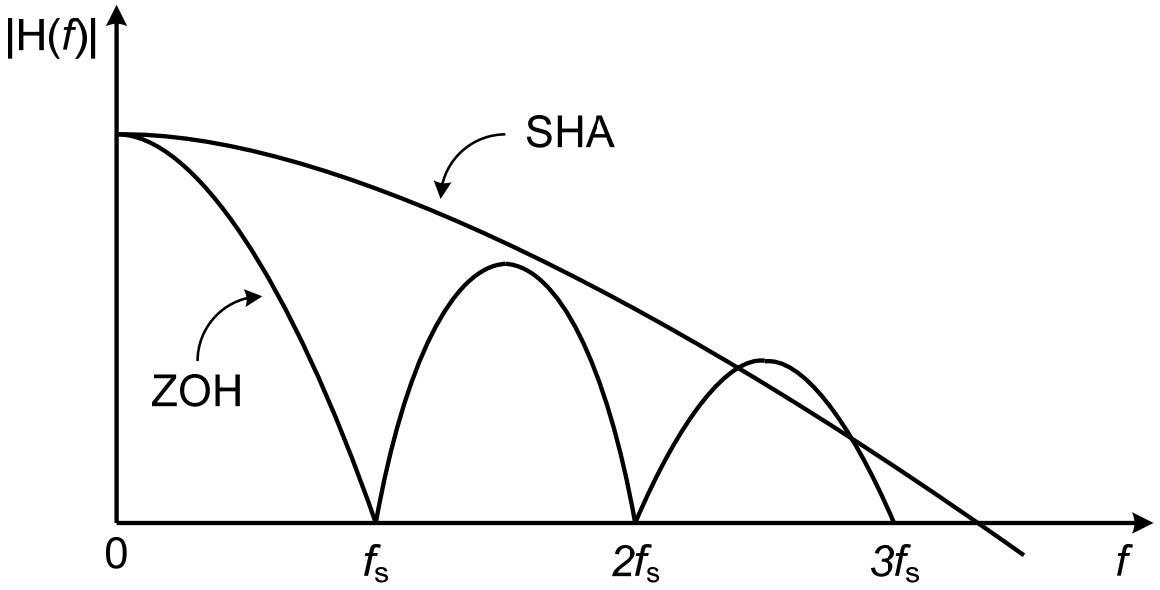


SHA samples the output of the DAC after it settles and then hold it for T, removing the glitching energy.



SHA output must be smooth (exponential settling can be viewed as pulse shaping → SHA BW does not have to be excessively large).

Frequency Response

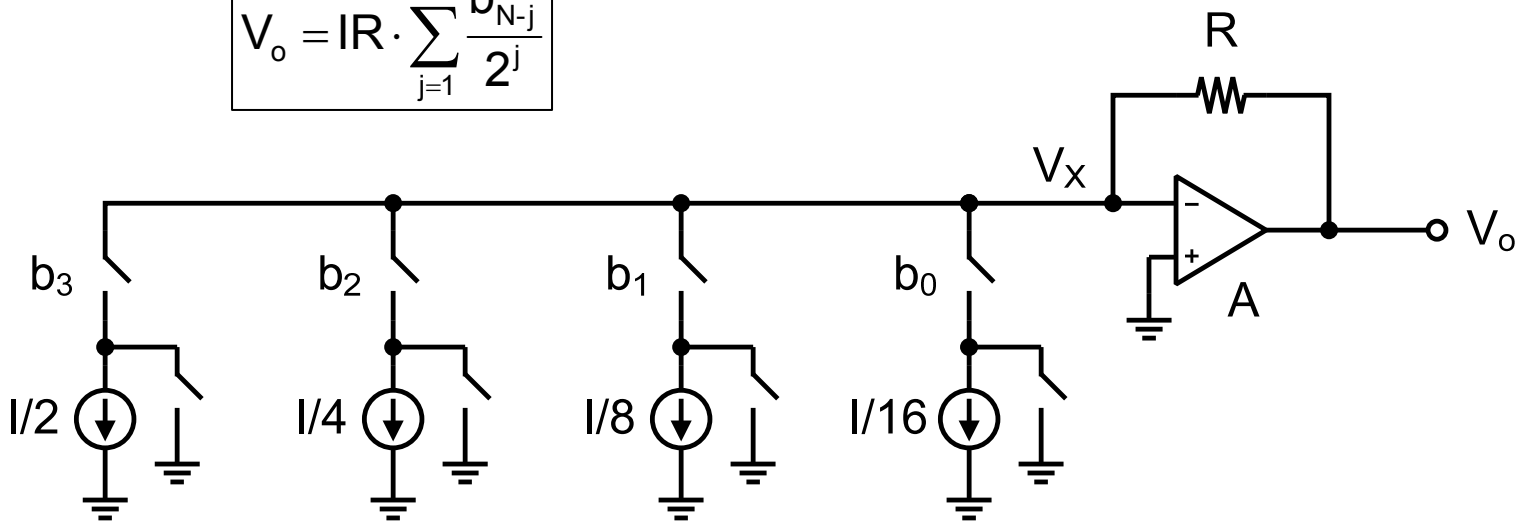


$$H_{ZOH}(j\omega) = e^{-j\frac{\omega T}{2}} \cdot \frac{\sin\left(\omega T/2\right)}{\omega T/2}$$

$$H_{SHA}(j\omega) = \frac{1}{1 + j\,\omega/\omega_{-3dB}}$$

Binary-Weighted Current DAC

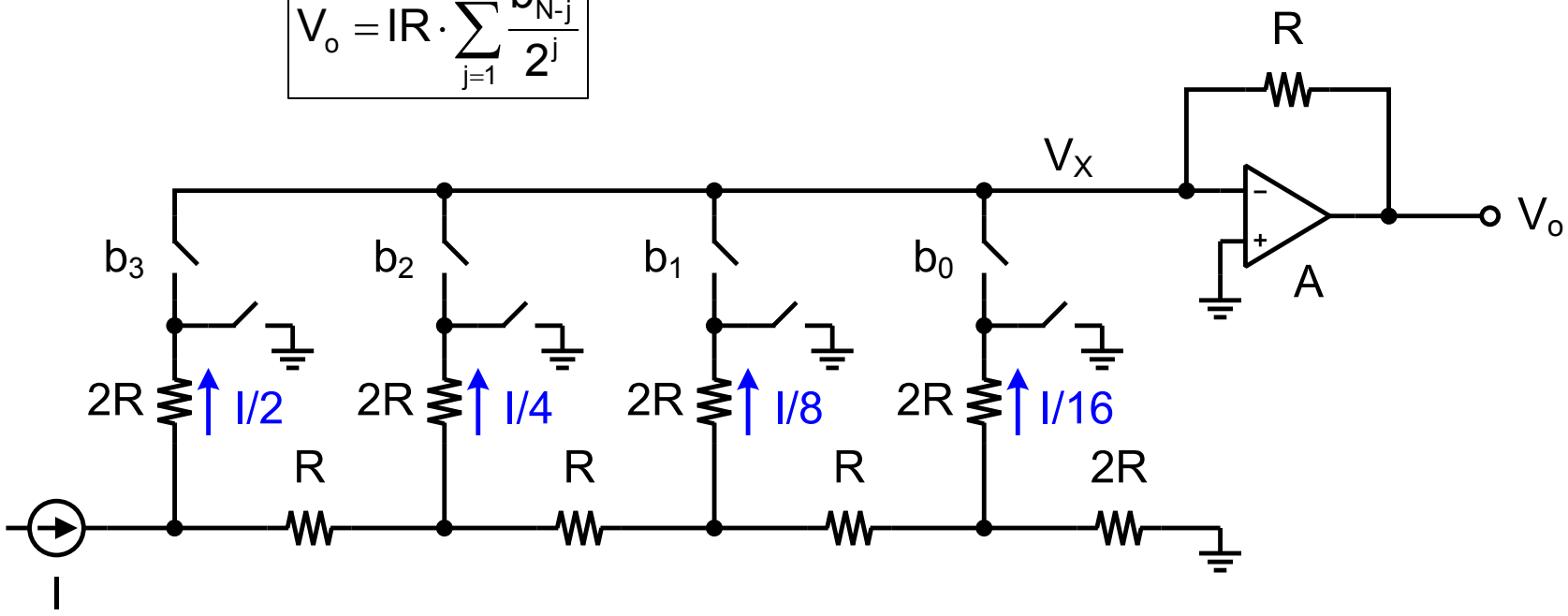
$$V_o = IR \cdot \sum_{j=1}^{N} \frac{b_{N-j}}{2^j}$$



- Current switching is simple and fast.
- V_o depends on R_{out} of current sources without op-amp.
- INL and DNL depend on matching, not inherently monotonic.
- Large component spread (2^{N-1}:1)

R-2R DAC

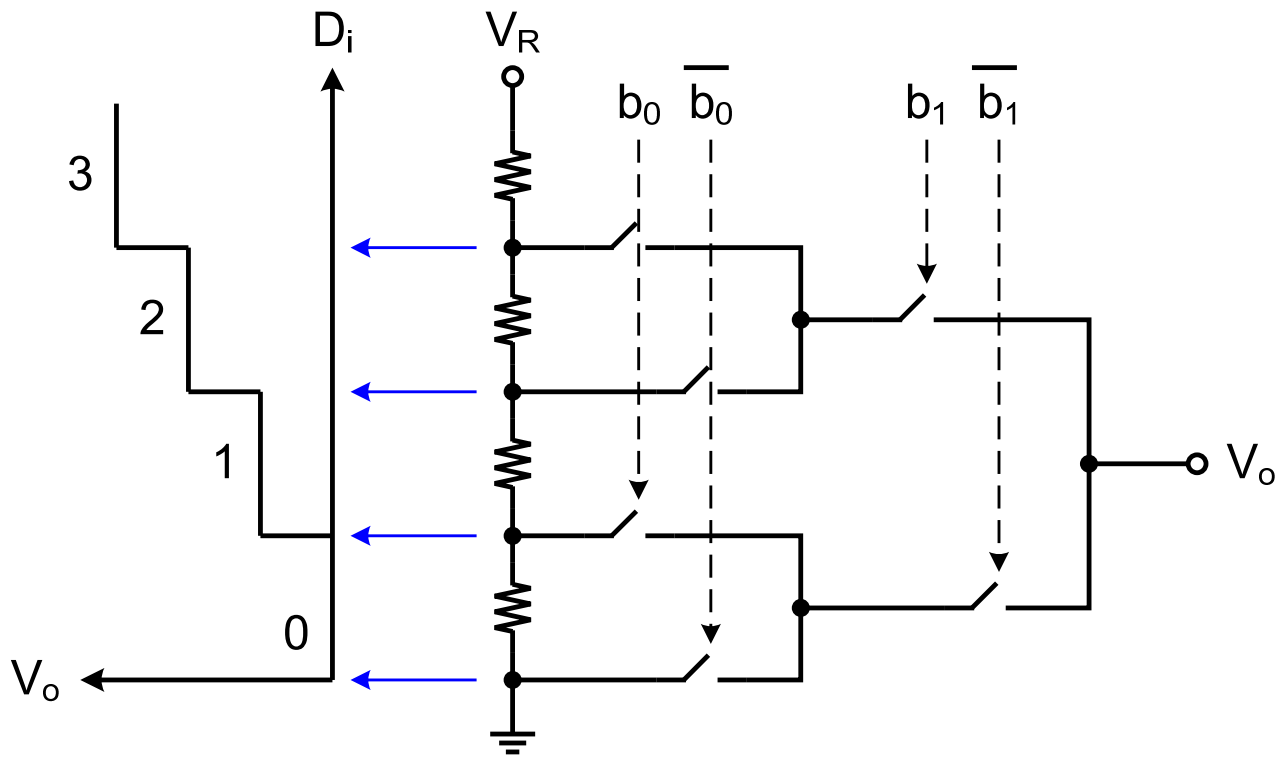
$$V_o = IR \cdot \sum_{j=1}^{N} \frac{b_{N-j}}{2^j}$$



- A binary-weighted current DAC
- Component spread greatly reduced (2:1)

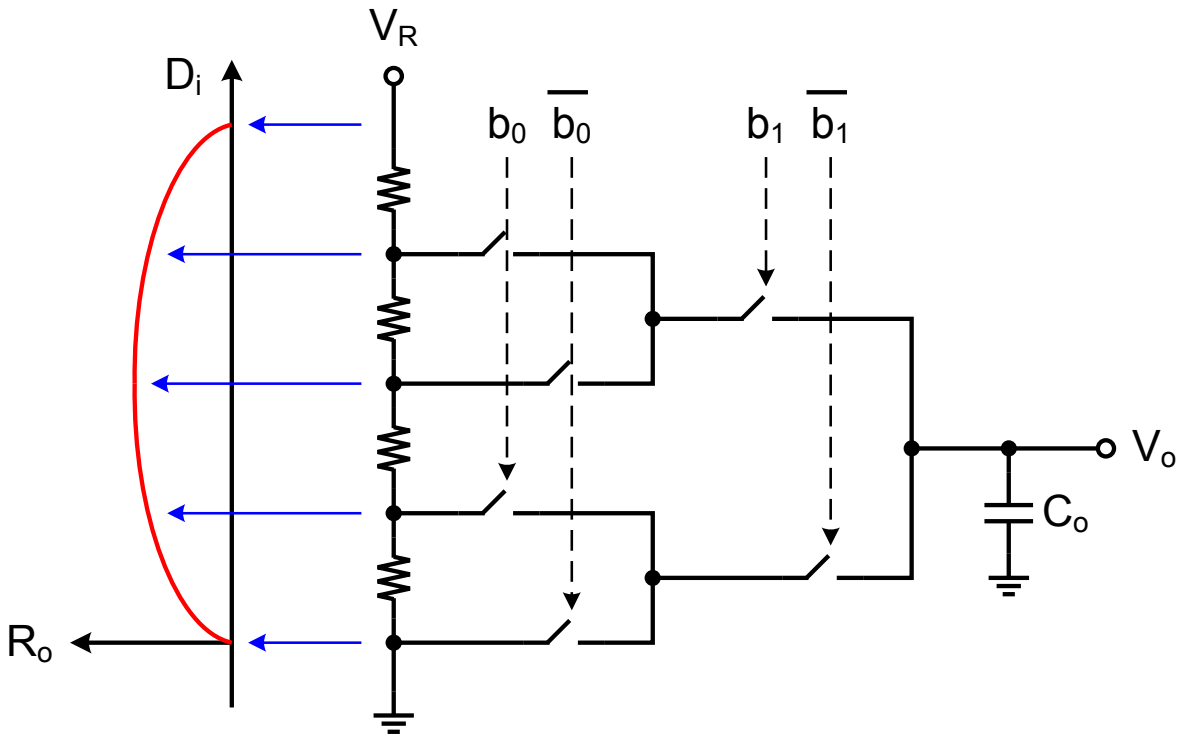
Unit-Element DAC

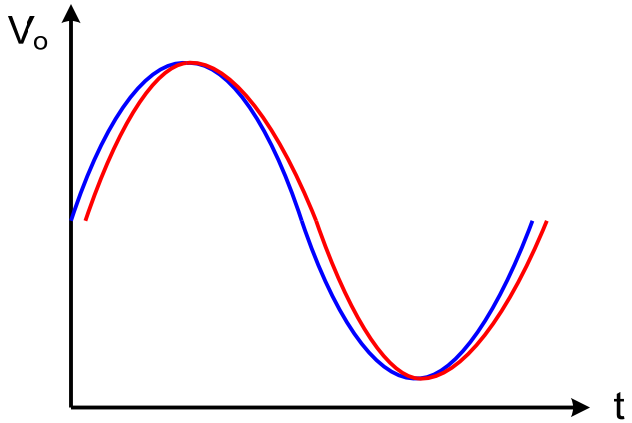
Resistor-String DAC



- Simple, inherently monotonic → good DNL performance
- Complexity ↑ speed ↓ for large N, typically N ≤ 8 bits

Code-Dependent R_o

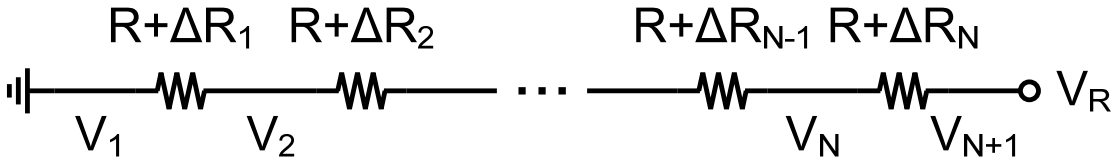




Signal-dependent R_oC causes HD.

- R_o of ladder varies with signal (code).
- On-resistance of switches depend on tap voltage.

INL and DNL



$$\Delta R = [0, \sigma_R]$$

$$V_j = \frac{\sum_{1}^{j-1} R_k}{\sum_{1}^{N} R_k} \cdot V_R = \frac{(j-1)R + \sum_{1}^{j-1} \Delta R_k}{NR + \sum_{1}^{N} \Delta R_k} \cdot V_R$$

$$V_{j-1} = \frac{(j-2)R + \sum_{1}^{j-2} \Delta R_k}{NR + \sum_{1}^{N} \Delta R_k} \cdot V_R$$

$$V_j - V_{j-1} = \frac{R + \Delta R_{j-1}}{NR + \sum_{1}^{N} \Delta R_k} \cdot V_R \approx \frac{V_R}{N} + \frac{\Delta R_{j-1}}{NR} \cdot V_R$$

$$DNL_j = \left(V_j - V_{j-1} - \frac{V_R}{N} \right) \Big/ \frac{V_R}{N} \approx \frac{\Delta R_{j-1}}{R} \quad \Rightarrow \quad \overline{DNL} = 0, \ \sigma_{DNL} = \frac{\sigma_R}{R}.$$

INL and DNL

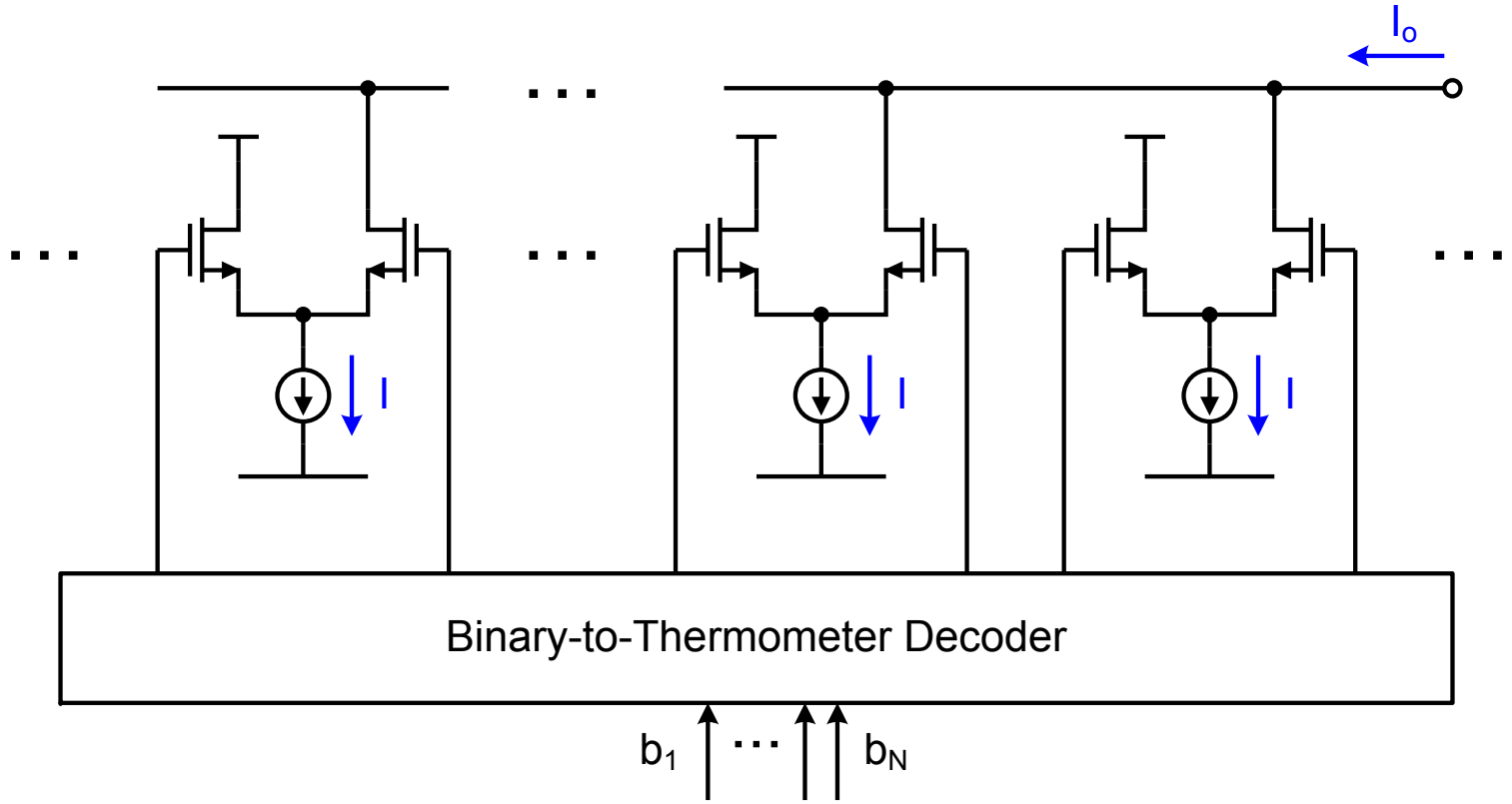
$$V_j = \frac{\sum_{1}^{j-1} R_k}{\sum_{1}^{N} R_k} \cdot V_R = \frac{(j-1)R + \sum_{1}^{j-1} \Delta R_k}{NR + \sum_{1}^{N} \Delta R_k} \cdot V_R \approx \frac{j-1}{N} V_R + \frac{(N-j+1)\sum_{1}^{j-1} \Delta R_k - (j-1)\sum_{j}^{N} \Delta R_k}{N^2 R} V_R$$

$$\Rightarrow \quad \overline{V_j} = \frac{j-1}{N} V_R, \quad \sigma_{V_j}{}^2 \approx \frac{(j-1)(N-j+1)}{N^3} \frac{\sigma_R{}^2}{R^2} V_R{}^2.$$

$$\Rightarrow \quad \sigma_{V_j}{}^2(\max) \approx \frac{1}{4N} \frac{\sigma_R{}^2}{R^2} V_R{}^2, \quad \text{when} \quad j = \frac{N}{2} + 1 \approx \frac{N}{2}.$$

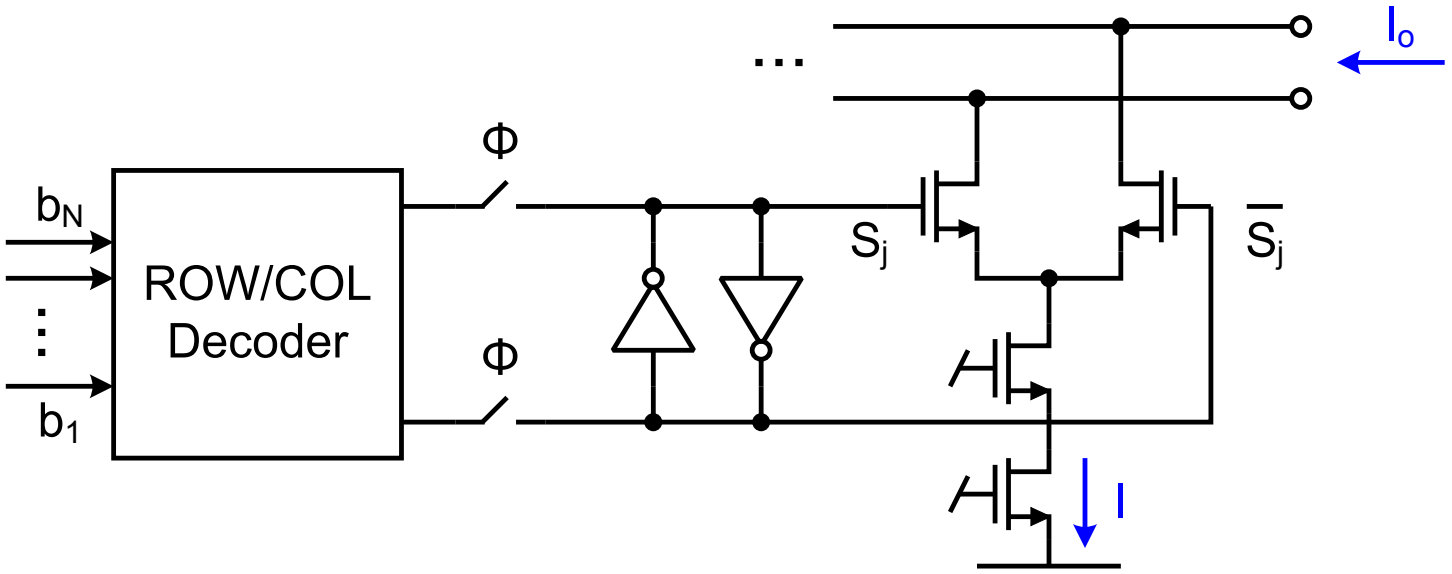
$$INL_j = \left(V_j - \frac{j-1}{N} V_R \right) \Big/ \frac{V_R}{N} \quad \Rightarrow \quad \overline{INL} = 0, \ \sigma_{INL}(\max) \approx \frac{\sqrt{N}}{2} \left(\frac{\sigma_R}{R} \right).$$

Current DAC



- Fast, inherently monotonic → good DNL performance
- Complexity increases for large N, requires B2T decoder.

Unit Current Cell



- 2^N current cells typically broken up into a ($2^{N/2}$ X $2^{N/2)}$ matrix
- Current source cascoded to improve accuracy
- Coupled inverters improve synchronization of current switches.

Segmented DAC

BW vs. UE DAC's

Binary-weighted DAC

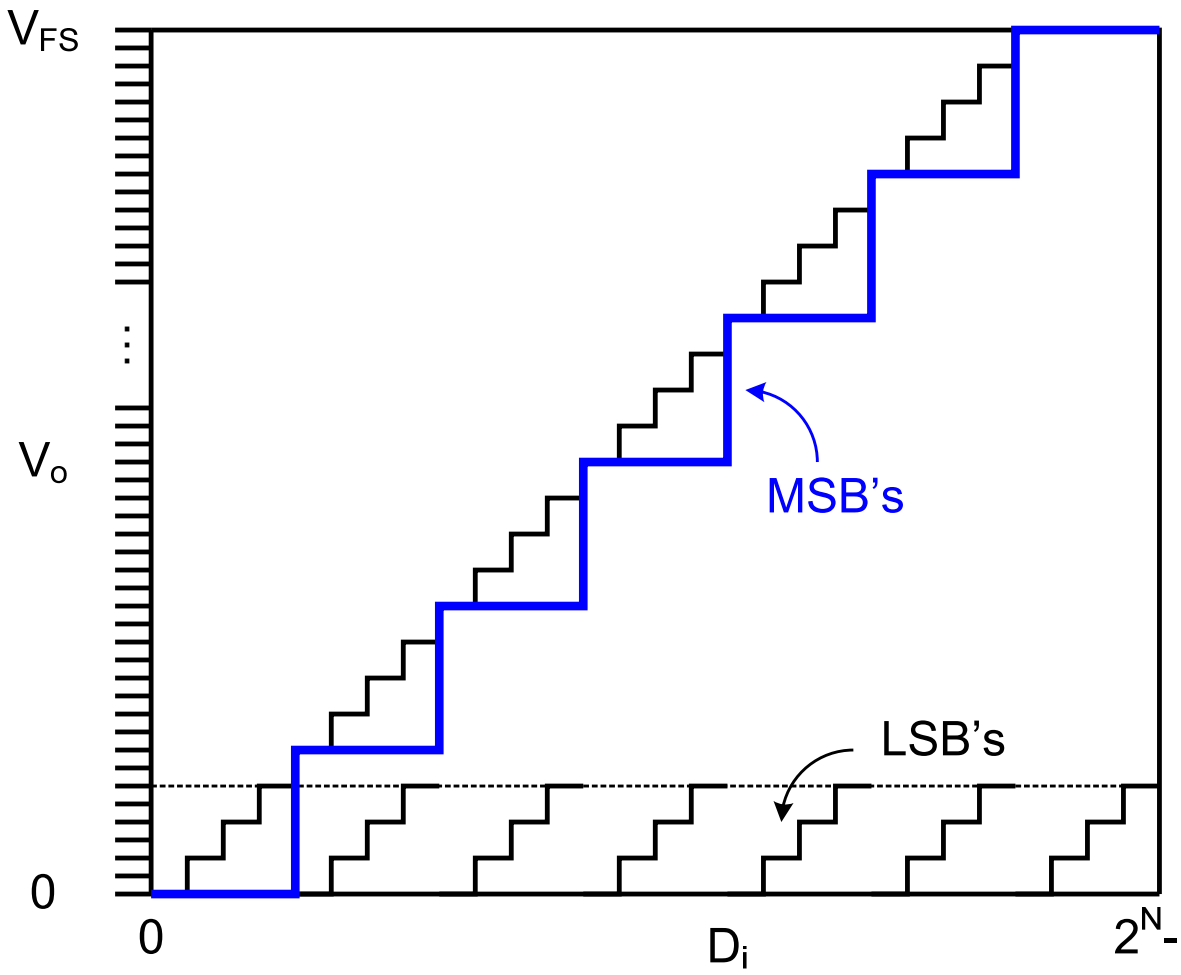
- Pros
  - Small
  - Simple
  - Min. switched elements
- Cons
  - Large DNL and glitches
  - Not guaranteed monotonic
- INL/DNL
  - INL(max) ≈ $(\sqrt{N}/2)\sigma$
  - DNL(max) ≈ 2*INL

Unit-element DAC

- Pros
  - Good DNL, small glitches
  - Linear glitch energy
  - Guaranteed monotonic
- Cons
  - Needs B2T decoder
  - Large area for N ≥ 8
- INL/DNL
  - INL(max) ≈ $(\sqrt{N}/2)\sigma$
  - DNL(max) ≈ σ

Combine BW and UE architectures → "segmentation"

Segmented DAC



- MSB DAC: M-bit UE DAC
- LSB DAC: L-bit BW DAC
- Resolution: N = M + L
- 2^M+L s.e.
- Good DNL
- Small glitches
- Same INL (depends on matching)

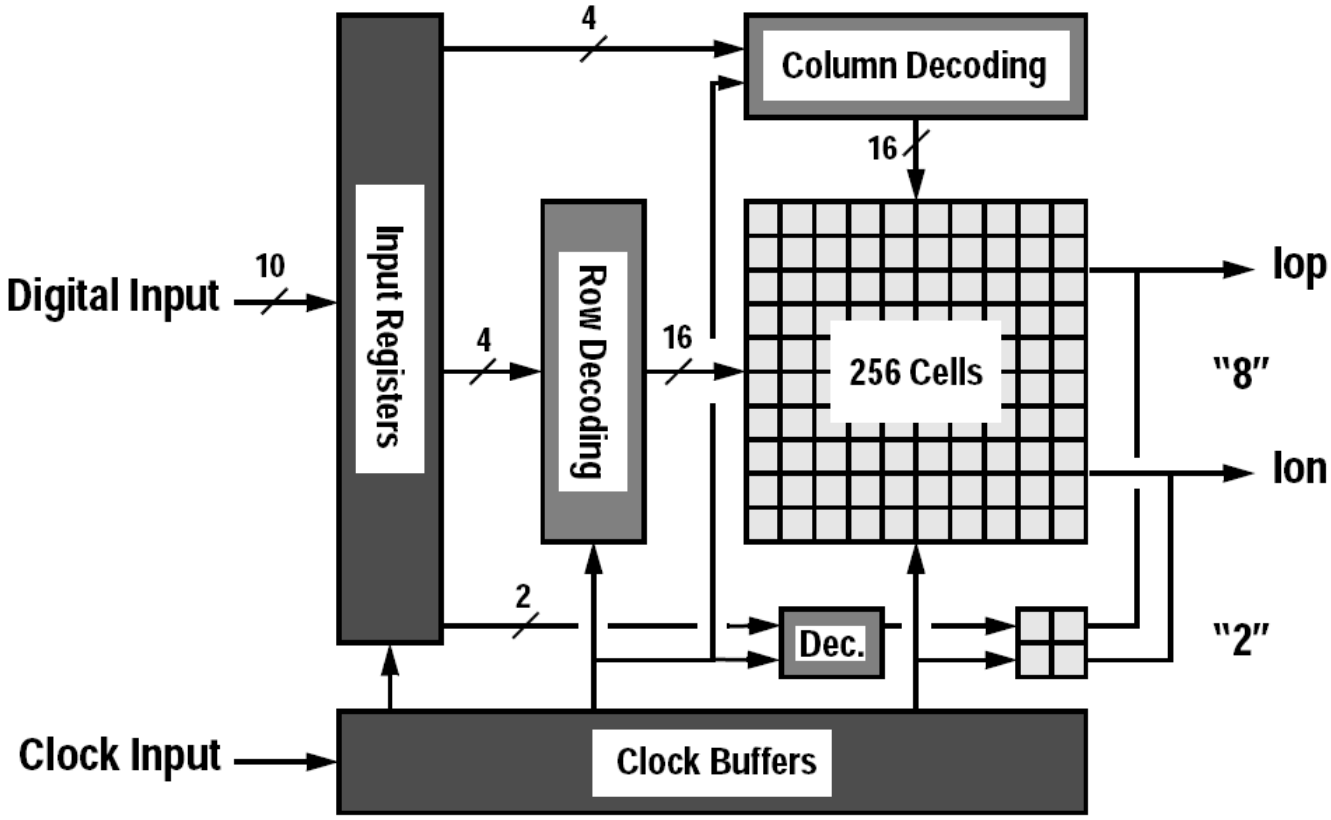
Comparison

Example: N = 12, M = 8, L= 4, σ = 1%

Architecture	σ_{INL}	σ_{DNL}	# of S.E.
Unit-Element	0.32 LSB's	0.01 LSB's	$2^N = 4096$
Binary-weighted	0.32 LSB's	0.64 LSB's	N = 12
Segmented	0.32 LSB's	0.06 LSB's	$2^M+L = 260$

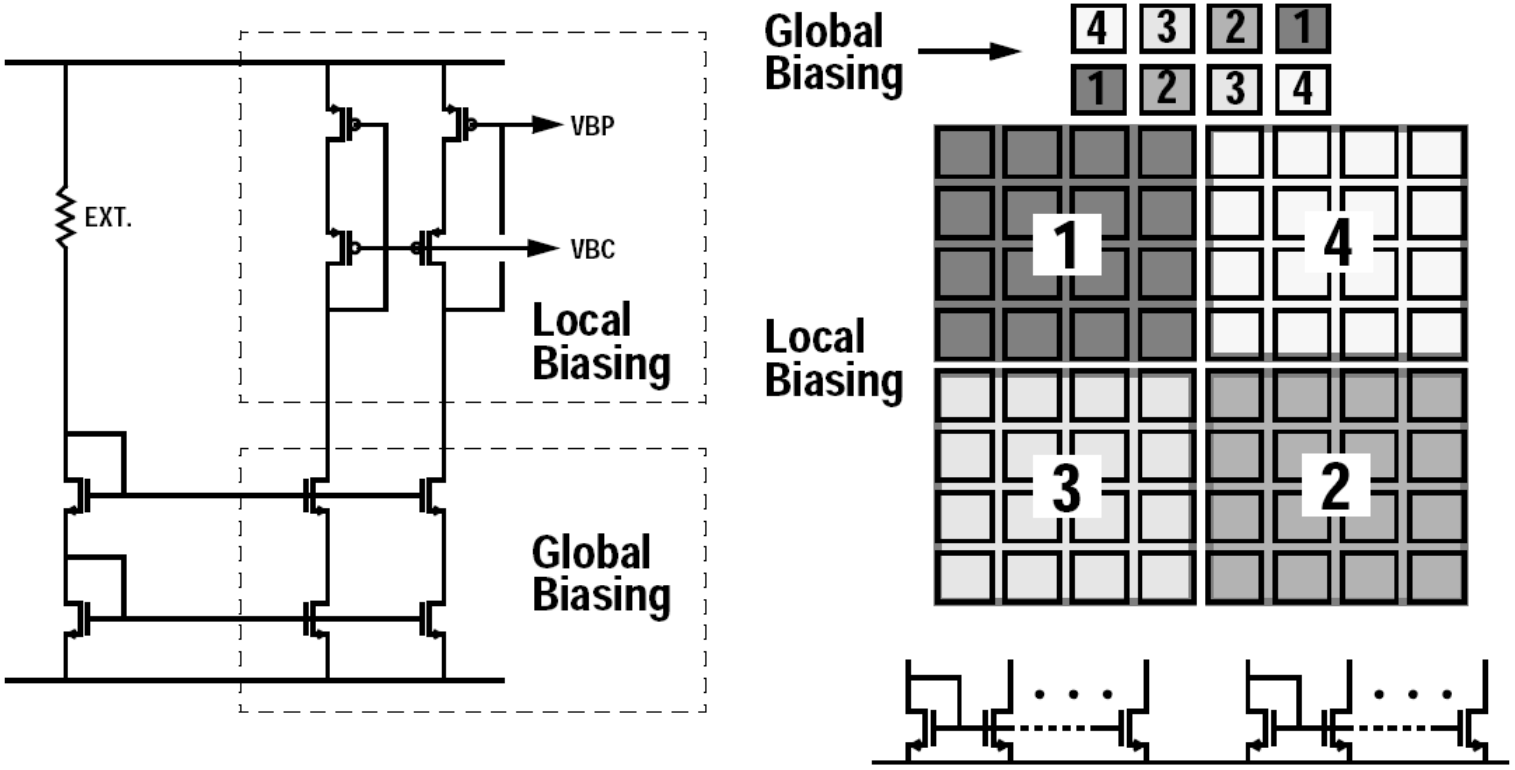
Max. DNL error occurs at the MSB segment transitions.

Example: “8+2” Segmented Current DAC



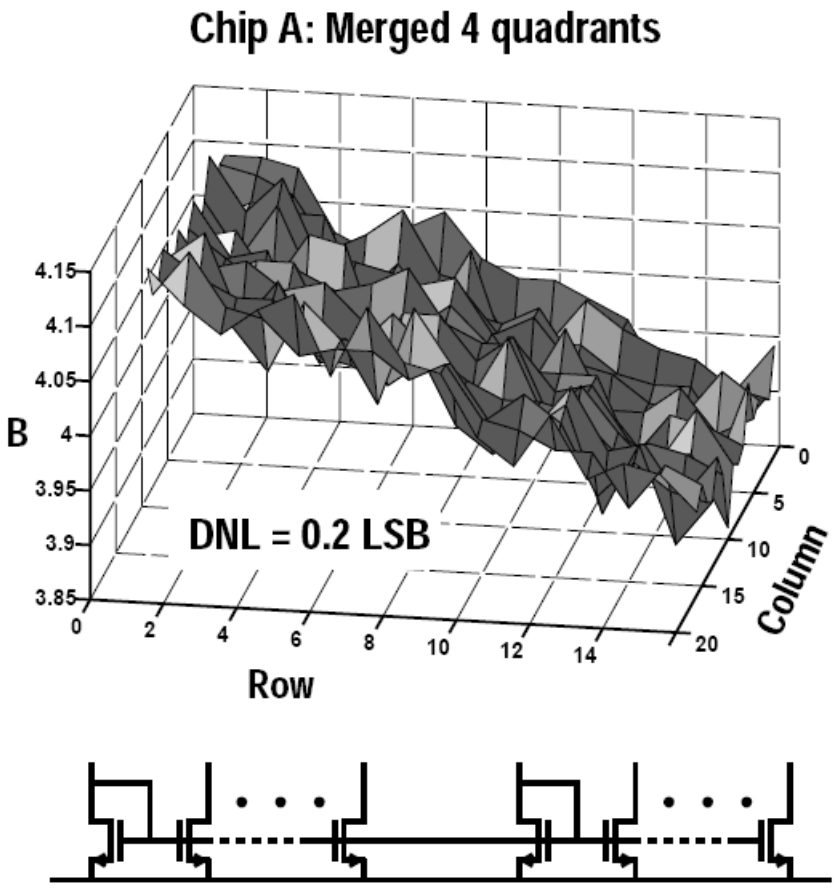
Ref: C.-H. Lin and K. Bult, "A 10-b, 500-MSample/s CMOS DAC in 0.6mm^2," *IEEE Journal of Solid-State Circuits*, vol. 33, pp. 1948-1958, issue 12, 1998.

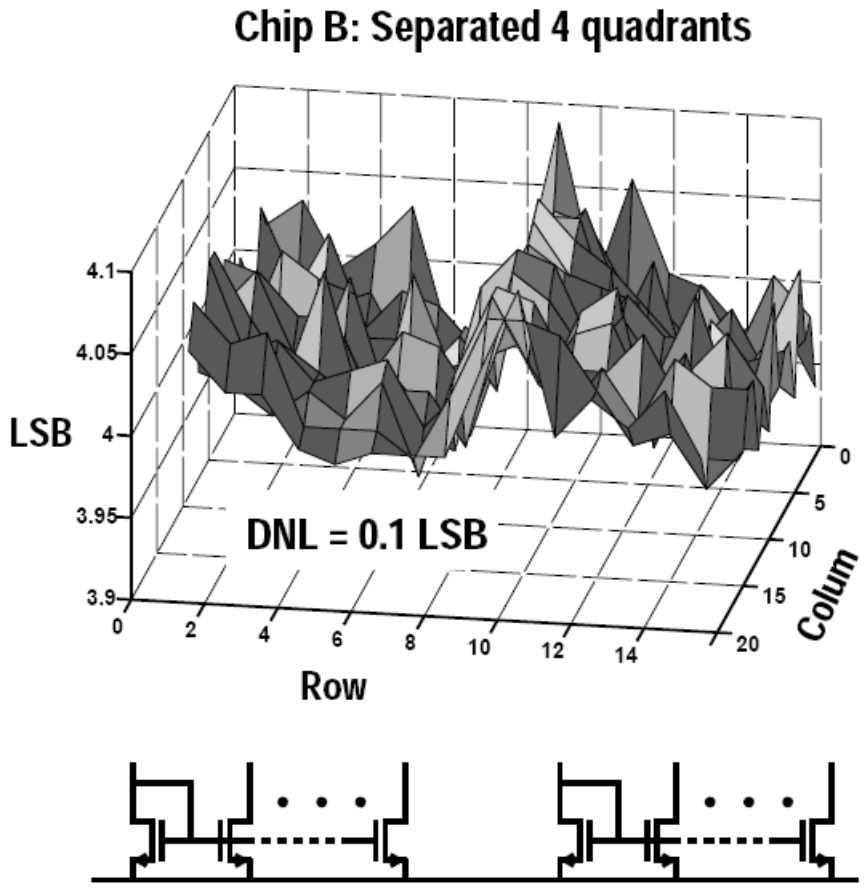
MSB-DAC Biasing Scheme



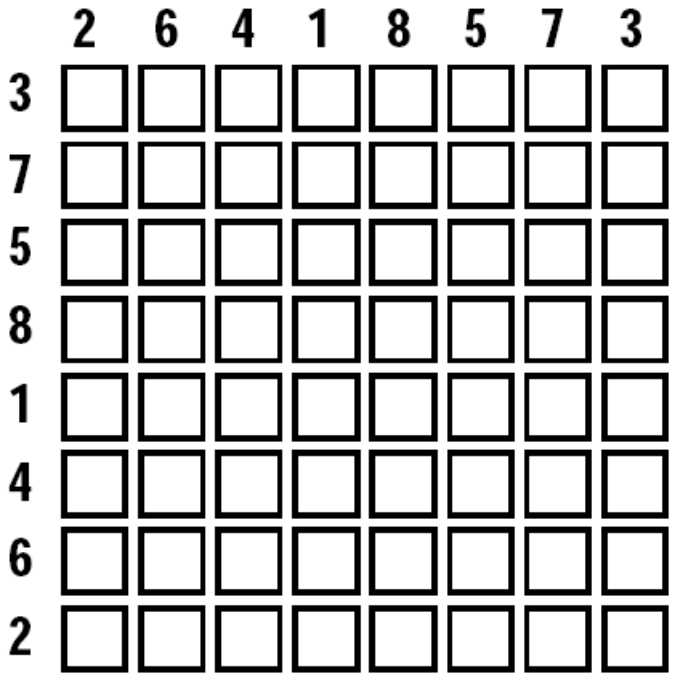
Common-centroid global biasing + divided 4 quadrants of current cells

MSB-DAC Biasing Scheme

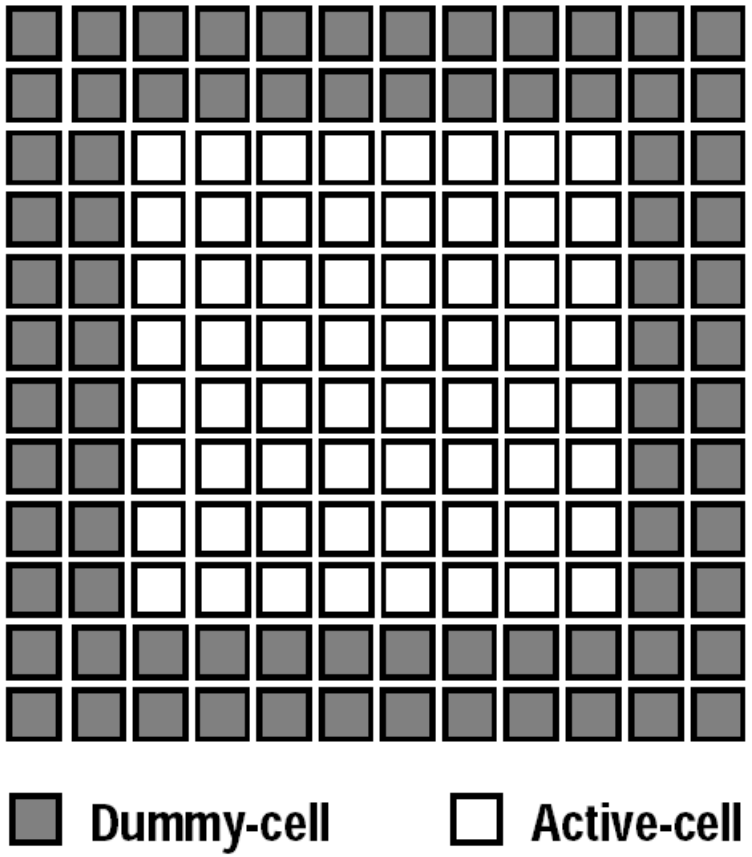




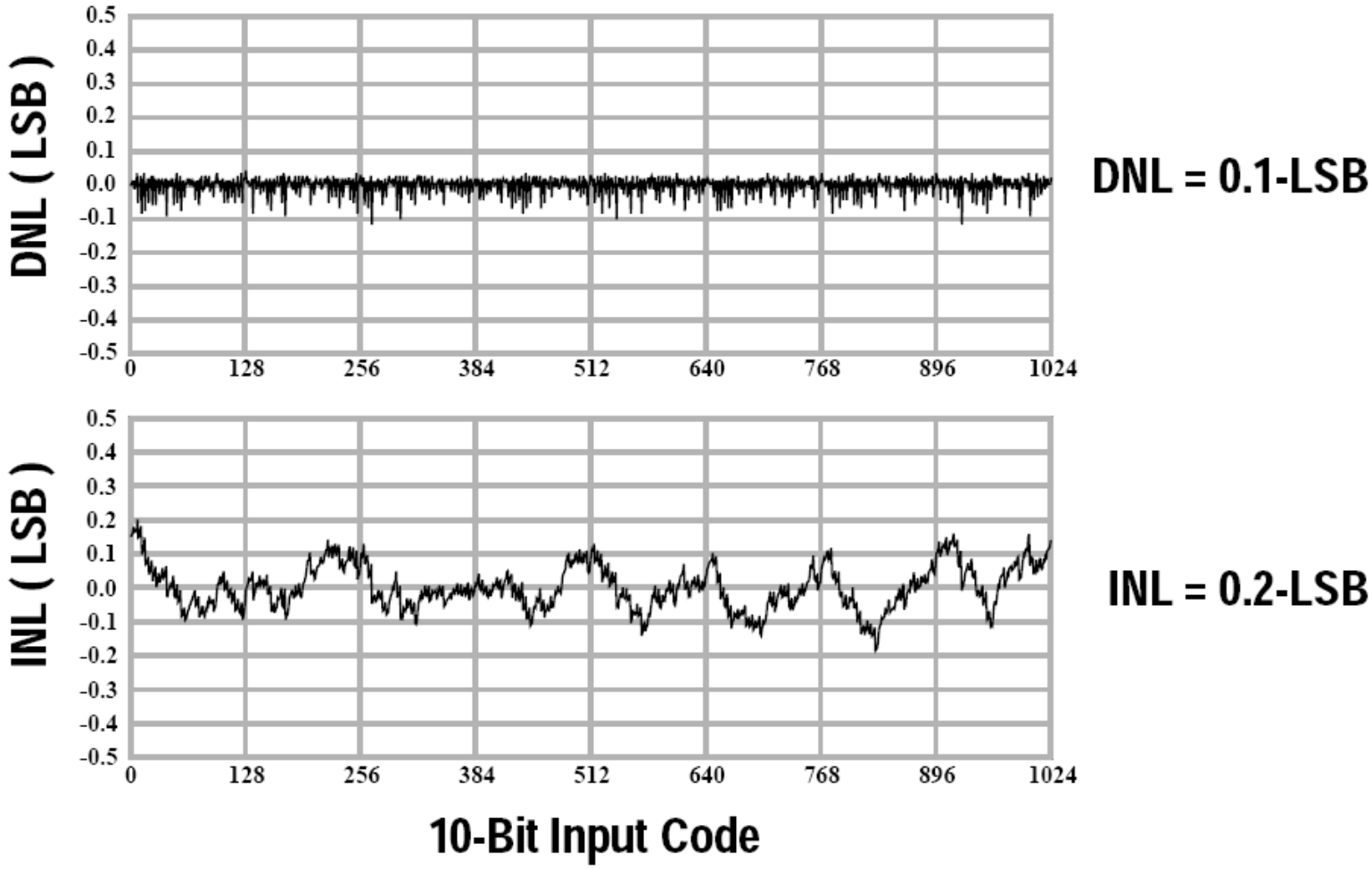
Randomization and Dummies



- Column and row randomization to improve INL



Measured INL and DNL



Summary

- Nyquist DAC architectures
  - Binary-weighted DAC
  - Unit-element (thermometer-coded) DAC
  - Segmented DAC
  - Resistor-string, current, charge-redistribution DAC's
- Oversampling DAC
  - Oversampling performed in digital domain (zero stuffing)
  - Digital noise shaping (ΣΔ modulator)
  - 1-bit DAC can be used
  - Analog reconstruction/smoothing filter

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