ELEN 689:Special Topics
Advanced Mixed-Signal Interfaces

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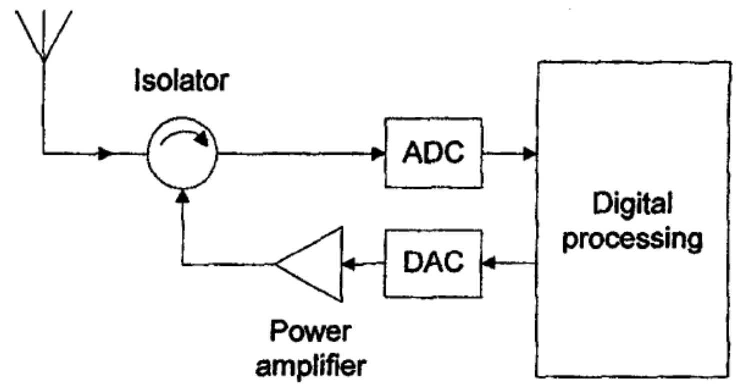
A Lot of New Names for Future Broadband Communication Systems

- The Names

  - Software Defined Radios
  - Multi-Standard Radios
  - Cognitive Radios
  - Universal Radios



- Common Features

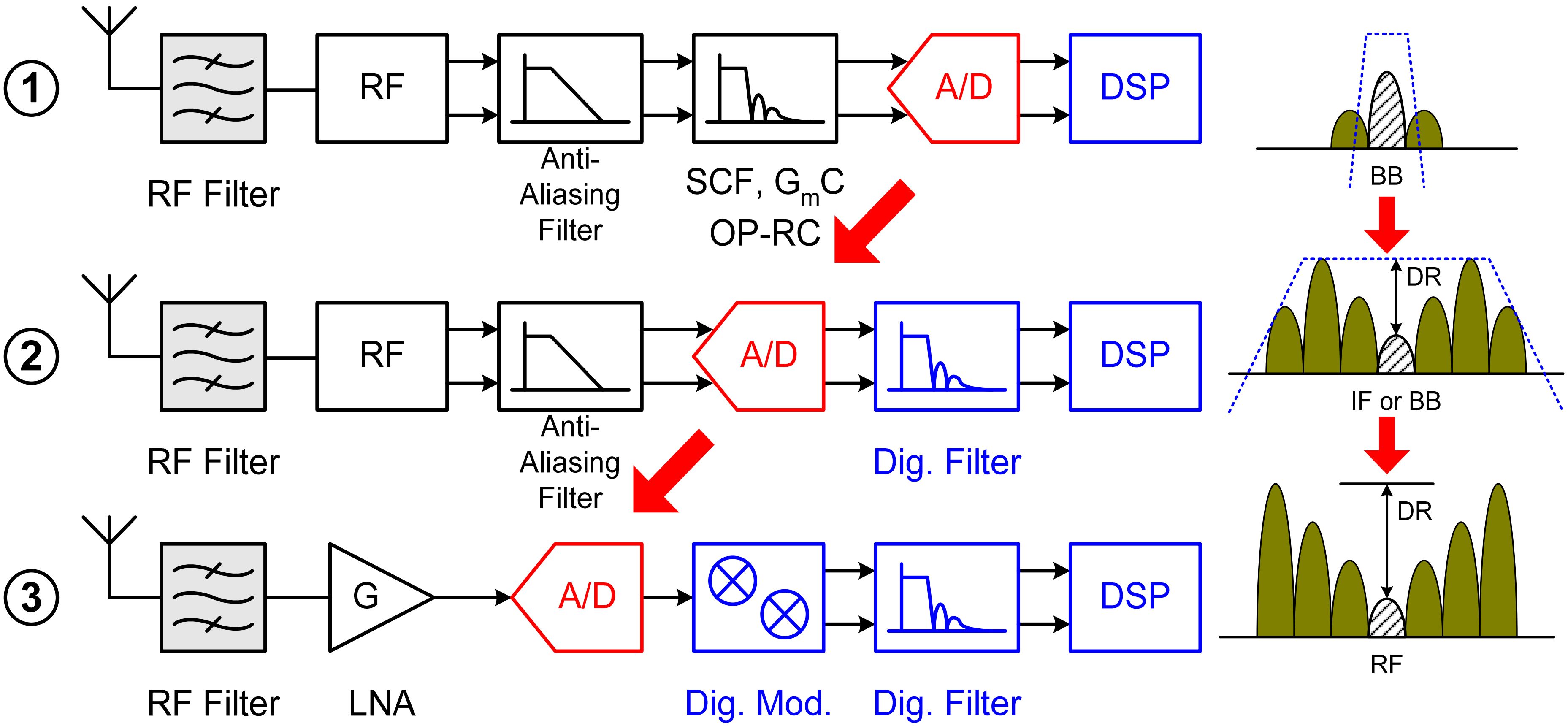
  - Very wideband systems, multiband channels, opportunistic frequency allocation, bandwidth reuse, intensely digital, scalable/reconfigurable RF/analog.

- Challenges

  - Conflicting requirements, large bandwidth/dynamic range but still want low power/small area.

Receiver Topologies

The Receiver Design Problem in Broadband Communications



- How much RF processing do I do before the ADC?
- How do I take advantage of technology scaling in this RF pre-procesing?
- How do I make the front-end scalable and configurable to fit multiple standards?

Conventional Receivers

- Superheterodyne Receiver
- Single Conversion Receiver
- Upconversion
- Dual Conversion
- Image-Reject Receiver (Complex I&Q mixing)
- Direct Conversion Receiver

Image Rejection

➢ In high-IF RF receivers, RF LC or SAW filters are used to suppress the image before the down-conversion. Larger IFs are preferable to relax the filter Q factor.

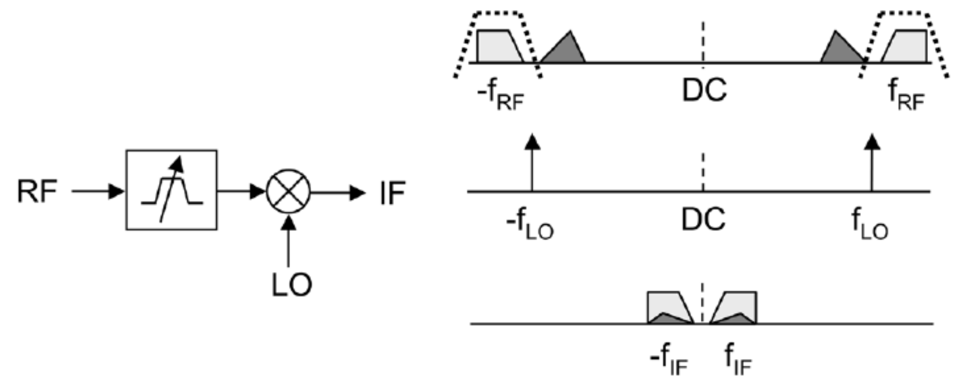


Fig. 1. Conventional receiver with RF image filter.

➢ Ideally zero IF does not require the RF filter but still suffers from gain and phase mismatches.

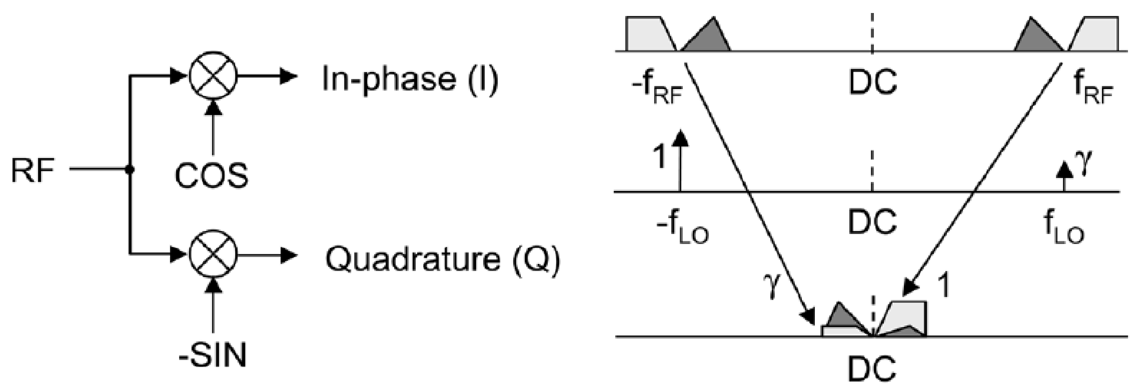


Fig. 2. Direct-conversion receiver.

Supisa Lerstaveesin, and Bang-Sup Song: "A Complex Image Rejection Circuit With Sign Detection Only," IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 41, NO. 12, DECEMBER 2006

Image Rejection Ratio

- The identities

$$\cos(x)\cos(y) = \frac{1}{2}[\cos(x-y) + \cos(x+y)]$$

$$\cos(x)\sin(y) = \frac{1}{2}[\sin(x+y) - \sin(x-y)]$$

$$I_{LO} = B\cos(\omega_{LO}t)$$
$$Q_{LO} = A\sin(\omega_{LO}t)$$
$$x_{RF} = \cos(\omega_{RF}t)$$

$$I_{LO} * x_{RF} = \frac{B}{2}[\cos((\omega_{RF}+\omega_{LO})t) + \cos((\omega_{RF}-\omega_{LO})t)] \xrightarrow{LPF} \frac{B}{2}\cos(\omega_{IF}t) \rightarrow \frac{B}{2}\cos(\omega_{IF}\tau) + \frac{A}{2}\cos(\omega_{IF}\tau)$$

$$Q_{LO} * x_{RF} = \frac{A}{2}[\sin((\omega_{RF}+\omega_{LO})t) - \sin((\omega_{RF}-\omega_{LO})t)] \xrightarrow{LPF} -\frac{A}{2}\sin(\omega_{IF}t) \xrightarrow{90^o} \frac{A}{2}\cos(\omega_{IF}t)\uparrow$$

$$\omega_{IF} = \omega_{RF} - \omega_{LO}$$
$$x_{IMAGE} = \cos((\omega_{LO} - \omega_{IF})t)$$

$$I_{LO} * x_{IMAGE} = \frac{B}{2}[\cos((\omega_{LO}-\omega_{IF}+\omega_{LO})t) + \cos((\omega_{LO}-\omega_{IF}-\omega_{LO})t)] \xrightarrow{LPF} \frac{B}{2}\cos(\omega_{IF}t) \rightarrow \frac{B}{2}\cos(\omega_{IF}t) - \frac{A}{2}\cos(\omega_{IF}t)$$

$$Q_{LO} * x_{IMAGE} = \frac{A}{2}[\sin((\omega_{LO}-\omega_{IF}+\omega_{LO})t) - \sin((\omega_{LO}-\omega_{IF}-\omega_{LO})t)] \xrightarrow{LPF} \frac{A}{2}\sin(\omega_{IF}t) \xrightarrow{90^o} -\frac{A}{2}\cos(\omega_{IF}t)\uparrow$$

$$IRR_{gain} = \left[\frac{A+B}{A-B}\right]^2 = \left[\frac{1+B/A}{1-B/A}\right]^2 = \left[\frac{1+(1+\varepsilon)}{1-(1+\varepsilon)}\right]^2 \approx \frac{4}{\varepsilon^2}$$

$$IRR_{phase} = 1 + 4*(\cot\Delta\phi)^2 = \frac{4}{(\Delta\phi)^2}$$

$$IRR_{total} \approx \frac{4}{(\Delta\phi)^2 + \varepsilon^2}$$

- 0.1% gain error and 1º phase error leads to IRR of about 41 dB.

The design of CMOS Radio-Frequency Integrated Circuits, Thomas H. Lee.

Image Rejection Ratio

- HW # 4: Find the IRR for the case the input comes with a quadrature component as well, i.e., $x_{RF} = I_D \cos(\omega_{RF} t) + Q_D \sin(\omega_{RF} t)$ and a direct zero-IF receiver is used.

Basic Equations of Image Rejection

- Gain mismatch *α* and phase mismatch *θ :*

$$I' = \left(1+\frac{\alpha}{2}\right)\cos(\omega t+\frac{\theta}{2})$$

$$= \left(1+\frac{\alpha}{2}\right)\left\{\frac{e^{j(\omega t+\frac{\theta}{2})}+e^{-j(\omega t+\frac{\theta}{2})}}{2}\right\} \quad (1)$$

$$Q' = \left(1-\frac{\alpha}{2}\right)\sin\left(\omega t-\frac{\theta}{2}\right)$$

$$= \left(1-\frac{\alpha}{2}\right)\left\{\frac{e^{j(\omega t-\frac{\theta}{2})}-e^{-j(\omega t-\frac{\theta}{2})}}{2j}\right\}. \quad (2)$$

Then, assuming α and θ are small, the non-ideal complex signal $I'+jQ'$ and the non-ideal complex image $I'-jQ'$ can be approximated using Taylor series.

$$I'+jQ' \approx e^{j\omega t}+\left(\frac{\alpha-j\theta}{2}\right)e^{-j\omega t} \quad (3)$$

$$I'-jQ' \approx \left(\frac{\alpha+j\theta}{2}\right)e^{j\omega t}+e^{-j\omega t}. \quad (4)$$

Supisa Lerstaveesin, and Bang-Sup Song: "A Complex Image Rejection Circuit With Sign Detection Only," IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 41, NO. 12, DECEMBER 2006

Matrix Formulation

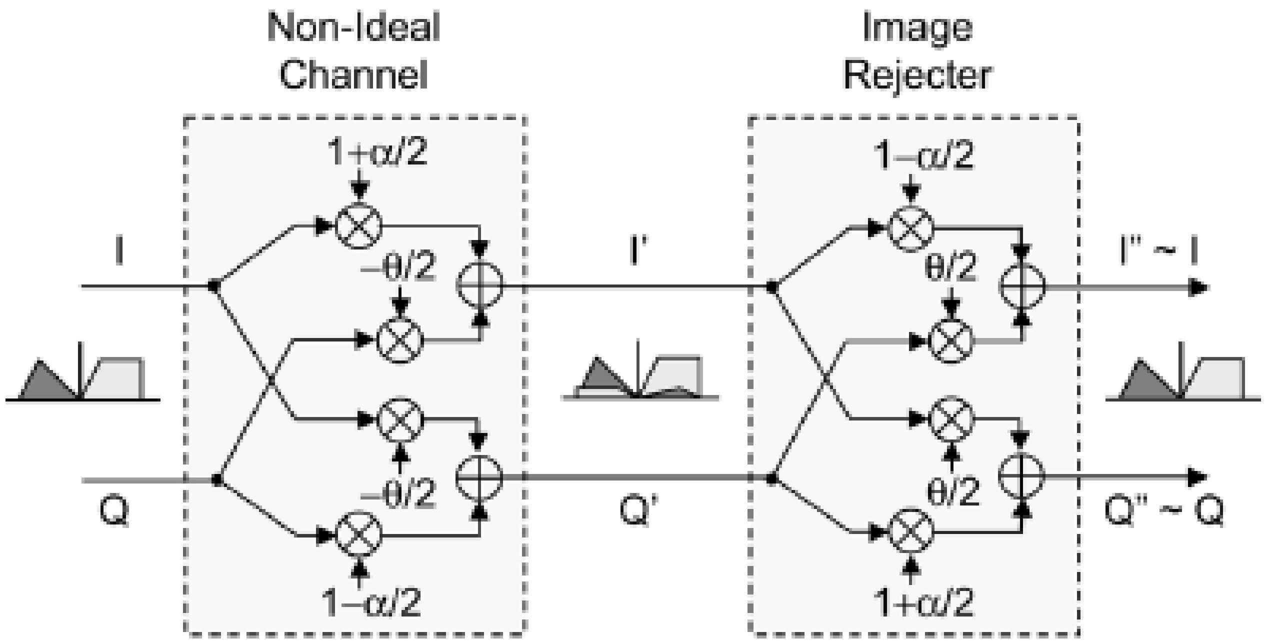


Fig. 5. Proposed image rejection concept.

- Matrix formulation of the non-ideal mixing :

$$\begin{bmatrix} I' \\ Q' \end{bmatrix} = \begin{bmatrix} 1+\frac{\alpha}{2} & -\frac{\theta}{2} \\ -\frac{\theta}{2} & 1-\frac{\alpha}{2} \end{bmatrix} \begin{bmatrix} I \\ Q \end{bmatrix}.$$

- Matrix formulation of the non-idealities correction :

$$\begin{bmatrix} I'' \\ Q'' \end{bmatrix} = \begin{bmatrix} 1-\frac{\alpha}{2} & \frac{\theta}{2} \\ \frac{\theta}{2} & 1+\frac{\alpha}{2} \end{bmatrix} \begin{bmatrix} I' \\ Q' \end{bmatrix}.$$

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LMS algorithm for the estimation of α and θ

$$\alpha'[k+1] = \alpha'[k] + \mu_\alpha \mathrm{sgn}[\mathrm{LPF}\{\mathrm{sgn}(I+Q) \cdot \mathrm{sgn}(I-Q)\}]$$

$$\theta'[k+1] = \theta'[k] - \mu_\theta \mathrm{sgn}[\mathrm{LPF}\{\mathrm{sgn}(I) \cdot \mathrm{sgn}(Q)\}]$$

- Fully-digital implementation

$$\mathrm{LPF}(I^2 - Q^2) = \frac{\left(1+\frac{\alpha}{2}\right)^2}{2} - \frac{\left(1-\frac{\alpha}{2}\right)^2}{2} \approx \alpha.$$

$$\mathrm{LPF}(IQ) = -\theta \frac{\left(1 - \frac{\alpha^2}{4}\right)}{2} \approx -\frac{\theta}{2}.$$

2^{20} iterations needed!!

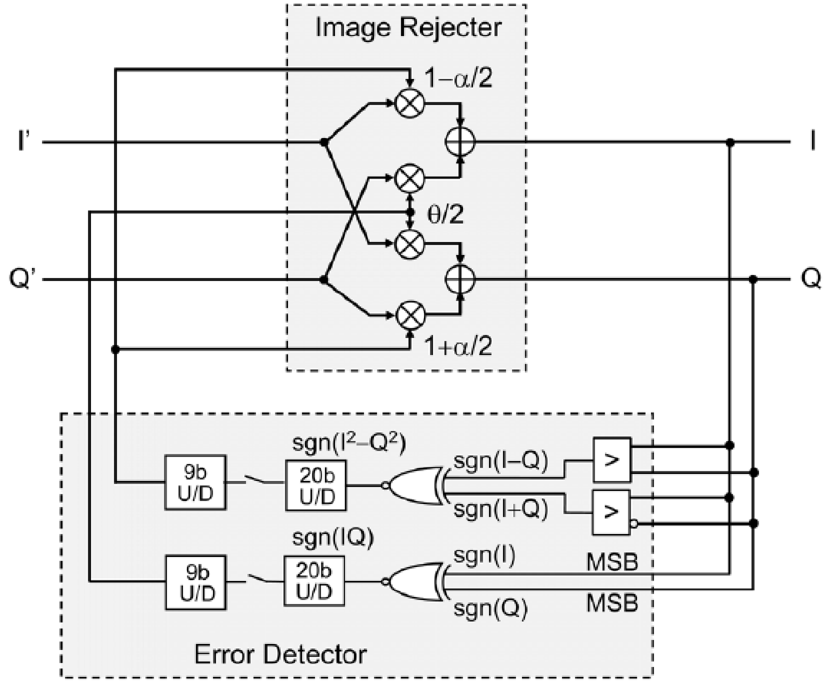

Fig. 12. Image rejection system.

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Analog Implementation

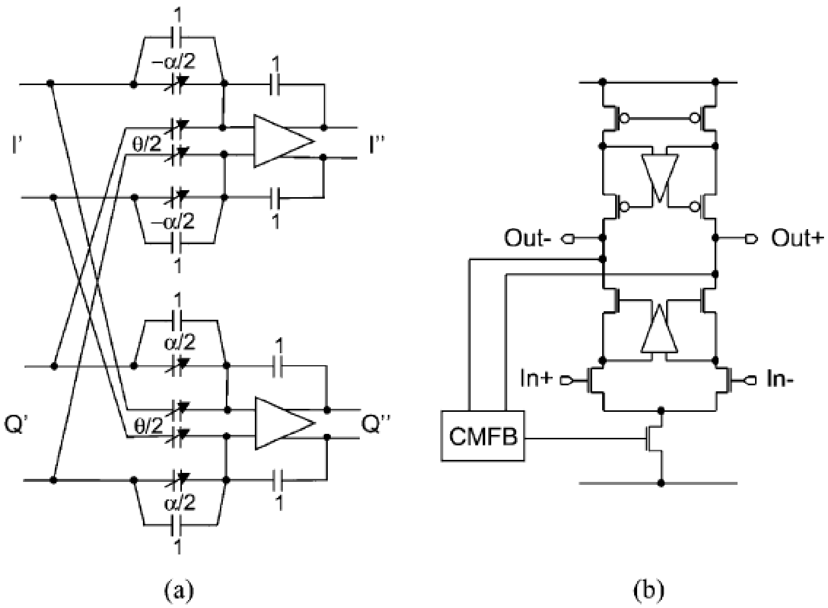


Fig. 13. (a) Complex baseband S/H. (b) Gain-boosted telescopic cascoded operational amplifier.

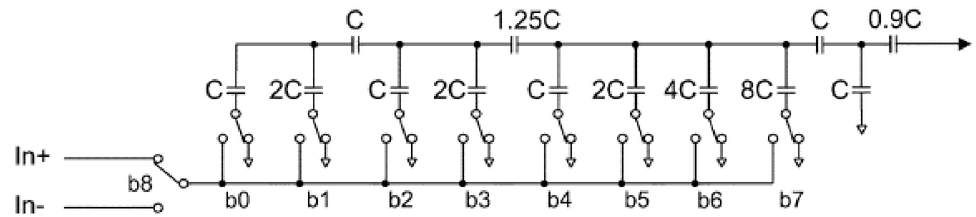


Fig. 14. Nine-bit trim capacitor.

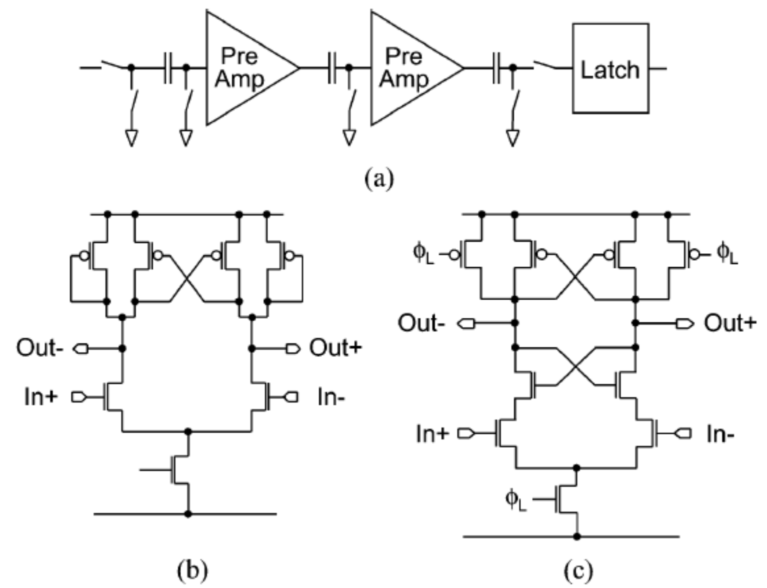


Fig. 15. (a) Analog comparator. (b) Preamplifier. (c) Latch.

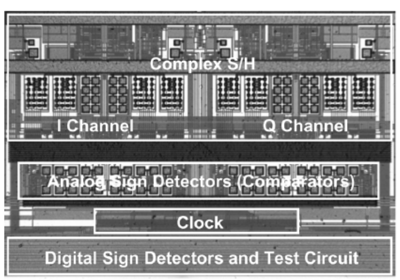


Fig. 17. Chip die photo.

Supisa Lerstaveesin, and Bang-Sup Song: "A Complex Image Rejection Circuit With Sign Detection Only," IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 41, NO. 12, DECEMBER 2006

256 QAM Spectra Before and After Image Rejection

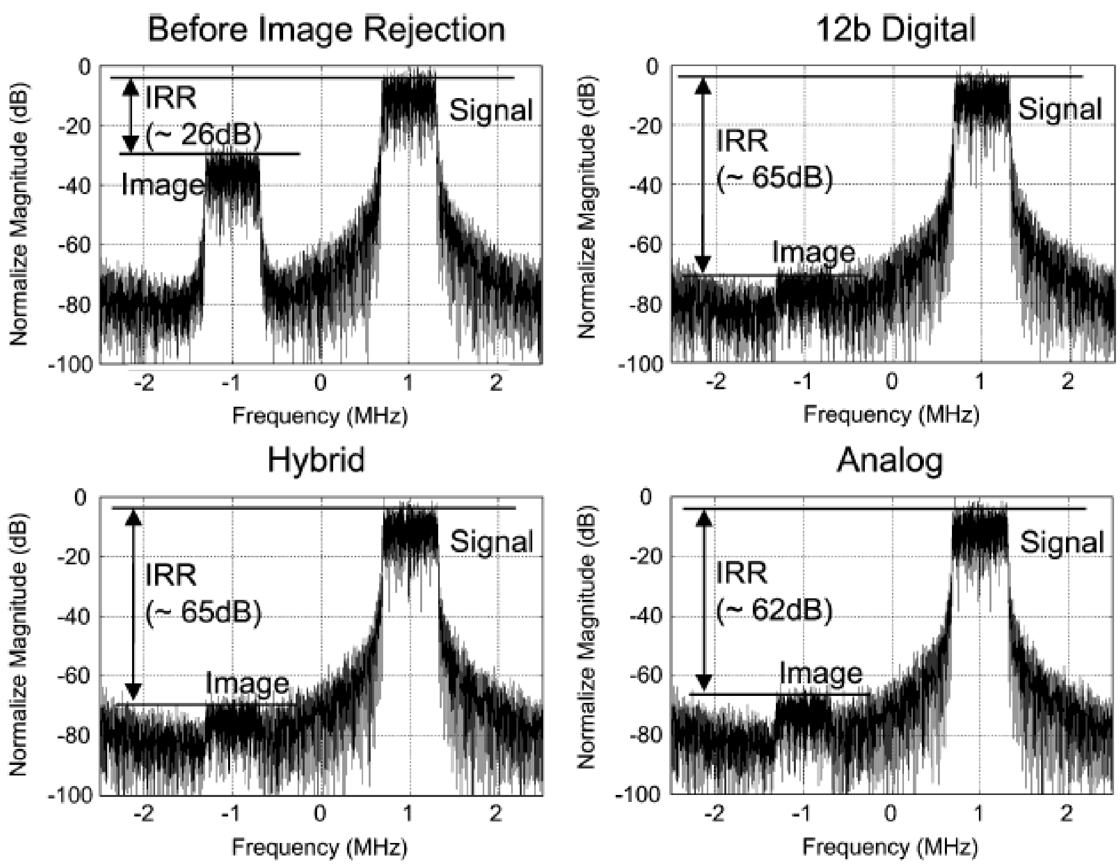
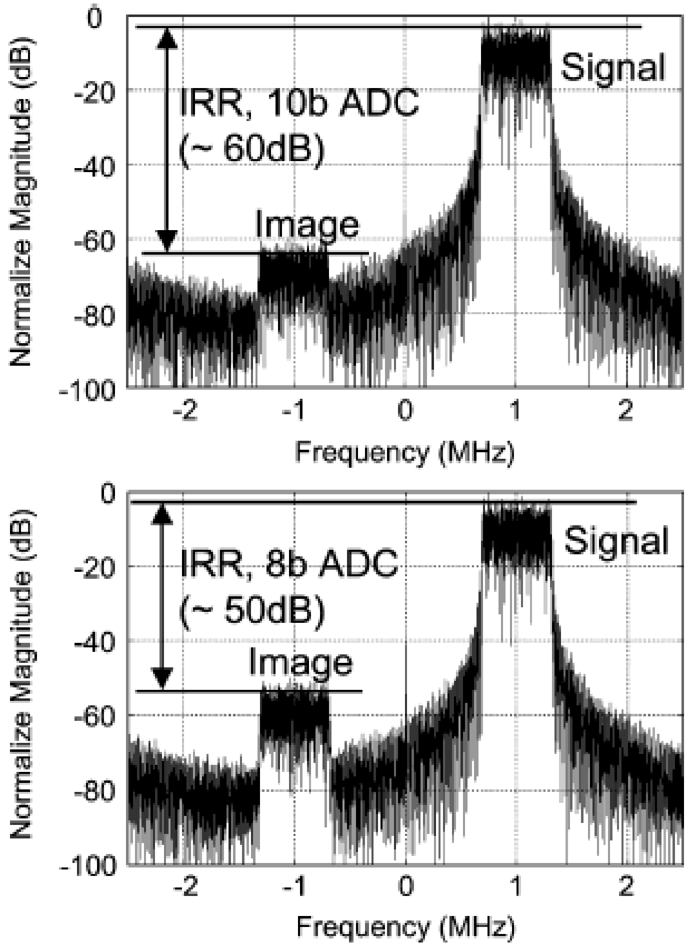


Fig. 18. Measured 256-QAM spectra before and after image rejection.

Supisa Lerstaveesin, and Bang-Sup Song: "A Complex Image Rejection Circuit With Sign Detection Only," IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 41, NO. 12, DECEMBER 2006

256 QAM Constellation Before and After Image Rejection



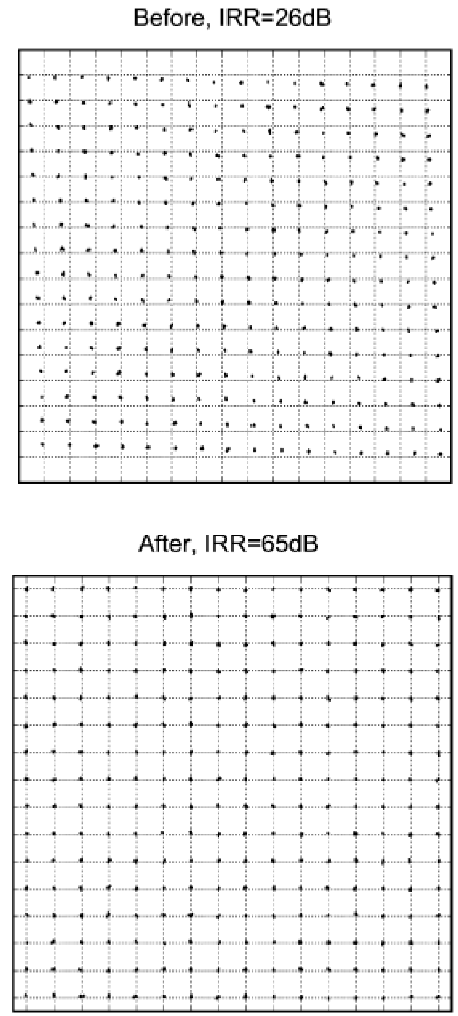


Fig. 19. Effect of ADC resolution on IRR for 256-QAM.

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Effect of IRR on Error Probability

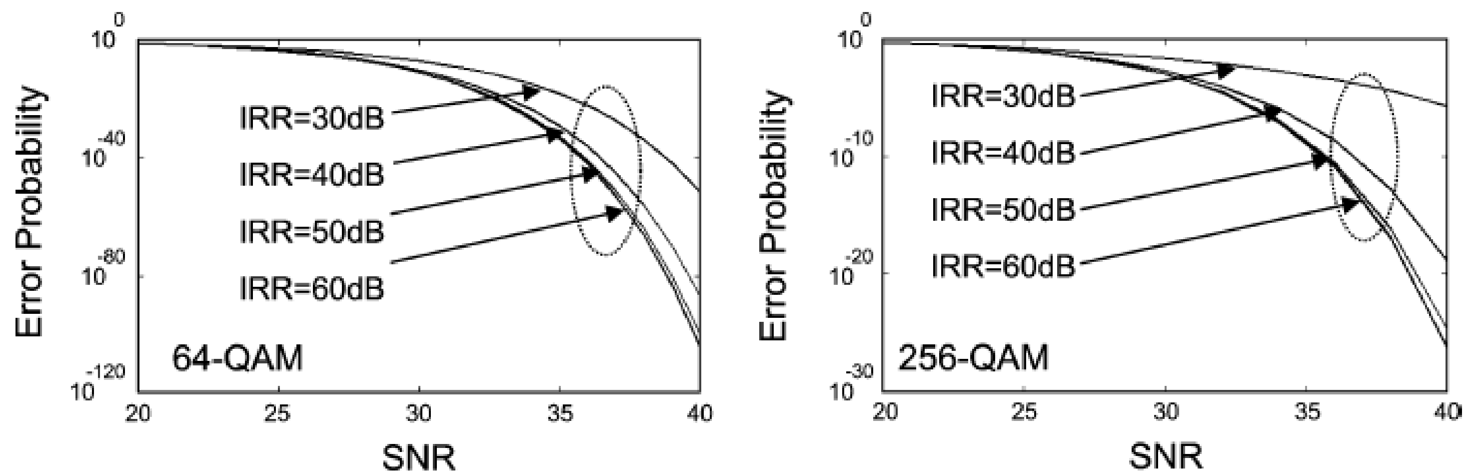


Fig. 22. Effect of IRR on error probability of 64-QAM and 256-QAM.

Supisa Lerstaveesin, and Bang-Sup Song: "A Complex Image Rejection Circuit With Sign Detection Only," IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 41, NO. 12, DECEMBER 2006

Non-linearities

Improvement of Mixer Nonlinearities (IIP2) for Active Mixers

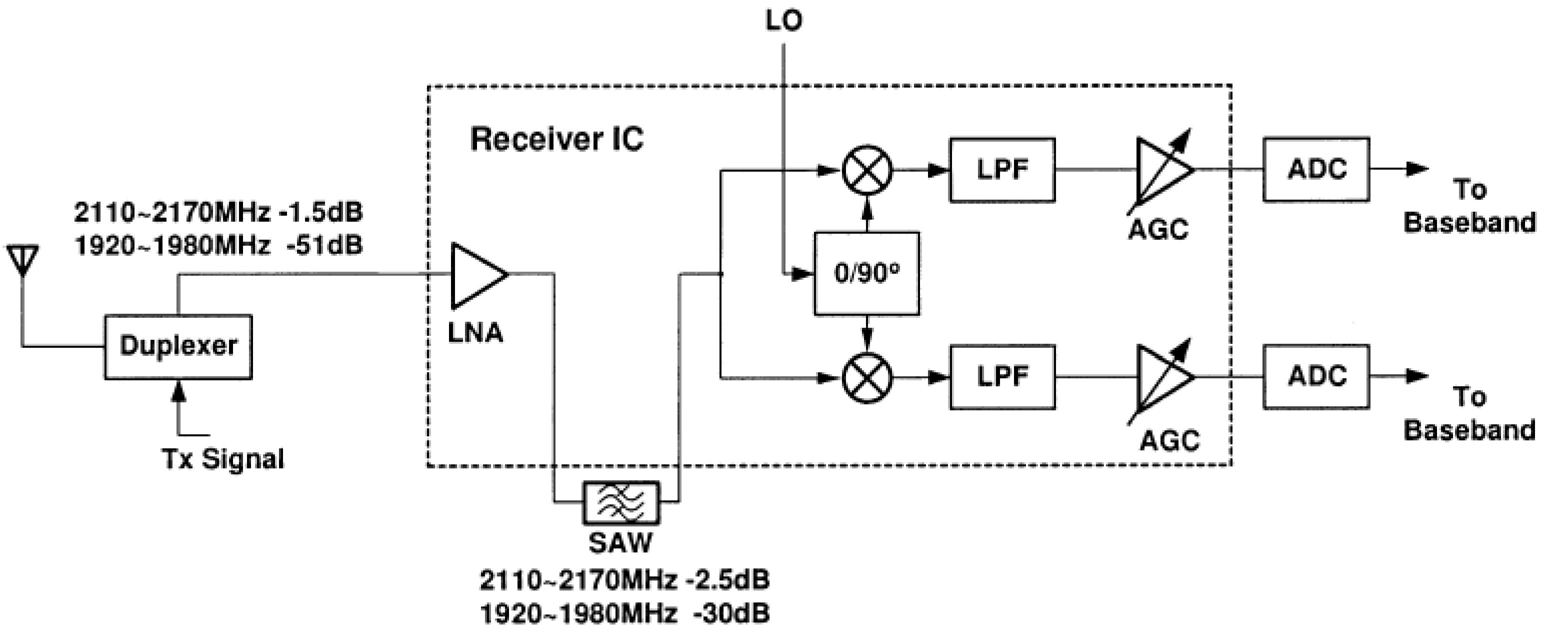


Fig. 1. Simplified block diagram of a direct-conversion WCDMA receiver.

- Detailed circuit analysis of nonlinearities in diff pairs and doubled balanced mixers.
- The proposed approach is analog,; trimming of current bias.

Liwei Sheng; Larson, L.E.;"**An Si-SiGe BiCMOS direct-conversion mixer with second-order and third-order nonlinearity cancellation for WCDMA applications,"** Microwave Theory and Techniques, IEEE Transactions on Volume 51, Issue 11, Nov. 2003 Page(s):2211 - 2220

Improvement of Mixer Nonlinearities (IIP2) for Active Mixers

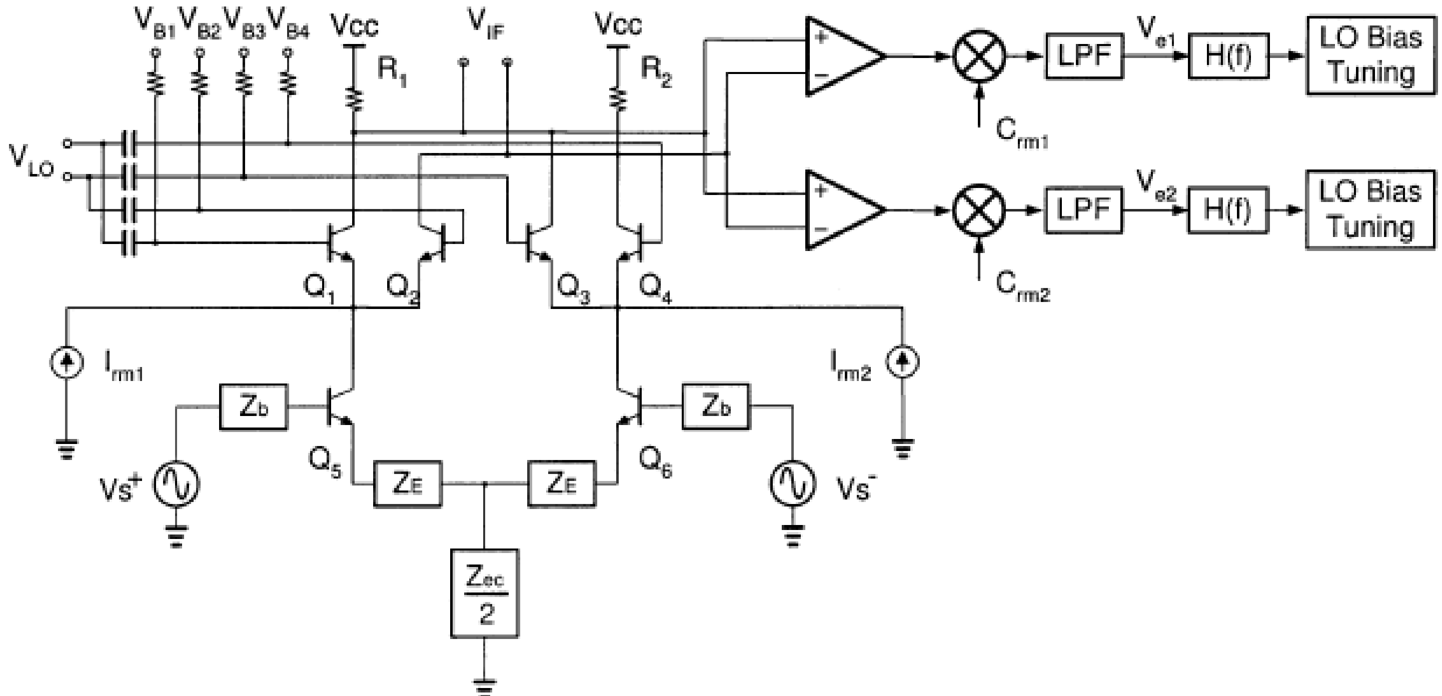


Fig. 8. Proposed even-order distortion cancellation scheme of the double-balanced mixer.

- Uses PN sequences and correlation to estimate the nonlinearities. The LO bias is tuned to minimize distortion.

Liwei Sheng; Larson, L.E.;"**An Si-SiGe BiCMOS direct-conversion mixer with second-order and third-order nonlinearity cancellation for WCDMA applications,"** Microwave Theory and Techniques, IEEE Transactions on Volume 51, Issue 11, Nov. 2003 Page(s):2211 - 2220

Some of the New Approaches to Broadband Receivers

- A high-frequency software defined radio

N. C. Davies, "A high performance HF software radio," in *Proc. 8th Int. Conf. HF Radio Systems and Techniques*, Guildford, U.K., 2000, pp. 249–256.

- Frequency channelizers

D. R. Zahirniak, D. L. Sharpin, and T. W. Fields, "A hardware-efficient, multirate, digital channelized receiver architecture," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 34, no. 1, pp. 137–152, Jan. 1998.

- Selectable RF filters and downconversion

H. Yoshida, T. Kato, T. Tomizawa, S. Otaka, and H. Tsurumi, "Multimode software defined radio receiver using direct conversion and low-IF principle: Implementation and evaluation," *Electr. Commun. In Japan (Part I: Communications)*, vol. 86, pp. 55–65, 2003.

- Subsampling and undersampling

- Analog decimation

D. Jakonis, K. Folkesson, J. Dabrowski, P. Eriksson, and C. Svensson, "A 2.4-GHz RF sampling receiver front-end in 0.18-mCMOS," *IEEE J. Solid-State Circuits*, vol. 40, no. 6, pp. 1265–1277, Jun. 2005.

Some of the New Approaches to Broadband Receivers (cont…)

- Sampling with built-in anti-aliasing

Y. S. Poberezhskiy and G. Y. Poberezhskiy, "Sampling and signal reconstruction circuits performing internal antialiasing filtering and their influence on the design of digital receivers and transmitters," *IEEE Trans. Circuits Syst. I*, vol. 51, no. 1, pp. 118–129, Jan. 2004.

- Sample rate, downsampling and filtering

R. Crochiere and L. Rabiner*, Multirate Digital Signal Processing*. Englewood Cliffs, NJ: Prentice Hall, 1983.

- A discrete-time RF sampling receiver

R. B. Staszewski, et. al. "All-digital TX frequency synthesizer and discrete-time receiver for Bluetooth radio in 130-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2278–2291, Dec. 2004.

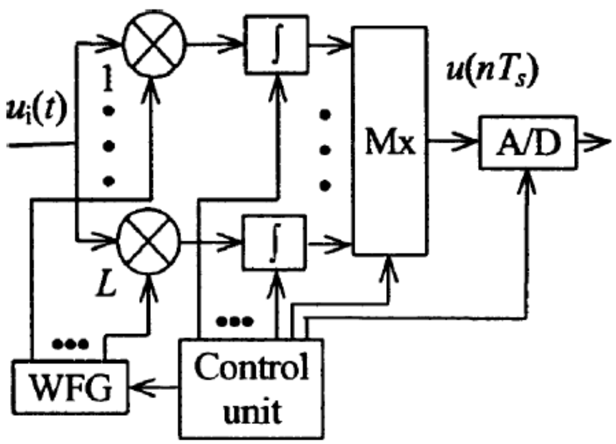
- UCLA SDR receiver

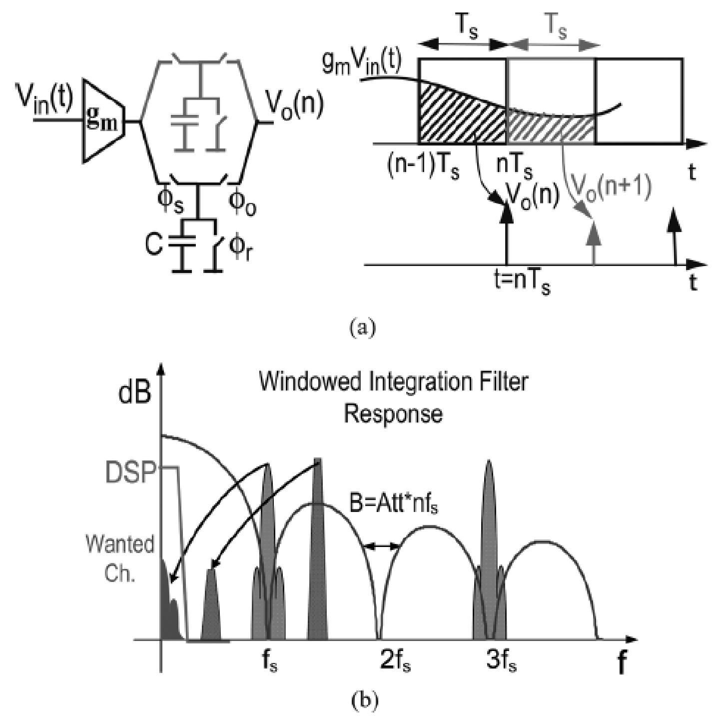
  - Bagheri, R.; Mirzaei, A.; Heidari, M.E.; Chehrazi, S.; Minjae Lee; Mikhemar, M.;Tang, W.K.; Abidi, A.A.; **Software-defined radio receiver: dream to reality**, Communications Magazine, IEEE, Volume 44, Issue 8, Aug. 2006 Page(s):111 - 118
  - Abidi, "The path to software-defined radio receiver", IEEE JSSC, May 2007

- Frequency-domain-sampling receivers

  - S. Hoyos, B. M. Sadler, and G. R. Arce, "**Broadband Multicarrier Communications Receiver Based on Analog to Digital Conversion in the Frequency Domain,**" *IEEE Transactions on Wireless Communications*, March 2006.
  - S. Hoyos and B. M. Sadler, "**Ultra-wideband analog to digital conversion via signal expansion,**" *IEEE Transactions on Vehicular Technology*, Vol. 54, No. 5, Sept. 2006, Pages: 1609-1622. Invited
  - S. Hoyos, B. M. Sadler **"UWB Mixed-Signal Transform-Domain Direct-Sequence Receiver,"** *Accepted for publication in IEEE Transactions on Wireless Communications*, 2007.

Sampling with built-in anti-aliasing

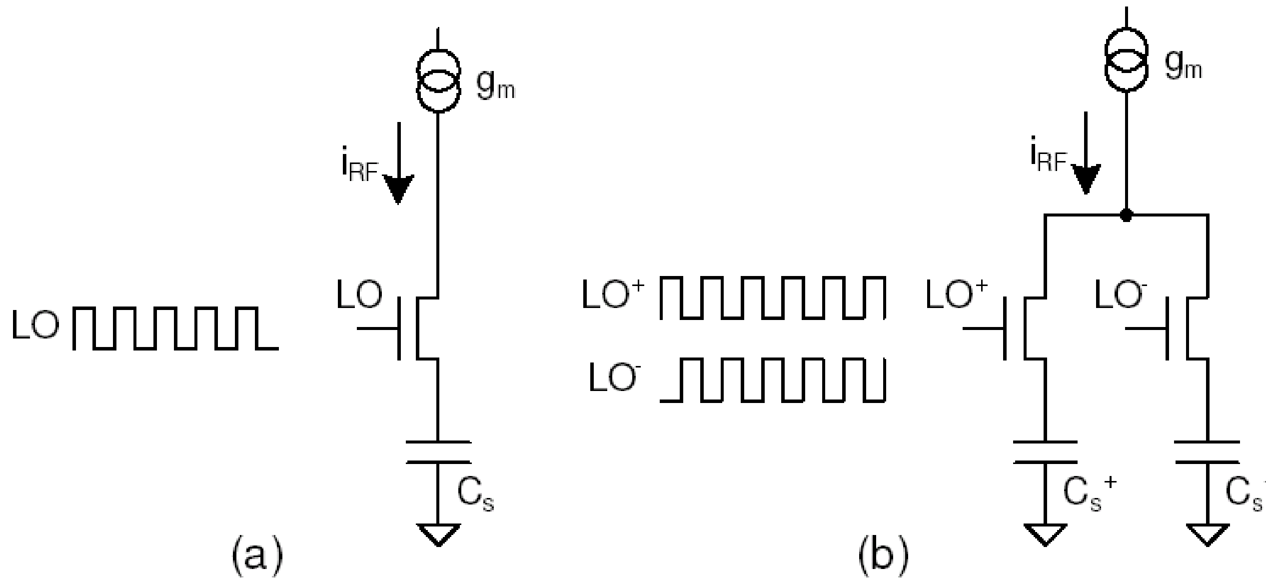




- Sinc(x) anti-aliasing provided by windowing and integration. The sidelobes decay at 20 dB/decade with zeros at fs, 2fs, ..
- More general mixing waveforms can be used, although complexity goes up.

Y. S. Poberezhskiy and G. Y. Poberezhskiy, “Sampling and signal reconstruction circuits performing internal antialiasing filtering and their influence on the design of digital receivers and transmitters,” *IEEE Trans. Circuits Syst. I*, vol. 51, no. 1, pp. 118–129, Jan. 2004.

A simple integrator



- Assume a low noise transconductance amplifier

- LO=2.4 GHz

- Pseudo-differential architecture (b) is preferable.

- This is just mixing followed by integration which provides down-conversion and filtering in a single stage.

- How do you read the voltage out of the caps?

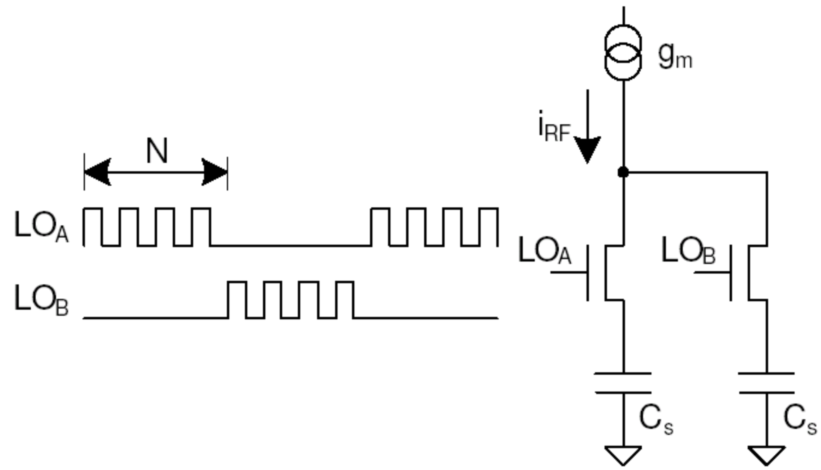
Cyclic Read-Out

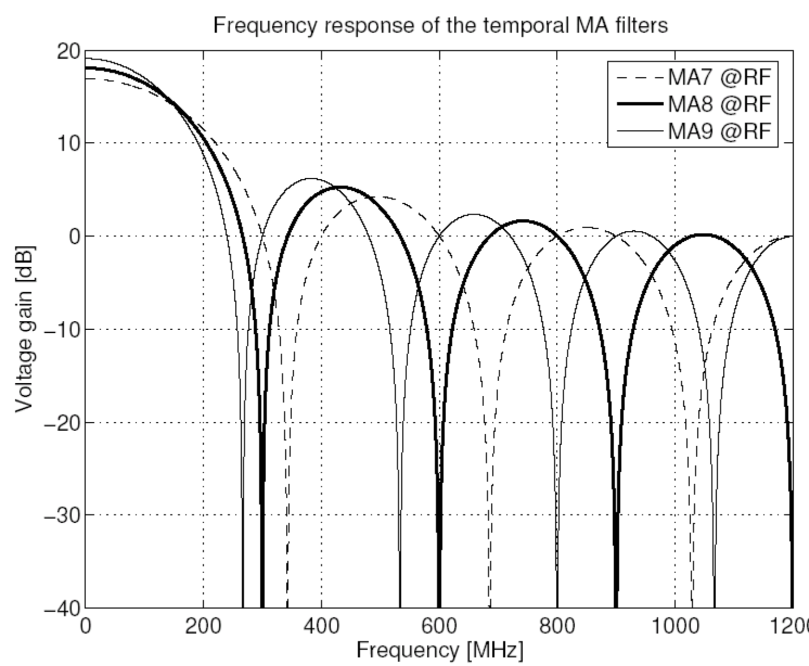
- Cyclic change and discharge of caps. every N cycles.

- This can be modeled as a moving average

$$w_i = \sum_{l=0}^{N-1} u_{i-l}$$

- If modeled as MA, the filter has a sinc frequency response whose lobes width and nulls positions depend on N.





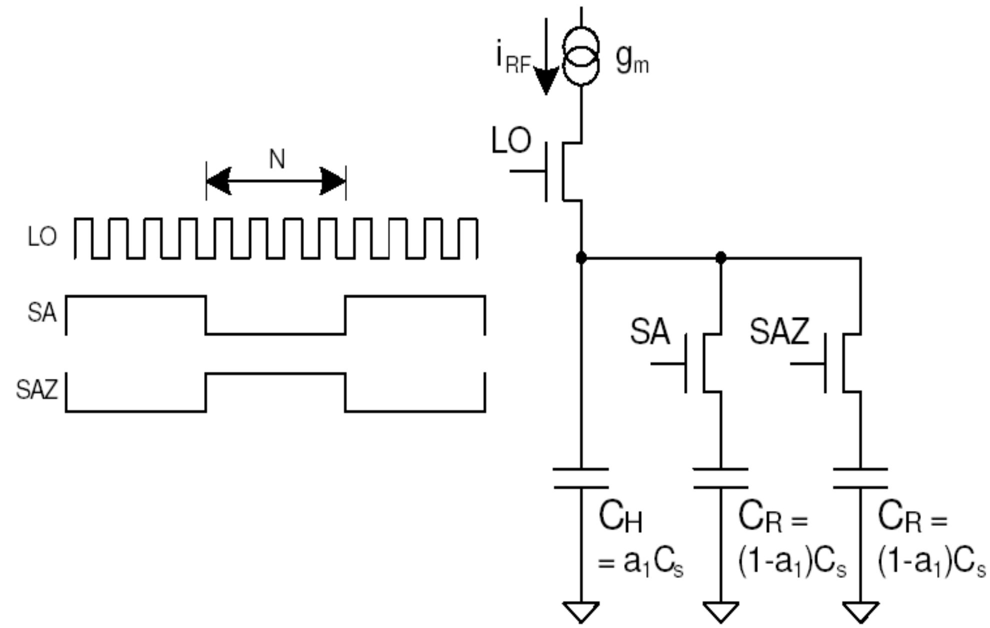
High-Rate IIR Filtering

- History capacitor C_H added
- LNTA sees constant capacitance C_S
- Let $a_1=C_H/(C_H+C_R)$
- At switching time, C_H retains a_1 portion of its total charge and shares $(1-a_1)$ to the discharged C_R cap. At sampling time j, the system charge s_j is:

$$s_j=a_1 s_{j-1}+w_j$$

-The output charge x_j is

$$x_j=(1-a_1)s_{j-1}$$



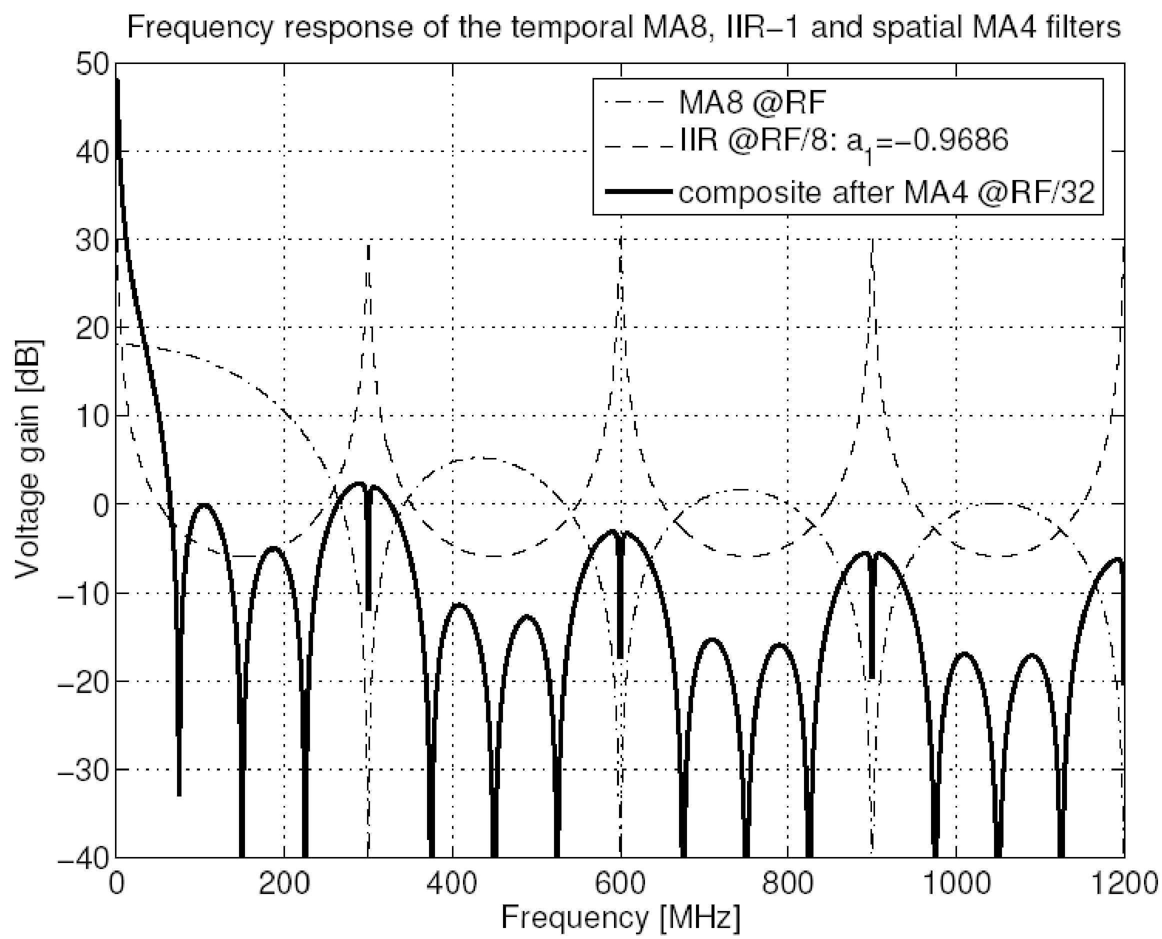
This is a IIR filter with sampling frequency of f_0/N and single pole at

$$f_{c1}=\frac{1}{2\pi}\frac{f_0}{N}(1-a_1)=\frac{1}{2\pi}\frac{f_0}{N}\frac{C_R}{C_H+C_R}$$

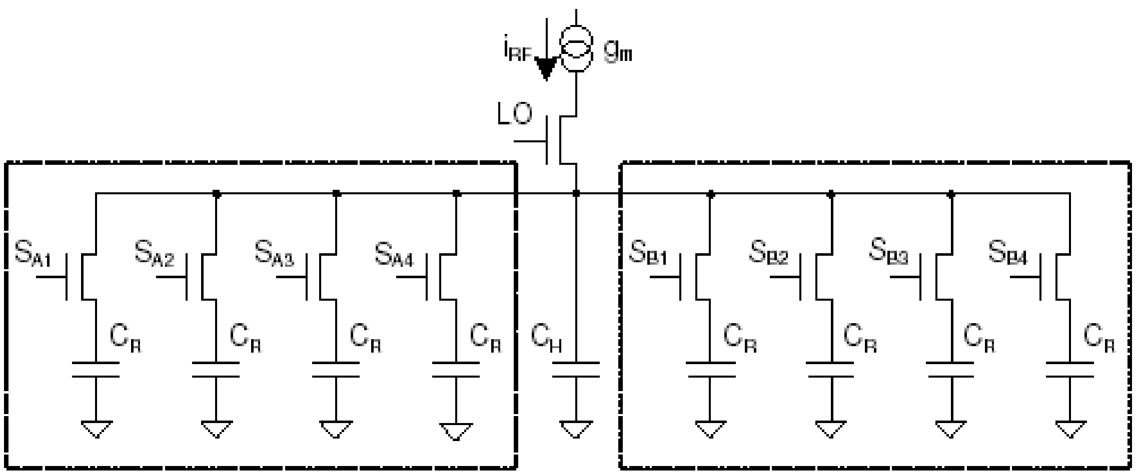
Example

- C_R= 0.5pF, C_H=15.425pF, a_1=0.9686
- f_0/N=2.4GHz/4=300MHz
- Additional zeros with M=4

Additional IIR filtering during read-out process can also be introduced



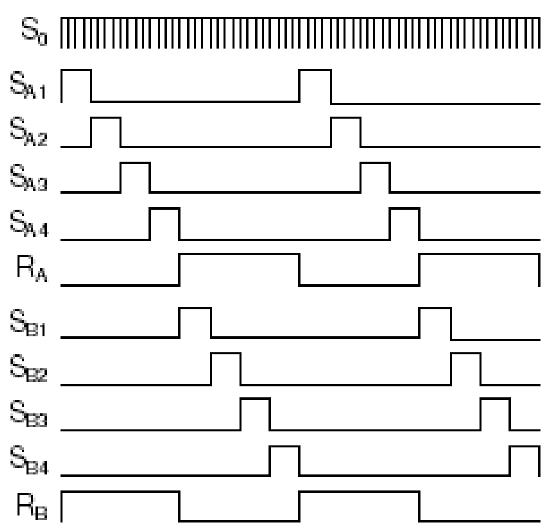
Adding more zeros to the FIR



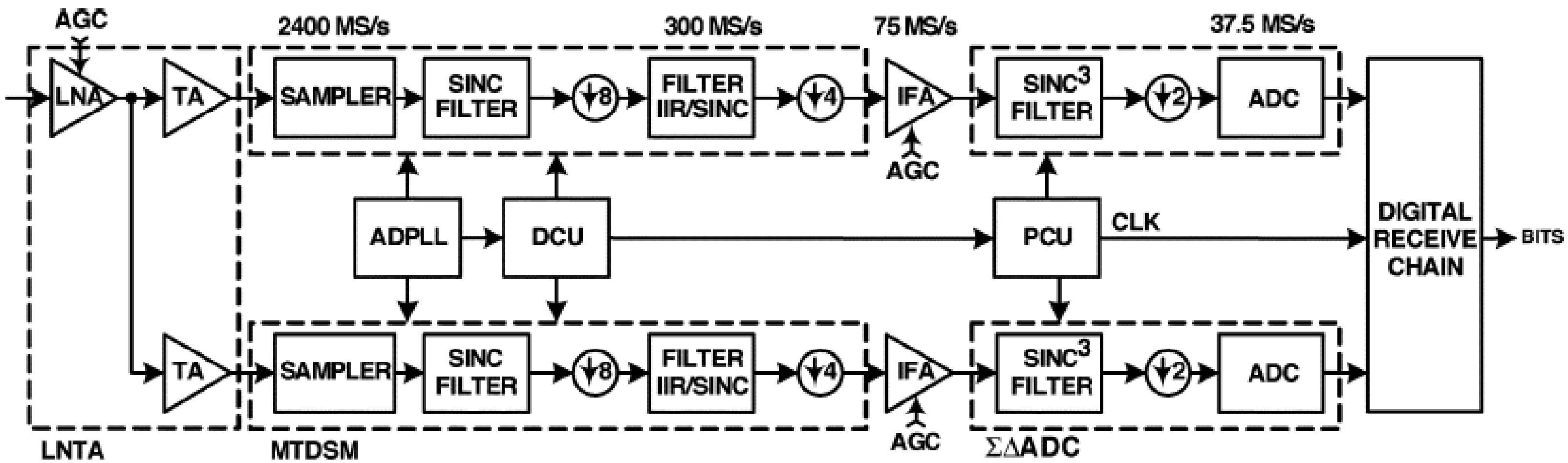
- Redundant switched caps. Introduce more zeros in the transfer function when adding up their charges during read out:

$$y_k = \sum_{l=0}^{M-1} u_{k-l}$$

-Illustrated is the case with M=4



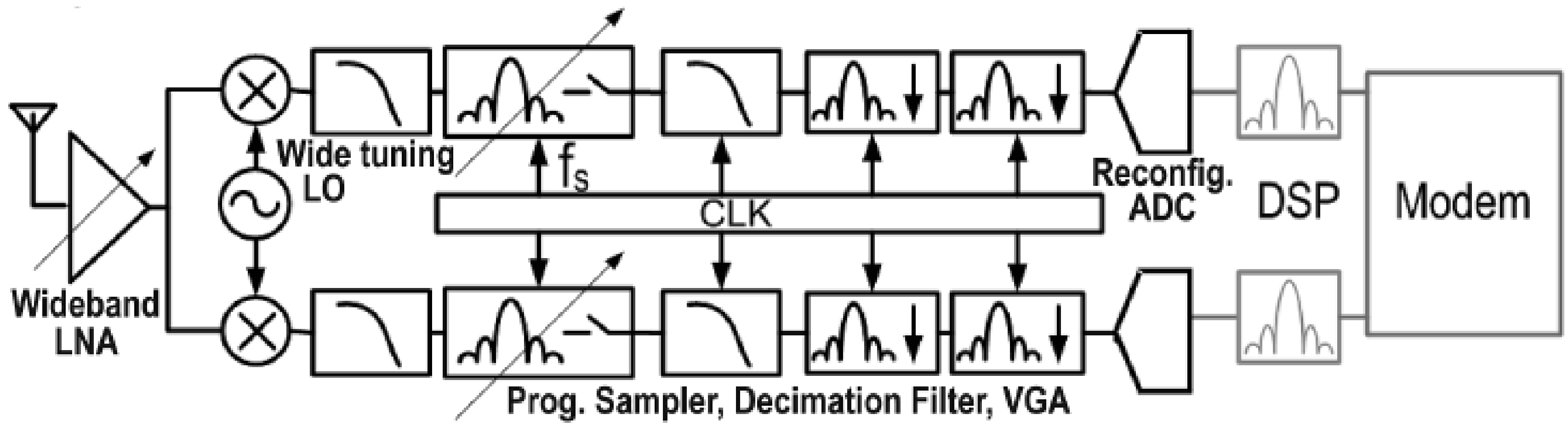
A discrete-time RF sampling receiver



- Bluetooth and GSM receivers from TI use integrate and dump sampling followed by down sampling and filtering.
- Programable filtering and decimation to achieve the anti-aliasing needed.

R. B. Staszewski, et. al. “All-digital TX frequency synthesizer and discrete-time receiver for Bluetooth radio in 130-nm CMOS, ” *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2278–2291, Dec. 2004.

UCLA SDR receiver



- Direct conversion with tunable LO in the freq. range 800 MHz to 6 GHz.
- Cascade of sinc^N filters followed by decimation to achieve the initializing needed.
- Good for narrowband signals as a single ADC can handle the bandwidth. But SDR should also be good for wideband and ultra-wideband signals. Need parallel ADC to sample at a fraction of Nyquist rate. Parallelization of the front-end will be needed if want to keep the ADC sampling rate down.

A. Abidi, "The path to software-defined radio receiver", IEEE JSSC, May 2007

SDR for narrowband, wideband and ultra-wideband signals

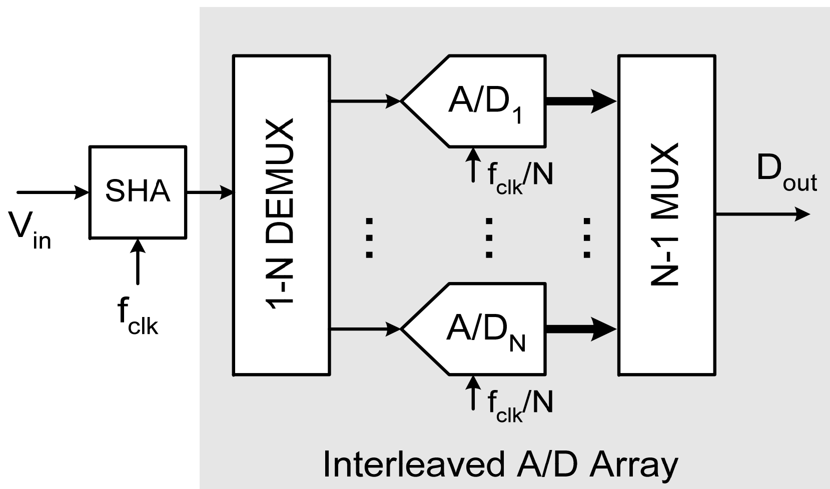
- Assume we have a tunable front-end that provides the downconversion and the antialiasing filtering needed for a wide range of standards.
- The problem now is that the signal bandwidth will have > 10X range. Example : 802.11g (ΣΔ ADC @ 50 Ms/s and 8 bits), UWB (ADC @ 500 Ms/s and 5 bits). Say you can run the ΣΔ ADC @ 100Ms/s and 5 bits, i.e. exchange OSR by DR). Can we use 5 of these ΣΔ ADCs to cope with UWB ?
- Note that the same ΣΔ ADC could operate @ 200 KHz and 14 bits for GSM and @ 1MHz and 12 bits for Bluetooth.
- How do you parallelize the ADCs and even the RF front-end to create a SDR for narrowband, wideband and ultra-wideband signals?

Motivation

Digital intensive RF receivers -> ADCs with wide bandwidths and large dynamic range.
Solution ? -> Parallelization

Parallelized ADCs

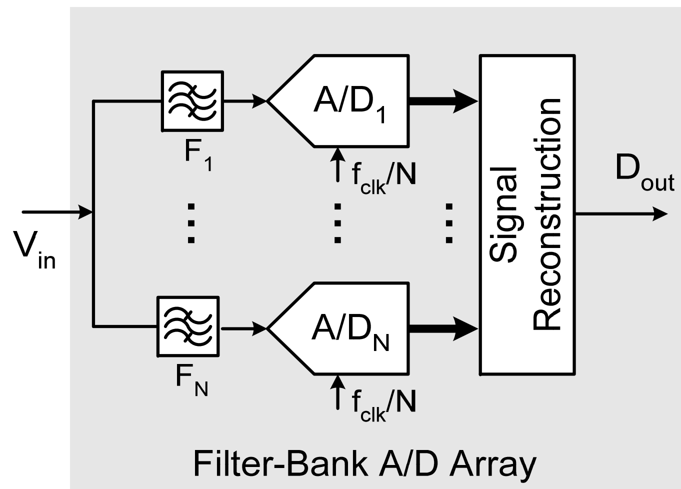
Time-interleaved ADC



Drawbacks

- SHA has stringent tracking bandwidth requirements
- Each ADC sees full input signal bandwidth (non-linearity and aliasing)

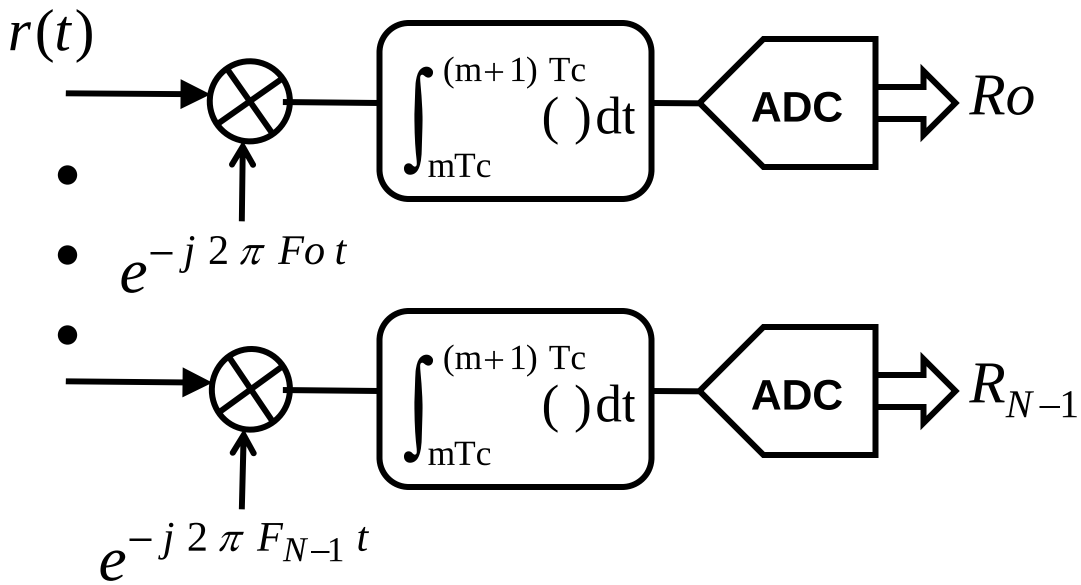
Filter-bank ADC

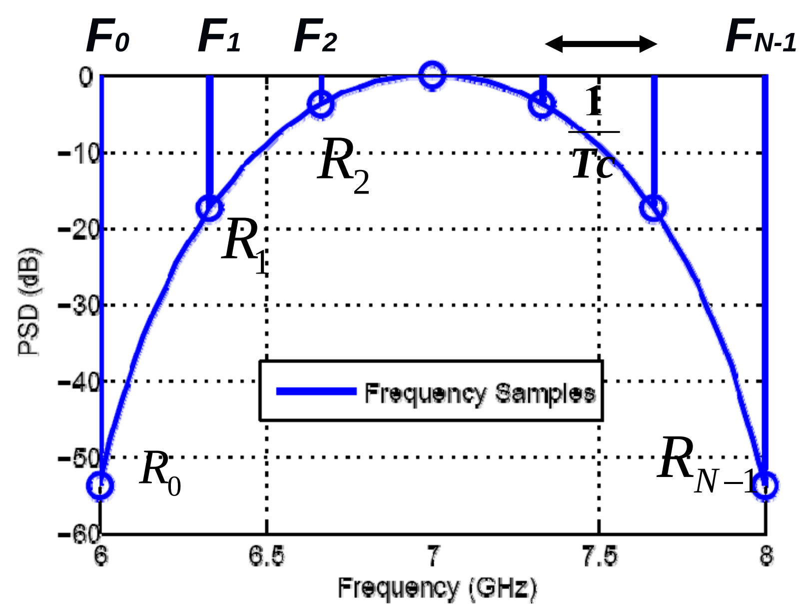


Drawbacks

- Filters with very tough specs (aliasing)
- Signal reconstruction increases complexity

Parallel-Path Sampling





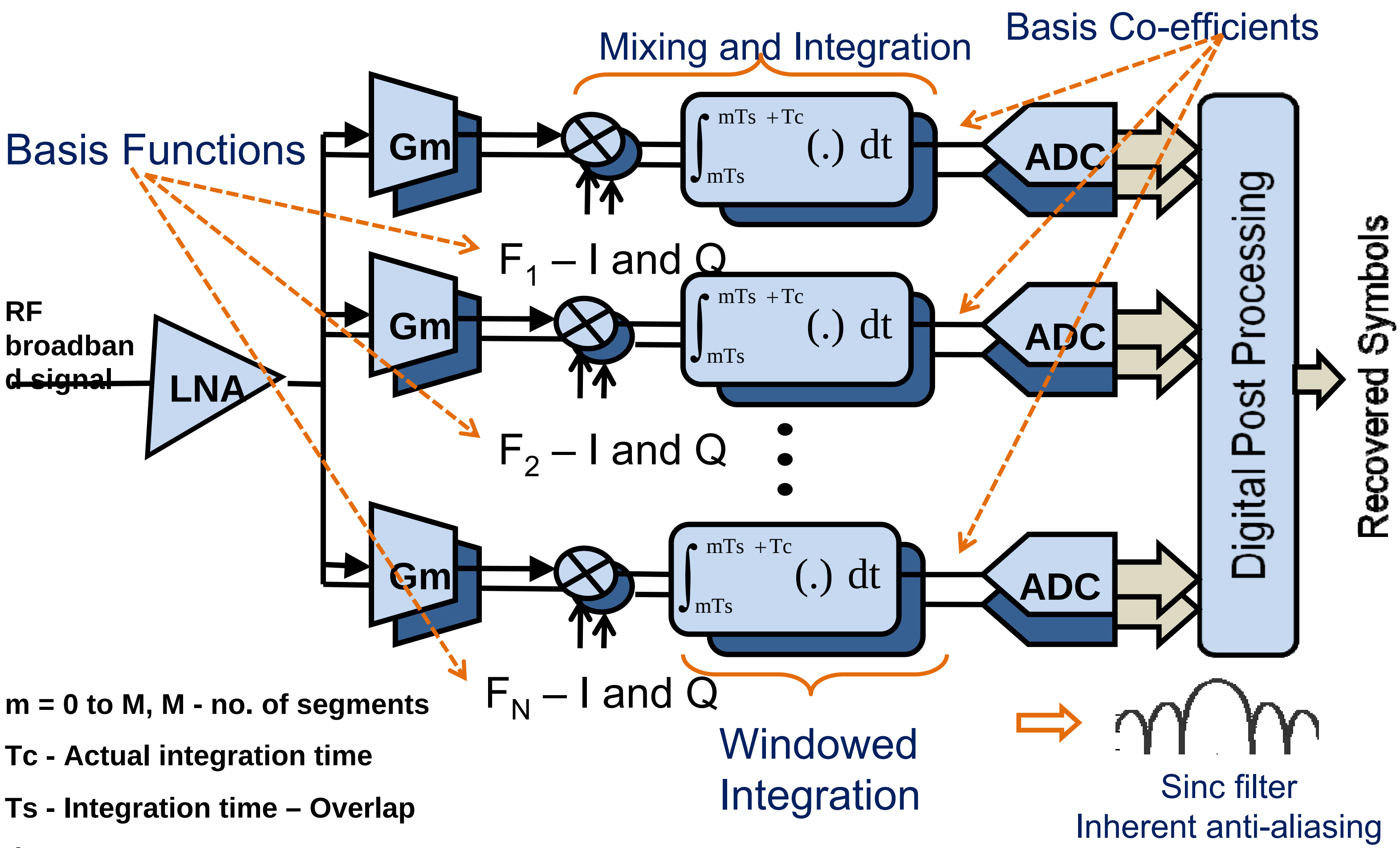
Salient Features

- ❑ Simple mixers and integrators in the front end
- ❑ Windowed integration provides inherent anti-aliasing. Relaxed Filter design.
- ❑ Relaxed sample and hold requirements
- ❑ No signal reconstruction. Direct digital processing of Frequency samples.
- ❑ Relaxed ADC design with lower speeds

Drawback

- ❑ Area overhead associated with parallelization

Parallel-Path Receiver Architecture



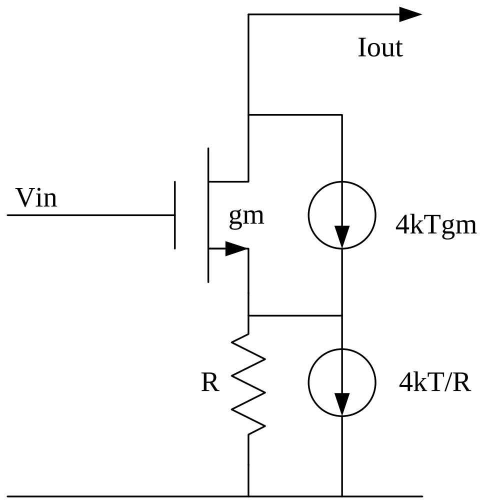
m = 0 to M, M - no. of segments

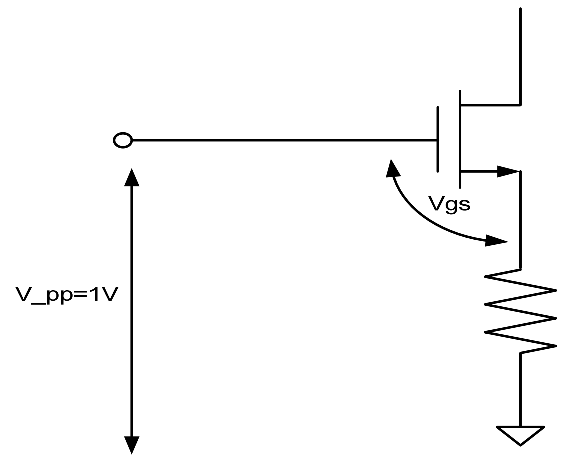
Tc - Actual integration time

Ts - Integration time – Overlap time

[Ref] P. K. Prakasam, M. Kulkarni, X. Chen, Z. Yu, S. Hoyos, J.,Silva-Martinez and E. Sanchez-Sinencio, " Applications of Multi-Path Transform-Domain Charge-Sampling Wideband Receivers", *IEEE Transactions on Circuits and Systems II, pp309-313, Vol. 55,Issue 4, April 2008.*

Circuit Implementation of the Gm Stage

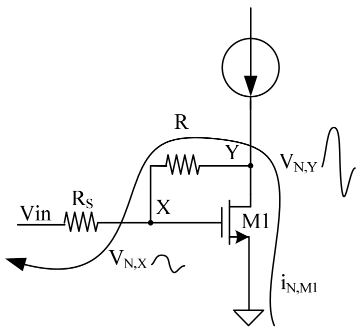




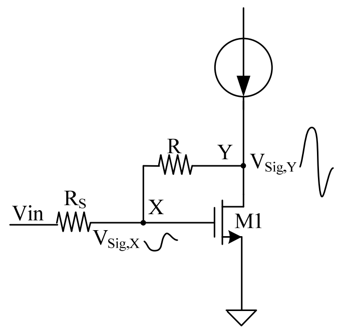
1. High Linear Gm stage

- Flicker noise is removed by the degeneration resistor
- IIP3 is boost to almost 30 dBm
- Large Vdd is required.
- Used in 10 bits full scale input receiver.

Circuit Implementation of the Gm Stage



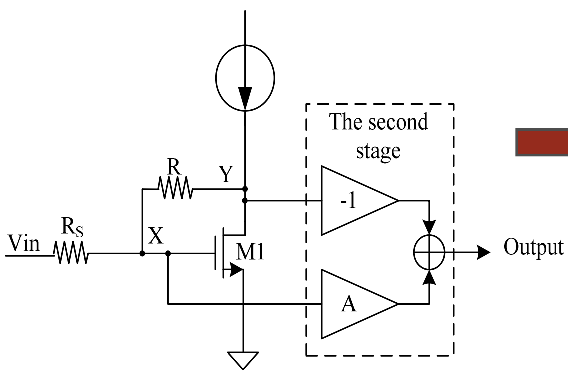
a)

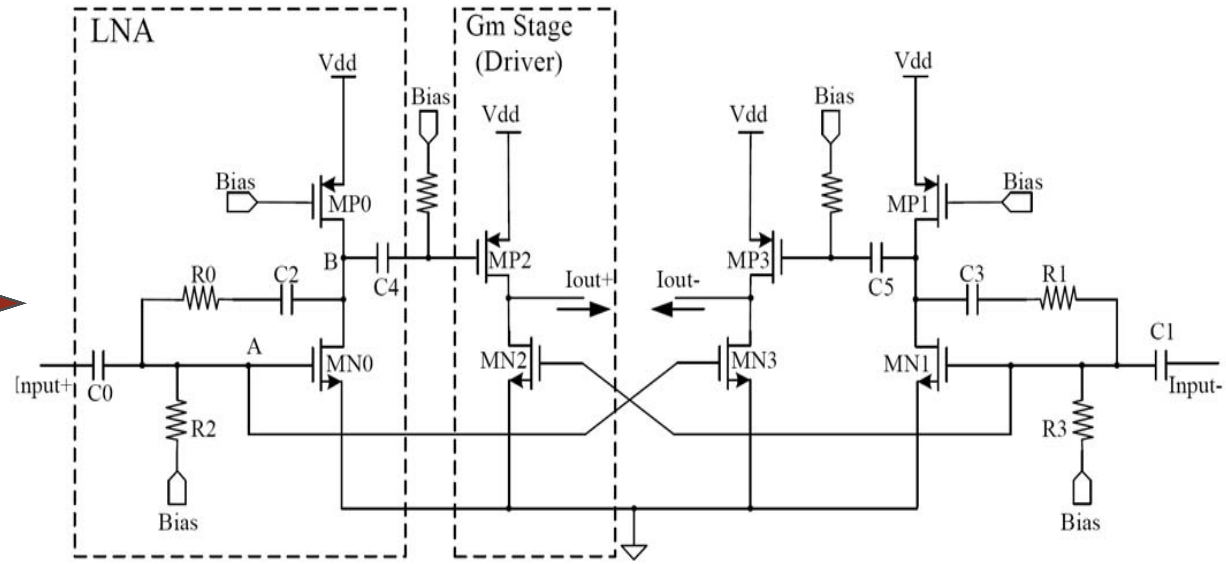


b)

2. Noise Cancelling Gm stage

- ❑ Noise of the first stage is eliminated
- ❑ Gain is boosted
- ❑ Noise Figure is improved
- ❑ Used in wireless receiver while input signal is small.



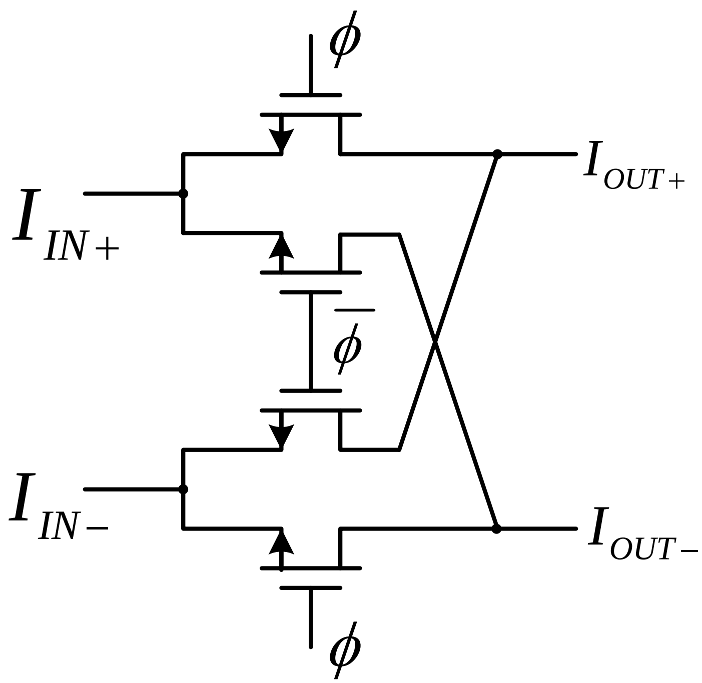


[Ref] X. Chen, J.,Silva-Martinez and S. Hoyos, " A CMOS differential noise cancelling low noise transconductance amplifier ", Circuits and Systems Workshop: System-on-Chip - Design, Applications, Integration, and Software, page(s): 1-4, 2008 IEEE Dallas

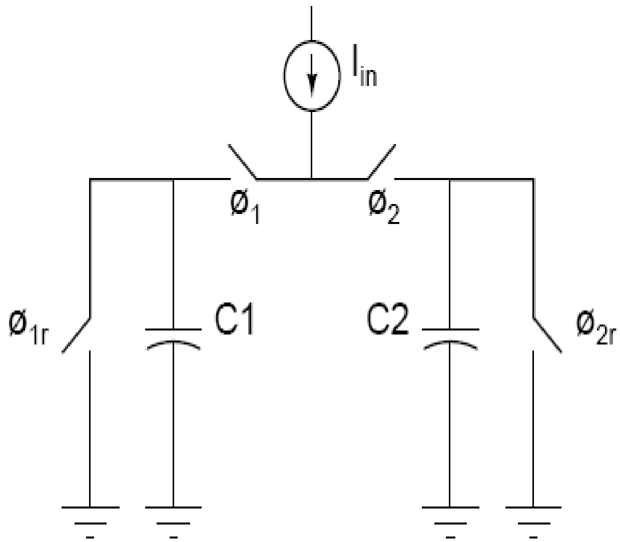
Circuit Implementation of the Mixer

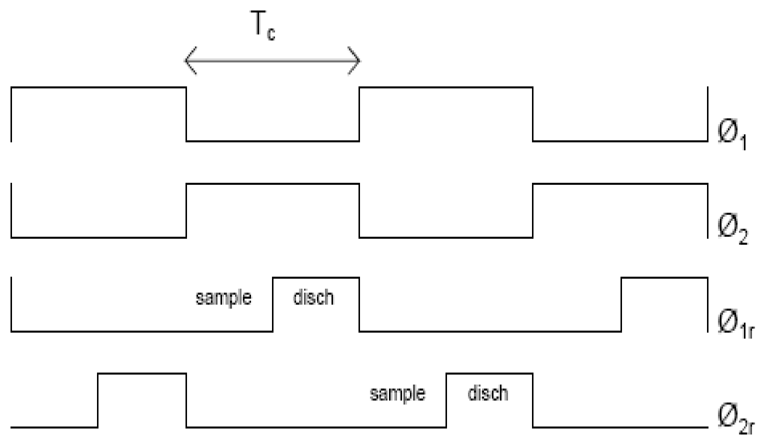
Double Balanced Passive Mixer

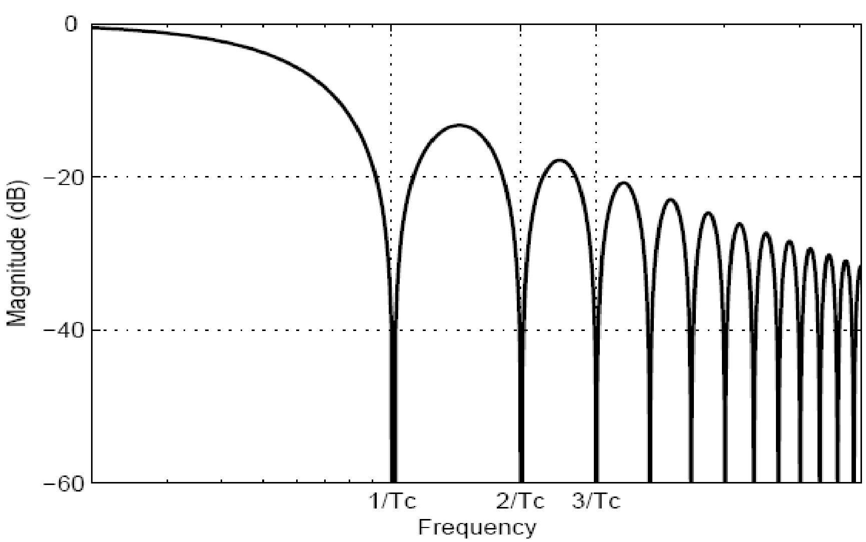
- ❑ Minimum signal and clock feed-through
- ❑ Even order harmonics are cancelled
- ❑ Almost noise free



Charge Sampling

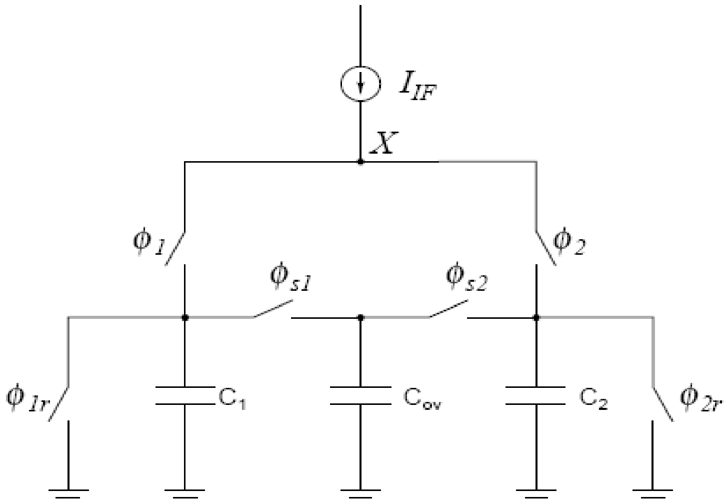


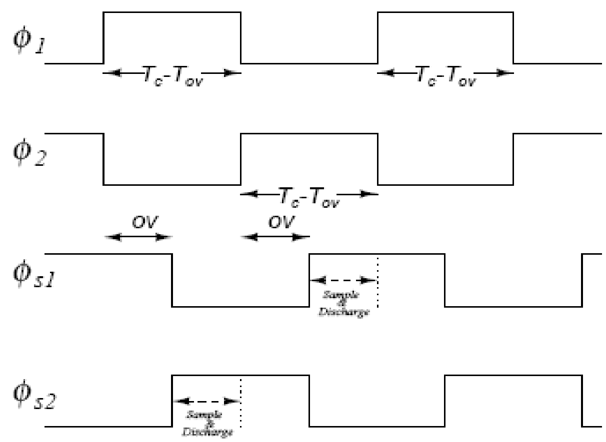


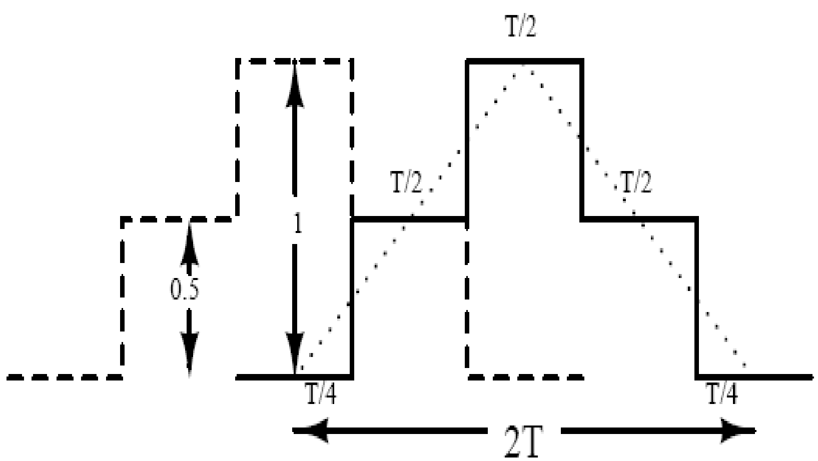


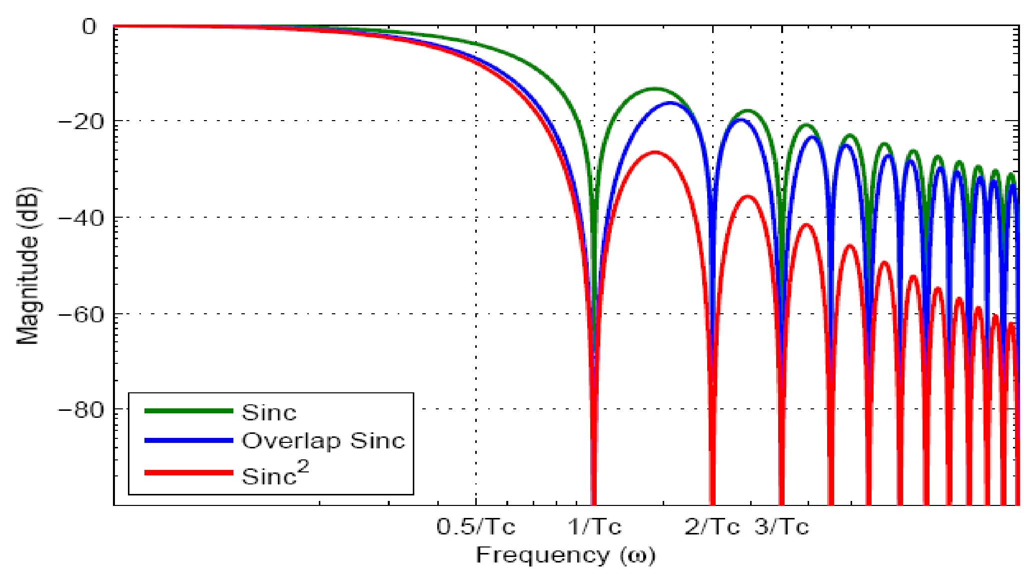
- ❑ Windowed integration of I_{in} on C1 and C2
- ❑ Inherent anti-aliasing *sinc* filter

Overlap in windows





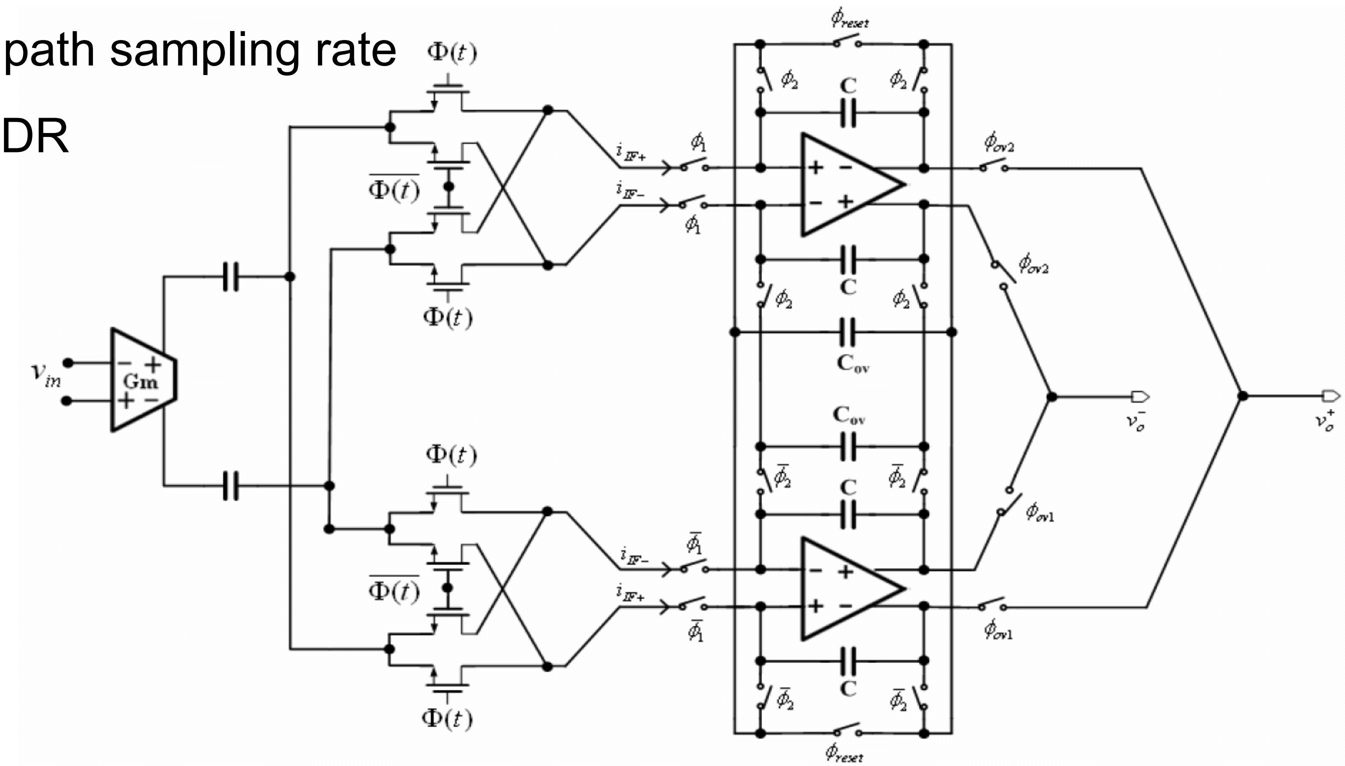




1 Path Circuit

Shooting for 10 bits 2.5 Gs/s ADC

- High linear Gm stage to accommodate fullscale input
- Overlapping windowing
- 200 Ms/s path sampling rate
- 55 dB SNDR

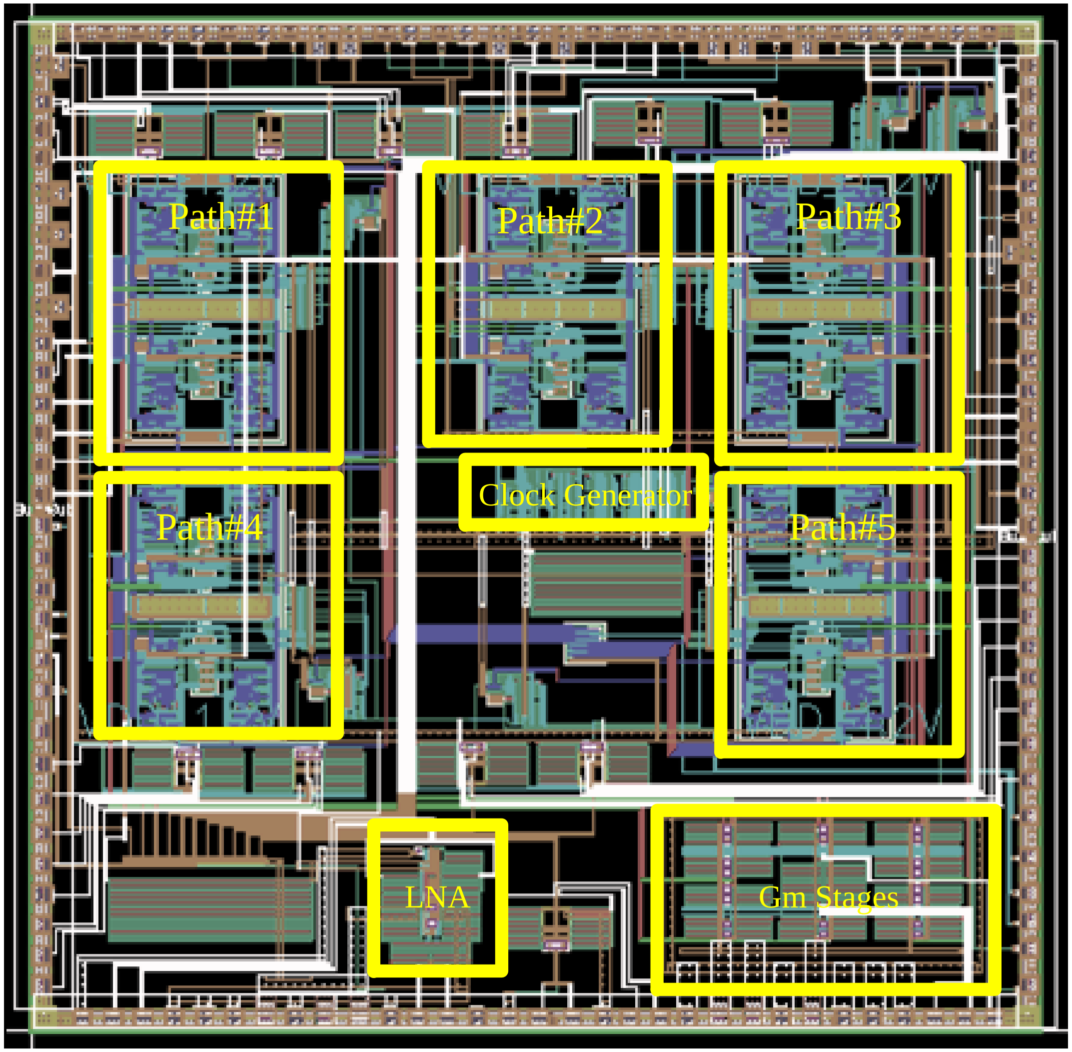


The whole front-end: 10 path (5 lo frequencies I/Q)

Chip Layout

45 nm (TI technology)

- ❑ Area: 2.5mm*2.5mm
- ❑ Core Power: 320 mW
- ❑ 64 mW / Path (I and Q)

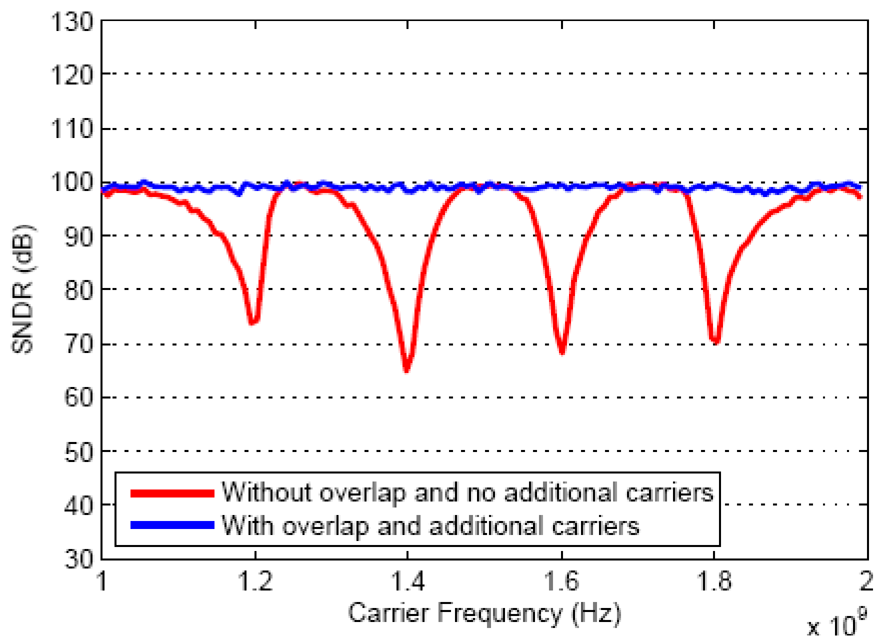


Overall Power consumption of the ADC:
320 mW + N * P_path,adc

System level issues of FD receiver

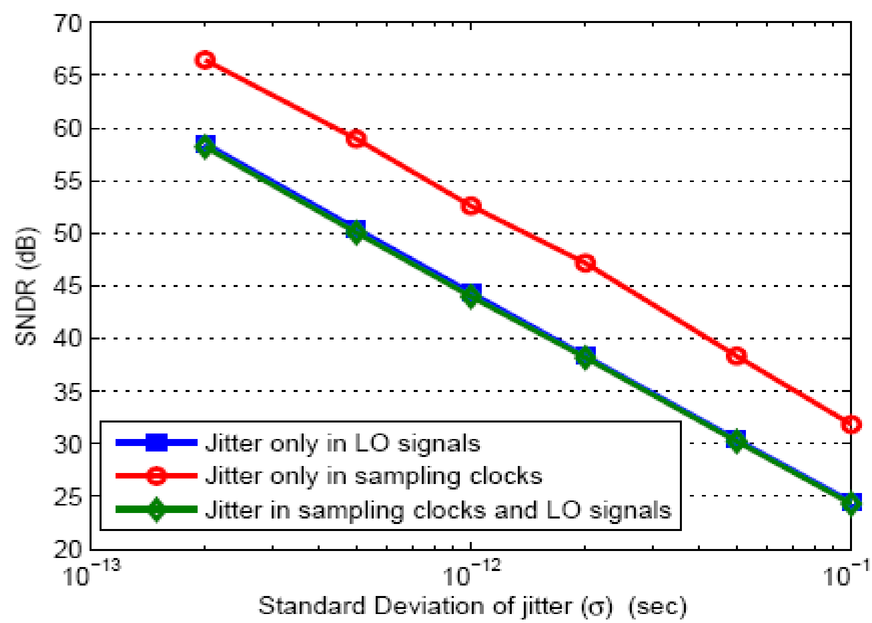
Noise Amplification

- Out-of-band noise folds back creating dips in performance
- Overlap improves the filter
- Overlap results in over-sampling which reduces aliasing.
- Additional carriers can be detected.



Effect of Jitter

- Jitter sources: LO signal, Sampling clocks
- Jitter from LO signal dominant
- Filter mitigates noise from LO jitter.
- Long integration windows reduces jitter from sampling clocks.



Least Squares Data Estimation

Input symbols modulated on carriers

$$\vec{a} = [a_i(0), a_q(0), a_i(1), a_q(1), \ldots a_i(S-1), a_q(S)]$$

Output sampled basis coefficients

$$\vec{r} = [R_{0,0}, R_{0,1} \ldots R_{0,N-1}, R_{1,0}, R_{1,1}, \ldots R_{M-1,N-1}]^T$$

Entire system represented as a linear transformation from data symbols (a) to output samples of multi-path receiver (r)

$$G \cdot \vec{a} = \vec{r}$$

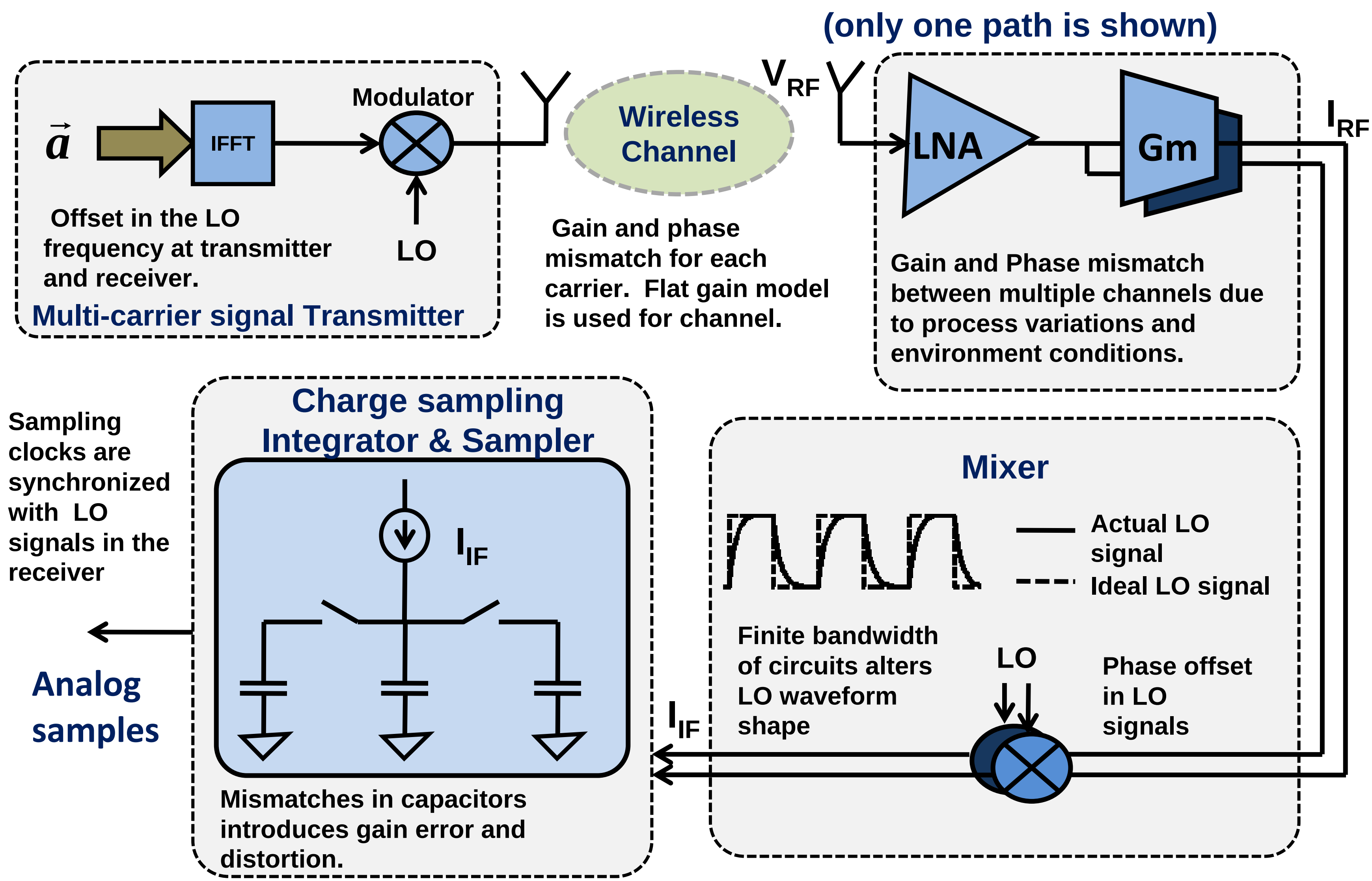
Least Squares (LS) solution for the system -> $H = (G^H G)^{-1} G^H$

Estimate Equation -> $\hat{a} = H \cdot \vec{r}$

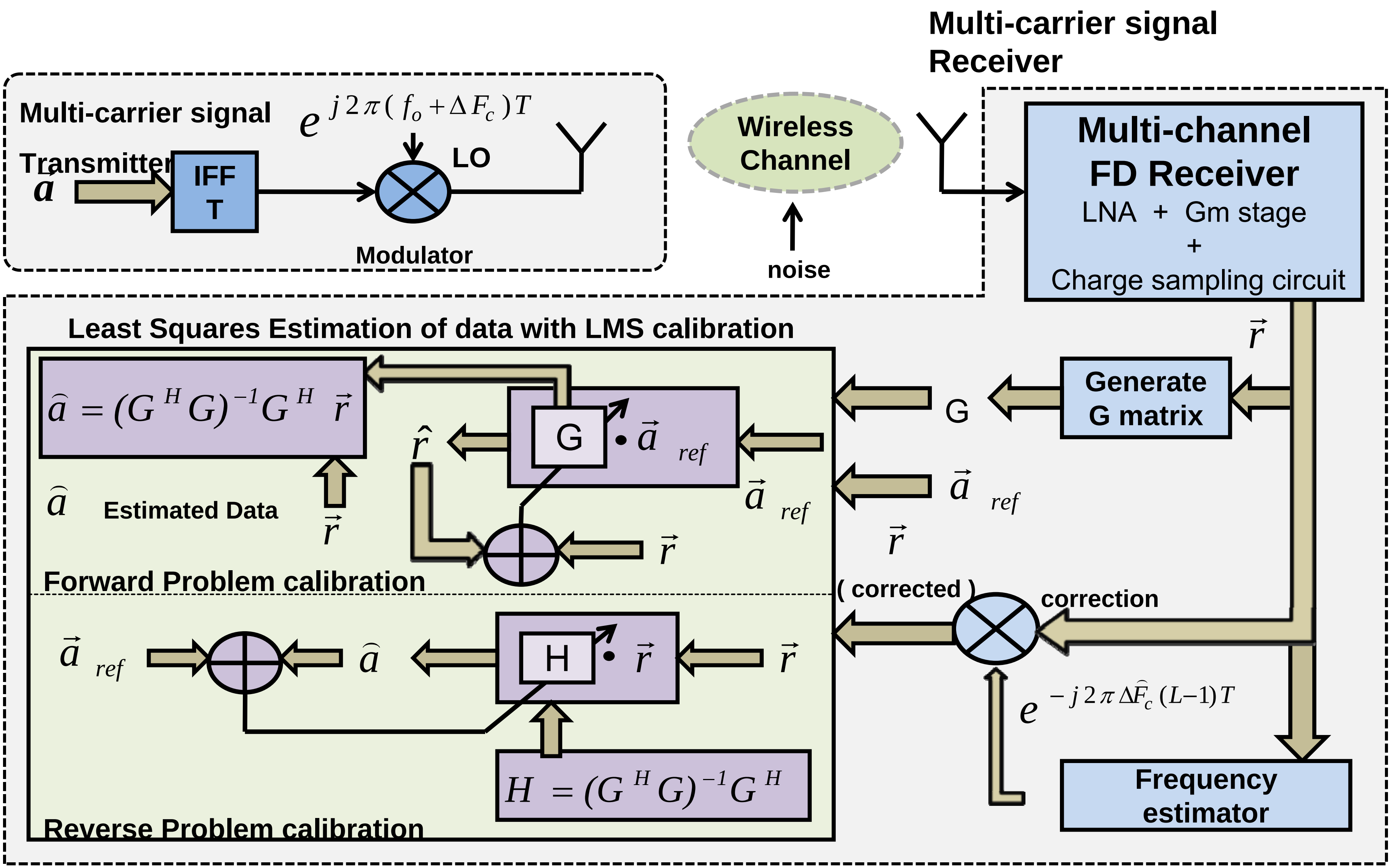
Need for Calibration ?

- H is sensitive to mismatches, offsets and imperfections in the system
- H must match the circuit implementation accurately for good SNR

Mismatches in the system



Complete System Calibration



LMS Calibration

Initialization of G matrix

$$G \cdot \vec{a} = \vec{r}$$

Input -> a1 a2 a3 . . . . aS

Output -> r1 r2 r3 . . . . rS

a1 -> $[1\ 0\ 0\ 0\ .\ .\ .\ 0]^T$

r1 forms 1st row of G matrix

a2 -> $[0\ 1\ 0\ 0\ .\ .\ .\ 0]^T$

r2 forms 2nd row of G matrix

a3 -> $[0\ 0\ 1\ 0\ .\ .\ .\ 0]^T$

r3 forms 3rd row of G matrix

aS -> $[0\ 0\ 0\ 0\ .\ .\ .\ 1]^T$

rS forms Sth row of G matrix

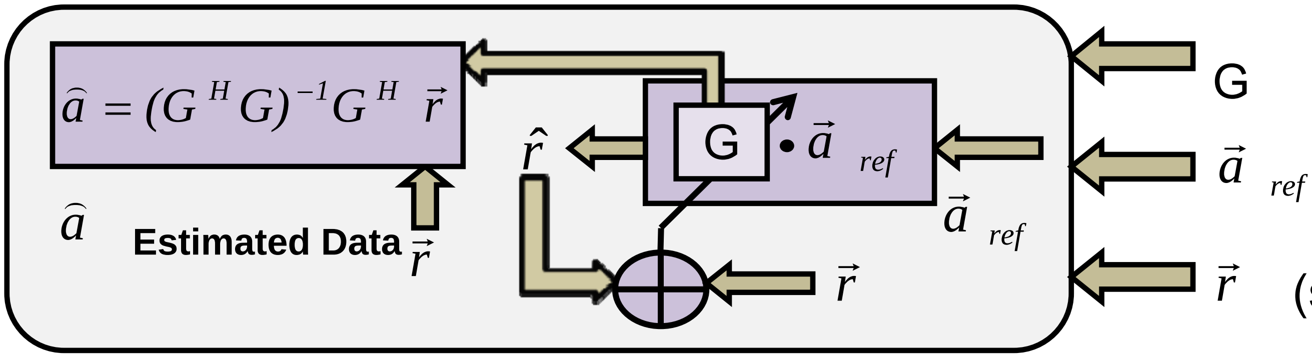
LMS calibration

Two methods:

1.Forward Problem Calibration

2. Reverse Problem Calibration

Forward Problem Calibration



Forward Problem

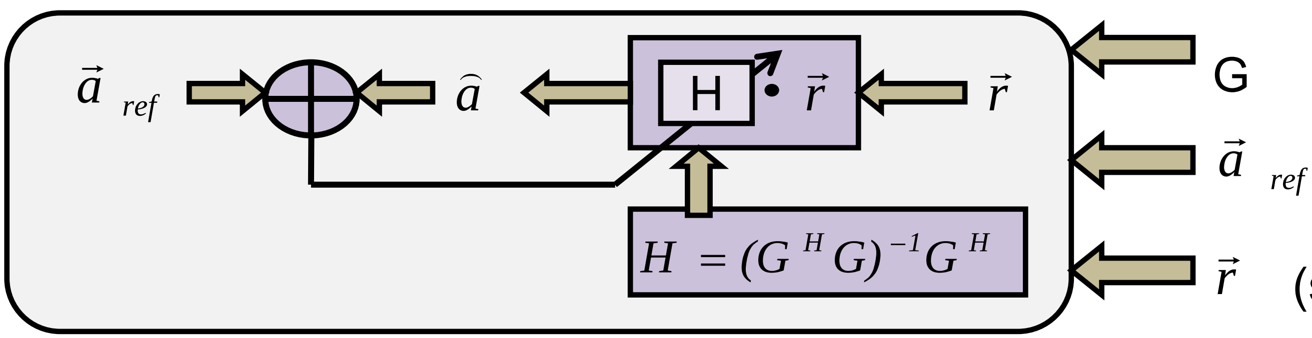
$G \cdot \vec{a} = \vec{r}$

(samples from receiver)

Forward Problem update equation

$$\hat{G}(L+1) = \hat{G}(L) + \frac{\vec{e_r}(L) * \vec{a}}{\|a\|^2}$$

Reverse Problem Calibration



Reverse Problem

$\hat{a} = H \cdot \vec{r}$

(samples from receiver)

Reverse Problem update equation

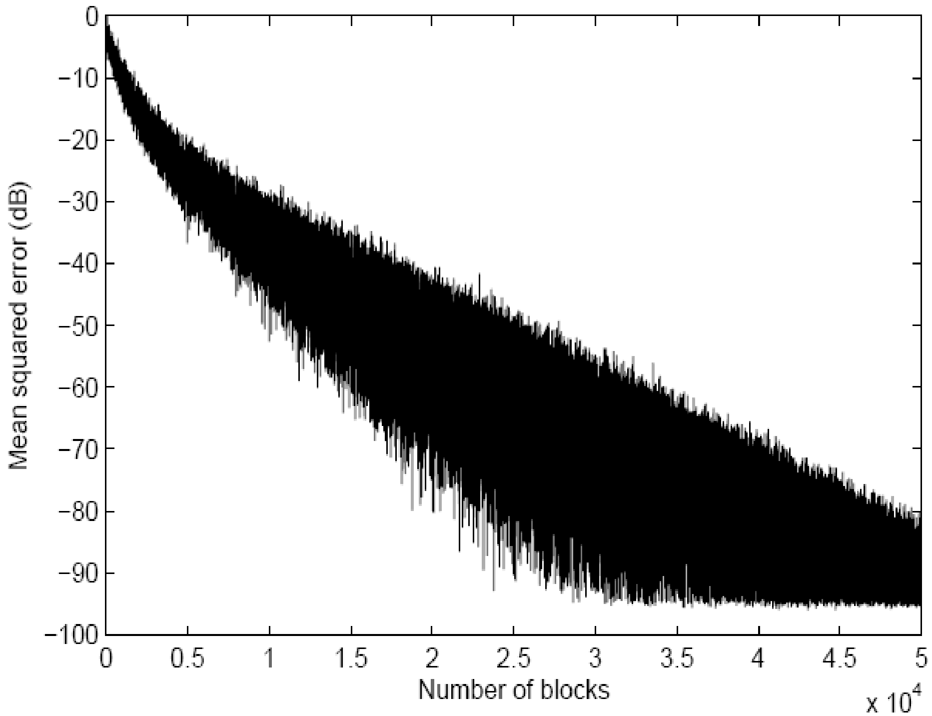
$$\hat{H}(L+1) = \hat{H}(L) + \frac{\vec{e}_a(L) * \vec{r}}{\|r\|^2}$$

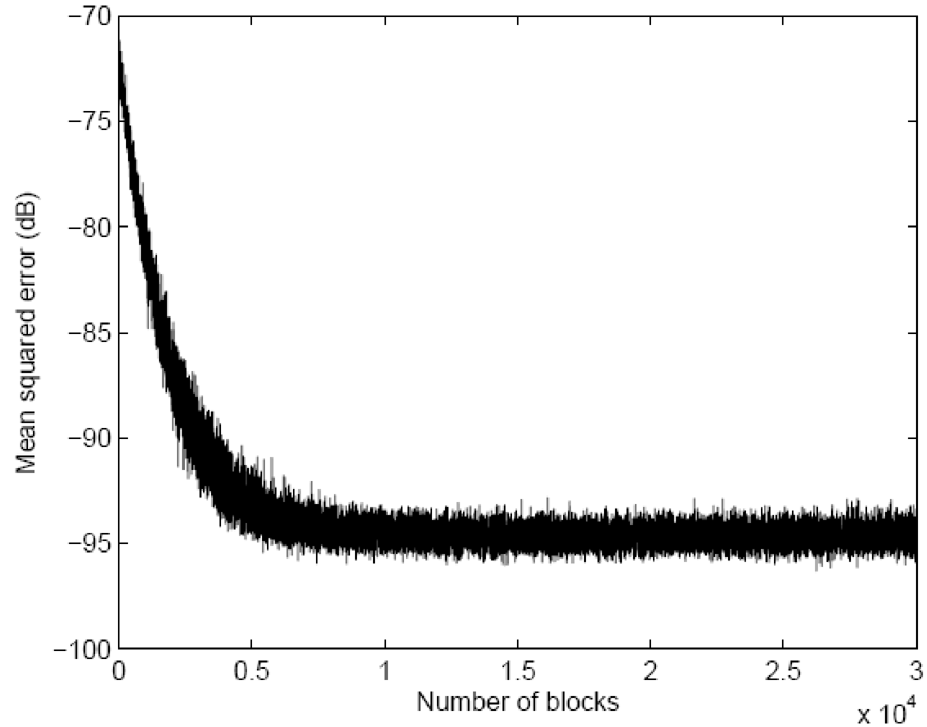
Simulations

Mean squared error convergence

1. With arbitrary H matrix

2. With H matrix initialized from ‘r’ vector





Very slow convergence

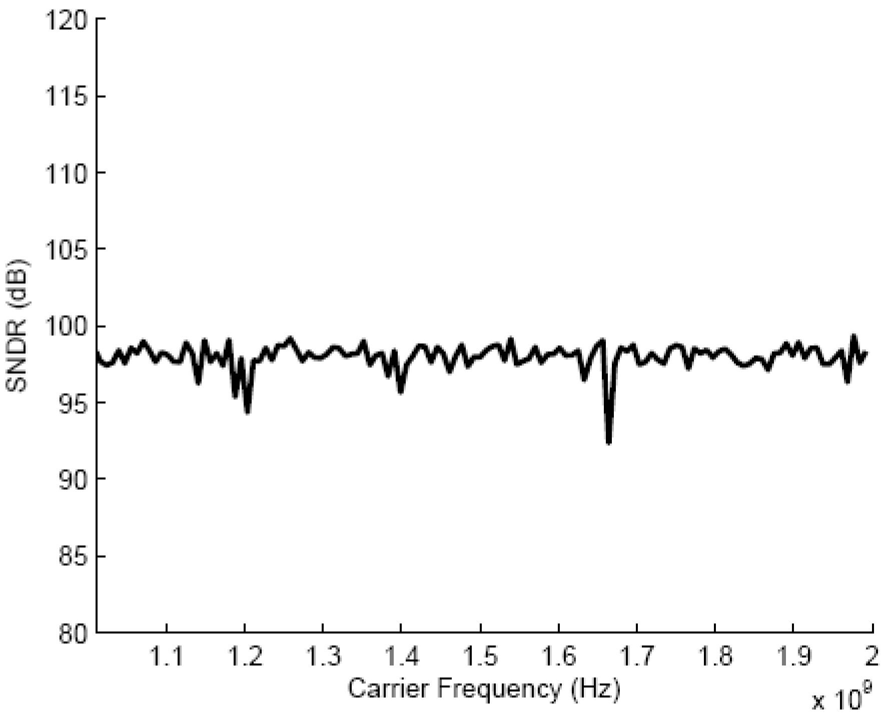
Fast convergence

Simulations

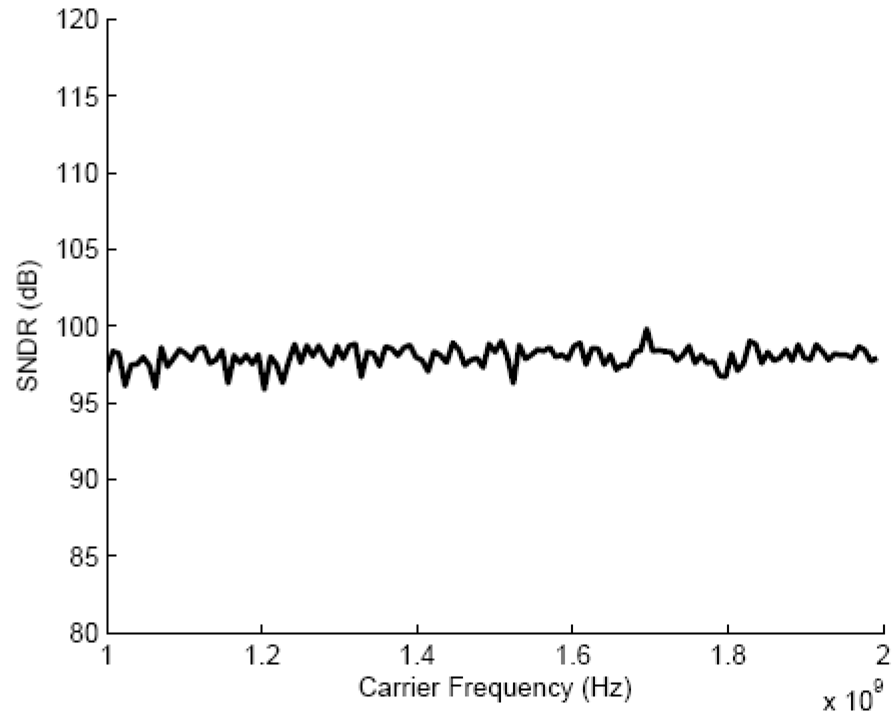
SNDR post calibration

Input SNR = 100 dB
Frequency offset in carriers is not included

1. With arbitrary H matrix



2. With H matrix initialized from ‘r’ vector



All static mismatches are calibrated in both cases.

Frequency offset Estimation

The sampled basis coefficients in block L,

$$R_{m,n,L} = \int_{mT_s+\Delta T}^{mT_s+T_c+\Delta T} x_L(t)\Phi_n^*(t)dt$$

where,

$$\Phi_n(t) = e^{-j[2\pi f_{LO}(n)t + \phi_{LO}(n)]} - \frac{1}{3}e^{j[3\cdot 2\pi f_{LO}(n)t + 3\cdot\phi_{LO}(n)]} + \frac{1}{5}e^{-j[5\cdot 2\pi f_{LO}(n)t + 5\cdot\phi_{LO}(n)]} - \ldots$$

LO signal

$$x_L(t) = \sum_{s=1}^{S}\left[a_i(s)cos\left(2\pi F_c^{'}(s)t + \phi_c(s) + 2\pi\Delta F_c(L-1)T\right) + a_q(s)sin\left(2\pi F_c^{'}(s)t + \phi_c(s) + 2\pi\Delta F_c(L-1)T\right)\right]$$

Input signal

$$F_c^{'}(s) = F_c(s) + \underbrace{\Delta F_c}_{\text{Frequency offset in carriers}}$$

Frequency offset Estimation

After a few steps of simplification,

Gain and phase mismatch in n^{th} channel

$$R_{m,n,L} \;=\; e^{2\pi j \Delta F_c (L-1)T} \int_{mT_s}^{mT_s+T_c} \sum_{s=1}^{S} A_n e^{j\theta_n} \times$$

Term inside integral is independent of L

$$\Big[\frac{a_i(s)}{2}\, e^{j[2\pi F_c^{'}(s)t + \phi_c(s) + 2\pi F_c^{'}(s)\Delta T - 2\pi f_{LO}(n)t + \phi_{LO}^{'}(n)]}$$
$$+\frac{a_q(s)}{2j}\, e^{j[2\pi F_c^{'}(s)t + \phi_c(s) + 2\pi F_c^{'}(s)\Delta T - 2\pi f_{LO}(n)t + \phi_{LO}^{'}(n)]}\Big]\, dt$$

If $R_{m,n,L} = \alpha_{m,n}\, e^{\,j\beta_{m,n}}$ then $R_{m,n,L+1} = e^{2\pi j \Delta F_c T} \times \alpha_{m,n}\, e^{\,j\beta_{m,n}}$

Including noise in these terms, the samples in the L^{th} and $(L+1)^{th}$ block are,

$$R_{m,n,L} \;=\; \alpha_{m,n}\, e^{\,j\beta_{m,n}} + W_{m,n,L}$$

$$R_{m,n,L+1} = e^{2\pi j \Delta F_c T} \times \alpha_{m,n}\, e^{\,j\beta_{m,n}} + W_{m,n,L+1}$$

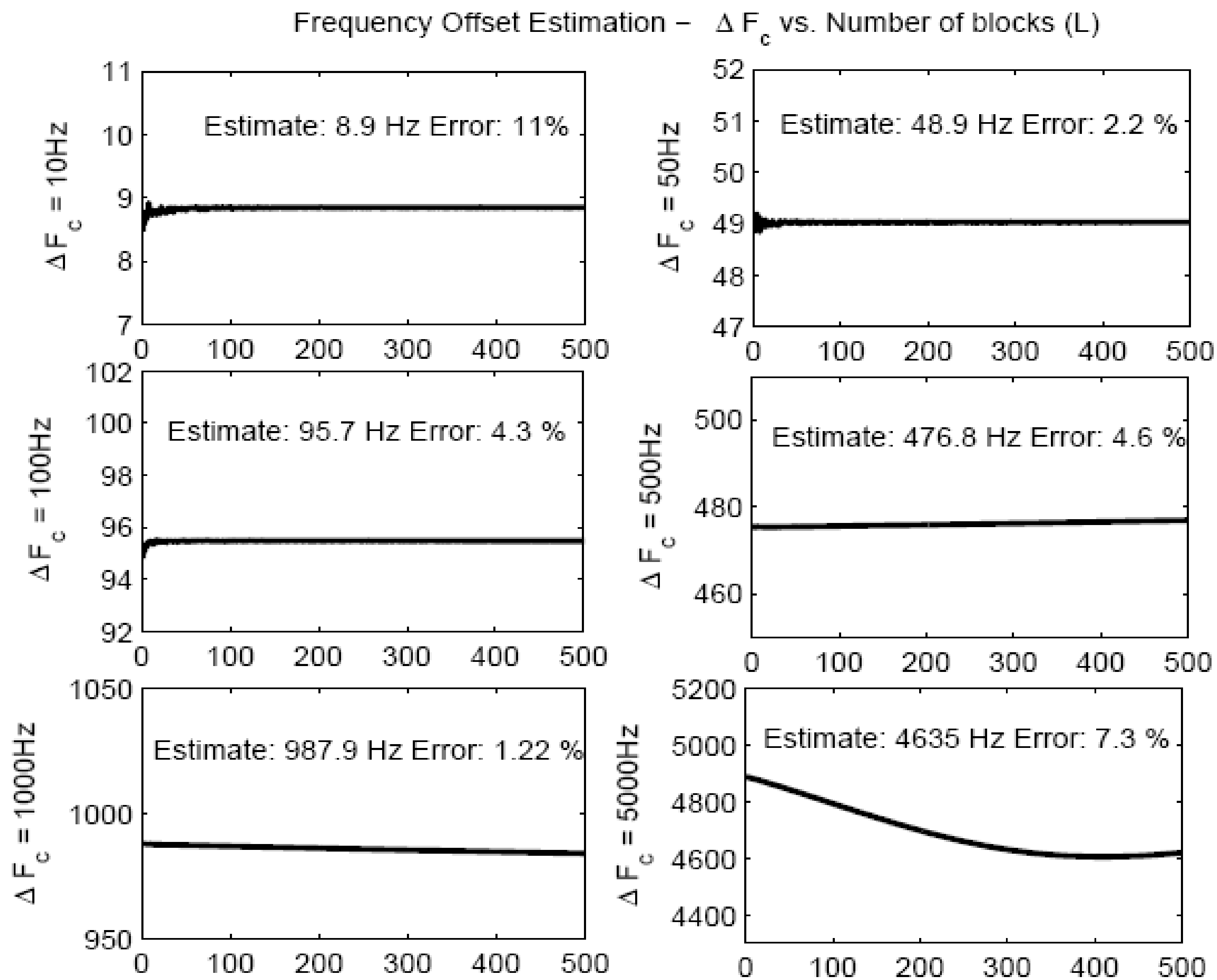
Maximum-Likelihood Estimation of Frequency offset,

$$\boxed{\Delta\hat{F}_c = \frac{1}{2\pi T}\, tan^{-1}\left[\frac{\sum_{L=1}^{K} Im(R_{m,n,L+1}R^{*}_{m,n,L})}{\sum_{L=1}^{K} Re(R_{m,n,L+1}R^{*}_{m,n,L})}\right]}$$

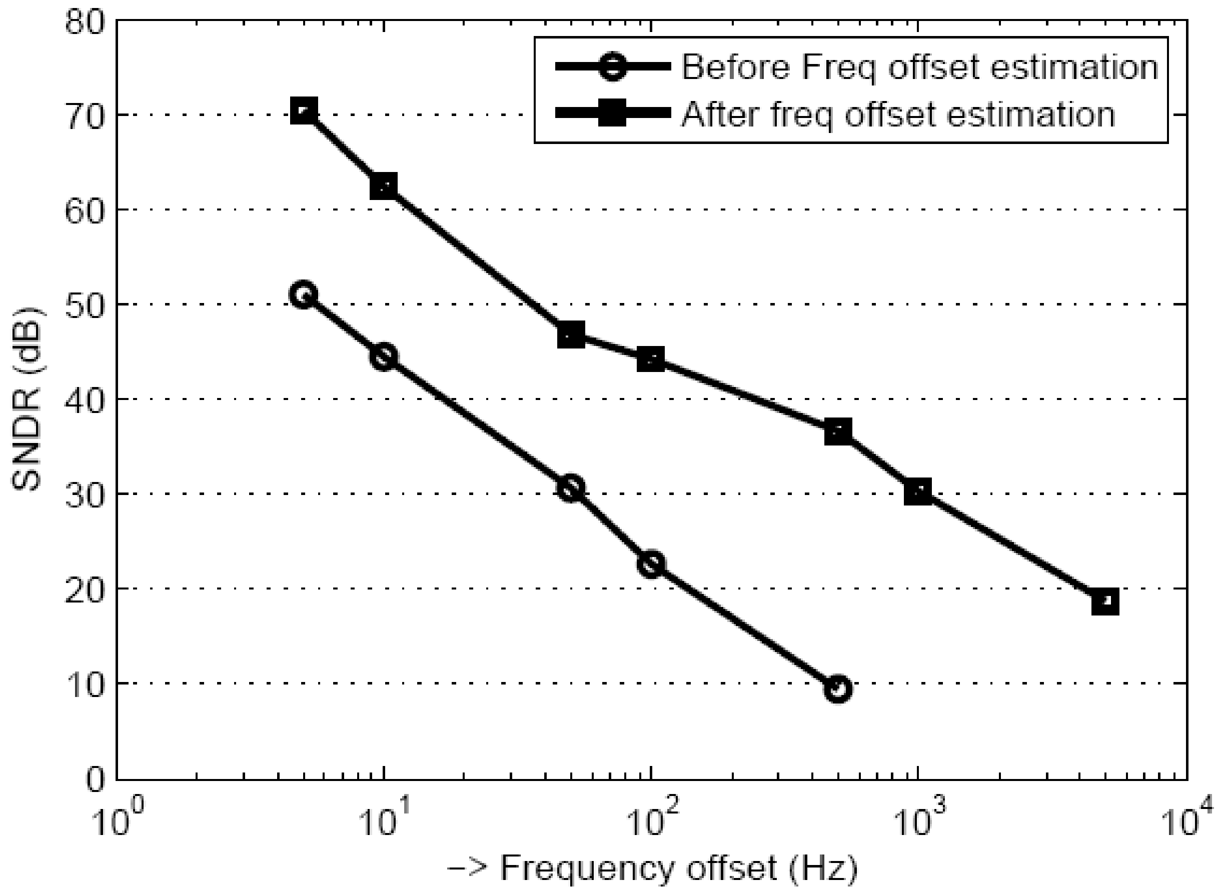
Correction to the ‘r’ vector

$$\vec{r_L}(update) = \vec{r_L} \cdot e^{\,-j2\pi\Delta F_c (L-1)T}$$

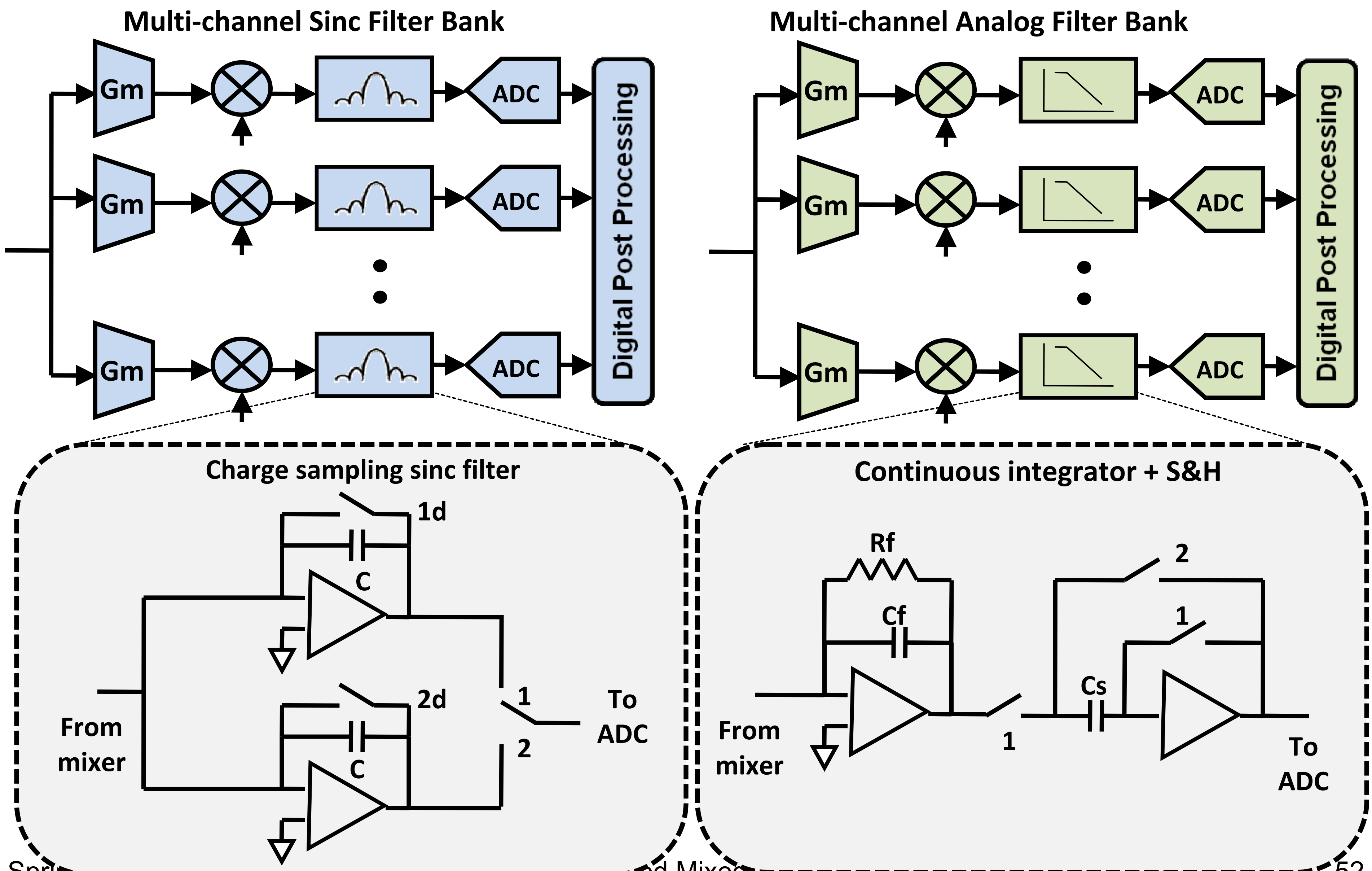
Simulations



Simulations



- ➢ About 20 dB improvement in performance with frequency offset estimation.
- ➢ Performance limited by the accuracy of the estimate.


Multi-channel Sinc Filter Bank
Gm
ADC
Digital Post Processing
Charge sampling sinc filter
1d
C
2d
1
2
From mixer
To ADC
Multi-channel Analog Filter Bank
Gm
ADC
Digital Post Processing
Continuous integrator + S&H
Rf
Cf
2
1
Cs
1
From mixer
To ADC

Analog Complexity

Sinc Filter Bank	Continuous integrator filter bank
$f_{-3dB} \approx 0.44 / Ts$	$f_{-3dB} \approx 1 / 2\pi R_f C_f$
DC gain = Gm Ts / C	DC gain = GmR_f
Int. noise = KT/C (2GmTs/C) + KT/C	Int. noise = $GmR_f .KT/C_f + KT/C_f + KT/C_s$
GBW (op-amp 1,2) >> $1/ 2\pi R_o C$ GBW (1,2) > 7/(settling time) (β~1) (10bits)	GBW (1) >> $1/ 2\pi R_f C_f$ GBW (2) > 7/(settling time) (β~1) (10bits)
Example: Assuming Gm = 1mA/V, Ts = 4ns,	
DC gain = 4, $f_{-3dB} \approx 110MHz$	For DC gain = 4, Rf = 4K For $f_{-3dB} \approx 110MHz$, $C_f \approx C/3$
Noise = 9KT/C	Noise = 13KT/C + KT/C_s
GBW (1,2) ≈ 1.75 GHz	GBW (1) ≈ 1.5 GHz (as $C_f \approx C/3$) GBW (2) ≈ 3.5 GHz (for settling time = 2ns)

Digital Complexity

$$\begin{aligned}\hat{a} &= H \cdot \vec{r} \\ &= (G^H G)^{-1} G^H \cdot \vec{r}\end{aligned}$$

Step 1: $\vec{p} = G^H \cdot \vec{r}$

Step 2: $\hat{a} = (G^H G)^{-1} \vec{p}$

Each element in G is given by,

$$\begin{aligned}G_{m,n,s} &= \int_{mT_s}^{mT_s+T_c} e^{-j2\pi F_c(s)t}\, \Phi_n(t) dt \\ &= e^{-j2\pi F_c(s) mT_s} \int_0^{T_c} e^{-j2\pi F_c(s)t}\, \Phi_{m,n}(t) dt\end{aligned}$$

$f_{LO}(n) \cdot T_s$ is an integer. So, $\Phi_{m,n}(t)$ is periodic repetition of $\Phi_{0,n}(t)$

$$\begin{aligned}G_{m,n,s} &= e^{-j2\pi F_c(s) mT_s} \int_0^{T_c} e^{-j2\pi F_c(s)t}\, \Phi_{0,n}(t) dt \\ &= e^{-j2\pi F_c(s) mT_s}\, Q_{s,n}\end{aligned}$$

$F_c(s) \cdot T_s = s/M + \text{integer}$

$$G_{m,n,s} = e^{-j2\pi sm/M}\, Q_{s,n}$$

$$\begin{aligned}p_s &= \sum_{m=0}^{M-1} \sum_{n=0}^{N-1} G^*_{m,n,s}\, R_{m,n} \\ &= \sum_{n=0}^{N-1} Q^*_{s,n} \sum_{m=0}^{M-1} R_{m,n}\, e^{j2\pi sm/M} \\ &= \sum_{n=0}^{N-1} Q^*_{s,n} T_{s,n}\end{aligned}$$

Complexity of computation of p: o(4NM logM) + o(4NS) ≈ o(4S(logM + N))

Digital Complexity

Sparsity of $(G^H G)^{-1}$

$G^H G$ is denoted by $X = [X_{i,j}]_{S\times S}$

$$X_{i,j} = \sum_{m=0}^{M-1}\sum_{n=0}^{N-1} e^{-j2\pi(i-j)m/M} Q_{i,n}Q_{j,n}^{*}$$

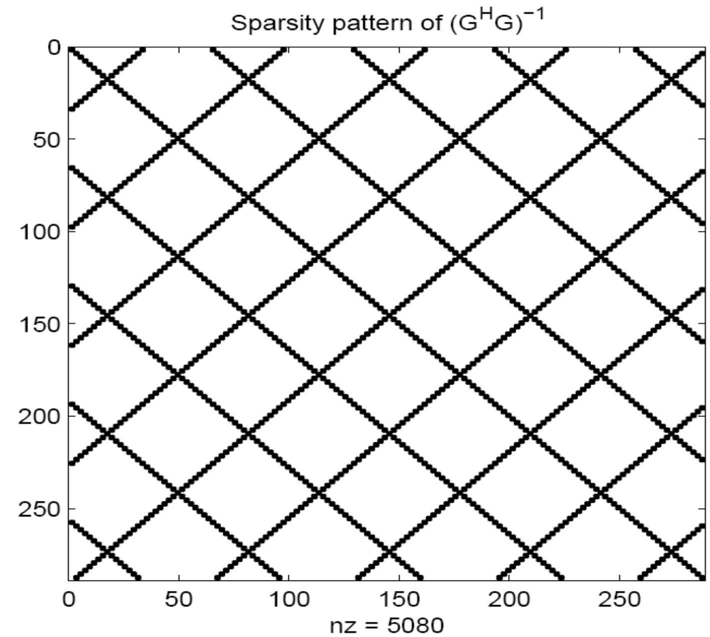
$$= \sum_{n=0}^{N-1} Q_{i,n}Q_{j,n}^{*} \sum_{m=0}^{M-1} e^{-j2\pi(i-j)m/M}$$

$$X_{i,j} = \left\{ \begin{array}{ll} M\sum_{n=0}^{N-1} Q_{i,n}Q_{j,n}^{*} & (i-j) mod\, M = 0 \\ 0 & otherwise \end{array} \right\}$$

$X_{i,j}$ is non-zero only when (i-j) mod M = 0

- $G^H G$ has only 2N non-zero elements in each row
- Inverse of $G^H G$ also has the same sparsity.

  Complexity of computation of
  - **$G^H G$ -> o(2N x 2N x 2S) = o($8N^2S$)**
  - **$(G^H G)^{-1}$ -> o(2N x 2N x 2S) = o($8N^2S$)**



Digital Complexity

Step 1: $\vec{p} = G^H \cdot \vec{r}$ Complexity: o(4S(logM + N))

Step 2: $\hat{a} = (G^H G)^{-1}\vec{p}$ Complexity: o(4NS)

Total Complexity of LS estimation : o(4S(logM + N)) + o(4NS)

Example: S = 128, M = 32, N = 5

Complexity of FFT: o(4SlogS) = **o(28S)**

Complexity of LS estimate,

Sinc filter bank: o(4S(logM + N)) + o(4NS) = **o(60S)**

Analog filter bank: o(4NMS) = **o(640S)**

Complexity of estimation during LMS calibration

Forward Problem:

$$\begin{aligned}\hat{a} &= H \cdot \vec{r} \\ &= \underbrace{\underbrace{(G^H G)^{-1}}_{o(16N^2S)} \underbrace{G^H \cdot \vec{r}}_{o(4S\,(\log M+N))}}_{o(4NS)}\end{aligned}$$

Reverse Problem:

$$\hat{a} = \underbrace{H \cdot \vec{r}}_{o(4NMS)}$$

Example: S = 128, M = 32, N = 5

Forward Problem:

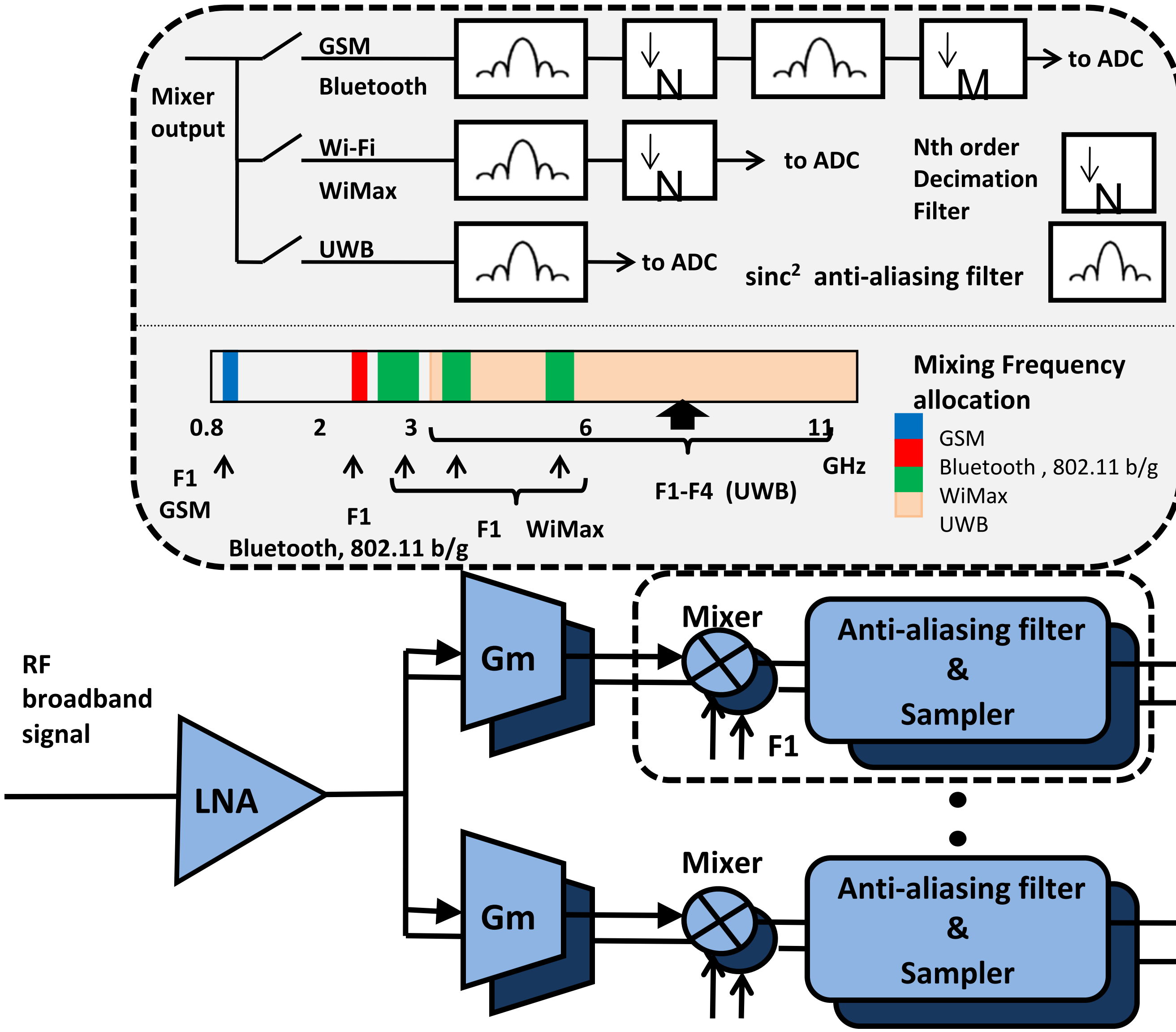
o($16N^2S$) + o(4S (logM+N)) + o(4NS) = **o(460S)**

Reverse Problem:

o(4NMS) = **o(640S)**

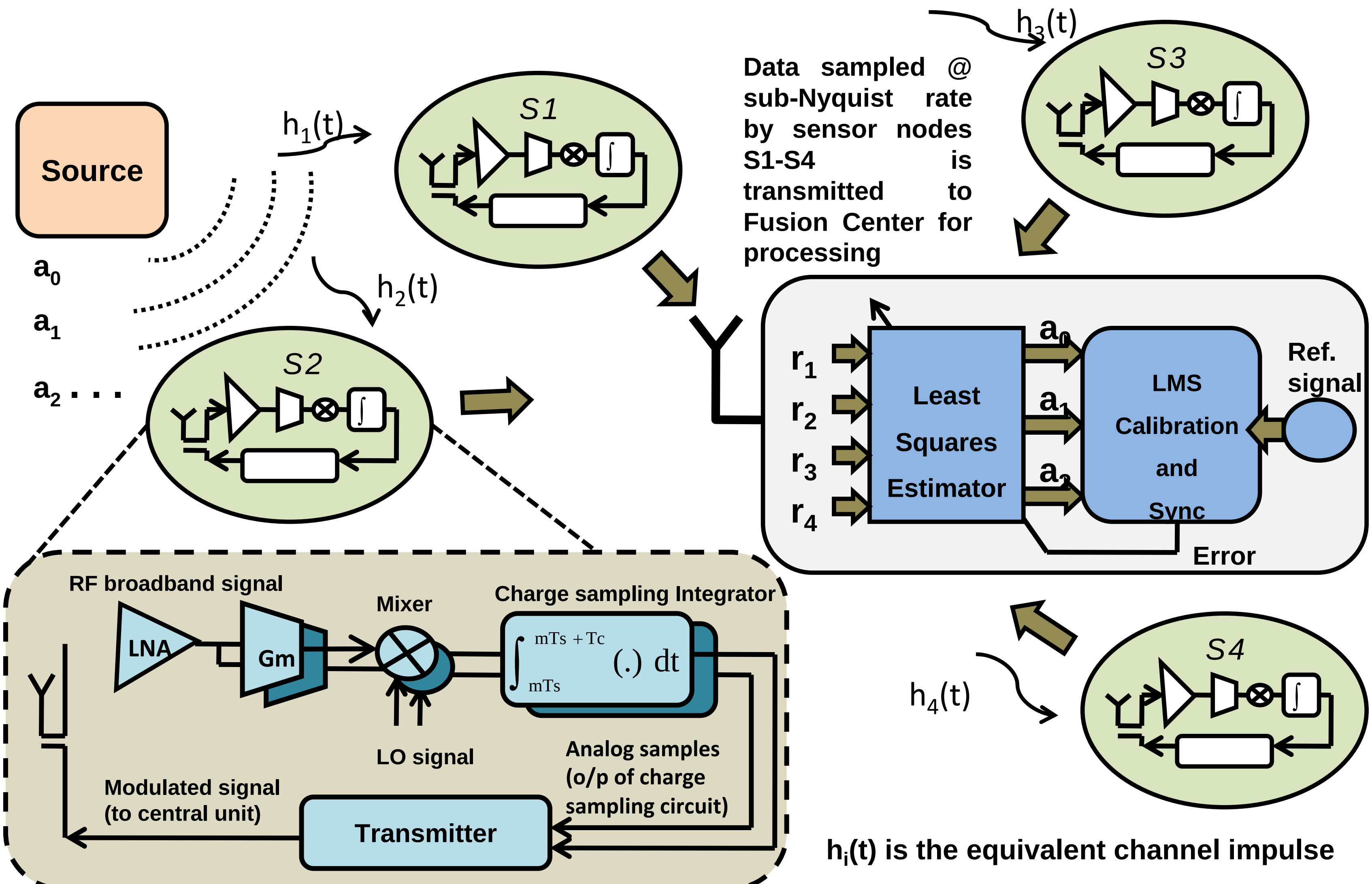
Comparative Study	Sinc Filter Bank	Analog Filter Bank
Analog Front end complexity	Larger capacitors No resistor required. Reset ensures finite DC gain. Lesser noise Smaller GBW for op-amps.	Smaller capacitors Resistor required for finite DC gain. Noise is high. Larger GBW for op-amps.
Analog Power consumption	Less	4 times higher
Digital complexity (Estimation)	o (4S (N + logM)) + o(4NS) Example: o (60S)	o (4NMS) Example: o (640S)
Digital complexity (Estimation @ calibration)	$o(16N^2S) + o(4S(\log M+N)) + o(4NS)$ Example: o(460S)	o (4NMS) Example: o (640S)
Digital power consumption	Low Example: About 10% of	High Example: 10 times more

Multi-Standard reconfigurable FD receiver



Standard	Bandwidth	Bits
UWB	500 MHz	5
WiMax	25 MHz	7
Wi-Fi	20 MHz	8
Bluetooth	1 MHz	12
GSM	200 KHz	14

Decentralized TD Sensor Network



Data sampled @ sub-Nyquist rate by sensor nodes S1-S4 is transmitted to Fusion Center for processing

$h_i(t)$ is the equivalent channel impulse response for sensor node Si