Chapter V

Complementary Metal-Oxide-Semiconductor Field Effect Transistor Circuits

The bipolar junction transistor (BJT) is very versatile three-terminal device that has been extensively used within integrated circuits since its invention in the late 1940s. Over the years, these multipurpose BJT devices have served as amplifiers, switches, and temperature sensors in many different types of analog and digital chips. Nowadays they are still popular, especially in amplifiers requiring a wide frequency range and in voltage/current reference circuits. Since BJTs are available as inexpensive individually packaged components, you can also encounter them in circuits assembled on printed circuit boards for machine control applications and instrumentation equipment. In this chapter, you will learn the BJT’s operation and small-signal model, as well as how to use BJTs to design circuits.

V.1. Fundamentals on CMOS Transistors.

The Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET or simple MOS) is fabricated employing a planar technology that facilitates its manufacturing resulting in a very compact and efficient device. The N-MOS device is built over a P-type substrate. Two highly doped N⁺ junctions are used as drain and source terminals. Notice that to isolate the drain and source terminals the diodes due to the interfaces between N⁺ and P-substrate must be reverse biased. The P-type substrate is connected to the lowest potential used to maintain the PN junctions biased in reverse direction. The gate voltage is biased at a positive potential with respect to the substrate to attract electrons (minority carriers in the substrate) to the interface between the thin SiOx and substrate layers, creating an inversion layer. The electrons accumulated in the channel are then swept between drain and source when a voltage \( V_{DS} \) is applied. Transistor operation is a strong function of the channel length \( L \) and width \( W \); these dimensions are displayed in Fig. 1b.

![Diagram of CMOS Transistor](image)

Fig. 5.1. N-type MOS transistor. a) Cross view of the transistor; b) top view displaying the definition of channel length and width; b) symbol of the N-type transistor.

The threshold voltage is, in a first approximation, the voltage required to turn-on the transistor. When \( V_{GS} \) is smaller than \( V_T \), the transistor operates in the so-called sub-threshold region; this region is also known as weak inversion. Under this condition, the gate-substrate electric field is not strong enough to attract a large number of quasi-free carriers to the channel, resulting in small drain-source currents usually in the range of nA-μA. When the condition \( V_{GS} > V_T \) is satisfied, the vertical electric field is strong enough to attract significant quasi-free carriers to the channel. These carriers are swept when a drain-source voltage \( V_{DS} \) is applied. The MOS transistor has two modes of
operation while in strong inversion: a) when the $V_{DS} < V_{GS} - V_T$ the MOS transistor operates in the linear region and b) if $V_{DS} > V_{GS} - V_T$ it operates in the saturation region.

**VI.2. MOS transistor operating in triode region.** The MOS transistor operates in strong inversion (strong vertical electric field) but the drain-source voltage is weak; then the lateral electrical field is weak. In this regime the drain current is approximated by the following quadratic function

$$I_{DS} = \left( K_n \frac{W}{L} \right) \left( V_{GS} - V_T - \frac{V_{DS}}{2} \right)^2, \quad \text{if} \quad V_{GS} - V_T > 0, \quad \text{and} \quad V_{DS} < V_{GS} - V_T$$  \hspace{1cm} (5.1)

Where $K_n (=\mu_C V_T)$ is a technological parameter equal to the product of channel carrier mobility and the permittivity of the gate-channel silicon-oxide over its thickness. $V_T$ stands for the threshold voltage, which is a technological parameter that depends on the source-to-substrate voltage;

$$V_T = V_{T0} + \gamma \left( \sqrt{2\phi_F} + V_{SB} - \sqrt{2\phi_F} \right),$$  \hspace{1cm} (5.2)

where $V_{T0}$, $\phi_F$ and $\gamma$ are technological parameters, and $V_{SB}$ is the source to substrate voltage. $V_{T0}$ is in a first order independent of the transistor voltages, then the threshold voltage can be considered constant if $V_{SB}$ is maintained constant. This statement is not valid for deep submicron technologies where more accurate models have to be used.

The linear small signal model of the MOS transistor operating in triode region can be obtained expanding equation 5.1 using a multi-dimensional series expansion. If both the gate-source voltage and drain-source voltage have small signal components on top of the DC components and if the threshold voltage is assumed voltage invariant, the series expansion of the bi-dimensional expression of $i_D(V_{GS}, V_{DS})$ yields,

$$i_{DS} \approx I_{DS} + \beta_n \left\{ \begin{array}{l}
\left( \frac{\partial i_d}{\partial V_{gs}} \right)_Q v_{gs} + \left( \frac{\partial i_d}{\partial V_{ds}} \right)_Q v_{ds} + \\
\frac{1}{2} \left( \frac{\partial^2 i_d}{\partial V_{gs}^2} \right)_Q v_{gs}^2 + 2 \left( \frac{\partial^2 i_d}{\partial V_{gs} \partial V_{ds}} \right)_Q v_{gs} v_{ds} + \left( \frac{\partial^2 i_d}{\partial V_{ds}^2} \right)_Q v_{ds}^2 \\
\frac{1}{6} \left( \frac{\partial^3 i_d}{\partial V_{gs}^3} \right)_Q v_{gs}^3 + 3 \left( \frac{\partial^3 i_d}{\partial V_{gs}^2 \partial V_{ds}} \right)_Q v_{gs}^2 v_{ds} + 3 \left( \frac{\partial^3 i_d}{\partial V_{gs} \partial V_{ds}^2} \right)_Q v_{gs} v_{ds}^2 + \left( \frac{\partial^3 i_d}{\partial V_{ds}^3} \right)_Q v_{ds}^3 + \ldots \end{array} \right\}$$  \hspace{1cm} (5.3)

where the sub-index Q stands for evaluation at the operating point (DC value of $V_{GS}$ and $V_{DS}$). It is not difficult to add the effects of threshold voltage variations with VSB, but the expressions are a bit more complex. Let us be focus on the most relevant terms in (5.1) and obtain its first order small signal model.
Employing this equation for the expansion of the drain current expression of the transistor operating in triode region, and assuming that \( V_{DS} < V_{DSAT} \) and \( V_{GS} > V_T \), then eqn (5.1) results in

\[
\begin{align*}
    i_{ds} &= \beta \left( V_{DS} v_{gs} + (V_{DSAT} - V_{DS}) v_{ds} + \frac{1}{2} \left( v_{gs} v_{ds} - v_{ds}^2 \right) \right),
\end{align*}
\]  

(5.4)

This equation shows that the drain current shows several components: the first one proportional to the AC signal applied at the gate-source terminals. If \( V_{DS} \) is kept constant, then the circuit operates as a linear transconductor where the equivalent transconductance value is controlled with \( V_{DS} \). This configuration is frequently used in applications where linear voltage controlled current sources are needed; Operational transconductance amplifiers, linear filters, etc. Ignoring the high order terms in (5.4), the small signal drain-source current can be approximated as

\[
\begin{align*}
    i_{ds} &= (\beta V_{DS}) v_{gs} + (\beta (V_{DSAT} - V_{DS})) v_{ds} = g_m v_{gs} + g_{ds} v_{ds},
\end{align*}
\]  

(5.5)

where the transistor transconductance \( g_m = \beta V_{DS} \) and drain-source conductance is computed as \( g_{ds} = \beta (V_{DSAT} - V_{DS}) \). It is worth mentioning that even if \( V_{DS} \) is zero, the conductance is not zero, but the transconductance becomes zero. This operating condition is very useful since power. The small signal model is represented in Figure 5.2b.

Fig. 5.3. a) N-type transistor symbol and b) simplified small signal model while operating in triode region.

If \( V_{GS} \) is maintained constant, the drain current can be controlled with the DC value of \( V_{DSAT} - V_{DS} \); this architecture is especially attractive when operating the transistor with small signal variations such as \( v_{ds} \ll V_{DSAT} - V_{DS} \); then the circuit behaves as a linear voltage controlled conductor whose conductance is approximately equal to \( \beta (V_{DSAT} - V_{DS}) \). Wider linear range and better linearity is usually obtained when \( V_{DS} = 0 \) since this condition maximizes the linear term while the quadratic term remains constant, leading to smaller second order harmonic distortion.

VI.3. MOS Transistor Small Signal model when operating in saturation region. The drain-source current of long channel (L>180nm) MOS transistors when operating in saturation region can be approximated by a quadratic function as follows

\[
\begin{align*}
    I_{DS} &= \left( \frac{K_n}{2} \right) \frac{W}{L} (V_{GS} - V_T)^2 \left( 1 + \lambda V_{DS} \right), \text{ if } V_{GS} - V_T > 0, \text{ and } V_{DS} > V_{GS} - V_T
\end{align*}
\]  

(5.6)

The parameter lambda (\( \lambda \)) models the drain current variation due to the drain-source electric field; this parameter is precisely modeled in high level models, but it has been shown that its value reduces with transistor length and it is usually approximated as

\[
\begin{align*}
    \lambda \approx \frac{1}{LV_{early}},
\end{align*}
\]  

(5.7)

where the early voltage per unit length (\( V_{early} \)) is expressed in Volts/\( \mu \)m. Since the drain voltage is primarily determined by the overdriving voltage \( V_{GS} - V_T \), equation 5.1 can then be expressed in a bit simplest form as
\[ I_{DS} = \left( \frac{\beta}{2} \right) \left( 1 + \lambda V_{DS} \right) V_{DSAT}^2, \]  

(5.8)

where the overdrive voltage (or saturation voltage) is defined as \( V_{DSAT} = V_{GS} - V_T \).

In this section, the small signal model of the MOS transistor operating in saturation region is obtained. Similar to the case of the transistor operating in triode region, the most relevant parameters are the small signal transconductance and output (drain-source) resistance. Usually the drain-source resistance is smaller than the output resistance of bipolar devices and can not be ignored in many practical applications.

If the gate voltage is composed by a DC component and an small AC component \( v_{\text{gs}} \), then the drain current can be expressed as function of the small signal variations \( v_{\text{gs}} \) and \( v_{\text{ds}} \) as

\[ i_d = \left( \frac{\beta}{2} \right) \left( 1 + \lambda (V_{DS} + v_{\text{ds}}) \right) \left( V_{DSAT} + v_{\text{gs}} \right)^2 \]

\[ = \left( \frac{\beta}{2} \right) \left( 1 + \lambda (V_{DS} + v_{\text{ds}}) \right) \left( V_{DSAT}^2 + 2V_{DSAT} v_{\text{gs}} + v_{\text{gs}}^2 \right) \]

(5.9)

The drain current is function of all the voltages applied to the transistor terminals; the DC voltages \( VGS, VDS \) and \( VSB \) as well as the AC signals present at the gate and drain terminals. In this section it is assumed that the \( VSB \) do not show significant voltage variations, and then we will consider the threshold voltage constant. This may not be the case in many practical applications such as source follower and common-base configurations. According to (5.8) the output current shows several components that are are more evident if (5.8) is expanded

\[ i_d = \frac{\beta}{2} V_{DSAT}^2 \left( 1 + \lambda V_{DS} \right) + \left( \beta V_{DSAT} \left( 1 + \lambda V_{DS} \right) \right) v_{\text{gs}} + \left( \frac{\beta \lambda}{2} V_{DSAT}^2 \right) v_{\text{ds}} + \]

\[ + \left( \frac{\beta}{2} \left( 1 + \lambda V_{DS} \right) \right) v_{\text{gs}}^2 + \left( \frac{\beta \lambda}{2} \right) v_{\text{gs}}^2 v_{\text{ds}} \]

(5.10)

Five current components are evident: i) the first one is AC signal independent and corresponds to the bias current \( I_D \) (eqn 5.3); ii) the second component is proportional to the input signal, and this component is the desired current component; the coefficient of \( v_{\text{gs}} \) is defined as the small signal transconductance; iii) the third term varies with the output signal, and this term correspond to the transistor output conductance; iv) The fourth term is proportional to the \( v_{\text{gs}}^2 \), and leads to the second order harmonic distortion; it is advisable to reduce its power as much as possible; v) The last term is due to the cross-product between \( v_{\text{gs}} \) and \( v_{\text{ds}} \). Since the output voltage is correlated with the input signal, this term usually results in third order distortion; this is more evident if we approximate the fundamental component of the drain-source voltage as an amplified version of the input signal \( v_{\text{ds}} = A_v v_{\text{gs}} \), then a third order distortion component becomes apparent.

The linear model of the transistor is obtained assuming that \( v_{\text{gs}} \ll 1 \), then the drain current is low sensitive to the nonlinear terms in (5.9); this is a reasonable approximation for small input signal conditions. The coefficient of \( v_{\text{gs}} \) in 5.9 can be recognized as the small signal transconductance of the MOS transistor. It can be formally obtained from equation 5.10 as

\[ g_m = \left. \frac{\partial i_d}{\partial v_{\text{gs}}} \right|_Q = \beta V_{DSAT} \left( 1 + \lambda V_{DS} \right) \]

(5.11)

The MOS transistor drain-source conductance can then be approximated as
\[ g_{ds} = \beta \frac{\partial i_d}{\partial V_{ds}} |_{Q} \approx \frac{\beta}{2} V_{DSAT}^2 \lambda \approx I_{DS} \lambda. \] (5.12)

For the case \( \lambda V_{DSAT} \ll 1 \), the following \( g_m \) expression can be used

\[ g_m \approx \beta V_{DSAT} \] (5.13)

The small signal model including the gate-source capacitance is displayed in Fig. 5.4. The value of \( C_{gs} \) is estimated as \( C_{gs} = W \varepsilon_{ox} L \), where \( W \) and \( L \) are the dimensions of gate width and length, respectively, \( \varepsilon_{ox} \) is the thickness of the gate oxide and \( \varepsilon_{ox} \) is the permittivity of the thin silicon oxide layer.

Notice that if \( C_{gs} \) is ignored, this model is identical to the one representing the transistor in triode region. The differences are in the equations used to compute the values of \( g_m \) and \( g_{ds} \). Another remarkable simplification in this model is the assumption that the substrate is connected to an AC ground terminal and that \( v_{be} \) does not have significant impact on the threshold voltage.

\[ \begin{align*}
V_g & \quad i_g = 0 \\
V_{gs} & \quad C_{gs} g_m V_{gs} \\
V_v & \quad g_{ds} \\
V_d & \quad i_{ds} \\
V_{gs} & \quad C_{gs} g_m V_{gs} \\
V_d & \quad g_{ds}
\end{align*} \]

Fig. 5.4. Simplified small signal model while operating in saturation region: a) Hybrid model and b) T-model. Use equations 5.11 and 5.12 for computing \( g_m \) and \( g_{ds} \), respectively.

The input impedance of the MOS transistor is capacitive, and is determined as \( 1/sC_{gs} \), which is quite relevant at high frequencies. The effect of \( C_{gs} \) is usually ignored when computing the low and medium frequency voltage gain of the amplifier. An evident effect of \( C_{gs} \) is its impedance reduction at high frequency, usually reducing the its drain current and so its drain current; in most of the practical cases this capacitance is the ultimate limitation for the frequency response of the amplifier. Indeed the frequency response of the MOS transistor is determined by \( f_t = g_m / 2\pi C_{gs} \), which represents the unity gain frequency of the transistor when driving an identical stage.

5.2.3. Harmonic Distortion Components.

\[ HD2 = \frac{V_{gs}^2}{4V_{DSAT} + \left( \frac{\lambda V_{DSAT}^2}{2(1 + \lambda V_{DS})} \right) \left( V_{ds} / V_{gs} \right)} \] (5.14)

In this expression, the term \( V_{ds}/V_{gs} \) represents the amplifier voltage gain, and it is usually larger than 1. Notice that the drain-gate voltage gain is usually negative, then \( l \) effects usually leads to higher harmonic distortion components. If \( V_{DSAT} V_{ds} << 1 \), the simplified expression often used for first order computations is obtained.
The third order distortion results due to the cross product of $v_{gs2}$ and $v_{ds}$; assuming that $v_{ds}=A v_{gs}$, then the third order distortion can be defined as follows

$$HD3 = \left( \frac{v_{ds}}{v_{gs}} \right) \left( \frac{\lambda \cdot v_{gs}^2}{V_{DSAT}} \right)$$

(5.16)

According to this result, smaller values for $l$ (longer devices) lead to smaller distortion components. It is worth mentioning that this result is valid assuming that the threshold voltage is voltage invariant. It can be shown expanding the expression for $V_T$ that additional third order distortion results when the transistor is exposed to $v_{sb}$ variations.

5.3. Common-emitter amplifier.

5.3.1. DC Analysis. The DC analysis requires considering the capacitors as open circuits. Gate current is zero since the gate terminal is because the gate channel interface is capacitive. Therefore,

$$V_G = \left( \frac{R_{G2}}{R_{G1} + R_{G2}} \right) VDD.$$  

(5.17)

The DC drain current is computed using the equation of the transistor (eqn 5.8) resulting in:

$$I_{DS} = \left( \frac{\beta}{2} \right) \left( 1 + \lambda V_{DS} \right) \left( V_{GS} - V_T \right)^2.$$  

(5.18)

Equation 5.25 can not be solved because it is function of two unknowns: $V_{DS}$ and $IDS$. The second equation that allows us to solve 5.25 is lumped to the drain voltage. Notice that $V_{DS}$ is computed as

$$V_{DS} = VDD - I_{DS} R_D.$$  

(5.19)
Equation 5.26 can be inserted into eqn 5.25, leading to a second order linear equation that determines the drain current as function of VGS, VDD and the technological parameters $\beta$, $\lambda$ and $V_T$

$$I_{DS} = \left(\frac{\beta}{2}\right)(1 + \lambda(VDD - I_{DS}R_D))(V_{GS} - V_T)^2.$$  (5.20)

For first order (and easy) computations, it can be assumed that the value of $\lambda$ is very small, then leading to a straightforward solution for IDS.

### 5.3.2. AC Analysis.

The small signal AC analysis is carried out by shorting the DC voltage sources and opening the DC current sources. The resulting circuit including the gate-source capacitance is depicted in Figure 6.6. Since $i = 0$, the gate-source voltage can be obtained employing the expression for the voltage divider, yielding

![Common-Source Amplifier: linear small-signal model.](image)

$$v_g = \left(\frac{R_G || 1}{sC_{gs}}\right) v_i = \left(\frac{sR_G C_1}{1 + sR_G (C_1 + C_{gs})}\right) v_i.$$  (5.21a)

The series capacitor $C_1$ blocks (high impedance) the low-frequency signal generating the zero in 5.21. The zero at the $f=0$ raises the transfer function at a rate of +20dB/decade until the frequency of the pole. After the frequency of pole ($\omega_p=1/R_G(C_1+C_{gs})$), the voltage gain $vgs/vi$ is flat and is determined by the capacitors. Notice that at high frequency $RG$ (in parallel with $C_{gs}$) can be ignored, leading to a simplified transfer function

$$\frac{v_{gs}}{v_i} = \frac{C_1}{C_1 + C_{gs}} \quad ; \text{if} \quad f > 1/\left(2\pi R_G \left(C_1 + C_{gs}\right)\right).$$  (5.21b)
The drain current generated by the voltage controlled current source is computed from $v_{gs}$ using ohms law ($=g_m v_{gs}$), and the drain voltage $v_d$ is then determined by evaluating the product of $g_m v_{gs}$ and the equivalent impedance at node $v_d$ ($= r_{ds}||\left(\frac{1}{RL}+1/sC_2\right)$). Some intuition on the operation of the circuit is gained by observing that the equivalent impedance at $v_d$ is equal to $R_d$ at low frequencies while its value decreases at high frequencies and became equal to $r_{ds}||RL$. This behavior suggests that when measured at $v_d$, the voltage gain is higher at low frequencies; a pole at intermediate frequencies makes the gain to drop with a rate of -20dB/decade, and a zero at higher frequency makes the gain to be constant. Demonstrate that the location of the pole and zero are $w_p=1/RLC_2$ and the zero is placed at $w_z=1/\left((RL||r_{ds})C_2\right)$. The output voltage $v_o$ can be obtained from $v_d$ making use of the voltage divider properties. It can also be obtained employing the current division principle to obtain the expression of the current flowing through $RL$, and then the computation of the $v_o$ is easy using ohms law. Following this approach, it can be shown that

$$v_o = -R_L i_d \left( \frac{R_D \| r_{ds}}{R_D \| r_{ds} + R_L + \frac{1}{sC_2}} \right) = -g_m R_L v_{gs} \left( \frac{s \left(R_D \| r_{ds}\right)C_2}{1 + s \left(R_D \| r_{ds} + R_L\right)C_2} \right),$$

(5.22)

This equation shows that the input circuit configuration has a high-pass transfer function due to the zero located at $\omega = 0$ and the pole at $\omega = 1/(r_{ds}+R_L)C_2$. The frequency components below the frequency of the pole will be attenuated due to the effect of the blocking capacitor connected in series; the $v_o$ to $v_{gs}$ voltage gain at high frequencies became equal to $-g_m R_L$.

$$\frac{v_o}{v_i} = -\left( \frac{s R_G \left(C_1 + C_{gs}\right)}{1 + s R_G \left(C_1 + C_{gs}\right)} \right) \left( \frac{s \left(R_D \| r_{ds}\right)C_2}{1 + s \left(R_D \| r_{ds} + R_L\right)C_2} \right) g_m R_L$$

$$= -\left( \frac{s}{\omega_{Z1}} \right) \left( \frac{s}{\omega_{Z2}} \right) \left( \frac{s}{\omega_{p1}} \right) g_m R_L$$

(5.23)

The overall voltage gain shows two poles generated by the blocking capacitors, and two zeros placed at the origin; the poles are located at the following frequencies:

$$\omega_{Z1} = \frac{1}{R_G C_1}$$
$$\omega_{P1} = \frac{1}{R_G \left(C_1 + C_{gs}\right)}$$
$$\omega_{Z1} = \frac{1}{\left(R_D \| r_{ds}\right)C_2}$$
$$\omega_{P2} = \frac{1}{\left((R_D \| r_{ds} + R_L\right)C_2}$$

(5.24)
The MOS transistor’s input capacitance \( C_{gs} \) decreases the frequency of the first pole, and its effect can be safely ignored if \( C_1 \) is in the range of nF or larger; typically \( C_{gs} \) is under 1pF, with the exception of the transistors used in power applications where \( C_{gs} \) might be even in the range of the nF. The second pole is usually dominated by the drain-source resistance of the transistor and \( C_2 \). The larger \( r_{ds} \) the smaller the frequency of the second pole. In the passband \((w > w_{P1}, w_{P2})\), the expression for the voltage gain simplifies to

\[
\frac{v_o}{v_i} = -\left(\frac{C_1}{C_1 + C_{gs}}\right) \left(\frac{R_D \ || \ r_{ds} \ || \ R_L}{g_m}\right) \quad (5.25)
\]

Eqn. 5.24 is useful for first order computations, but we have to keep in mind that this expression is only valid for frequencies beyond the location of the pole’s frequencies.

**Fig. 5.7. Common source amplifier’s magnitude response**

Fig. 5.7 shows the transfer function assuming that \( w_{P1} < w_{P2} \). The typical practice in audio amplifiers is to increase as much as possible the capacitance values of \( C_1 \) and \( C_2 \); those approach is limited by form factor and cost. Another common practice is to increase the value of \( R_G \); this approach push \( w_{P1} \) to lower frequencies. For high frequency applications, this practice shows significant limitations because large capacitors are usually electrolytic. These capacitors show significant inductance and losses, leading to an equivalent circuit composed by the series combination of the capacitor, resistor and inductor. Therefore, the high frequency impedance at high frequency behaves as an inductor. The inductive behavior may appear even in the range of few MHz. Ceramic or tantalum capacitors are preferred for video applications; however, their values are limited.

The amplifier input impedance \( Z_i \) is entirely determined by the parallel of \( R_g \) and the impedance of the capacitor, as depicted in Fig. 5.6. Since \( i = 0 \), then
Z_i = \frac{R_G}{sC_{gs}} = \frac{R_G}{1 + sR_G C_{gs}} . \tag{5.26}

Z_i is mainly resistive (\cong R_G) for frequencies below the pole frequency but capacitive beyond the pole frequency (\cong 1/sC_{gs}). Since the input impedance reduces with frequency, it demands more power at the input to maintain large signal at the amplifier’s gate.

5.3.4. Practical Design Considerations. Practical issues when designing the common source amplifier includes avoiding clipping issues when the different nodes experience large signal swings to achieve low distortion figures. *Harmonic Distortion due to non-linear drain current.* The designer should limit the signal swing otherwise the non-linear behavior of the transistor’s voltage-to-current conversion results in limited signal to distortion ratios. The harmonic distortion generated by the standalone transistor is described by eqns 5.14 and 5.16.
The gate-\(v_i\) voltage gain is given by 5.21; for in-band signals, the computation of HD2 yields,
\[
HD2 \approx \frac{C_1}{C_1 + C_{gs}} \left(1 - \frac{\lambda V_{DSAT}}{8(1 + \lambda V_{DS})} \right) \frac{V_{i-pk}}{4V_{DSAT}}
\] (5.26a)

With
\[
\left| \frac{v_{ds}}{v_{gs}} \right| \approx g_m \left( \frac{r_{ds} R_L}{r_{ds} + R_L} \right)
\] (5.27)

Equation 5.26a is a very stringent constraint when designing low-distortion amplifiers. The dominant parameter determining the amplifier linearity is the ratio of input signal power to the saturation voltage. If \( l \) is very small, then a simpler yet useful expression for hand calculations results

\[
HD2 \approx \left( \frac{C_1}{C_1 + C_{gs}} \right) \left( \frac{V_{i-pk}}{4V_{DSAT}} \right) = \frac{i_{d-pk}}{8I_{DS}}
\] (5.26b)

Since \( v_{o-pk} = i_{d-pk}(R_D||R_L) \), and if the value of the maximum value of HD2 than can be tolerated is known, then the DC drain current can be bounded (from 5.26b) as

\[
I_{DS} \geq \left( \frac{C_1}{C_1 + C_{gs}} \right) \frac{v_{o-pk}}{8 \cdot HD2 \cdot (R_L || R_D)}
\] (5.28)

Evidently, the larger the output signal swing the larger the bias current to maintain the harmonic distortion figure. This is a very useful equation when designing low-distortion single-ended amplifiers. The third order distortion is determined by 5.16, leads to

\[
HD3 \approx \frac{v_{ds}}{v_{gs}} \left( \frac{v_{ds}}{V_{DSAT}} \right) - \frac{\lambda}{2} \frac{v_{ds}}{V_{DSAT}} \right) \left( \frac{v_{gs}}{V_{DSAT}} \right)
\] (5.28b)

Low HD3 figures require large VDSAT values as well; long channel devices that lead to smaller \( \lambda \) values help reducing HD3 as well. Large drain-to-gate voltage gain figures increase HD3 since the output voltage swing increases, then the power of the cross product distortion components present in 5.14 and 5.16 increase as well. The non-linear voltage-to-current conversion is displayed in Fig. 5.8. Small vgs signals are converted into current in a more linear fashion than large signals; limiting the amplitude of the input signal to VDSAT/2.5 yields HD2 \(-20 \text{ dB} \) while for \( |v| = VDSAT/10 \) leads to HD2 \(-32 \text{ dB} \). A more efficient approach employs fully-differential architectures where the even harmonic distortions are less critical; the overhead is that those architectures are more complex and require additional circuitry for controlling the operating point. The study of these architectures is out of the scope of this book, but readers interested in these devices can read [Reference].

**Signal swing limitations.** The signal swing is bounded by the power supply and the minimum drain-source voltage required to maintain the transistor operating in saturation region. If the operating point is selected such that VDS is small (see Q1 in Fig. 5.8b), the negative peak value of the drain voltage swing is then limited as follows:
\[ V_{DS} = VDD - I_{DS} R_D > V_{DSAT} + V_{d-pk} \]  
(5.2930)

Where \( V_{d-pk} \) is the peak value of the drain voltage. If on the other hand the Q point is selected with large \( V_{DS} \) voltage, the positive swing is then limited by the power supply, as displayed in Fig 5.8b, Q2. The \( V_{DS} \) voltage is constrained to satisfy the following condition

\[ V_{DS} = VDD - I_{DS} R_D < VDD - V_{d-pk} \]  
(5.319)

Equations 5.29 and 5.30 are combined in the following expression:

\[ \frac{VDD - V_{DSAT} - V_{d-pk}}{R_D} > I_{DS} > \frac{V_{d-pk}}{R_D} \]  
(5.324)

The design problem consists on finding the resistances and IDS values that satisfy the gain, input impedance, and linearity condition. In case additional degrees of freedom exist, other conditions such as minimum power consumption can be added.

5.3.5. Common-Source amplifier with source degeneration. Better linearity figures can be obtained by adding a (linear) resistor between the source of the transistor and an AC ground. In order to obtain first order solutions, let us ignore the I effects. The drain current of the source degenerated amplifier is obtained from 5.18 as

\[ I_{DS} = \left( \frac{\beta}{2} \right) (V_{GS} - V_T)^2 = \left( \frac{\beta}{2} \right) (V_G - V_T - I_{DS} R_S)^2 \]  
(5.33)

Equation can now be solved because it is function of VG and technological parameters. The solution of the second order equation results in

\[ V_{DS} = VDD - I_{DS} R_D \]  
(5.34)

Equation 5.26 can be inserted into eqn 5.25, leading to a second order linear equation that determines the drain current as function of VGS, VDD and the technological parameters \( \beta \), \( \lambda \) and \( V_T \)

\[ I_{DS} = \frac{1}{1 + 2\beta R_S (V_G - V_T)} \]  
(5.35)

---

Fig. 5.9. Common-source amplifier with source degeneration: a) schematic and b) small signal equivalent circuit
Let us find first order equations to predict the linearity of the source degenerate topology. If \( V_G \) is replaced by \( V_G + v_i \), then (5.35) can be expanded as

\[
i_{DS} = \frac{1}{\beta R_s^2} + \frac{V_G - V_T}{R_s} - \left( \frac{1 + 2\beta R_s (V_G - V_T)}{\beta R_s^2} \right) \sqrt{1 + \frac{2\beta R_s v_i}{1 + 2\beta R_s (V_G - V_T)}}
\]

(5.35)

This expression can be expanded using a Taylor series, yielding

\[
i_{DS} \approx \frac{1}{\beta R_s^2} + \frac{V_G - V_T}{R_s} \left( \frac{1 + 2\beta R_s (V_G - V_T)}{\beta R_s^2} \right) \sqrt{1 + \frac{2\beta R_s v_i}{1 + 2\beta R_s (V_G - V_T)}}
\]

\[
+ \left( \frac{1}{R_s} - \frac{1}{R_s \sqrt{1 + 2\beta R_s (V_G - V_T)}} \right) v_i
\]

\[
+ \left( \frac{\beta}{2(1 + 2\beta R_s (V_G - V_T))^{3/2}} \right) v_i^2
\]

\[
- \left( \frac{\beta^2 R_s}{2(1 + 2\beta R_s (V_G - V_T))^{5/2}} \right) v_i^3
\]

(5.36)

\[
g_m = \frac{1}{R_s} \left( \frac{1 + 2\beta R_s (V_G - V_T)}{2\beta R_s^2} \right) \approx \frac{1}{R_s + \sqrt{1 + 2\beta R_s (V_G - V_T)}}
\]

\[
+ \left( \frac{1 + 2\beta R_s (V_G - V_T)}{8\beta R_s^2} \right) v_i^2
\]

\[
- \left( \frac{3\sqrt{1 + 2\beta R_s (V_G - V_T)}}{48\beta R_s^2} \right) v_i^3
\]

(5.36)
\[ i_{DS} \approx \frac{1}{\beta R_s} + \frac{V_G - V_T}{R_s} \left( \frac{\sqrt{1 + 2\beta R_s (V_G - V_T)}}{\beta R_s^2} \right) \]

\[ + \left( \frac{1}{R_s} - \left( \frac{\sqrt{1 + 2\beta R_s (V_G - V_T)}}{2\beta R_s^2} \right) \right) v_i \]

\[ + \left( \frac{\sqrt{1 + 2\beta R_s (V_G - V_T)}}{8\beta R_s^2} \right) v_i^2 \]

\[ - \left( \frac{3\sqrt{1 + 2\beta R_s (V_G - V_T)}}{48\beta R_s^2} \right) v_i^3 \]

(5.36)

\[ i_{DS} \approx \frac{1}{\beta R_s} + \frac{V_G - V_T}{R_s} \left( \frac{\sqrt{1 + 2\beta R_s (V_G - V_T)}}{\beta R_s^2} \right) \]

\[ + \left( \frac{1}{R_s} - \left( \frac{\sqrt{1 + 2\beta R_s (V_G - V_T)}}{2\beta R_s^2} \right) \right) v_i \]

\[ + \left( \frac{\sqrt{1 + 2\beta R_s (V_G - V_T)}}{8\beta R_s^2} \right) v_i^2 \]

\[ - \left( \frac{3\sqrt{1 + 2\beta R_s (V_G - V_T)}}{48\beta R_s^2} \right) v_i^3 \]

(5.36)

5.4. Common-base amplifier.

5.3.1. DC Analysis

5.3.2. AC Analysis

5.3.4. Design Considerations

5.3.5. Applications

5.4. Common-collector configuration.
5.3.1. DC Analysis

5.3.2. AC Analysis

5.3.4. Design Considerations

5.3.5. Applications.
Since the complexity of the non-linear systems increases with the number of transistors in the circuits, we have to limit our analysis in order to derive simple expressions based on the assumption that the AC input signals are small. The idea is to make reasonable approximations that give us more insights into the operation of the circuits. Although the accuracy of the results will be limited, the solutions are reasonably close to our targets with errors within ±10% in many cases. Once the circuit is designed, we have to simulate it and re-adjust some of the parameters to obtain more accurate results. The design of circuits is usually an iterative process due to the limited accuracy of the theoretical equations and sometimes even due to the discrepancies of the simulation models.

A typical amplifier combines DC and AC signals at the input of the transistor. The circuits used for this operation will be discussed later on, but for the following analysis we assume that the base-emitter voltage has two components as shown in Figure 5.4.

![Fig. 5.4. Typical common-emitter amplifier. The base-emitter voltage has both DC (operating point) and AC (signal) components.](image)

The voltage applied to the base-emitter terminal (V_{BE} + v_{be}) is converted into a current i_C by the transistor. Notice that the transistor is a base-emitter voltage to collector current converter. Since the relationship is exponential, any small signal applied to the base-emitter terminals is mapped into large collector current variations, as can be seen in Figure 5.4. This is the main principle behind the BJT operation. It is worth to make a couple of important observations at this stage:

i) The larger the selected bias (time-invariant) current I_{CQ} is, the larger is the AC current generated by the input signal. Or in other words, larger DC bias current I_{CQ} will result in higher gain during the conversion of an AC input voltage to an AC output current.

ii) If the AC (time-variant signal) input signal v_{be} to be processed is small, then the exponential collector current can be predicted by a linear approximation, which will be apparent shortly. Figure 5.5 visualizes the input-output relationship for a BJT with a set DC bias and an additional sinusoidal AC input signal with small amplitude at the base terminal. You can also recognize in the plot that the superposition principle holds in such a situation since the output current is simply the addition of the AC and DC input voltages. However, in many practical applications we are interested in processing AC signals, and only select the DC bias conditions to guarantee the appropriate transistor properties as discussed later in this chapter.

![Fig. 5.5. Relation between i_C and V_{BE} when a small AC input signal is applied to a BJT device that is biased at a DC Q-point in the linear region.](image)
When a combination of DC and AC signals is applied to the transistor’s base-emitter junction, we can write the expression for the collector current based on equation 5.3 as

\[
i_c = I_S \left( \frac{V_{BE} + V_{th}}{e^{V_{BE}/V_{th}} - 1} \right) \approx I_S e^{V_{th}/V_{BE}} e^{V_{th}/V_{BE}} = I_{CQ} e^{V_{th}/V_{BE}}, \tag{5.7}
\]

where \(I_{CQ}\) is the DC component (collector bias current) of the output current. In this expression we assumed that the transistor is operating in the linear region and that \(V_{BE} > 4V_{th} \approx 100\) mV. As will be elaborated in the following sections, this condition is normally satisfied because the DC base-emitter voltage is usually greater than 500 mV in linear amplifier applications. In the previous equation, the small signal we want to amplify is denoted as \(v_{be}\) in lower-case letters. Since the equation is a smooth function of \(v_{be}\), it can be expanded in a Taylor series around the operating point \(Q (V_{BE}, I_{CQ})\), which is:

\[
i_c = I_{CQ} + I_{CQ} \left( \frac{V_{be}}{V_{th}} \right) + \frac{I_{CQ}}{2} \left( \frac{V_{be}}{V_{th}} \right)^2 + \frac{I_{CQ}}{6} \left( \frac{V_{be}}{V_{th}} \right)^3 + .... \tag{5.8}
\]

The first term in this equation corresponds to the DC current component. The second term is the desired collector current component, which is linearly related to the incoming AC signal \(v_{be}\). The remaining terms lead to the undesired high-order harmonic distortion components due to the transistor’s non-linear characteristics.

To get more insights into the effects of the higher-order terms, let us consider the case of a sinusoidal input signal \(v_{be} = V_{pk} \sin(\omega_0 t)\). Using trigonometric properties and considering the first four terms of equation 5.8, it can be shown that the collector current can be also written as

\[
i_c = I_{CQ} + \frac{I_{CQ} V_{pk}}{4V_{th}} V_{pk}^2 \sin(\omega_0 t) + \frac{I_{CQ}}{8V_{th}} V_{pk}^2 \sin(2\omega_0 t) + \frac{I_{CQ}}{24V_{th}} V_{pk}^2 \sin(3\omega_0 t) \tag{5.9}
\]

The second term in this equation shows that the transistor non-linearity creates a small change of the DC current. Furthermore, it reveals the generation of undesirable signals called harmonic distortion components, which are located at frequencies that are multiples of the fundamental signal frequency \(\omega_0\). The ratios of the amplitudes of these unwanted components to the desired signal are defined as the harmonic distortions. These ratios are frequently used to measure the quality of output signals and to provide quantitative information to the engineers who design systems based on the output signals of analog amplifiers. The first two harmonic distortion quantities are defined as

\[
HD_2 = \frac{\text{Amplitude @ } 2\omega_0}{\text{Amplitude @ } \omega_0} = \frac{I_{CQ} V_{pk}^2}{4V_{th}^2 V_{pk}^2} \approx \frac{1}{4} \left( \frac{V_{pk}}{V_{th}} \right)^2, \tag{5.10a}
\]
In the above equations, the approximations can be made because the second term within the parentheses of the denominator is much smaller than the first term under the assumption that the AC signal current is small compared to the DC current. A piece of information that will help you to interpret the equations for the harmonic distortion quantities is that the unwanted harmonic distortions reduce the quality of the output signal. Thus, it is desirable to maintain a small input signal amplitude ($V_{pk}$) to reduce distortion components and to obtain a linear output signal. Although the largest harmonic distortion is the second-order component ($HD_2$), it can often be suppressed by properly designing the circuit as a fully-differential system with two symmetrical signal paths that process the same signal with opposite polarity. The outputs of a fully-differential circuit can be subtracted, leading to significant cancellation of even-order distortion components ($HD_2$, $HD_4$, etc.) without affecting the fundamental signal. Cancellation methods for $HD_3$ and other odd-order distortion components is a lot more complicated, which is why it is less frequently done to optimize linearity performance. Notice that if we want to reduce the third harmonic component down to 1% of the fundamental component ($HD_3 = 0.01$), then the peak value of the incoming signal $V_{pk}$ must be limited to $V_{th}/2 = 13 \text{ mV}$. For this reason, we will often limit the signals directly at the base-emitter terminal to $v_{be} < 10 \text{ mV}$ such that the circuit can be regarded as a “linear” system. Using this approximation, the resulting model for the transistors AC behavior is termed small-signal model.

Figure 5.6a shows the distorted output current of a BJT in the frequency and time domains. Since the distortion components can be very small, it is usually better to observe the output current using a logarithmic scale. In general, the amounts of distortion are conventionally reported as a percentage or in decibels. For example, the $HD_3$ of 0.01 (1%) corresponds to -40dB since $HD_3_{dB} = 20 \cdot \log(HD_3)$. If the magnitudes of the harmonic components are plotted...
in dB, then HD\textsubscript{2ab}, HD\textsubscript{3ab},... can be easily determined as the difference between the fundamental component and the components at 2\textit{n}, 3\textit{n},... respectively. In comparison, Figure 5.6b depicts the output current spectrum and corresponding transient waveform with reduced distortion components. The improvement can be achieved by lowering the input signal amplitude. Sometimes, selection of non-ideal DC bias conditions creates distortion, especially when the \( V_{CE} > 0.3V \) condition is not guaranteed for the maximum output signal swing, or when the output signal swing is so large that it reaches the supply voltage \( V_{CC} \) which leads to clipping of the signal. While designing analog circuits, you should always check your transient output signal for the maximum expected input signal amplitude to verify that it does not become distorted due to poor choices of component values or DC bias voltages and currents.

Very simple but useful equations can be derived by assuming that the magnitude of the AC signal is smaller than \( 0.4 \cdot V_{be} \approx 10 \text{ mV} \). For this case, the collector current according to equation 5.8 can be approximated as a linear function of the AC base-emitter voltage given by

\[
i_C = I_{CQ} + \left( \frac{I_{CQ}}{V_{th}} \right) V_{be}.
\]

(Fig. 5.11)

Fundamentally, the collector current has two components: the bias current \( I_{CQ} \) and the AC current component that is linearly related to the base-emitter signal voltage. Usually, the AC component is the information that we want to be processed. The parameter that is mapping the AC input voltage \( V_{be} \) into the AC output current is the first derivative of the \( i_C-V_{BE} \) curve evaluated at the operating point \((I_{CQ}, V_{BEQ})\). This parameter is defined as the small-signal transconductance gain:

\[
g_m = \left. \frac{\partial i_C}{\partial V_{BE}} \right|_Q = \frac{I_{CQ}}{V_{th}}.
\]

(Fig. 5.12)

With units of A/V (Siemens, S), the small-signal transconductance of the transistor represents the slope of the linear approximation at the operating point as annotated in Figure 5.7. From this plot, you can also intuitively verify the mathematically expected increase of harmonic distortion components for larger input signal swings. The tangent line that represents the linearization agrees well with the exponential \( i_C-V_{BE} \) relationship around the Q point, but the actual output current \( i_C \) deviates from the line more as the \( V_{BE} \) amplitude is increased around \( V_{BEQ} \). This deviation causes distortion of sinusoidal signals due to the non-linear input-output characteristics.

![Linear approximation for the transistor’s input characteristics at the operating point Q. Around Q, the \( i_C-V_{BE} \) non-linear relationship is approximated by a straight line with a slope given by \( I_{CQ}/V_{th} \).](image)

A simple transistor model can be obtained based on the above assumptions and analysis. In the actual BJT, there is a forward biased diode connected between base and emitter. The base-emitter voltage controls the collector current that can be modeled as a voltage controlled current source, resulting in the small-signal model of the BJT that is depicted in Figure 5.8a. As mentioned earlier, the output current has both DC and AC components. Hence, the diode at the base input should be modeled as a DC voltage source in series with the diode’s resistance \( r_d \), where the base-emitter resistance \( r_e \) is \( 1/g_e \). The transconductance \( g_m \) is determined by differentiating the base current with respect to the base-emitter voltage around the operating point as follows:

\[
g_m = \frac{\partial i_C}{\partial V_{BE}} = \frac{I_{CQ}}{V_{th}}.
\]
\[
g_{m} = \frac{1}{r_{\pi}} = \frac{\partial i_{B}}{\partial V_{BE}} \bigg|_{Q} = \frac{I_{BQ}}{\theta_{th}}. \tag{5.13}
\]

Notice that both DC and AC signals are applied to the BJT’s input at the same time, and that the small-signal parameters \(r_{\pi}\) and \(g_{m}\) depend on the DC operating point since these parameters are determined by the collector and base current derivatives evaluated at \(Q\).

For small signal conditions \(|v_{be}| < 10\, mV\), the transistor operates as a quasi-linear device. Under these conditions, we can use the superposition principle that applies to all linear systems, and analyze the circuit for two different cases: DC signals only, AC signals only. You will see in the following discussions that splitting the analysis into two parts simplifies it. But at the same time, keep in mind that the output voltage consists of the two components and that many AC parameters such as \(g_{m}\) and \(r_{\pi}\) depend on the DC operating conditions.

**V.4. Design Considerations.**

**V.4.1. DC analysis: operating point and definition of the small-signal parameters.** The first analysis is carried out only for DC conditions. Hence the AC signal sources are set to zero by replacing AC voltage sources with short circuits and AC current sources with open circuits in the diagram. Next, the voltages and currents that define the operating point \(Q\) can be calculated in order to find the small-signal parameters (e.g. \(r_{\pi}\) and \(g_{m}\)). Alternatively, the appropriate operating point and bias conditions can be selected to meet given small-signal parameter requirements. The DC analysis of the circuit shown in Figure 5.4 is carried out by making \(v_{be} = 0\), which leads to the diagram in Figure 5.9 and following analytical results:

\[
I_{CQ} = I_{S} e^{\frac{V_{BEQ}}{\theta_{in}}}. \tag{5.14}
\]

From this equation, the \(V_{BEQ}\) voltage controls the collector current and therefore the operating point on the input characteristic curve. Usually \(V_{BE}\) is in the 0.5-0.8 V range.

![Fig. 5.9. Diagram for the DC analysis of the common-emitter amplifier.](image)

The collector-emitter voltage \(V_{CE}\) depends on both collector current and \(R_{C}\). From the circuit shown in Figure 5.9 we can find that

\[
V_{CC} = V_{CEO} + I_{CQ}R_{C}. \tag{5.15}
\]

There is a linear relationship between \(V_{CE}\) and \(I_{C}\), termed load line. For a given \(V_{BEQ}\), both equations 5.14 and 5.15 define the operating point \(Q\) \((V_{BEQ}, I_{CQ}, V_{CEO})\) of the amplifier as shown by the plots in the Figure 5.10a.
The operating point Q must be selected based on the following considerations:

- Since both equations 5.14 and 5.15 affect the operation of the amplifier, the operating point Q is determined by the intersection of the transistor output characteristic associated with V<sub>BE</sub> and the load line. The load line depends on the power supply V<sub>CC</sub> and R<sub>C</sub>. In fact, its crossing point on the x-axis is equal to V<sub>CC</sub>. Furthermore, the slope of the linear equation 5.15 in the i<sub>C</sub>-V<sub>CE</sub> plane is given by -1/R<sub>C</sub>. Therefore, V<sub>CEQ</sub> decreases as the resistor value is increased, which can be seen in Figure 5.10b. Notice that increasing R<sub>C</sub> reduces the slope of the load line, pushing the operating point Q closer to the non-linear regime of the transistor on the i<sub>C</sub>-V<sub>CE</sub> plane when V<sub>CE</sub> < 0.3 V. This is an unfavorable design condition because the output could be very non-linear. It is always good practice to locate the operation point Q within the flat region of the red curve in Figure 5.10b such that V<sub>CE</sub> > 0.3V under all conditions, even when the output voltage at the collector reaches its minimum point due the processed AC signal that will be superimposed with the DC voltage V<sub>CEQ</sub>.

- When an AC signal is added to the DC base-emitter voltage, the overall input voltage is modulated by that signal as shown in Figure 5.10. Accordingly, the operating point moves on the load line to follow the signal. By this process, the signal variations at the base-emitter junction are mapped to the V<sub>CE</sub>-axis, generating the collector-emitter output voltage. Since slope of the load line is -1/R<sub>C</sub>, a larger resistor value at the collector terminal will lead to a more amplified output signal. However, R<sub>C</sub> cannot be increased unconditionally because the operating point Q moves towards the non-linear saturation region where large harmonic distortion components might be generated.

Selection of a proper operating point is one of the most critical considerations during the design of linear amplifiers. The operating point Q must be selected based on the following criteria:

i) The Q point must be able to accommodate the signal variations. Since both DC and AC signals are present at the same time, the overall collector-emitter voltage must vary such that 300 mV < V<sub>CEQ</sub> < V<sub>ce-peak</sub> < V<sub>CC</sub>. Otherwise, the transistor will enter the saturation region or the signal will be limited (clipped) by the supply voltage V<sub>CC</sub>.

ii) The AC parameters r<sub>e</sub> and g<sub>m</sub> are functions of I<sub>BQ</sub> (= I<sub>CQ</sub>/β) and I<sub>CQ</sub>, respectively. The larger the DC current gain of the transistor (β) is, the smaller will be the base current, and the larger will be the base-emitter
resistance $r_s$. Often, the collector current $I_{CQ}$ is directly computed from the required small-signal transconductance $g_{m}$ that determines the amount of AC collector current generated by the AC input signal.

**V.4.2. AC analysis: the $\pi$-hybrid model for BJTs.** The second analysis is carried out only for the AC signals, while the DC voltage sources are shorted and the DC current sources are considered as open circuits. This is the analysis that defines all AC parameters such as input and output impedance, current and voltage gain, as well as the operating frequency range. A simplified AC small-signal model of the amplifier in Figure 5.4 is displayed in Figure 5.12a.

![Fig. 5.12. Schematics for AC analysis: a) AC equivalent diagram of the amplifier, b) equivalent circuit with the $\pi$-hybrid model for the BJT.](image)

Solutions for AC equivalent circuits can be obtained by using fundamental circuit analysis. In this circuit, the AC output voltage is obtained by multiplying the collector current with the load resistance $R_C$. Since the base-emitter voltage in this circuit is equal to the AC input signal, the expression for the voltage gain becomes

$$\frac{V_o}{V_{be}} = -g_m R_C = -\frac{I_{CQ} R_C}{V_{th}}.$$  \hspace{1cm} (5.16a)

The voltage gain depends on the DC voltage drop ($I_{CQ} R_C$) across the load resistor $R_C$. As observed during the load line analysis, a larger load resistor $R_C$ increases the small-signal voltage gain is, but also notice that what really matters is the product $I_{CQ} R_C$. At room temperature, the thermal voltage is around 26 mV. Hence, the previous equation can be rewritten as

$$\frac{V_o}{V_{be}} = -\frac{I_{CQ} R_C}{V_{th}} \approx -40 I_{CQ} R_C \quad @ \text{room temperature}.$$  \hspace{1cm} (5.16b)

This result will be routinely used in the following sections. On the other hand, it should be mentioned that the input impedance at the base terminal is $r_i = V_o/I_{BQ}$. The smaller the base current, the larger is the input impedance. In future analyses you will see that the input impedance has a more significant impact on the overall gain when the signal voltage source at the base has finite output impedance.

**V.4.3. Inclusion of the transistor’s collector-emitter resistance.** A non-ideal effect present in the BJT operation is the collector current modulation due to the collector-emitter voltage. The collector current increases for large collector-emitter voltages because more carriers are attracted to the collector due to the higher electric fields. If the base-emitter voltage is fixed while the collector-emitter voltage is swept, the transistor’s output characteristics in Figure 5.13 is obtained. This figure visualizes this sweep of $V_{CE}$ for four different $V_{BE}$ voltages, where the finite slopes above $V_{CE} > 0.3V$ are caused by the finite collector-emitter resistance $r_{ce}$. Extrapolating the current-voltage characteristics for negative collector-emitter voltages gives us the so-called Early voltage $V_{early}$, which is the point where they intersect the x-axis. The Early voltage has little sensitivity to the bias conditions, and it depends strongly on the specific process technology used to fabricate the BJTs. Typical Early voltages have magnitudes in the range of 50-100 V for standalone BJT devices. The slope of the $i_C-V_{CE}$ characteristics is defined as the transistor’s output conductance given by
Fig. 5.13. $i_C$-$V_{CE}$ characteristics of the BJT. The slope of the curves represents the transistor’s output conductance $g_o$.

The approximation in the previous equation is under the assumption that $V_{CEQ} \ll V_{\text{early}}$, which is a realistic assumption for discrete transistors but not necessarily for BJTs within integrated circuits. An improved model for AC signals is depicted in Figure 5.14a that takes the effect of the current modulation due to $V_{CE}$ into account. Here, the collector-emitter resistor ($r_{ce} = 1/g_o = V_{\text{early}}/I_{CQ}$) has been added. It will be evident in the following sections that this model is very useful for the analysis of common-emitter topologies wherein the emitter is connected to a DC voltage source or ground. However, for the analysis of some other topologies it is more convenient to use the T-model presented in Figure 5.14b.

**V.4.4. The T-model for BJTs.** The T-model in Figure 5.14b is based on the collector current representation in terms of the emitter current rather than in terms of the voltage $v_{be}$ that is generated from the base current in the π-model. If the transistor is now analyzed at the emitter, the current flowing through the emitter-base diode is the entire emitter current. Therefore the diode’s conductance seen from the emitter terminal is given by

$$g_e = \left. \frac{\partial i_E}{\partial V_{BE}} \right|_Q = \frac{I_{EQ}}{V_{th}}, \quad (5.18a)$$

and the emitter resistance is

$$r_e = \frac{V_{th}}{I_{EQ}} = \frac{V_{th}}{(1 + \beta)I_{BQ}} = \frac{r_\pi}{(1 + \beta)}. \quad (5.18b)$$

The collector current must be modeled as current-controlled current source in the T-model, which is $i_C = \alpha i_E$. Another condition that must be added to this model is the KCL condition $i_E = i_C + i_B$. By taking these equations into
account, the equivalent T-model shown in Figure 5.14b is fully explained. As in the \( \pi \)-hybrid model, the \( r_{ce} \) is also included between the collector and emitter terminals. Both models will be extensively used in the following sections. The models represent the same set of equations, and the final numerical results will be independent of the model used in the analysis. However, one of the models often allows easier algebraic analysis for a given circuit. When you investigate a new circuit with one model and experience difficulties to obtain solutions in the first attempt, it is usually helpful to restart the analysis with the other model. In general, the \( \pi \)-hybrid model is very popular, but for some topologies it is simpler to gain insights into the circuit’s performances by using the T-model to derive expressions.

### V.4.5. Practical transistor limitations.

The aforementioned models are valid if and only if the transistor is operating in the linear region. Some practical constraints of the transistor model are:

1. **Transistors operating with very small collector-emitter voltage** \((V_{CE} < 300 \text{ mV})\) will operate in the non-linear saturation region. If the base-emitter voltage is large enough \((V_{BE} \approx 0.5 \text{ – } 0.8 \text{ V})\) under this condition, then the input diode is on and huge base-emitter current can be generated. The collector current however is almost linearly related to \( V_{CE} \) since the electric field between the base and emitter terminals is not strong enough to attract the minority carriers that are traveling throughout the base. As a result, the collector current can be very small compared with the emitter current, and both the \( \alpha \) and \( \beta \) current gain factors reduce drastically when the transistor is operated in the saturation region. Since the transistor is quite inefficient if operated in this region, it is recommended to maintain \( V_{CE} > 300 \text{ mV} \) under all possible operating conditions when designing linear amplifiers.

2. **Although the exponential behavior of the collector current is valid over several decades** (in many cases from 0.1 \( \mu\text{A} \) until 10 mA), the collector current is limited due to non-ideal effects such as parasitic resistances embedded in the transistor, velocity saturation of the carriers, and other second-order effects. These effects reduce the amplification efficiency of the BJT at high current levels, limiting its current-gain factor especially in power amplifier applications. Figure 5.15 illustrates the typical evolution of the current-gain \( \beta \) as the collector current increases. In this figure, you can also observe the sensitivity of \( \beta \) to temperature changes.

![Fig. 5.15. Typical variations of \( \beta \) as a function of the collector current at different temperatures.](image)

3. **Since most AC parameters such as \( r_n \), \( g_m \), and \( \beta \) are quite sensitive to temperature variations**, it is critical in many practical applications to improve the design’s robustness to these variations as much as possible by minimizing the circuit’s sensitivity to temperature changes. The normalized sensitivity of a function \( H \) to variations of a parameter \( T \) is defined as

\[
S_T^H = \frac{T \frac{\partial H}{\partial T}}{H} \approx \frac{\Delta H}{\Delta T}. \tag{5.19}
\]

Here, function \( H \) could be the equation that describes a performance parameter such as the amplifier’s gain, and parameter \( T \) could be the temperature or another parameter such as \( \beta \) that changes due to manufacturing variations. When equation 5.19 is too complex to be evaluated analytically, then simulation programs can be used to find the
sensitivity by repeating simulations with incremental changes or wide-range sweeps of parameter $T$, while recording the corresponding values of the output parameter $H$ under investigation. The sensitivity function represents the ratio of the variations of both $H$ and $T$ with respect to the nominal value, i.e. it is normalized. Sensitivity of 1 means that the normalized variation of $T$ affects the normalized function $H$ in the same proportion. For instance, if a 10% temperature change from 25°C to 27.5°C generates a 10% increase of $\beta$ from 150 to 165, then we say that the normalized sensitivity is 1.

iv) Very large base-emitter voltages produce very large collector currents, which will cause the temperature of the BJT device to change as a result of self-heating. Additionally, drastic increases of the collector currents occur when voltages exceed the breakdown voltages in the junctions. For example, the breakdown voltage $V_{CEB}$ labeled in Figure 5.16 depends on the technology with which the BJT is fabricated, and its value can be found together with the specifications of the other breakdown voltages in the device datasheet provided by transistor’s manufacturer. As you can see in the figure, $V_{CEB}$ also has some dependence on $V_{BE}$, which is why it is good practice to list and pay attention to the operating conditions under which specifications are reported in the datasheet. In conclusion, it is strongly advisable not to reach the specified voltage and power breakdown limits.

v) Another practical constraint is that the BJT’s current-gain drops at high frequencies. This behavior is not observable when you analyze and simulate circuits based on the small-signal model that has been introduced in this section because this model does not include any capacitances. In reality, there are parasitic junction capacitances within the BJT device that form poles with the BJT’s internal resistances, causing current-gain roll-off at high frequencies. Figure 5.17 shows a simplified plot of $\beta$ vs. frequency in logarithmic scale. The current-gain for small-signal AC calculations can be approximated as $\beta_{AC}$, which is relatively flat over frequencies below a corner frequency $f_C$. When using the presented small-signal model, it is important to be aware of the assumption that the BJT is operating in this frequency range. Otherwise, your hand calculations will not agree well with actual measurement results or with simulation results based on transistor models that include parasitic capacitances. As the frequency is increased, there will be a point at which the BJT does not provide current amplification anymore. This frequency is called the transition frequency $f_T$, which is also sometimes referred to as unity-gain frequency since $\beta = 1$ at this frequency. Datasheets normally include the specifications of $f_T$ and $f_C$, or a plot similar to Figure 5.17. Depending on the fabrication technology, $f_T$ of BJTs could as low several megahertz and as high as tenths of gigahertz.
The transition frequency depends on parasitic capacitances within the BJT, but it is also proportional to the transconductance parameter $g_m$. Since $g_m$ can be increased by biasing the transistor with a larger collector current according to equation 5.12, you can improve the frequency response of BJTs by selecting the proper bias conditions. As shown in Figure 5.18, $f_T$ is low for small values of $I_{CQ}$, and it tends to increase with $I_{CQ}$ until the non-idealities explained in ii) begin to degrade $\beta$.

![Fig. 5.18. Transition frequency vs. collector current.](image)

V.5. Basic Amplifier Configurations and Equivalent Circuits.

V.5.1. Common-emitter amplifier with the loading effects.

The circuit shown in Figure 5.19a is known as common-emitter amplifier because the emitter is connected to a terminal that has a DC voltage, which is ground in this case. When the AC analysis is carried out as shown in Fig. 5.16b, where DC voltage sources are replaced by short circuits, the emitter terminal becomes an “AC ground” even if a DC voltage source is connected to it. The DC analysis of the circuit is also performed in the same manner as the previous example by replacing AC voltage sources with short circuits and AC current sources with open circuits. A new aspect related to this loaded common-emitter amplifier is that it has a coupling capacitor $C_C$ connected between the collector and load resistor $R_L$ at the output. Recalling that the impedance of the capacitor is $Z_C = 1/(j\omega C_C)$, we can deduce that it acts like an effective short circuit when the frequency $\omega$ is high, and like an open circuit at DC when $\omega$ equals zero. Thus, it isolates the DC voltage at the collector from the DC voltage at the output terminal which is zero here. Since $C_C$ “blocks DC components”, it is often called blocking capacitor in this kind of configuration between amplification stages. The fundamental equations to be solved for DC operating point analysis are:

\[
I_{CQ} = I_S e^{\frac{V_{BEQ}}{V_{th}}},
\]

and from writing the equation to relate $I_{CQ}$ and $V_{CEQ}$ from the circuit in Figure 5.19:

\[
V_{CC} = V_{CEQ} + I_{CQ} R_C,
\]

where $i_C$ was replaced by $I_{CQ}$ in this DC analysis. Termed static load line, this equation is a linear relationship between $I_{CEQ}$ and $V_{CEQ}$ that can be plotted on top of the transistor’s output characteristics as in Figure 5.20a. For a given $V_{BEQ}$, the plotted sets of equations dictate the operating point $Q (V_{BEQ}, I_{CQ}, V_{CEQ})$ of the amplifier.

To conduct AC analysis, the transistor must be replaced by a small-signal model while the DC voltage and current sources are set to zero. We are allowed to do so according to the superposition principle, which helps us to identify the AC response of the circuit. The small-signal model of the amplifier including the load resistor $R_L$ and the coupling capacitor $C_C$ is depicted in Figure 5.19b. This equivalent circuit can be solved using conventional circuit analysis methods. For instance, it can be shown that the output voltage is given by
The voltage transfer function in equation 5.22 has a zero at DC and a pole determined by the sum of the two resistors \((R_C + R_L)\) and the coupling capacitor \(C_C\). Thus, all low-frequency signals will be attenuated under the influence of the zero until the frequency of the pole. If you cannot visualize this transfer function, then you should refer to the descriptions of plotting methods in Chapter II. For frequencies above the pole frequency, the voltage gain can be approximated from equation 5.22 with \(s = j\omega = j\cdot\infty\), which results in

\[
\frac{v_o}{v_{be}} \approx \left(\frac{R_C R_L}{R_C + R_L}\right) g_m .
\]

(5.23a)

Notice that the equivalent load impedance is the parallel combination of \(R_C\) and \(R_L\). This intuitively makes sense at high frequencies because the capacitor has very small impedance and can be regarded as a short circuit if its impedance is significantly smaller than that of the series resistor \(R_L\). Clearly, \(R_L\) reduces the gain according to equation 5.23a. Many engineers call this phenomenon “loading effect”. The AC evaluation that has led to the result in equation 5.23a gives a good indication of the amplifier’s frequency response at low and medium frequencies. However, you should not forget that the gain will drop at very high frequencies due to the \(\beta\) degradation described in Section V.4.5. Considering that a reduction of the AC current-gain leads to a smaller AC collector current, the impact of low \(\beta\) at high frequencies can be observed by rearranging equation 5.23a to write the output voltage in terms of the collector current:

\[
v_o = -\left(\frac{R_C R_L}{R_C + R_L}\right) g_m v_{be} = -\left(\frac{R_C R_L}{R_C + R_L}\right) i_c .
\]

(5.23b)

The loading effect implications are evident in Figure 5.20b, where the slope of the static load line for DC analysis is -1\(R_C\), but the AC voltage gain is defined by the dynamic load line with a slope of -1\((R_C || R_L)\) according to equation 5.23b. The load resistance \(R_L\) reduces the voltage gain, which is why it is important to maximize this resistance when the goal is to achieve high gain. In case multiple amplifiers are cascaded, the resistance \(R_L\) is replaced by the input impedance of the following amplification stage. Therefore, each cascaded amplifier should be designed with high input impedance to avoid gain reductions from the loading effect on its previous stage. Notice in Figure 5.20 that the same AC base-emitter input voltage signal (shown on the right side of each plot) produces different output signal amplitudes depending on the loading conditions: The blue lines in Figure 5.20a cross the load line defined by 1\(R_C\), which maps into the large collector-emitter output voltage swing that is shown below the x-axis. In contrast, the red dynamic load line with the influence of \(R_L\) in Figure 5.20a crosses the blue lines at different points, which produces less collector-emitter output voltage swing.
V.5.2. Common-emitter amplifier with resistive biasing.

In the simplest common-emitter amplifier, the emitter terminal is connected to ground as depicted in Fig. 5.21. The DC base-emitter voltage is determined by the resistors $R_1$ and $R_2$, while the input signal is AC coupled through the DC blocking capacitor $C_B$. As a result, $v_B$ has two components: a DC voltage generated from the resistive divider connected to $V_{CC}$, and an AC signal due to $v_i$.

As previously, the superposition principle can be applied to any linear system. Hence, assuming that the transistor is operated in the vicinity of the Q point, the amplifier can be approximated as a quasi-linear device for which the DC and AC modes of operation can be analyzed independently. Notice that the output signal will be composed of both DC and AC components, but the analysis of the circuit can be split to consider each signal at a time.

First, let us analyze the effect of the DC signal based on the simplified diagram in Figure 5.22a, where $v_i = 0$. Since the impedances of the capacitors $C_B$ and $C_C$ are extremely high at DC and low frequencies, they isolate the DC biasing of this circuit from the rest of the system. This has the advantage that the DC bias circuitry can be designed independently from any previous or subsequent stages on an integrated circuit, as well as the DC voltage levels associated with any external sources or loads. For this reason, the use of blocking capacitors is particularly common in multi-stage amplifiers.
V.6. Transistor characterization and design approach.


Let us consider the design of an amplifier with a high-frequency gain requirement of 34 dB. The Q2N222 bipolar transistor will be used in this example because it is available as a part in most PSPICE simulator versions. Even though the model contains the small-signal parameters of the transistor, it might not always model the high-frequency current gain roll-off accurately. You can check whether the model in your simulator accounts for high-frequency effects by setting up a test circuit such as the one displayed in Figure 5.25. In this case, the BJT is biased with ideal sources having zero series resistance. Thus, when you perform an AC simulation over a wide frequency range (e.g., 0.1 Hz – 10GHz), then the change of the ratio of the AC collector current and the AC base current (i_C/i_B) will be solely due to transistor non-idealities if these are taken into account by the simulation model that you are using. If this ratio does not decrease at high frequencies, you should use f_T and f_C from the datasheet to determine up to which frequency range your simulation results are reliable based on the plot in Figure 5.17.

In general, some of the small-signal parameters of this transistor are: \( \beta_{AC} \approx 200 = \beta_{DC} \approx 200 \). These parameters correspond to the transistor 2N222 offered by Philips, whose parameters were obtained through LT-SPICE; the model used in PSPICE, however, shows \( \beta_{AC} \approx 170 \) and \( \beta_{DC} \approx 170 \) which correspond to the device offered by another vendor. These parameters can also be extracted from PSPICE simulations provided that you use the SPICE model provided by the vendor. For this example, let us assume they are both equal to 200 from previous characterization. Their typical ranges also vary among different manufacturers, but are usually listed in the datasheet. You can take these values as a reference, but should also perform your own transistor characterization as explained next.

DC transistor characterization. A simple transistor characterization setup with two voltage sources is shown in Figure 5.25. The input characteristic curve can be obtained by setting the collector-emitter voltage \( V_{CEQ} \) to a reasonable value such that the transistor operates in the linear region (\( V_{CE} > 0.3 \) V). In this example, \( V_{CEQ} \) is equal to 1 V. If the base-emitter DC voltage is swept from 0 up to 0.7 V or more, then the input characteristic curve in Figure 5.26 is obtained. The small-signal transconductance can be determined from this plot by finding the slope around the operating point, as marked in the figure. Please compare the value obtained from the plot and the one calculated with the previously introduced theoretical approximation: \( g_m \approx 40 \cdot I_{CQ} = 48 \) mA/V at \( I_{CQ} = 1.2 \) mA. During the design procedure of an amplifier, you will often have obtained a desired transconductance value from the analytical small-signal analysis and calculations. In such a situation, you can use the input characteristic plot to determine the collector current \( I_{CQ} \) and corresponding \( V_{BEQ} \) voltage required to bias the transistor so that it has this desired transconductance.
Fig. 5.25. Basic simulation setup for transistor characterization. Since $0.3 \, \text{V} < V_{CE} = 1\, \text{V}$ and $V_{BE} = 0.75\, \text{V}$, the transistor is biased in the linear region.

Fig. 5.26 Input characteristic curve for the selected BJT device: $I_C$ vs. $V_{BE}$, where $V_{CEQ} = 1\, \text{V}$ for this case.

The transistor’s output characteristic curve is obtained by setting the DC base-emitter voltage in the simulation setup such that the desired collector current is generated. Sweeping $V_{CE}$ while keeping $V_{BE}$ fixed will result in the output characteristic plot depicted in Figure 5.27. In this example case, the DC base-emitter voltage is fixed to 0.65 V, leading to a collector current around 1.2 mA. Recall that we have previously defined the boundary of the linear region with $V_{CE} > 0.3$ V, but also with $V_{CE} > 0.5$ V. This boundary depends on the type of BJT being used, and it also has a small dependence on $V_{BEQ}$. Nonetheless, you can see from the figure that the requirement of $V_{CE} > 0.3$ V for linear operation is more appropriate for the Q2N222 device.
The transistor’s output conductance $g_o$ can be obtained from the output characteristic plot by finding the slope of the curve when the device is operating in the linear region. For the example shown in Figure 5.28, $g_o$ is approximately $2 \times 10^{-5}$ A/V around the operating point defined by $I_{CQ} = 1.2$ mA and $V_{CEQ} = 2.5$ V. The corresponding output resistance is $r_{ce} = 1/g_o = 50$ kΩ.

The input impedance is obtained by plotting $I_B$ vs. $V_{BE}$ as shown in the simulation result displayed in Figure 5.29, which was generated with a DC sweep of $V_{BE}$ while maintaining $V_{CE}$ at 1 V. The transistor’s input resistance $r_i$ is equal to $V_{th}/I_{BQ}$. Since $r_i = 1/g_{os}$, the input resistance can be derived from the slope ($g_{os}$) of the $I_B$-$V_{BE}$ curve at the proper base-emitter voltage, which is 0.65 V in this example.
Other important parameters are the static current gain $\beta_{DC}$ and the small-signal current gain $\beta_{AC}$. The former parameter must be used for the computation of the DC-operating point, and it is defined as the ratio of $I_{CQ}$ to $I_{BQ}$. In the following simulation, $\beta_{DC}$ is approximately equal to 200, where $I_{BQ} = 30 \mu A$ is the value from the DC operating point information after a DC simulation. The dynamic small-signal current gain relates the AC collector current and the AC base current, therefore it has to be used whenever AC analysis is carried out. It can be extracted from a plot of $I_C$ vs. $I_B$ around the operating point. To do so, you can use the $V_{BE}$ DC sweep range in Figure 5.29, and afterward place $I_C$ on the y-axis and change the data on the x-axis from $V_{BE}$ to $I_B$. Using the resulting plot (Figure 5.30) to calculate $\beta_{AC} = \Delta I_C / \Delta I_B$ around the operating point with $I_{CQ} = 5 mA$ gives $\beta_{AC} = 200$ for this bias condition.
V.6.2. Example design procedure. A particular case of the previously discussed common-emitter amplifier is depicted in Figure 5.31, which is biased with a single resistor between the base terminal and the supply voltage. Let us use the topology in Figure 5.31 for the design on an amplifier with a required voltage gain of 54 (= 34.6 dB). In a first approximation, the voltage gain can be inferred from equation 5.31:

\[ |A_v| = g_m4R_C = I_{CQ} \cdot R_C / V_{th}, \]

which can be rearranged to:

\[ I_{CQ}R_C = 53.8 \cdot 26mV = 1.4V. \]

Based on this design constraint, the required output impedance is around 1KΩ if a collector current of 1.4 mA is chosen. Although the selection of the collector current is somewhat arbitrary in this example, the value of the load impedance is quite critical. It should be selected such that R_L is much larger than the input impedance of the following stage. In addition to the collector current’s impact on the gain (equation 5.32), it defines the base current together with the transistor’s value of α, and thereby it also affects the input resistance r_β. However, at this stage of the discussion we would like to focus the attention to the analysis of the DC bias conditions. With a collector current I_CQ of 1.4 mA and the assumption that β is around 200, the expected base current is I_BQ = I_CQ / β = 7μA. Assuming V_{BEQ} = 0.7 V in a first design iteration, the value of resistor R_1 connected at the transistor’s base can be calculated as: R_1 = (V_{supply} - 0.7V) / I_{BQ} = (5V - 0.7V) / (7\times10^{-6}) = 614 KΩ.

Let us simulate the circuit in PSPICE to assess the voltages and currents of the BJT that define its DC operating point with the above selection of resistance values. The results can be obtained from the output file available in PSPICE, from which you can make several important observations:

1. The values obtained from SPICE are
   
   | V(vbase):        | 0.664408 | voltage |
   | V(collector):    | 3.55373  | voltage |
   | Ic(Q1):          | 0.00144627 | device_current |
   | Ib(Q1):          | 7.06122e-006 | device_current |
   | Ie(Q1):          | 0.00145333 | device_current |

2. Therefore, the expected voltage gain (= I_{CQ}R_C/26mV) should be slightly greater (34.9 dB) than required.
3. The actual base-emitter voltage of 0.66 V is less than the 0.7 V that was assumed in our previous calculations. Accordingly, we have to re-calculate the value for R_1 that results in a better operating point.
4. Since the voltage across R_1 is larger than expected, the base current is larger than in the hand calculations. This is the reason for the higher collector current.

Before we recalculate the amplifier’s components, let us simulate the circuit to find out its AC response. The following results were obtained with the AC analysis option in PSPICE. The circuit has a low-frequency pole that it is defined by the capacitor C_1 and the parallel combination of R_1 and r_β according to the discussion in Section V.5.2. If this is not obvious to you by inspection, then it would be helpful for you to draw the AC equivalent circuit with a π-hybrid model for the transistor, from which you can see that r_β and R_1 of this circuit appear in parallel. The base resistance r_β of around 3.7 kΩ dominates the value of the input impedance because it is much smaller than R_1. Thus the location of the pole is around 1/r_βC_1 = 27 rad/sec (= 4.3 Hz), which is reasonably close to the pole (not visible in Fig. 5.32) in the simulated AC response. The simulated medium-band frequency gain is around 34.8 dB according to the plot in Figure 5.32. This result is not bad at all, since the ideal gain is 34.6 dB.
Let us find out the reasons for the gain discrepancy between the first analytical design iteration and the simulation results. Prior to the second design iteration, it is imperative that you check the transistor’s simulation parameters. In PSPICE schematic simulation program, this can be done by analyzing the OUTPUT FILE as follows: Click the analysis tab and select the option “Examine Output”. The output file that will be opened is important because it lists the AC and DC parameters that are used by the simulator based on the device model parameters. In the second design iteration, it is advisable to use the proper β<sub>DC</sub> and V<sub>BEQ</sub> from the first DC simulation. To find the value for R<sub>1</sub> in this design example, we take into account that the collector current is defined by the base-emitter current. Therefore, the priority is to adjust the base current using the proper values for bias resistor R<sub>1</sub>, V<sub>BE</sub>, and β<sub>DC</sub>. After repeating the DC simulation with a newly selected value for R<sub>1</sub>, the collector current and collector voltage are closer to the expected DC value (V<sub>CEQ_ideal</sub> = 3.6 V). It is expected that the small-signal gain is also closer to the design target. The circuit was re-simulated in PSPICE, and the frequency response from the AC simulation is plotted in Figure 5.34. The AC gain is 34.6 dB, which is closer to the 34 dB target value. This agreement is acceptable for most practical applications, but the above design steps could be repeated if necessary.
Fig. 5.32. Gain and Phase responses of the example amplifier for medium-band frequencies after the first design iteration.

Fig. 5.33. Second DC simulation of the common-emitter amplifier: the displayed voltages for the new operating point are closer to the desired values due to the new value of bias resistor $R_1$. 
V.6.3 General characterization procedure for SPICE simulators.

To design a good amplifier is not an easy task because it depends on many factors. Usually, there is not a universal solution, but a good engineer must be able to find an appropriate trade-off between performances and cost in terms of power, silicon area (or circuit board area), and required components. In most of the practical cases, the solution must be tailored to system specifications that reflect the priorities of customers and managers. Generally speaking, the design of amplifiers involves several fundamental steps:

i) **Understand the problem and obtain the specifications for your design.** Before you start your design, obtain the most important amplifier specification requirements: input impedance, output impedance, voltage/current/power gain. You also have to know or estimate the expected signal swing in various amplifier stages. This step is fundamental for the selection of components or the fabrication technology to be used because there are voltage range restrictions associated with these choices.

ii) **Characterization of transistors.** The component vendors provide the technical information about the devices, which is why you should familiarize yourself with the datasheets of all components that are under consideration for the design. It is also advisable to perform SPICE simulations in order to characterize the active devices using the proper models as discussed in Section V.6.1.

iii) **Choose proper components and devices.** This is an application-dependent selection. You must be sure that both passive and active devices operate properly for the given specifications such as maximum frequency of operation, power dissipation, supply voltages, expected signal swings, impedance matching, etc.

iv) **Identification of the correct operating points for the transistors in the circuit involves the most critical design decisions.** The amplifier’s overall gain, frequency response, and power dissipation are strongly affected by the operating point selection. For this reason, you should write the DC equations that relate the operating point parameters of the transistor(s), such as \(V_{BEQ}\) and \(I_{CQ}\), with the components of the auxiliary bias circuitry based on conventional circuit analysis. In addition, it helps to write down the corresponding equations for small-signal parameters such as \(r_e\) and \(g_m\) in order to take their dependence on the bias conditions into account. This approach has been briefly described in the previous examples, and it will be elaborated in the remainder of this chapter. During this design step, you should also ensure that the transistor operates properly when it is connected to its previous stage and its load or the following amplification stage. It happens very often that the standalone circuit works fine, but the performance of the circuit is degraded when it is
incorporated into a system because of finite impedances at its input and output terminals. Such interaction between blocks in a system can occur for both DC and AC characteristics.

v) **Perform first approximations (hand calculations) to pick initial component values.** At the beginning, we can make use of a very simple model for the active devices such as the one for the BJT that assumes $V_{BEQ} = 0.7$ V. The primary goal at this stage of the design is to perform an approximate analysis that gives insights into the trade-offs and basic requirements to achieve the main specification targets. Sometimes, you might decide to modify your amplifier configuration or change to a different circuit topology after this first assessment. To obtain expressions that relate the key component parameters to specification targets, you can write down the fundamental AC equations for the specific amplifier circuit:

a. Input impedance
b. Output impedance
c. Small-signal gain
d. Poles and zeros (if needed to determine the bandwidth)

vi) **Assess your first design in a SPICE simulator.** Since the simple models for the hand calculations only give rough approximations, we have to simulate the circuit and compare the results with the predictions from hand calculations. First, make sure to check the transistor parameters for the selected operating point to identify critical deviations, then verify all your AC specifications, and finally run transient simulations to check that none of the signals show any significant distortion. In case your simulations do not agree with your calculations, think about the following issues and reconsider your initial design choices:

a. Is the selected transistor suitable for your application or are the conditions forcing it to operate outside of the ranges specified in the datasheet? Begin by finding any DC operating point discrepancies, and take a look at related parameters such as $\beta$ and $V_{BEQ}$.

b. Are your assumptions reasonable? In particular, you should check the impedances of the previous stage (or signal source) as well as the load (or next stage). If the design includes DC blocking capacitors, then you should check that the values are large enough to allow the AC signal components to pass, which you can check by running AC simulations to obtain the frequency response from the input to the output.

c. Where is the main design issue? Often minor mistakes such as specifying a bias current source as 1 A instead of 1 mA can be the cause of the problems. You will also be surprised how often engineers forget to specify the supply voltage or the correct input signal. After troubleshooting to make sure that none of those mishaps are the root cause of the problem, you can begin to search for aspects of your design that might require major improvements. For example, did you leave sufficient voltage headroom in your DC calculations to allow the maximum output voltage swing without clipping the signal? Do the small-signal parameter calculations contain errors? Are your expressions in step v) correctly describing the AC characteristics of the circuit, or should they be revised? Does the collector-emitter resistance $r_{ce}$ reduce the gain by lowering the equivalent impedance at the output node? If $r_{ce}$ is not significantly larger than the load resistance, then it should be included in the second iteration of the hand calculations. Notice that $r_{ce}$ is listed as RO in the transistor operating point information provided in the previous subsection.

d. How can you overcome the main design drawbacks? Once the problems or deficiencies have been identified, the solution often involves redesign by selecting a better operating point. As mentioned before, your hand calculations in the second design iteration should include the transistor parameters listed in the operating point information after the first simulation. Normally, you have an improvement goal such as increasing the gain, which can be done by using a larger resistor at the collector output or by biasing the transistor with more collector current to boost the small-signal transconductance $g_m$. Those actions unfortunately have trade-offs. For example, both the aforementioned changes lead to a reduction in the voltage margin for signal swings at the collector terminal. Furthermore, increasing the collector current will lower the value of $r_{ce}$, which might become a problem after the change because it affects the equivalent output impedance at the collector node. You can raise your awareness of those trade-offs by referring to the equations that you wrote in your first hand calculations.
vii) Re-evaluate your specifications, assumptions, and circuit architecture. You should recalculate all amplifier components after changing one or several parameters. As you can see from the analysis in this chapter, the transistor parameters and bias circuit component values are typically interrelated in a way that one change mandates a completely new design iteration. Always start by checking the simulated $V_{BEQ}$ voltage of the transistor(s) and the current gains ($\beta$) for DC and AC analysis. Then, use the latest simulation values to recalculate new components.

viii) Check your final design through simulations. It is not uncommon that you need at least 2 iterations to come up with a reasonable solution. Your characterization should always cover the complete set of simulations. For instance, if you make a design change to increase the gain, it is not sufficient to run AC simulations and stop after determining that the gain meets your target. Instead, you should repeat all DC simulations and other AC simulations such as the input/output impedance assessments. An important final verification step is to run transient simulations to verify that the signal gain is achieved without clipping or other distortion.

**V.7. Common-Emitter Amplifier with Emitter Degeneration Resistors.**

A very general common-emitter configuration is displayed in Figure 5.35. The DC operating point is more robust when an additional resistance is added between the emitter terminal and ground. As will be evident in the following discussion, this resistance ($R_{E1} + R_{E2}$) makes the circuit less sensitive to temperature variations and it allows more control over the operation point. Without capacitor $C_E$, a drawback of this topology would be that the resistors $R_{E1}$ and $R_{E2}$ both decrease the small-signal voltage gain. To alleviate this issue, the large capacitor $C_E$ eliminates the effect of $R_{E2}$ on the AC voltage gain without affecting the DC operating point. Hence, $C_E$ enables more freedom to select a resistance ($R_{E1} + R_{E2}$) for DC operating point stabilization, while $R_{E1}$ becomes the emitter degeneration resistance at AC signal frequencies. In the future, you might encounter circuits in which the emitter degeneration resistance $R_{E1}$ is used to improve the linearity characteristics of the amplifier. As discussed later in this section, the AC input resistance of the amplifier is increased due to added emitter resistance.

![Fig. 5.35. General common-emitter amplifier configuration.](image)

**V.7.1. DC analysis.** The DC equivalent circuit of the general common-emitter amplifier is shown in Figure 5.36a. Using the same circuit analysis approach as used for the previous examples, the following set of equations can be written to relate the operating point parameters:

$$V_{BB} = \left( \frac{R_B}{R_{B1}} \right) V_{CC} = I_{BQ}R_B + 0.7V + I_{EQ}(R_{E1} + R_{E2}) = 0.7V + I_{CQ}\left( \frac{R_B}{\beta} + \frac{1}{\alpha}(R_{E1} + R_{E2}) \right), \quad (5.34a)$$

$$R_B = R_{B1} || R_{B2}, \quad (5.34b)$$

$$V_{CC} = V_{CEQ} + I_{CQ}R_C + I_{EQ}(R_{E1} + R_{E2}) = V_{CEQ} + I_{CQ}\left( R_C + \frac{R_{E1} + R_{E2}}{\alpha} \right). \quad (5.34c)$$
Fig. 5.36. Common-emitter amplifier with source degeneration: a) DC equivalent circuit, b) small-signal model for AC analysis. The resistance $R_S$ of the signal source is ignored in the AC analysis under the assumption that it is very small compared to the input impedance $z_b$.

V.7.2. AC analysis. The AC analysis of the topology is a bit more complicated due to the resistor $R_{E1}$ connected at the emitter of the transistor. It is easier to analyze the circuit with the T-model for the BJT, resulting in the small-signal circuit in Fig. 5.23b. For first approximate calculations, we ignore the effect of the collector-emitter resistance. To further simplify the analysis of this topology, we will consider the case with $R_S = 0$. Even though this approximation leads to reasonable results when $R_S \ll z_b$, it will be apparent at the end of this subsection that the effect of $R_S$ can be easily incorporated into the final equations.

To reveal one benefit of adding resistor $R_{E1}$, let us determine the input impedance of this topology. Looking into the base of the amplifier, this input impedance can be shown to be

$$z_b = \frac{v_i}{i_b} = \frac{v_i}{i_e/(1+\beta)} = \frac{(1+\beta)(r_e + R_{E1})}{r_e + (1+\beta)R_{E1}}. \quad (5.35)$$

A desirable effect of the resistor $R_{E1}$ is the term $(1+\beta)R_{E1}$ in the above expression. It allows the input impedance to be boosted by adding emitter degeneration resistance. If large input impedance is required, the resistors $R_{B1}$ and $R_{B2}$ must be increased as well because the impedance $(z_b = z_0||R_B)$ seen by the input voltage source $v_i$ is the parallel combination of $z_b$ and $R_B$. From the small-signal equivalent circuit, the amplifier’s voltage gain is derived based on the following equations:

$$v_o = -\alpha_i_e \left( R_C || R_L \right). \quad (5.36)$$

where:

$$i_e = \frac{v_i}{r_e + R_{E1}} = \frac{v_i}{\alpha + R_{E1}} = \frac{g_m}{\alpha + g_m R_{E1}} v_i. \quad (5.37)$$

Therefore, the overall voltage gain can be obtained as

$$A_V = \frac{v_o}{v_i} = \frac{\alpha g_m (R_C || R_L)}{\alpha + g_m R_{E1}}. \quad (5.38)$$

A drawback of the emitter degeneration resistor $R_{E1}$ is that the voltage gain is reduced due to the term $g_m R_{E1}$. There is a clear design trade-off whenever we add the emitter degeneration resistor: the larger the resistor $R_{E1}$ is, the larger becomes the input impedance according to equation 5.35, but the smaller is the voltage gain as can be seen in equation 5.38. This exchange is unavoidable in BJT based circuits, and the emitter resistance $R_{E1}$ must be judiciously selected to satisfy the input impedance constraint without excessive degradation of the voltage gain.
Another benefit of the emitter degeneration is that it reduces the circuit’s sensitivity to temperature variations. Remember that $\beta$, $g_m$, $r_n$, and $r_e$ are temperature-dependent parameters. At room temperature, the voltage gain can be approximated as follows:

$$A_V \approx \frac{40 \cdot I_{CQ} (R_C || R_L)}{1 + 40 \cdot I_{CQ} R_{E1}}, \quad \text{(5.39)}$$

where we assumed that $\alpha$ is very close to 1. If a robustness required, it is advisable to design the circuit such that $40 I_{CQ} R_{E1} >> 1$. In practice, $40 I_{CQ} R_{E1}$ is often designed to be between 4 and 10. In that case the above expression can be further reduced, leading to the following approximation:

$$A_V \approx -\frac{R_C || R_L}{R_{E1}}. \quad \text{(5.40)}$$

This result shows that if the emitter degeneration resistance is sufficiently high, the voltage gain is not very sensitive to temperature-dependent transistor parameters such as $r_n$, $r_e$ or $g_m$. The voltage gain mainly depends on the ratio of the load impedance $R_C || R_L$ and the emitter degeneration resistance $R_{E1}$. A design example based on this circuit is discussed in Section V.10.

**V.8. Common-Collector Amplifier.**

The common-collector amplifier is frequently used for coupling circuits with insufficient driving capabilities to heavy loads. Here, “driving capability” refers to an amplifier’s ability to provide enough current to the load in order to generate the output voltage swing that is expected for the specified gain. When using this terminology, a “heavy” load is a load that requires a relatively large output current, such as a small-valued resistor. On the other hand, a “light” load only draws a small amount of current at the amplifier output. As a side comment, be cautious when using technical jargon with such a relative nature because the classifications vary among engineers who work on circuits that are intended for diverse applications, which often require different transistor fabrication technologies. For example, a designer of an integrated circuit that drives the speaker of a portable MP3 player might consider 10mA as a heavy load, while an electrical engineer designing motor control circuitry with discrete components for a manufacturing plant could regard the same current as a light load. With that said, let us get back to the common-collector amplifier, which has a voltage gain less than but close to unity. However, its current gain is around $1+\beta$. Due to this property, the amplifier can be considered as a power amplifier because it preserves almost the same voltage swing while amplifying the current. Therefore, it is often used as a so-called “buffer” for driving low load impedances such as speakers, motors, etc. The schematic of such a common-collector amplifier is presented in Figure 5.37. As you can see, the collector is connected to the supply voltage $V_{CC}$ that becomes an AC ground in the small-signal analysis, which is why the configuration is often named “common-collector” amplifier. As mentioned above, the output voltage at the emitter closely follows the input voltage at the base. Due to this property, some engineers prefer to call the circuit an “emitter-follower”.

Fig. 5.37. Common-collector configuration, where the signal is injected at the base terminal and the output is at the emitter terminal.
To conduct the DC analysis, the AC input signal source is short-circuited and the capacitors are replaced by open circuits. The resulting circuit is shown in Figure 5.38a. Resistors $R_{B1}$ and $R_{B2}$ together with the effect of $V_{CC}$ can be modeled by an equivalent circuit as depicted in Figure 5.38b, in which the equivalent voltage $V_{BB}$ and resistance $R_B$ are:

$$V_{BB} = \left( \frac{R_{B2}}{R_{B1} + R_{B2}} \right) V_{CC} = \left( \frac{R_B}{R_{B1}} \right) V_{CC},$$

(5.41)

$$R_B = R_{B1} || R_{B1} = \frac{R_{B1}R_{B2}}{R_{B1} + R_{B2}}.$$  

(5.42)

At the input, the base and emitter currents are related by the expression

$$V_{BB} = R_B I_{BQ} + 0.7V + R_E I_{EQ} = 0.7V + \left( \frac{R_B}{\beta} + \left( \frac{1 + \beta}{\beta} \right) R_E \right) I_{CQ},$$

(5.43)

and the equation at the transistor’s output yields

$$V_{CC} = V_{CEQ} + R_E I_{EQ} = V_{CEQ} + \alpha R_E I_{CQ}.$$  

(5.44)

![Fig. 5.38. a) Common-collector equivalent circuit for DC analysis, and b) modified equivalent circuit.](image)

The AC equivalent circuit for the amplifier in Figure 5.37 is obtained by setting $V_{CC}$ equal to zero and replacing the transistor by its small-signal model. It is easier to find expressions for this common-collector configuration when the T-model is used as shown in Figure 5.39a. Here, $r_{ce}$ in the model is omitted for simplicity under the following assumption: $r_{ce} >> R_E || R_L$. Remember that the common-collector amplifier typically drives a low impedance load, which makes this a very safe assumption for many cases. Similar to the common-emitter configuration, the small-signal transfer function has two poles due to the coupling capacitors ($C_b, C_L$) and the resistors associated with them. In the medium frequency band, where the capacitors can be considered as short circuits, the equivalent circuit can be simplified as in Figure 5.39b.
Fig. 5.39. Small-signal diagram for the common-collector amplifier: a) valid model for low and medium frequencies, in which the AC coupling capacitors are included; b) small-signal model valid for medium frequencies only, where the poles introduced by the capacitors are ignored.

Based on the simplified small-signal model, the common-collector amplifier’s input impedance \( z_b \) is given by

\[
 z_b = \frac{v_b}{i_b} = \frac{v_b}{i_e} = \frac{v_b}{1 + \beta} = \left(1 + \beta\right) \left(\frac{v_b}{r_e + R_E || R_L}\right).
\]

Notice that the input impedance measured at the base of the transistor depends on the overall resistance seen at the emitter terminal. In this case, the impedance looking into the base terminal is equal to the multiplication of the term \( r_e + R_E || R_L \) with the emitter-base current gain \( 1 + \beta \). It is interesting to point out that equation 5.45a can be expressed as

\[
 z_b = r_e + (1 + \beta)(R_E || R_L),
\]

where the relationship \( r_e = r_e/(1+\beta) \) was substituted to rewrite the equation. The above impedance is an important property of BJTs with emitter resistances. From inspection of the \( \pi \)-hybrid BJT model with grounded emitter, the impedance looking into the base is only \( r_e \). But, the resistors attached at the emitter terminal increase the input impedance seen at the base terminal from \( r_e \) to a value of \( r_e + (1+\beta)(R_E || R_L) \). Now, the overall input impedance seen by the input voltage source \( v_i \) can be identified:

\[
 z_i = R_B || z_b = R_B || \left(\frac{r_e + (1 + \beta)(R_E || R_L)}{R_B}\right).
\]

Furthermore, the voltage \( v_b \) directly at the base is generated from the input voltage source and the voltage divider involving \( R_S \) and \( z_i \), for which the transfer function is

\[
 \frac{v_b}{v_i} = \frac{z_i}{R_S + z_i} = \frac{z_b || R_B}{R_S + z_b || R_B}.
\]

To avoid signal attenuation in the input stage, it is desirable to design the circuit such that \( R_S \ll z_i = z_b || R_B \). As aforementioned, the impedances connected at the emitter help us to this end. From Figure 5.39b, it can be noticed that the output voltage depends on \( v_b \) as follows:
By combining equations 5.46 and 5.47, the overall voltage gain can be obtained as

\[
\frac{v_o}{v_i} = \left( \frac{v_b}{v_i} \right) \left( \frac{v_o}{v_b} \right) = \frac{z_b \| R_B}{R_S + z_b \| R_B} \frac{R_E \| R_L}{r_c + R_E \| R_L}.
\]

(5.48)

Clearly, the amplifier’s voltage gain is less than unity because it is composed of the multiplication of two factors that we could call the input and output attenuation factors. The input voltage source impedance \( R_S \) reduces the overall transfer function, and its effect is minimized if the input impedance of the amplifier is much larger than \( R_S \). The overall attenuation of this common-collector amplifier is minimized if the conditions \( z_b \| R_B >> R_S \) and \( R_E \| R_L >> r_c \) are satisfied. While it is relatively easy to satisfy the former condition in most of the practical designs, this is not the case for the latter one since \( R_L \) could be very small. For instance, the \( R_L \) associated with many speakers is equal to 8 ohms. Consider a case where the emitter resistance \( r_c = V_b/I_{EQ} \) is also equal to 8 ohms, which implies that the emitter current is 3.25 mA. Under these conditions, equation 5.48 leads to an overall voltage gain of less than 0.5. Assuming that \( z_b \| R_B >> R_S \) and \( R_E >> R_L \), what emitter current is needed if a voltage gain of 0.9 is required? To meet this target, the emitter resistance \( r_c \) must be equal to 0.88 ohms, leading to an emitter current requirement of roughly 30 mA. What is the emitter current requirement if you have to drive a 4-ohm speaker with a voltage gain of 0.9?

The fundamental equations for the DC and AC analyses of the common-collector structure have been discussed above. It is left to you to demonstrate that the small-signal current gain of the common-collector topology is close to \( \beta_{AC} \) if the amplifier is properly designed. Hence, its power gain is close to \( \beta_{AC} \) as well.


Contrary to the previous topologies, the input signal in the common-base configuration is injected into the emitter while the output is at the collector terminal, as shown in Figure 5.40. The base terminal is AC-grounded through a large capacitor \( C_B \) connected between the transistor’s base and ground. Since the blocking capacitor provides DC isolation so that the bias resistors \( R_{B1} \) and \( R_{B2} \) determine the base current, the control over the DC base current is maintained. The other DC blocking capacitors \( C_I \) and \( C_L \) are used to make the biasing of this amplifier stage independent of the previous and subsequent stages. As described before, these capacitors introduce pole-zero pairs, and their values should be increased as much as possible to push the poles to very low frequencies.

The DC analysis of the common-base amplifier is similar to the analysis of previous circuits. By going through the same first steps of the DC analysis described in the previous subsections, the modified equivalent circuit depicted in Figure 5.41a can be obtained, where the equivalent base voltage \( V_{BB} \) and base resistor \( R_B \) are given by
\[ V_{BB} = \left( \frac{R_B}{R_{B1}} \right) V_{CC} = \left( \frac{R_B}{R_{B1}} \right) V_{CC}, \quad (5.49) \]

\[ R_B = R_{B1} || R_{B1} = \frac{R_{B1} R_B}{R_{B1} + R_B}. \quad (5.50) \]

The base and emitter currents are related by the following expression:

\[ V_{BB} = R_B I_{BQ} + 0.7V + R_E I_{EQ} = 0.7V + \left( \frac{R_B}{\beta} + \left( \frac{1 + \beta}{\beta} \right) R_E \right) I_{CQ}. \quad (5.51) \]

Application of Kirchhoff’s voltage law to the output section of the circuit produces:

\[ V_{CC} = V_{CEQ} + R_C I_{CQ} + R_E I_{EQ} = V_{CEQ} + (R_C + \alpha R_E) I_{CQ}. \quad (5.52) \]

5.41. Common-base configuration: a) DC equivalent circuit, b) small-signal equivalent circuit for AC analysis.

The small-signal AC analysis can be carried out by using the \( \pi \)-hybrid or the T-model. Since the input signal is applied to the emitter terminal, it is easier to visualize the circuit’s properties with the T-model. Assuming large DC blocking capacitors are selected so that the poles generated by \( C_B \), \( C_t \), and \( C_L \) are located at very low frequencies, the effect of these poles can be ignored during the AC analysis for medium band frequencies. With this condition, the small-signal equivalent depicted in Figure 5.41b is appropriate to derive the basic equations. If your hand calculations disagree with your first simulation results, then you should take a look at the collector-emitter resistance \( r_{ce} \) in the simulated operating point information of the BJT. For simplicity and more insightful equations, the expressions below are derived under the stipulation that \( r_{ce} \) is relatively large. If the value of \( r_{ce} \) is only in the same order of magnitude as the other resistors in the AC equivalent circuit, then it is advisable to repeat the analysis without removing \( r_{ce} \) in the T-model. Let us begin the simplified analysis without \( r_{ce} \) by assessing the AC input impedance. Since the base terminal is AC-grounded, it can be seen by inspection that the input impedance is

\[ z_i = \frac{v_i}{i_i} = r_e || R_E = \frac{r_e R_E}{r_e + R_E} = \frac{r_e}{1 + (r_e / R_E)}. \quad (5.53a) \]

If \( R_E \) is selected such that \( R_E >> r_e \), then the input impedance is dominated by the emitter resistance \( r_e \). Under this condition and recalling that \( r_e = V_{th}/I_{EQ} = \alpha V_{th}/I_{CQ} = \alpha g_m \), the following important approximation can be made:
\[ z_i \cong r_e = \frac{\alpha}{g_m} = \frac{aV_{th}}{I_{CQ}} , \quad \text{if} \quad \frac{r_e}{R_E} = \frac{\alpha}{g_m R_E} = \frac{aV_{th}}{I_{CQ} R_E} \ll 1. \quad (5.53b) \]

At room temperature, this result yields
\[ z_i \cong r_e = \frac{\alpha}{40 \cdot I_{CQ}} , \quad \text{if} \quad \frac{\alpha}{40 \cdot I_{CQ} R_E} \ll 1. \quad (5.53c) \]

Therefore, the input impedance of the common-base configuration can be reduced by increasing the DC collector current. This is a very important property of the common-base configuration, and it is often exploited in transimpedance amplifiers where the input signal is in form of a current and the output signal is in form of a voltage. For instance, light-sensing photodiodes in optical communication systems convert the photonic energy into AC current that must be converted into a voltage signal for further processing. As visualized in Figure 5.42, the sensor injects current into the electrical circuit, and the most basic model for it is comprised of a current source with a finite frequency-dependent impedance \( Z_p(f) \). Since \( V_{CC} \) is grounded in the small-signal equivalent circuit, \( Z_p(f) \) is effectively connected in parallel with the photodiode \( D_p \) that constitutes the signal current source. Based on the current division principle, you can deduce that the ideal interface stage to the sensor has a very low input impedance to ensure that most of the injected current flows into it rather than into the impedance \( Z_p(f) \). Common-base amplifiers are well suited as transimpedance amplifiers for such applications because they can present a low impedance at the interface to the photodiode, which improves the overall efficiency of the sensor circuit by minimizing the lost current \( i_{loss} \).

![Fig. 5.42. A transimpedance amplifier with low input impedance processes the output current of a photodiode.](image-url)

Now, let us continue with the AC analysis of the equivalent circuit in Figure 5.41 for the common-base amplifier. Since the base terminal is AC-grounded, the emitter current is fully determined by the transistor’s emitter resistance and the fraction of the input voltage that appears directly at the emitter terminal: \( i_e = -v_e/r_e \). Consequently, the collector current is also proportional to the emitter voltage, leading to the following transfer function:
\[ \frac{v_o}{v_e} = \left( \frac{-i_c}{v_e} \right) \left( R_c \parallel R_L \right) = \left( \frac{-\alpha i_e}{v_e} \right) \left( R_c \parallel R_L \right) = \alpha \frac{R_c \parallel R_L}{r_e} , \quad (5.54a) \]

where the substitutions \( i_c = \alpha i_e \) and \( r_e = -v_e/i_e \) based on Figure 5.41b were made in the equalities. The emitter resistance depends on the DC emitter current and the thermal voltage, hence equation 5.54a can be simplified as
\[ \frac{v_o}{v_e} = \left( R_c \parallel R_L \right) \frac{I_{CQ}}{V_{th}} = \left( R_c \parallel R_L \right) \left( g_m \right) . \quad (5.54b) \]
Notice that this equation is similar to that of the common-emitter transistor, but the common-base configuration does not invert the signal since the equation does not contain a negative sign. The main difference of the two structures is the input impedance. Usually, the input impedance of the common-emitter configuration is high, especially if an additional resistor is added to the emitter terminal. In contrast, the common-base configuration has a very small input impedance.

To calculate the overall voltage gain of the common-base amplifier, the resistances connected to the emitter must be taken into account because they impact the attenuation of the input signal from the source. This input attenuation factor can be added to equation 5.54a by applying the voltage division principle to the equivalent circuit in Figure 5.41b, which gives an overall voltage gain of

\[
\frac{v_o}{v_i} = \left(\frac{z_i}{R_s + z_i}\right) \frac{R_c \| R_L}{r_e}, \quad \text{where} \quad z_i = r_e \| R_E. \tag{5.55}
\]

The above expression for the voltage gain reveals that increasing \(R_C\) and \(R_L\) improves the gain. Furthermore, the combination of a low source resistance and high input impedance will maximize the achievable gain of the common-base amplifier when it is processing the input signal in voltage mode. However, optimization of \(z_i\) is an intricate design issue because \(r_e\) must be increased to raise \(z_i\), which in turn will reduce the second factor in equation 5.55. During the design process, you can use the numerical results from the above equations to determine the optimum trade-off for the selection of parameters under the given conditions, i.e., under the constraints by specified values such as \(R_L\), \(R_s\), or the required gain. Notice, the collector-emitter resistance \(r_{ce}\) has been neglected in the analysis. How do you expect it to affect the gain? If your intuition tells you that a low \(r_{ce}\) value will decrease the gain, then you are on the right track. Still, you should verify this assumption by deriving the equation for the gain while including \(r_{ce}\) in the T-model.

To get more insights into the common-base amplifier’s practical usefulness to process current-mode input signals, let us reconsider the application in Figure 5.42 and suppose that the common-base configuration in Figure 5.41 is used as transimpedance amplifier. The simplified small-signal equivalent diagram for this situation is displayed in Figure 5.43. The equation for the output voltage in terms of the emitter current is

\[
v_o = -i_e \cdot (R_C \| R_L) = -\alpha i_e \cdot (R_C \| R_L). \tag{5.56}
\]

Using the current division principle at the input of the amplifier, the emitter current can be expressed as

\[
i_e = -i_p \cdot \left(\frac{R_c \| Z_p}{r_e + R_c \| Z_p}\right), \tag{5.57}
\]

where the frequency-dependent impedance \(Z_p(f)\) was replaced with a fixed impedance magnitude \((Z_p = |Z_p(f_p)|)\) at the specific input signal frequency \(f_p\) of the current \(i_p\). Combining equations 5.56 and 5.57 to obtain the transimpedance gain results in:

\[
\frac{v_o}{i_p} = \alpha \cdot (R_C \| R_L) \cdot \left(\frac{R_c \| Z_p}{r_e + R_c \| Z_p}\right). \tag{5.58}
\]

From the above expression, it is evident that the condition \(r_e << R_{E\|Z_p}\) is optimal for high transimpedance gain because it implies that \(i_e \approx -i_p\). When \(R_E\) is selected appropriately in the design to ensure that \(R_{E\|Z_p} \gg r_e\), then \(i_{loss}\) can be reduced by increasing the collector current \(I_{CQ}\) according to equation 5.53b. This benefit of the common-base amplifier is clearly demonstrated by the simple analysis. Nevertheless, you will encounter limitations during the design for high transimpedance gain, which ideally requires you to increase the resistance values of \(R_C\), \(R_L\), and \(R_E\) while increasing \(I_{CQ}\) in order to reduce \(r_e\). These design objectives will create voltage headroom constraints because they will lead to decreased \(V_{CEO}\) in Figure 5.41a, which will reduce the maximum output voltage signal swing that is permissible while guaranteeing that the BJT remains in the active region of operation.
V.10. Design Considerations for BJT-Based Amplifiers: Graphical methodology.

V.10.1. Design of a high gain amplifier using a common-emitter structure with limited input impedance: A graphical approach. A major concern of the analog circuit designer is to determine the appropriate transistor device parameters and circuit component values to meet a set of given specifications. This part of the design is often obscure, which is the reason why new designers sometimes think that analog design is a kind of black art. In fact, selecting proper operating points for transistors is not a trivial task because many parameters and constraints are involved. However, the simple graphical design approach discussed in this section can help us to understand the main trade-offs so that reasonable solutions can be found. A couple of design examples will be used to introduce this approach and its usefulness to you.

The first example deals with the use of the basic common-emitter configuration shown in Figure 5.44a for the design of an amplifier with a voltage gain of -20 V/V that has to drive a load impedance of 10 kΩ. The limitations due to signal swing must also be incorporated as design constraints. Usually, those conditions impose some boundary conditions to the possible solution. In additions to the equations listed in Table 5.1, the following design constraints are applicable to this design:

i) Expected maximum amplitude \( V_{\text{omax}} \) of the output signal (often called the “maximum output swing”)
ii) Required voltage gain $A_V$

iii) Input and load impedance requirements

iv) Restricted supply voltage $V_{CC}$

---

Fig. 5.44. Basic common-emitter amplifier: a) circuit schematic; b) Conceptual schematic showing the DC and AC components at base and emitter.

Although the input impedance is not considered in this case, it will be incorporated into the design equations in the next subsection. The following equations define the operating point of the amplifier based on the DC analysis at its output. As described in previous subsections and according to Table 5.1, the DC equation involving the collector-emitter voltage is:

$$V_{CC} = V_{CEQ} + I_{CQ} R_C.$$  \tag{5.59}$$

It is very important to consider that the DC collector-emitter voltage $V_{CEQ}$ must be large enough to tolerate the maximum voltage swing of the AC signal. This constraint is visualized in Figure 5.44b. The condition to ensure that the transistor operates in the linear region can be expressed as $V_{CEmin} = V_{CEQ} - V_{opk} > \sim 300 \, \text{mV}$. To leave room for potential temperature variations and component tolerances, let us design for a minimum collector-emitter voltage of $V_{CEmin} = 500 \, \text{mV}$. With this safety margin, the $V_{CEQ}$ voltage must be chosen such that the collector-emitter voltage is greater or equal than 500 mV for the most negative signal swing at the amplifier output. This condition can be substituted into equation 5.59 to obtain the following design constraint:

$$I_{CQ} < \frac{V_{CC} - V_{CEmin}}{R_C} = \frac{V_{CC} - V_{opk} - 0.5V}{R_C}. \tag{5.60}$$

On the other hand, $V_{CE}$ should not be too close to $V_{CC}$ in order to provide room for the positive signal swing. Otherwise, the signal would be clipped when it reaches the supply voltage level. The DC voltage drop ($I_{CQ} R_C$ in Figure 5.44b) across the resistor $R_C$ at the collector must be greater than $V_{opk}$, leading to the following restriction for the collector current:

$$I_{CQ} > \frac{V_{opk}}{R_C}. \tag{5.61}$$

Another important design parameter is the small-signal voltage gain from the transistor’s base to the amplifier output. From our previous analysis, this voltage gain is given by
\[ |A_v| = \left| \frac{v_o}{v_{be}} \right| = g_m(R_C\|R_L) = \frac{I_{CQ}(R_C\|R_L)}{V_{th}}. \] (5.62a)

which can be rearranged to:

\[ I_{CQ} = \left( \frac{|A_v| \cdot V_{th}}{R_C + R_L} \right) \left( \frac{R_C}{R_C - R_L} \right). \] (5.62b)

These equations can be plotted in the I_c-R_C plane as shown in Figure 5.45. Equations 5.60 and 5.61 represent the boundaries for the acceptable solutions, and the combination of I_c and R_C for the selected operating point must fall within these two boundaries to allow sufficient signal swing (V_{omax}) at the output under a given supply voltage limitation (V_{CC}). Equation 5.62b gives the solutions for the amplifier’s voltage gain. These plots depend on the required voltage gain A_v and the load impedance R_L in addition to I_c and R_C. In Figure 5.45, equation 5.62b is plotted for four different amplifier gains (A_v = -10, -20, -40, and -100). Notice that the boundaries (equations 5.60 and 5.61) are independent of the desired voltage gain. However, they do depend on the maximum voltage swing expected at the amplifier’s output. When only the input signal swing is specified (fixed), then you should take into account that the maximum output voltage swing and the boundaries will vary as you plot equation 5.62b for different voltage gains.

The results shown in Figure 5.45 are generated with V_{CC} = 5V, V_{omax} = 1V, V_{th} = 26 mV, R_L = 10k\Omega. Notice in this plot that the acceptable region is more limited for large voltage gains. For example, the solution of equation 5.49b with A_v = -100 does not intersect the acceptable region. Hence, we cannot design the amplifier with a voltage gain of -100 for the given supply voltage and the desired output voltage swing. For the case of A_v = -20, we can achieve the specifications by satisfying all design constraints if and only if the collector resistance is in the range of 9.5k\Omega to 58 k\Omega while the quiescent collector current is in the range of 60\muA-100\muA. Another advantage of using this graphical approach is that the power consumption can be easily optimized by selecting the largest possible collector resistor R_C. For practical applications, however, it is always good practice to design the amplifier with some margin in order to accommodate both temperature variations and tolerances of the devices and components. This can be done by selecting a combination of I_c and R_C values on the desired voltage gain-dependent curve (equation 5.62b) that falls closer to the middle of the two boundaries (equations 5.60 and 5.61).

Once the output stage of the circuit is defined and the collector current is determined, the base current can be calculated. The values of the resistors attached to the base terminal can be computed based on the needed base current and the input impedance requirement. There are two basic equations (see Table 5.1, common-emitter
configuration with \( R_{E1} = R_{E2} = 0 \) and two unknown variables. Thus, we do not have any freedom for optimization when solving these equations, which are repeated here for convenience. From the DC analysis, we have

\[
\left( \frac{R_B}{R_1} \right) V_{CC} = I_B R_B + 0.7V , \tag{5.63}
\]

and the amplifier’s input impedance from the AC analysis is given by

\[
Z_{in} = r_\pi \| R_B = \frac{r_\pi R_B}{r_\pi + R_B} = \frac{r_\pi}{1 + \frac{r_\pi}{R_B}} . \tag{5.64}
\]

If \( R_B \gg r_\pi \), the effect of the bias network on the input impedance becomes negligible so that the input impedance is dominated by the transistor’s base-emitter resistance \( r_\pi \). For many applications it is common practice to increase the input impedance as much as possible. Thus, selecting a high-beta transistor helps because a high \( \beta \) value reduces the base current for a given collector current requirement, which increases the input impedance of the amplifier \( (r_\pi = V_{BEQ}/I_B) \). Nevertheless, most high-\( \beta \) BJTs cannot tolerate large currents and are therefore used as high-gain preamplifiers to avoid damage. Such a high-gain amplifier can then be connected to a low-gain buffer stage that can provide larger current to the load device. Typically, the transistors used as power amplifiers have limited \( \beta \) values, which could be well below 50. From the above discussion, the following important interrelation is evident: By selecting the smallest possible collector current, the required base current can be minimized, which will increase the input impedance and reduce the power consumption at the same time.

V.10.2. Design examples.

**Example 1.** To design the amplifier in Figure 5.44 with a gain of -20 V/V and \( V_{omax} = 1 \ V_{pk} \), we select \( I_C = 80 \ \mu A \) and \( R_C = 11 \ k\Omega \) based on the plots in Figure 5.45. For this collector current, the beta of the 2N2222 transistor is close to 200, and therefore the DC base current is around 0.4 \( \mu A \). The base-emitter resistance \( r_\pi \) is around 49 k\( \Omega \). Therefore, \( R_B \) can be selected should be at least 300 k\( \Omega \) to maintain an overall input impedance around 40 k\( \Omega \). Let us use \( R_B = 400 \ k\Omega \) for this example, then \( V_B = V_{BEQ} + I_B R_B = 0.6V + 0.6 \ \mu A \cdot 0.81 \ V \). In this hand calculation, the estimate \( V_{BEQ} = 0.6V \) was used rather than \( V_{BEQ} = 0.7V \) because the base current is very small. Anyway, the actual base-emitter voltage and other operating point parameters should be obtained with SPICE simulations, and the resistors should be adjusted accordingly in order to meet the collector current requirement. With some basic algebra, the value of the resistors connected to the base terminal can be determined from the chosen value of \( R_B = R_{B1} || R_{B2} \). In this example, \( R_{B1} \) could be picked as 2.2 M\( \Omega \), and \( R_{B2} \) calculated correspondingly as 490k\( \Omega \) to achieve the desired DC bias point and input impedance. When you are planning to build a circuit in the lab, be aware that your choice of resistor values will be restricted to those that you can find in the lists of standard component values. Figure 5.46 shows the voltage waveform at the transistor’s collector from a SPICE simulation of the amplifier with the selected component values with a 5 mV\( pk \) input signal swing.
The simulated voltage gain is 15% larger than expected. Analyzing the PSPICE output file, we discovered that the $\beta_{DC}$ is 15% higher than the value used in the hand calculations. As a result, the DC collector current is also 15% larger, which is evident in Fig. 5.46, where the DC voltage component (average of the transient waveform) is around 3.7 V instead of the expected 4.1 V ($= V_{CC} - R_{C}I_{C}$). If needed, the base current and resistors at base can be recalculated using the $\beta$ obtained from the SPICE output file.

Although large voltage gain can be obtained with this amplifier design, the input signal must be limited to 10 mV. Otherwise, the small-signal approximations are no longer valid. There are two main limitations with this amplifier topology. First, the input signal appears directly across the base-emitter terminals, limiting the allowed amplitude of the input signals for linear operation. Second, the input impedance is determined by the base-emitter resistance, which is not very high. To demonstrate the linearity performance limit, a 20 mV sinusoidal input signal was applied to the same circuit, for which the relevant SPICE simulation results are shown in Figures 5.47 and 5.48. Notice that the transient output waveform deviates from an ideal sinusoid. A Fourier analysis of this waveform can be carried out with the option in PSPICE that is available after running the transient simulation. The result in Figure 5.48 reveals that the fundamental signal component at 10 KHz has an amplitude of roughly 500 mV, while the second harmonic component at 20 KHz is 80 mV. The second-order harmonic distortion of roughly 16% is too much for most practical applications. Equation 5.10a predicts $HD_2 \approx 20\%$, which is relatively close to the simulation results. The smaller third-order harmonic component of 10 mV at 30 KHz can also be seen in the figure, leading to $HD_3 = 2\%$ in agreement with the expected 2.5% based on equation 5.10b.
Example 2. Design of a common-emitter amplifier with larger input impedance but limited voltage gain. In many situations, the amplifier’s input impedance is also an important design parameter. The AC input impedance can be increased by adding an emitter resistance as shown in Fig. 5.49. The DC and AC equations for this scenario are given in Table 5.1, where $R_{E1} = R_E$ and $R_{E2} = 0$. 

---

Fig. 5.47. Transient output waveform for an input signal of 20 mVpk.

Fig. 5.48. Frequency spectrum with the fundamental as well as second-order and third-order harmonic distortion components of the output voltage waveform shown in Fig. 5.47.
In the subsequent analysis it will be assumed that $R_B >> \beta R_E >> r_n$. Hence, the expression for the input impedance of this topology can be simplified with this approximation:

$$Z_i = (r_e + R_E)(1 + \beta) R_B \cong (1 + \beta) \left\{ \alpha \frac{V_{th}}{I_{CQ}} + R_E \right\}. \quad (5.65a)$$

or

$$R_E = \left( \frac{Z_i}{1 + \beta} - \frac{\alpha}{I_{CQ}} \right). \quad (5.65b)$$

With a high $R_B$ value, the overall input impedance only increases slightly. In addition to 5.65b, the set of equations that describe this amplifier’s DC and AC operation are revisited and rearranged below to acquire more design insights.

$$I_{CQ} = \frac{V_{CC} - V_{CE\min}}{R_c + \frac{R_E}{\alpha}} \leq \frac{V_{CC} - V_{cpk} - V_{epk} - 0.5V}{R_c + \frac{R_E}{\alpha}} \cong \frac{V_{CC} - V_{cpk} \left( 1 + \frac{1}{A_v} \right) - 0.5V}{R_c + \frac{Z_i}{\beta}}; \quad (5.66)$$

where substitutions with equation 5.65 and $\alpha = 1$ were made; it is also assumed that the voltage swing at the emitter is equal to the swing of the collector divided by the amplifier’s gain. As before, the condition $V_{CE\min} > V_{cpk} + 0.5V$ guarantees that the BJT stays in linear region with maximum signal swing. To avoid signal clipping for positive output swing, the collector voltage has to be properly selected. Since the circuit must be able to handle output voltage variations of at least $V_{omax}$, the following condition applies as well:

$$I_{CQ} > \frac{V_{cpk}}{R_c}. \quad (5.67)$$

From the small-signal analysis of the circuit, the amplifier’s voltage gain can be expressed as

$$\left| \frac{v_o}{v_i} \right| = \alpha \frac{R_c \parallel R_L}{r_e + R_E} = \frac{I_{CQ} \left( R_c \parallel R_L \right)}{V_{th} \left( 1 + \frac{I_{CQ}}{r_e + R_E} \right)}. \quad (5.68)$$

Notice that the resistor attached to the emitter reduces the overall voltage gain. The amount of gain reduction depends on the ratio of the voltage drop ($I_{CQ} R_E$) across $R_E$ and the thermal voltage $V_{th}$. The above expression does not include resistance $R_S$ of the input voltage source, but this can be easily incorporated by accounting for the voltage division associated with $Z_i$ and $R_S$; the analysis yields
\[ \frac{v_o}{v_i} = \frac{v_o}{v_b} \frac{v_b}{v_i} = \left( \frac{Z_i}{Z_i + R_S} \right) \left( \frac{R_C}{R_L} \frac{R_L}{r_e + R_E} \right) \approx \frac{R_C}{r_e + R_E + \frac{R_S}{1 + \beta}} \]  

Equation (5.69)

This equation is very helpful for the selection of \( I_{CQ} \) because it is a function of the specified AC voltage gain, load impedances \( R_C \) and \( R_L \), and the input impedance requirement. Eqn 5.69 is function of \( R_C \) and \( R_E \). \( R_S \) could be computed from 5.65 if the input impedance is provided. The input impedance specification is usually given in form of a bound; e.g. \( Z_i > a \) given value. Thus, an infinite number of solutions might be possible for 5.69. It is better practice to use this degree of freedom to guarantee the linear operation of the amplifier. Linear operation requires limiting the base-emitter voltage under a value that maintains the harmonic distortion components under the specifications. Detailed equations for the 2nd and 3rd harmonic distortions are given in the appendix; see also eqn 5.10. It is enough for his example to analyze the non-linear exponential term in equation A5.1. The non-linearity arises from the fact that the small signal drain current is generated according to the expression

\[ e^{v_{be}} = 1 + \frac{v_{be}}{V_{th}} + \frac{1}{2} \left( \frac{v_{be}}{V_{th}} \right)^2 + \frac{1}{6} \left( \frac{v_{be}}{V_{th}} \right)^3 + \ldots \]  

Equation (5.70)

Where the most relevant harmonic distortion is lumped to the quadratic term; in advanced applications, the design is usually fully differential then the second harmonic distortion becomes irrelevant, then the 3rd harmonic component is the most relevant one. The second harmonic distortion is small (\(<1/16\)) if we limit the base-emitter voltage to \( \left| \frac{v_{be-pk}}{V_{th}} \right| < 1/4 \); e.g. peak value of the base-emitter voltage should be limited to 6mVpk. To guarantee this condition, the relationship between base-emitter and input voltage can be found as follows

\[ \left| \frac{v_{be-pk}}{v_{i-pk}} \right| = \left( \frac{Z_i}{Z_i + R_S} \right) \left( \frac{r_e}{r_e + R_E} \right) = \frac{r_e}{r_e + R_E + \frac{R_S}{1 + \beta}} \]  

Equation (5.71)

Then, from 5.69 and 5.71, the voltage gain becomes

\[ \left| \frac{v_{o-pk}}{v_{i-pk}} \right| \approx \frac{R_C}{r_e} \left( \frac{R_L}{v_{th}} \right) \left| \frac{v_{be-pk}}{v_{i-pk}} \right| = I_{CQ} \left( \frac{R_L}{v_{be-pk}} \right) \]  

Equation (5.72a)

This equation can be more practical if expressed in the following format:

\[ I_{CQ} \approx \frac{V_{th}}{R_C} \left( \frac{v_{i-pk}}{v_{be-pk}} \right) |A_v|. \]  

Equation (5.72b)

Thus, designing a low-distortion amplifier requires to know-a-priori the peak value of the input signal. It is highly desirable to limit the swing of the base-emitter signal to be under 6mVpk to maintain good linearity.

To complete the design procedure, Eqs 5.65 and 5.71 can be combined in a simplified result that relates the collector current and the input impedance requirement, leading to

\[ I_{CQ} \approx \frac{\beta V_{th}}{Z_i} \left( \frac{v_{i-pk}}{v_{be-pk}} \right) - 1 \]  

Equation (5.73)

Equations 5.66-5.72b and 5.73 can be plotted in the \( I_C-R_C \) plane as in Figure 5.50. To generate these plots, the following parameters and design constraints were used: \( \beta = 200 \), \( Z_i \) (equation 5.65) \( \approx 150 \, k\Omega \), \( R_L = 10 \, k\Omega \), \( V_{omax} = 1 \) Vpk, and \( V_{CC} = 5V \). In Figure 5.50, equations 5.72b is plotted for two different amplifier gains (\( A_v = -5 \) and -10). Notice that the acceptable solution region is significantly more limited than the one discussed in the previous example. In fact, the optimal solution is determined by the intersection of curves corresponding to equation 5.72b (which determines the voltage gain) and equation 5.73 (which guarantees input impedance value), but inside of the acceptable region bounded by equation 5.66. In this case, there are no acceptable solutions for \( |A_v| = 10 \).
Fig. 5.50. Design example 2: plots of the main design equations in the $I_C$-$R_C$ plane to determine the ranges with acceptable combinations of $I_C$ and $R_C$ for a specified voltage gain.

For the optimal solution annotated in Figure 5.50, the collector current $I_CQ$ is roughly 350 µA and the collector resistance is around 6 kΩ. The circuit has been simulated in PSPICE with the component values displayed in Figure 5.51. Resistor values for $R_{B1}$ and $R_{B2}$ were selected to be very large such that $R_B = 600$ kΩ in order to avoid degrading the input impedance, since impedance since from the base is around 150 kΩ. Before you run AC and transient simulations, inspect the DC operating point of the circuit to verify the $V_{CE}$ voltage and the collector current values.

The transient response for a sinewave input signal with an amplitude of 100 mVpk is plotted in Figure 5.52. The AC signal at the base terminal of the transistor is superimposed on the DC base voltage close to 0.9 V, while the output signal is centered around 2.75 V. The amplitude of the transient signal directly at the base is approximately 100 mVpk. The output voltage amplitude is 0.5Vpk. Hence, the overall voltage gain of the amplifier is very close to the target -5V/V.

The frequency response can also be obtained from PSPICE simulations using the AC analysis option. Although the magnitude and phase responses are not shown, we encourage you to obtain these plots to find the amplifier’s bandwidth (-3 dB frequency), which is in the range of 100 MHz. In comparison, the bandwidth of the high-gain amplifier design example discussed in Section V.6 is around 30 MHz. This demonstrates another common design trade-off: the bandwidth tends to be smaller for high-gain amplifiers than for low-gain amplifiers with comparable devices and power consumption.
Fig. 5.51. Common-emitter amplifier with emitter degeneration resistor $R_E$ for improved linearity performance and higher input impedance.

![Common-emitter amplifier diagram](image)

Fig. 5.52. PSPICE transient waveforms for a 200 mV$_{pk}$ input signal, revealing the voltage gain of -4.6 V/V.

The linearity of the amplifier with emitter degeneration can also be evaluated with the PSPICE transient simulation option. The first three spectral components are depicted in Figure 5.53 using the Fast Fourier Transform (FFT) tool. It can be seen that the fundamental component is close to -10dB while the second harmonic component is approximately at -50dB, which calculates to an HD2 around -40 dB. The third harmonic component is around -60 dB. An evident question is how the amplitude of the output voltage in Fig. 5.52 is correlated with the -9dB shown in Fig. 5.53? The FFT plot shows the RMS value of the output voltage; $V_{\text{collector-RMS}}=0.5^{*}.2^{1/2}$, which indeed corresponds to -9dB.
Fig. 5.53. Spectral analysis of the output voltage at the collector. HD2 ≈ -41 dB and HD3 ≈ -62 dB.

Although the input voltage amplitude is relatively high, an important benefit of the emitter degeneration is that the swing of the base-emitter voltage reduces significantly due to the voltage swing present at the emitter. If the input signal increases such that the base-emitter voltage exceeds 10mV, the harmonic distortion components become more prominent. In figure 5.54, the harmonic distortion components for the case $V_{in}=200\text{mVpk}$ are shown.

Let us consider the small-signal equivalent circuit, which is similar to the one shown in Figure 5.36b with the exception that the signal source has a series resistance $R_S$ and that $R_{E1} = R_E$. The AC base-emitter voltage can be expressed as

$$
V_{be} = \frac{r_e}{r_e + R_E} V_p = \left( \frac{r_e}{r_e + R_E} \right) V_i.
$$

(5.74)
With the components and bias conditions in this example design, the emitter resistance \( r_e \) is 74 \( \Omega \). Therefore, assuming linear operation, the base-emitter voltage \( v_{be} \) is attenuated to

\[
v_{be} = \frac{675\Omega}{675\Omega + 74\Omega} \cdot v_i = 0.098 \cdot v_i.
\]  

(5.75)

For an input voltage \( v_i \) of 100 mV\(_{pk}\), the effective base-emitter voltage is around 10 mV\(_{pk}\). This simple analysis helps us to understand the fundamental concept behind the linearization effect of the emitter resistor: \( R_E \) effectively attenuates the base-emitter voltage swing then making the circuit more linear. Nevertheless, the accurate prediction of the harmonic distortion components based on the \( v_{be} \) reduction is more complicated. Some basic equations can be found in the appendix at the end of this chapter.

Before concluding this section, let us have a look on the base and base-emitter waveforms for the two cases: \( v_{in\_pk} = 100 \text{mV} \) and \( v_{in\_pk} = 200 \text{mV} \). The signal swing at the base is exactly equal to the input signal swing since we are not considering the source resistance \( R_S \). Notice that both base voltage and base-emitter voltages look linear in Fig. 5.55a; base-emitter voltage swing is less than 10 mV\(_{pk}\). This is not the case in Fig. 5.55b where the amplitude of the input signal is 200 mV\(_{pk}\); base-emitter signal swing is over 20 mV\(_{pk}\), making circuit non-linearities evident. The theoretical harmonic distortion values agree well with the simulation results.

Fig. 5.55. Base and Base-Emitter voltage measured for the case: a) \( v_{in\_pk} = 100 \text{mV} \) and b) \( v_{in\_pk} = 200 \text{mV} \).
V.12 P-Channel Transistor.

V.12.1. PNP device modeling. A complementary device to the NPN BJT in Figure 5.1 can be fabricated by interchanging the doping regions of the transistor. Such a so-called PNP BJT is visualized in Figure 5.60 together with its schematic symbol. In this transistor the emitter and collector regions are composed of p-type silicon. Consequently, the current flow is predominantly due to the movement of holes. Notice that the conduction of large currents in the PNP requires different relative voltages between the emitter-base and emitter-collector junctions than in the NPN case. Furthermore, the currents of the PNP transistor flow in opposite directions compared to the NPN transistor.

\[ i_C = I_{SE} \left( \frac{v_{EB}}{e^{\eta V_{th}} - 1} \right) \]  

(5.80)

The biasing and design procedures presented in this chapter can be used for PNP transistors as well. The only significant difference is that the DC bias conditions for the regions of operation are different. A PNP BJT is in cutoff region when \( V_{EB} \) is less than 0.7 V. If \( V_{EB} > 0.7 \) V and \( V_{EC} < 0.3 \) V, then it is biased in the saturation region. To operate the PNP in the active region requires that \( V_{EB} > 0.7 \) V and \( V_{EC} > 0.3 \) V. As in the case of NPN transistors, the voltage ranges for the PNP’s operating regions depend on the device materials, fabrication characteristics, and manufacturer of a given transistor.

AC analysis of PNP-based circuits can be performed by using the small-signal models in Figure 5.14 without a change in the polarities. The π-hybrid model and T-model are both identical for NPN and PNP BJTs, and the same equations apply for the calculation of their parameters. However, the movement of holes across the depletion layer tends to be slower than that of electrons. As a result, PNP BJTs typically have less transconductance \((g_m)\) and a lower transition frequency \((f_T)\) compared to NPN BJTs when their fabrication dimensions and DC bias currents are similar. Figure 5.61 shows the schematic of a PNP-based common-emitter amplifier and its small-signal equivalent.
circuit with the $\pi$-hybrid model. By inspecting the two diagrams, you can observe that the usage of the small-signal model is exactly the same as in the previous examples with NPN transistors.

![Fig. 5.61. a) A common-emitter amplifier with collector and load resistors, b) its small-signal equivalent circuit employing the $\pi$-hybrid transistor model.](image)

**V.12.2. Circuit examples with PNP transistors.** At this point, you might ask yourself what the benefit is of having a PNP transistor that is a dual of the NPN transistor but with reduced transconductance and worse high-frequency performance. If you decide to study advanced microelectronic circuits, then you will discover that PNP are often used in voltage reference circuits, temperature sensors, and biasing circuitry because they are often easier to fabricate with conventional integrated circuit technologies. One advantage of having the availability of complementary transistors becomes evident from inspecting the amplifier in Figure 5.62, which is named push-pull follower. This circuit is very useful as a buffer when the input signal swing covers the complete span between a positive supply voltage $V_{CC}$ and negative supply voltage $-V_{SS} = -V_{CC}$. In this configuration, both transistors operate as common-collector (emitter-follower) amplifiers, having a voltage gain slightly less than one and a current gain around $1+\beta$. Recall that this property allows driving a low impedance load, which is why the common-collector stages are commonly found as last stage of multi-stage amplifiers. The study of the amplifiers in this chapter with single NPN devices revealed that they all have input and output voltage swing limitations which prevent signal swings from the positive supply voltage all the way to the negative supply (or ground). But such a swing can be achieved with complementary PNP and NPN devices. In the push-pull configuration for instance, the PNP transistor conducts during positive half cycles of the input signal, while the PNP transistor processes the signal during negative half cycles. Thus, the output can be linear for the input signal swing from $V_{CC}$ to $-V_{SS}$. However, there is “dead band” when the input signal is between 0.7V and $-0.7V$ and both transistors are in the cutoff region because the input voltage is too small. This causes distortion known as “crossover distortion” that is visible in the output signal waveform.

![Fig. 5.62. A push-pull follower amplifier.](image)

Let us examine the circuit in Figure 5.63a to emphasize the similarity of the DC analysis for the PNP transistor to the NPN transistor case. Assuming a $\beta$ of 150 and a $V_{EB}$ voltage drop of 0.7 V, what is the expected voltage $V_C$ at the collector terminal? To answer this question, we can begin by calculating the emitter current based on the assumed $V_{EB}$ voltage drop, which gives $i_E = (V_{CC} - 1V + V_{EB}) / R_E = 0.588$ mA. Solving equation 5.6 for $\alpha$ with $\beta$ =
150 results in α = 0.9934. Hence, \( I_C = \alpha I_E = 0.584 \text{ mA} \) and \( V_C = I_C R_E = 1.17 \text{ V} \). To check that the transistor is biased in active region, we can calculate \( V_{EC} = (V_{CC} - i_E R_E) - V_C = 3.53 \text{ V} \). Since \( V_{EB} \) is larger than 0.3 V, the transistor is in active region.

Now consider the circuit in Figure 5.63b, in which the base terminal of the additional NPN transistor is connected to node \( V_C \). Since there is no DC blocking capacitor between the transistors, the NPN transistor will affect the voltage at the collector of the PNP transistor. The calculation of current \( i_C = 0.584 \text{ mA} \) remains the same as in the previous example, but the voltage \( V_C \) is now determined by the reduced current flowing through resistor \( R_C \). The equation that we can write for this voltage is \( V_C = (i_C - i_{B2}) R_C \). Assuming \( \beta = 150 \) and \( V_{EB} = 0.7 \text{ V} \) for the NPN BJT, its base current can be expressed as \( i_{B2} = i_C/\beta = \alpha (V_C - 0.7V)/(\beta R_{E2}) \). Solving these two equations simultaneously for their two unknown variables yields \( i_{B2} = 81.0 \mu \text{A} \) and \( V_C = 1.01 \text{ V} \). The addition of the second stage has led to a \( V_C \) reduction by 0.16 V. To avoid such loading effects, the multi-stage amplifier discussed in the previous section has the DC blocking capacitors between stages, which also simplify the DC analysis since each stage can be analyzed individually.

![Fig. 5.63. Example circuits for DC analysis.](image-url)