The Operational Amplifier and Application

The operational voltage amplifier (more commonly referred to as operational amplifier) is one of the most useful building blocks for the implementation of low- and medium-frequency analog signal processors.

The ideal operational amplifier processes a differential input signal (at its non-inverting and inverting inputs) with very high impedance at each input, very high voltage gain, wide bandwidth, and very low output impedance. These properties are desirable because they make the operational amplifier versatile, easy to interface with other blocks, and robust when combined with passive and active elements.

Operational amplifiers are usually cost-effective solutions for the realization of analog signal processing such as amplification, filtering, comparisons of voltage, etc.

A vast variety of operational amplifiers are offered by numerous integrated circuit vendors. Hence, the selection of the optimal operational amplifier for a particular application is in many cases not trivial.

This chapter deals with the fundamental concepts related to operational amplifiers. Basic amplifier circuits will be studied and analyzed with first- and second-order system approximations.
3.1. Basic Operational Amplifier Modeling.

To obtain macromodel parameters of a single-input voltage amplifier with a single output, let us consider a linear two-port system with two terminals grounded, as shown in Fig. 3.1.

This chapter presents four variables (\(v_i\), \(i_i\), \(v_o\), and \(i_o\)) for study. The interaction between the four variables can be defined in many different ways. In real-world applications, these definitions depend on the input variable (current or voltage) and the most relevant output variable. Usually, for voltage amplifiers, the input signal is defined as \(v_i\) while the output is \(v_o\).

Fig. 3.1. Electronic circuit represented by a black box.
Since we are assuming that the circuit is linear, one way to describe the electronic circuit is by using g-parameters in the following matrix representation:

\[
\begin{bmatrix}
i_i \\
v_o
\end{bmatrix} = \begin{bmatrix} g_{11} & g_{12} \\ g_{21} & g_{22} \end{bmatrix} \begin{bmatrix} v_i \\ i_o \end{bmatrix},
\]

or

\[
i_i = g_{11} v_i + g_{12} i_o
\]

\[
v_o = g_{21} v_i + g_{22} i_o.
\]

In the above equations, the parameter \( g_{11} \) is the input conductance, which relates the input current and the input voltage of the circuit without considering the effect of the output current (i.e., when \( i_o = 0 \)). The circuit’s input conductance is formally defined as follows:

\[
g_{11} = \frac{1}{Z_i} = \left. \frac{i_i}{v_i} \right|_{i_o=0}.
\]
This parameter is measured by applying a voltage \( (v_i) \) at the input and measuring the input current \( (i_i) \) while the output node is left open such that \( i_o = 0 \).

The parameter \( g_{12} \) defines the reverse current gain of a topology, and it is defined as

\[
g_{12} = \left. \frac{i_i}{i_o} \right|_{v_i=0}.
\]

The reverse current gain \( g_{12} \) is the current generated at the input due to the output current. In the ideal case this parameter is zero for voltage amplifiers, which we usually like to be unidirectional, such that the input signal generates an output signal.

To measure this parameter, one must short-circuit the input port such that \( v_i = 0 \), to apply a current at the output, and to measure the current generated at the input port. In practical circuits, this parameter is very small and is often ignored.
The forward voltage gain is defined as the ratio of the output voltage and input voltage with an open-circuit at the output:

\[ g_{21} = A_V = \left. \frac{v_o}{v_i} \right|_{i_o=0}. \]  \hspace{1cm} (3.4)

Parameter \( g_{11} = A_V \) is certainly one of the most important parameters of the two-port system. We also refer to \( A_V \) as the open-circuit gain (or open-loop gain when the feedback of a circuit is also removed). It represents the circuit’s voltage gain without any load impedance attached at the output, resulting the in zero output current.

Another important parameter is the system’s output impedance, which relates the output voltage and the output current without the effects of the input signal. It is defined as

\[ g_{22} = Z_o = \left. \frac{v_o}{i_o} \right|_{v_i=0}. \]  \hspace{1cm} (3.5)
A two-port system can be represented by the four aforementioned parameters, which are captured by the schematic of the macromodel in Fig. 3.2a.

![Schematic of a two-port system](image)

Fig. 3.2. Linear macromodels using hybrid parameters: a typical voltage amplifier and **Model for an OPAMP.** The **ideal OPAMP** is a device that can be modeled by using the circuit of Fig. 3.2b, which was obtained from the one in Fig. 3.2a with

\[ A_V = \infty, \ g_{12} = 0, \ Z_i = \infty, \ \text{and} \ Z_o = 0. \]

Input \( v_{i+} \) is commonly known as non-inverting input, and the other input (\( v_{i-} \)) as inverting input.
3.2. Basic Configurations: Inverting and Non-inverting Amplifiers.

**Inverting configuration.** The simplified linear macromodel of the OPAMP is used here for the representation of the inverting amplifier. The equivalent circuit is shown in Fig. 3.3b. By using basic circuit analysis techniques, it can be found that

\[ i_1 + i_2 = \frac{v_i - v_x}{Z_1} + \frac{v_o - v_x}{Z_2} = 0, \]  

\[ v_o = A_v (\theta - v_x). \]  

Solving these equations as a function of the input and output voltages yields

\[ \frac{v_o}{v_i} = -\left( \frac{1}{1 + \frac{1 + Z_2/Z_1}{A_v}} \right) \left( \frac{Z_2}{Z_1} \right). \]  

If the open-loop gain of the OPAMP \( A_v \) is very large, then
This result shows that if negative feedback is used and if the open-loop gain of the OPAMP is large enough, then the overall closed-loop voltage gain of the amplifier depends on the ratio of the feedback and input impedances.

Unlike the open-loop gain of the OPAMP that can vary by more than 50% due to transistor parameters variations and temperature changes, the closed-loop gain is more accurate, especially if same type of impedances are used.

Normally, the ratio of impedances is significantly more precise than the absolute values of components. Both, ratios of resistors and ratios of capacitors fabricated in the same integrated circuit can have mismatch errors as low as 0.1-0.5%

Absolute values of the components may vary by more than 30%. Thus, designing amplifiers with feedback leads to robust gains in the presence of manufacturing variations.
Fig. 3.3. Inverting amplifier: a) schematic of the circuit and b) the linear macromodel assuming that the OPAMP input impedance is infinity and that the output impedance is zero.

Another important observation is that the differential voltage ($v_x$ in Fig. 3b) at the OPAMP input is ideally zero with infinite gain. $v_o = A_v (0 - v_x)$ or $v_x = -\frac{v_o}{A_v}$

The OPAMP input voltage $v_x$ is very small if $A_v$ is large enough. It follows that the larger the open-loop gain of the OPAMP, the smaller the signal will be at its input.
The inputs of the OPAMP can be considered as a virtual short circuit. We use the word “virtual” because the voltage difference between the two input terminals ($v_+$ and $v_-$) is very small but they are not physically connected.

In this circuit, the non-inverting terminal is grounded, and the inverting terminal has the same voltage as the non-inverting terminal due to the virtual short-circuit when the OPAMP’s open-loop gain is very high.

Since $v_x = 0$ (virtual short-circuit approximation), the input current becomes $i_i = (v_i - v_x) / Z_1 = v_i / Z_1$. Since the input impedance of the ideal OPAMP is infinite, $i_i$ flows throughout $Z_2$ leading to an output voltage equal to $v_o = -i_i \cdot Z_2$.

Hence, the closed-loop voltage gain is $v_o / v_i = -Z_2 / Z_1$, which agrees with Eq. 3.9.

$$\frac{v_o}{v_i} = -\frac{R_2}{R_1}.$$  

(3.10)
Fig. 3.4. Resistive feedback amplifiers: a) inverting configuration and b) non-inverting configuration.

Non-inverting configuration. The feedback is still negative. If $R_2$ was connected to the positive terminal, the circuit would become unstable and useless for linear applications, which will be elaborated in the following sections.

The closed-loop voltage gain of the non-inverting configuration can be easily obtained if the virtual short principle is used. Due to the high gain of the OPAMP, the voltage difference between the inverting and non-inverting terminals is very small. Hence, the voltage at the non-inverting terminal of the OPAMP is equal $v_i$. The current flowing through $R_1$ and $R_2$ (towards the real ground) is therefore equal to $(v_i - 0) / R_1 = v_i / R_1$. Taking this observation into account, the output voltage can be expressed as

$$v_o = v_i + i_1 R_2 = v_i + \left( \frac{v_i}{R_1} \right) R_2 = \left( 1 + \frac{R_2}{R_1} \right) v_i.$$  \hspace{1cm} (3.11)

According to the above equation, the voltage gain $v_o/v_i$ is greater or equal than 1.
An important characteristic of the non-inverting configuration is that its input impedance is ideally infinity. Hence, several stages can be connected in cascade without loading issues.

A special case of the non-inverting configuration is the buffer configuration depicted in Fig. 3.5.

![OPAMP in unity-gain buffer configuration](image)

Fig. 3.5 OPAMP in unity-gain buffer configuration.
3.3. Amplifier with Multiple Inputs and Superposition.

R₁ and R₂ implement a voltage divide such that the input voltage at the non-inverting (v⁺) terminal is

\[ \frac{v_+}{v_{i2}} = \frac{R_2}{R_1 + R_2}. \]  \hspace{1cm} (3.12)

If a virtual short circuit at the OPAMP inputs is assumed, using KCL at the inverting terminal of the circuit (with v₋ = v⁺) leads to

\[ \frac{V_o - v_+}{R_4} = \frac{v_+ - v_{i1}}{R_3}. \]  \hspace{1cm} (3.13)

![Fig. 3.6. Amplifier configuration with two input signals applied to the non-inverting and inverting terminals.](image-url)
The output voltage can be determined using Eqs. 3.12 and 3.13, which after algebraic rearrangement gives

\[
v_o = -\left(\frac{R_4}{R_3}\right)v_{i1} + \left(\frac{R_2}{R_1 + R_2}\right)\left(1 + \frac{R_4}{R_3}\right)v_{i2}.
\]  

(3.14)

Application of the superposition principle to OPAMP circuits. If the OPAMP is considered as a linear device and only linear elements are used for its external network, then the output voltage is a linear combination of all input signals. If several inputs are applied to the linear OPAMP circuit, then the output can be obtained considering each individual input signal—one at a time (by replacing voltage sources with a short circuit to ground and current sources with an open circuit).

Mathematically, the output’s linear combination can be written as
\[ v_o = K_1 v_{i1} + K_2 v_{i2}, \ldots, K_N v_{iN} = \sum_{j=1}^{N} (K_j v_{ij}) \]  

(3.15a)

where \( K_1 \ldots K_N \) are the voltage gains from each input to the output.

Then:

\[ v_o(v_{i1}, v_{i2}, \ldots, v_{iN}) = v_o(v_{i1}, 0, 0) + v_o(0, v_{i2}, 0) + \ldots + v_o(0, 0, \ldots, v_{iN}). \]  

(3.15b)

Let us apply this principle to the circuit with two inputs in Fig. 3.6.

The circuit can be analyzed by applying one input signal at a time: If \( v_{i1} \) is considered, \( v_{i2} \) is set to zero as in the equivalent circuit of Fig. 3.7a.
Fig. 3.7 Equivalent circuits for the computation of the output voltage using superposition: a) for $v_{i1}$ and b) for $v_{i2}$. 

\[ R_3 \quad R_4 \]

\[ R_1 \quad R_2 \]

\[ v_{i1} \quad v_{i2} \]

\[ v_+ \]

\[ v_o \]
Generalization of basic configurations.

\[ v_o = -\sum_{j=1}^{N} \left( \frac{R_f}{R_j} \right) v_{ij}. \]  

(3.16)

Fig. 3.8. a) Analog inverting adder and b) its equivalent circuit for analyzing the output voltage due to \( v_{ij} \).

An analog non-inverting adder is depicted in Fig. 3.9a. Similarly to the previous case, the output voltage can be found using superposition. Fig. 3.9b shows the equivalent circuit for the \( j_{th} \)-input signal with all other inputs set to zero.
\[
\frac{v_{+j}}{v_{ij}} = \frac{R_1 \parallel R_2 \cdots R_{j-1} \parallel R_{j+1} \cdots \parallel R_N \parallel R_X}{(R_1 \parallel R_2 \cdots R_{j-1} \parallel R_{j+1} \cdots \parallel R_N \parallel R_X) + R_j}.
\] (3.17a)

![Non-inverting adder with multiple inputs and its equivalent circuit](image)

Fig. 3.9. a) Non-inverting adder with multiple inputs and b) its equivalent circuit for the \( j \)th input.

Since many components of the non-inverting adder are in parallel, it is often more convenient to use admittances instead of impedances for the analysis of this type of network. For this example, the previous equation can also be written as
\[ v_{+j} = \frac{1}{R_j} \left( \frac{1}{R_j} + \frac{1}{R_1 \parallel R_2 \parallel \cdots \parallel R_{j-1} \parallel R_{j+1} \parallel \cdots \parallel R_N \parallel R_X} \right) \]

where \( g_i = 1/R_i \). The numerator \((g_j)\) is identified as the admittance of the element connected between the input signal and \( v_{+j} \). The denominator represents the parallel combination of all elements attached to \( v_+ \). Equation 3.17b can be expressed with a shorter equation:

\[ v_{+j} = \frac{g_j}{\sum_{i=1}^{N} (g_i) + g_X} \]  

Once \( v_{+j} \) is obtained, the output voltage generated by \( v_{ij} \) can be found since \( v_{+j} \) is the voltage at the non-inverting terminal; hence, to find the output voltage for this input is straightforward as \( v_{oj} = (1+R_f/R_i) \cdot v_{+j} \). Taking into account all the input signals and applying the superposition principle, it can be shown that the overall output voltage is a linear combination of all inputs:
\[ v_o = \left(1 + \frac{R_f}{R_i}\right) \cdot \left(\sum_{j=1}^{N} v_{+j}\right) = \left(1 + \frac{R_f}{R_i}\right) \cdot \left(\sum_{j=1}^{N} \left(\frac{g_j v_{ij}}{\sum_{i=1}^{N} (g_i) + g_X}\right)\right) = \left(1 + \frac{R_f}{R_i}\right) \cdot \left(\sum_{j=1}^{N} g_j v_{ij}\right). \] (3.19)

In the non-inverting adder configuration, each input signal has a contribution to the output voltage that depends on all resistors unlike the case where inverting topology occurs. The input impedance for each input depends on the array of resistors. For instance, the input impedance seen by the \(j\)th-input signal is

\[ Z_j = R_j + (R_1 \parallel R_2 \parallel \cdots \parallel R_{j-1} \parallel R_{j+1} \cdots \parallel R_N \parallel R_X). \] (3.20)

Similar expressions can be obtained for all input resistances at the other sources.
**Design Example.** Let us construct a circuit that implements the following equation:

\[ v_o(t) = 10 \cdot v_1(t) + 20 \cdot v_2(t) + 5 \]

Assume that only supply voltages of +/-15 V are available if needed. The circuit in Fig. 3.10 can be used to realize the above equation, but keep in mind that this is not the only solution. For instance, an alternative circuit could be built using a combination of inverting and non-inverting OPAMP circuits. When using the circuit in Fig. 3.10, the design procedure consists of finding the proper resistance values. Thus, according to Eq. 3.19, the following equations must be solved:

\[
10 = \left(1 + \frac{R_5}{R_4}\right) \left(\frac{g_1}{g_1 + g_2 + g_3}\right) = \left(1 + \frac{R_5}{R_4}\right) \left(\frac{R_1 || R_2 || R_3}{R_1}\right)
\]

\[
20 = \left(1 + \frac{R_5}{R_4}\right) \left(\frac{g_2}{g_1 + g_2 + g_3}\right) = \left(1 + \frac{R_5}{R_4}\right) \left(\frac{R_1 || R_2 || R_3}{R_2}\right)
\]

\[
5 = \left(1 + \frac{R_5}{R_4}\right) \left(\frac{g_3}{g_1 + g_2 + g_3}\right) = \left(1 + \frac{R_5}{R_4}\right) \left(\frac{R_1 || R_2 || R_3}{R_3}\right)
\]

Since the design space consists of three equations and five unknowns, two conditions can be added to solve the set of equations. For instance, design considerations on noise and
power consumption may require specific values for some resistors. Without such restrictions, you have more freedom to choose the resistance values.

\[
\begin{align*}
R_4 & \quad R_5 \\
R_1 & \\
v_1 & \\
R_2 & \\
v_2 & \\
R_3 & \\
+15 & \\
\end{align*}
\]

Fig. 3.10. Non-inverting adder example circuit to sum up two input signals and a DC voltage.

Find the expression for \( V_o \): Fig. 310 is a Very good test sample! Solve it yourself!
3.4. Amplifiers with Very High Gain/Attenuation Factors.
The amplifier in Fig. 3.11 with a feedback resistor network can be used to “increase the effective feedback resistance.” Observations:

1. Since the inverting terminal is at the ground potential due to the virtual short at the OPAMP input, the resistor $R_2$ is connected between node $v_x$ and (virtual) ground.

$$v_x = \left( \frac{R_2}{R_2 || R_3} \right) \cdot v_o \quad (3.21)$$

2. Also, as a result of the virtual ground at the OPAMP’s input, the current flowing through $R_2$ is equal to $v_x/R_2 = -i_i = -v_i/R_1$.

3. Substituting the above relations into the expression of the current $i_i$ provides an equation that relates the output voltage and input voltage to each other in terms of the resistors:
\[
\begin{align*}
    i_i &= \frac{v_i}{R_1} = -\frac{v_x}{R_2} = -\left( \frac{R_2||R_3}{R_2||R_3 + R_4} \right) \cdot \left( \frac{v_o}{R_2} \right). \\
    \text{(3.22)}
\end{align*}
\]

After rearranging Eq. 3.22, the voltage gain becomes

\[
\begin{align*}
    \frac{v_o}{v_i} &= -\left( \frac{R_2}{R_1} \right) \cdot \left( \frac{(R_2||R_3) + R_4}{R_2||R_3} \right). \\
    \text{(3.23)}
\end{align*}
\]

Fig. 3.11. Resistive voltage amplifier for high-gain applications.
Furthermore, voltage $v_y$ is an attenuated version of $v_o$. More specifically, these voltages are related by the following expressions:

$$\frac{v_x}{v_y} = \frac{R_2 \| R_3}{(R_2 \| R_3) + R_4}, \quad (3.24)$$

$$\frac{v_y}{v_o} = \frac{((R_2 \| R_3) + R_4) \| R_5}{[(R_2 \| R_3) + R_4] \| R_5 + R_6}. \quad (3.25)$$

The closed-loop voltage gain can be obtained based on the above relationships between the voltages:

$$\frac{v_o}{v_i} = \left( \frac{v_o}{v_y} \right) \left( \frac{v_y}{v_x} \right) \left( \frac{v_x}{v_i} \right) = \left( \frac{((R_2 \| R_3) + R_4) \| R_5 + R_6}{(R_2 \| R_3) + R_4} \right) \left( \frac{R_2}{R_1} \right). \quad (3.26)$$

This voltage gain can be very high because it is determined by the multiplication of three terms, making it equivalent to a 3-stage amplifier. Notice that the input impedance of this inverting circuit is equal to $R_1$. 
Very large attenuation factors. The circuit in Fig. 3.13 uses a T-network at the input for signal attenuation. The voltage $v_x$ is an attenuated version of the incoming signal, and the voltage gain is adjusted to the proper level by the typical inverting configuration with dependence on the resistances at the inverting terminal.

Assuming again a virtual ground at the inverting terminal of the OPAMP, the input attenuating factor is determined by $R_1$ and the parallel combination of $R_2$ and $R_3$. The voltage gain from $v_x$ to $v_o$ depends on the ratio of resistors $R_4$ and $R_3$. Therefore, the output voltage is given by:
\[
\frac{v_o}{v_i} = \left(\frac{v_o}{v_x}\right) \left(\frac{v_x}{v_i}\right) = \left(-\frac{R_4}{R_3}\right) \left(\frac{R_2/R_3}{R_1 + (R_2/R_3)}\right).
\]  

(3.27)

The first factor in Eq. 3.27 is the result of the voltage divider at the input of the structure, while the second factor is the result of the non-inverting amplification of \(v_x\). You can also use the double T-network from Fig. 3.12 for large input attenuation factors. It is left to you to find the voltage gain of the circuit in Fig. 3.13 with a double T-network at the input.

![Fig. 3.13. Resistive amplifier using a T-configuration for large attenuation factors.](image)

- 28 -
3.5. **RC Circuits: Integrators and Differentiators.**

**Basic integrators.** If the feedback resistor of the standard inverting amplifier is replaced by a capacitor, then we obtain the lossless integrator shown in Fig. 3.14. The analysis of this circuit can be performed in the frequency domain with an impedance of the capacitor equal to \(1/(j\omega C_2)\). The transfer function of the inverting configuration is, as in the previous cases, determined by the ratio of the impedance in feedback and the impedance at the input, leading to the following result:

\[
H(s) = \frac{v_o}{v_i} = \frac{1}{sR_1C_2}
\]  

(3.28)

where \(s = j\omega\).

This circuit has a pole at the origin (when \(\omega = 0\)). The magnitude response has extremely high values at low frequencies, and it decreases with a frequency at the rate of -20 dB/decade. The phase is +90 (-270) degrees at all frequencies. Notice that the magnitude of the voltage gain is unity at \(\omega = 1/(R_1C_2)\).

Usually this configuration is not used as a standalone circuit, but it is a key building block for high-order filters and analog-to-digital converters.
In general, the combination of resistors and capacitors leads to the generation of poles and zeros. For example, the circuit implementation of a first-order filter is displayed in Fig. 3.15a. This circuit is also known as a lossy integrator because the resistor $R_3$ discharges the capacitor (i.e., $R_3$ introduces losses) while $R_1$ injects charge into $C_2$. The gain of this circuit is determined by the ratio of the equivalent impedance in feedback and the impedance at the input. In this circuit, the equivalent feedback impedance is composed of the parallel combination of the capacitor’s impedance ($1/j\omega C_2$) and $R_3$. At frequencies at which the impedance of the capacitor can be ignored, the low-frequency gain ($-R_3/R_1$) depends only on the ratio of the two resistors. At very high frequencies, the impedance of $C_2$ dominates the feedback and the circuit behaves as the lossless integrator shown in Fig. 3.14.
3.14 with a high-frequency gain defined by \(-1/sR_1C_2\). The overall voltage gain of the circuit in Fig. 3.15a at any frequency is given by:

\[
H(s) = -\frac{R_3}{R_1}\frac{1}{1+sR_3C_2}. \tag{3.29}
\]

(a)

(b)

Fig. 3.15. First-order low-pass filter: a) circuit schematic and b) sketch of its magnitude response.
Equation 3.29 confirms that the low-frequency gain is determined by the ratio of the resistors. The pole is located at \( \omega = 1/(R_3C_2) \), and for frequencies beyond this frequency, the voltage gain decreases with a rolloff of –20 dB/decade.

The main differences between this circuit and the passive low-pass filter (voltage divider with a resistor and a capacitor) are twofold: a) in the active realization (with OPAMP) the low-frequency gain can be greater than unity by adjusting the ratio of the resistors, while in the passive filter the gain is always less than one or equal to unity; b) the OPAMP allows us to connect the circuit to the next stage without affecting the transfer function, which is thankfully a result of the low output impedance of the OPAMP. A typical magnitude response obtained with this circuit is plotted in Fig. 3.15b.

If \( R_3 \geq R_1 \) the unity-gain frequency is another important parameter of the circuit in Fig. 3.15a. It can be obtained by taking the magnitude (or squared magnitude) of Eq. 3.29, and equating it to 1. The resulting equation can be solved for the unity-gain frequency, leading to the following result that you should verify for yourself:
\[ \omega_u = \left( \frac{1}{R_2C_2} \right) \sqrt{\left( \frac{R_1}{R_1} \right)^2 - 1}. \]  

For \( R_3 \gg R_1 \), this frequency is approximately given by \( \omega_u = 1/R_1C_2 \). Notice that for \( R_3 < R_1 \) the solution is imaginary, meaning that the unity-gain frequency does not exist. In fact, you cannot find any frequency where the gain is unity for an attenuator (with DC gain less than 1). For \( R_3 < R_1 \), the low-frequency gain is less than unity, and consequently there is no unity-gain frequency.
A general first-order transfer function can be implemented by using the topology in Fig. 3.16. Since the elements are connected in parallel, it is very convenient to find the voltage gain as the ratio of the equivalent input admittance and the equivalent feedback admittance as follows:

$$H(s) = -\frac{g_1 + sC_1}{g_2 + sC_2} = -\left(\frac{R_2}{R_1}\right)\left(\frac{1 + sR_1C_1}{1 + sR_2C_2}\right).$$  \hspace{1cm} (3.31)

With this transfer function for the circuit in Fig. 3.16, you can design the following filters:

(a) Low-pass filters if $C_1$ is removed. → The pole’s frequency is given by $1/(R_2C_2)$.

(b) Amplifier if $C_1$ and $C_2$ are removed. → Gain = $-R_2/R_1$.

(c) Amplifier if the resistors are removed. → Gain = $-C_1/C_2$

(not very practical because very high resistance values are needed, especially for low-frequency applications)

(d) High-pass if $R_1$ is removed. → The pole’s frequency is at $1/(R_2C_2)$, and the high frequency is equal to $-C_1/C_2$. 
The high-pass transfer function can also be realized if a series combination of a capacitor and resistor is used at the input, as shown in the Fig. 3.17. Low-frequency signal components are blocked by the capacitor due to its high impedance at low frequencies. At high frequencies, the capacitor behaves as a short circuit, and the gain is dictated by the ratio of the resistors as in the standard inverting configuration. Using conventional circuit analysis techniques, the overall transfer function can be obtained as

\[
H(s) = - \frac{R_2}{R_1 + \frac{1}{sC_1}} = - \left( \frac{sR_2C_1}{1 + sR_1C_1} \right). \tag{3.32}
\]

A DC zero and a pole located at \(\omega=1/(R_1C_1)\) can be observed from the above transfer function. After the pole’s frequency the voltage gain approaches \(-R_2/R_1\).
Non-inverting integrator. A non-inverting integrator can be implemented with the circuit in Fig. 3.18. It is usually an expensive implementation because the topology requires matched elements (i.e., high-precision components). The transfer function can be obtained by noting that the voltage at the non-inverting terminal is the result of a voltage divider between $R_1$ and $C_1$, such that $v_+/v_{in} = 1/(1+sR_1C_1)$. The voltage at the non-inverting terminal is then amplified by a factor of 1 plus the ratio of the feedback impedance $1/(sC_2)$ and the resistor $R_2$. The resulting transfer function yields:

$$H(s) = \left(\frac{1}{sR_2C_2}\right)\left(\frac{1+sR_2C_2}{1+sR_1C_1}\right).$$

(3.33)
This circuit behaves as a non-inverting integrator if $R_1C_1 = R_2C_2$, such that the voltage gain decreases with a roll off of -20 dB/decade when the frequency increases and its phase shift is -90 degrees at all frequencies.

Fig. 3.18. Non-inverting lossless integrator.
3.6. **Instrumentation Amplifiers.**

In many practical applications, it is desirable to use amplifiers with very high input impedance and very low output impedance. This is the case when the sensors have large output impedance or limited current delivering capabilities. For those applications, the inverting amplifier based on two resistors cannot be used since its input impedance is finite; i.e., defined by the input resistor(s). The only option is to use non-inverting amplifiers, as the ones shown in Fig. 3.19. Here, the incoming signal is assumed to be differential and delivered by \( v_{i1} \) and \( v_{i2} \); therefore, two non-inverting amplifiers are used in this case. In a differential system, the information is determined by the voltage difference between the two inputs (\( v_{i1} - v_{i2} \)) rather than by the voltage at each node.

The circuit in Fig. 3.19 is composed of two single-ended non-inverting amplifiers. Each amplifier is a particular case of the circuit shown in Fig. 7b where \( R_1 = 0, R_2 = \infty, R_3 = \infty \) and \( R_4 = 0 \), leading to a unity-gain amplifier (buffer) with very high input impedance. Since the OPAMP output impedance is very small you can safely connect inverting and non-inverting amplifiers at the output of this structure if required. The benefits of such buffers will be evident in the following chapters.
Fig. 3.19. Fully-differential amplifier based on two buffers.
The topology shown in Fig. 3.20 is more useful and can provide voltage amplification greater than 1. Its input impedance is also very high and entirely determined by the input impedance of the OPAMP. The analysis of this circuit is straightforward if we take advantage of the virtual short-circuit principle. As annotated in Fig. 3.20, the voltages at the two inverting terminals are equal to $v_{i1}$ and $v_{i2}$. The current flowing through $R_1$ is $i = (v_{i1}-v_{i2})/R_1$. This current flows through the resistors $R_2$, generating a voltage drop of $(v_{i1}-v_{i2}) \cdot (R_2/R_1)$ across each resistor $R_2$. The output voltage $v_{o1}$ is then equal to $v_{i1} + (v_{i1}-v_{i2}) \cdot (R_2/R_1)$, while $v_{o2}$ is equal to $v_{i2} - (v_{i1}-v_{i2}) \cdot (R_2/R_1)$. The differential voltage gain is therefore given by

$$\frac{v_{o1}}{v_{o2}} = \frac{v_{o1} - v_{o2}}{v_{i1} - v_{i2}} = 1 + \frac{2R_2}{R_1}. \quad (3.34)$$

Fig. 3.20. Practical fully-differential instrumentation amplifier input stage.
Notice in Eq. 3.34 that the output voltage is also differential: $v_{od} = v_{o1} - v_{o2}$. Since the gain in this equation is defined as the ratio of the differential output voltage and the differential input ($v_{id}$), it is known as the differential voltage gain.

For common-mode signals ($v_{ic} = v_{i1} = v_{i2}$) applied at the input of the circuit of Fig. 3.20, the voltage difference across $R_1$ is zero, leading to $i = 0$. As a result, the voltage drop across $R_2$ resistors is zero, and $v_{oc} = v_{o1} = v_{o2} = v_{ic}$. Hence, the differential output voltage $v_{od} = v_{o1} - v_{o2}$ is zero, indicating that the common-mode input signals do not have any effect on the circuit’s differential output signal. In other words, this instrumentation amplifier input stage completely suppresses any common-mode input signal components when the OPAMPs are ideal. In many measurement applications, common-mode input signals interfere with the differential measurement, which is why this amplifier topology is very helpful. For instance, the circuit is tolerant to electromagnetic interferences that equally affect both inputs. Notice that when $v_{o1} = v_{o2} = v_{ic}$, the common-mode signals are present at each amplifier output. But, common-mode signals that are present at the circuit’s input will not have any effect on the circuit’s output after subtracting the two differential output signals of each amplifier.

A popular single-ended instrumentation amplifier architecture is depicted in Fig. 3.21. There are two inputs, and the information of interest is in differential form: $v_{id} = v_{i1} - v_{i2}$. A major advantage of fully-differential circuits is that they have low sensitivity to noise.
and signal interference that affect both inputs; e.g., signals present at amplifier inputs with same phase and same magnitude. The single-ended output should be proportional to $v_{id}$, and signals that are present at both inputs with same amplitude and same phase are cancelled by the differential nature of the amplifier. Applying the superposition principle to the circuit shown in Fig. 3.21, it can be shown that the output voltage is given by a linear combination of $v_{o1}$ and $v_{o2}$ as follows:

$$v_o = \left(1 + \frac{R_5}{R_4}\right)\left(\frac{R_7}{R_6 + R_7}\right)v_{o2} - \left(\frac{R_5}{R_4}\right)v_{o1}. \quad (3.35)$$

Using Eqs. 3.34 and 3.35, the output voltage can be obtained as

$$v_o = \left(1 + \frac{R_5}{R_4}\right)\left(\frac{R_7}{R_6 + R_7}\right)\left(\left(1 + \frac{R_3}{R_1}\right)v_{i2} - \frac{R_3}{R_1}v_{i1}\right) - \left(\frac{R_5}{R_4}\right)\left(\left(1 + \frac{R_2}{R_1}\right)v_{i1} - \frac{R_2}{R_1}v_{i2}\right). \quad (3.36)$$

After some algebra we get the following result:

$$v_o = \left[\frac{R_7(R_4 + R_5)}{R_4(R_6 + R_7)}\left(1 + \frac{R_1}{R_i}\right) + \left(\frac{R_5}{R_3}\right)\left(\frac{R_2}{R_1}\right)\right]v_{i2} - \left[\frac{R_7(R_4 + R_5)}{R_4(R_6 + R_7)}\left(\frac{R_3}{R_i}\right) + \left(\frac{R_5}{R_3}\right)\left(1 + \frac{R_2}{R_1}\right)\right]v_{i1}. \quad (3.37)$$
If we introduce the conditions $R_2 = R_3$, $R_4 = R_6$ and $R_5 = R_7$, this equation simplifies to the following output:

$$v_o = \left( \frac{R_5}{R_4} \right) \left( 1 + \frac{2R_2}{R_1} \right) (v_{i2} - v_{i1}).$$  \hspace{1cm} (3.38)

The important properties of this amplifier are:

1. The **input impedance is extremely high** and depends on the selected OPAMP. Therefore, it can be easily connected to a number of sensors regardless of the sensor’s output impedance. Since the amplifier’s input impedance is high, it does not significantly affect the operation of the sensor when connected; i.e., loading effects are avoided.

2. The **output voltage is sensitive to differential input signals** $v_{id} = v_{i1} - v_{i2}$ only.

3. **Common-mode signals present at both input terminals are rejected** by the differential nature of the topology provided that the resistors are matched. Hence, accurate resistors with low tolerance specifications should be selected during the design of this type of instrumentation amplifier. With proper design, the ability to reject common-mode noise (electromagnetic interference at both amplifier inputs for instance) is a major advantage of this architecture.
Fig. 3.21. Practical single-ended instrumentation amplifier.
3.6.1. Multiple Feedback 2nd-order Low-pass Filter. Filters are used in electronics for the selection of information that is located in a specific frequency band. A popular structure is the so-called multiple feedback filter topology displayed in Fig. 3.22. Two feedback paths can be observed in this circuit: The first one due to the admittance $Y_4$, and the second one due to $Y_5$. Both elements provide negative feedback, making the circuit stable. The voltage gain can be found by solving the nodal equations with KCL at node $v_x$ and the OPAMP’s inverting terminal. These equations can be summarized in matrix form:

$$
\begin{bmatrix}
Y_1 + Y_2 + Y_3 + Y_4 & -Y_3 & -Y_4 \\
-Y_3 & Y_3 + Y_5 & -Y_5
\end{bmatrix}
\begin{bmatrix}
v_x \\
v_o
\end{bmatrix}
= \begin{bmatrix}
Y_1v_i \\
0
\end{bmatrix}.
$$

(3.39)

The solution of the system of equations allows us to find the output voltage of the circuit. Notice that we are not writing any equation for the output node of the OPAMP. When finding the solution of Eq. 3.39, we can set $v_i = 0$ since there is a virtual ground at the input of the OPAMP.

From inspection, we can observe that:
1. For the **first row, we consider the nodal equation (KCL) at node** $v_x$. For the element 1,1 (first row and first column) of the admittance matrix we have to consider all the admittances connected to $v_x$ in Fig. 3.22, which are $Y_1$, $Y_2$, $Y_3$, and $Y_4$.

2. The element 1,2 of the matrix associated with the first row second column is determined as the negative of the admittance between $v_x$ and $v_-$ because the second node considered in the admittance matrix is $v_-$. Hence, the element is listed as $-Y_3$.

3. The element on the first row and third column is the negative of the admittance(s) connected between $v_x$ and $v_o$, which is $-Y_4$ in this case.

4. For the right hand side term, we consider the input voltage and the admittance connected between $v_i$ and $v_x$, which is $Y_1$.

5. For the **second row we considered the nodal equation (KCL) at node** $v_-$. The matrix term in second row and first column is the negative of the admittance connected between $v_-$ and $v_x$.

6. The element on second row, second column is composed of all admittances connected to $v_-$ (the node under consideration for this equation).

7. Finally, the matrix term in second row and third column is the negative of the admittances connected between $v_-$ and $v_o$.

8. The second row of the right hand side column is zero because we do not have any elements connected between $v_-$ and $v_i$. 
Fig. 3.22. Multiple feedback second-order filter.

\[ v_x = \frac{Y_1}{Y_1 + Y_2 + Y_3 + Y_4} v_i + \frac{Y_4}{Y_1 + Y_2 + Y_3 + Y_4} v_o. \]  (3.40)

Also, notice that \( v_o \) depends on \( Y_5, Y_3 \) and \( v_x \) as follows:

\[ v_o = -\frac{R_5}{R_3} v_x = -\frac{Y_3}{Y_5} v_x. \]  (3.41)

\[ H(s) = \frac{v_o}{v_i} = \frac{-Y_1 Y_3}{Y_5(Y_1 + Y_2 + Y_3 + Y_4) + Y_3 Y_4}. \]  (3.42)
Fig. 3.22 shows a specific aspect of the circuit called the **second-order lowpass transfer function**. By properly selecting the admittances, the circuit shown in Fig. 3.23 behaves as a second-order lowpass filter. From Eq. 3.42 it can be derived that its transfer function is

\[
H(s) = \frac{-G_1 G_3}{s^2 C_5 C_2 + s C_5 (G_1 + G_3 + G_4) + G_3 G_4}
\]

(3.43)

where the admittances \( Y_1, Y_3 \) and \( Y_4 \) were replaced by the conductances of the resistors, and the substitutions \( Y_2 = sC_2 \) and \( Y_5 = sC_5 \) were made.
The basic properties of the circuit in Fig. 3.23 become evident from just interpreting the locations of the poles and zeros of Eq. 3.43. There are two poles defined by the components in the network external to the OPAMP. If the poles are real, then the magnitude response will remain relatively flat depending on the frequency of the dominant pole. For frequencies above the first (dominant) pole, the magnitude response decreases monotonically with a rolloff of -20 dB/decade. Beyond the frequency of the second pole the rolloff becomes -40 dB/decade as portrayed in Fig. 3.24.

![Magnitude response for a second-order transfer function with two real poles.](image)

For better rejection of high-frequency components the poles are often located close to each other as visualized by the dashed line in Fig. 3.24. In this case, the high-frequency
rolloff of the magnitude response is -40 dB/decade. For the design of a second-order lowpass filter it is more convenient to express Eq. 3.43 as follows:

\[
H(s) = \frac{-G_1 G_3}{s^2 + s \left( \frac{G_1 + G_3 + G_4}{C_2} + \frac{G_3 G_4}{C_2 C_5} \right)} = -\frac{1}{R_1 R_2 C_2 C_5} \frac{1}{s^2 + s \left( R_1 || R_2 || R_3 \right) C_2 + \frac{1}{R_3 R_4 C_2 C_5}}, \tag{3.44a}
\]

or

\[
H(s) = -\frac{\frac{R_4}{R_1} \left( \frac{1}{R_1 R_2 C_2 C_5} \right)}{s^2 + s \left( \frac{1}{R_1 || R_3 || R_4} C_2 + \frac{1}{R_3 R_4 C_2 C_5} \right)}, \tag{3.44b}
\]

The poles of the above transfer function can be determined by finding the roots of the denominator, which are:
\[ \omega_{p1,2} = \left( \frac{G_1 + G_3 + G_4}{2C_2} \right) \left\{ 1 \pm \sqrt{1 - \frac{4G_3G_4}{C_2C_4} \left( \frac{G_1 + G_3 + G_4}{C_2} \right)^2} \right\} \]

\[ \omega_{p1,2} = \left( \frac{G_1 + G_3 + G_4}{2C_2} \right) \left\{ 1 \pm \sqrt{1 - \frac{4G_3G_4}{C_2C_4} \left( \frac{G_1 + G_3 + G_4}{C_2} \right)^2} \right\} \]

(3.45)

Depending on the values of the components, the poles can be real or complex conjugates. The conditions for these cases are:

\[ \omega_{p1,2} = \begin{cases} 
\begin{align*}
\text{Real if } & 
\frac{4G_3G_4}{(G_1 + G_3 + G_4)^2} \leq 1 \\
\text{Complex conjugated if } & 
\frac{4G_3G_4}{(G_1 + G_3 + G_4)^2} > 1
\end{align*}
\end{cases} \]

(3.46)

The phase response of Eq. 3.44 is also important for the full characterization of the lowpass filter. The inverting filter configuration has a phase shift of -180 degrees at very
low frequencies. This can be verified by evaluating the transfer function in Eq. 3.44 at $s = 0$. Each pole introduces a phase shift of -45 degrees around its pole frequency as discussed in Chapter II. If the poles are far away from each other, the phase response looks like the one depicted by the solid line in Fig. 3.25. If the system has the two poles close to $\omega_{P1}$, then the system’s phase response has a rolloff of -90 degrees/decade around $\omega_{P1}$ due to phase contribution of the two poles, as exemplified by the dashed plot in the figure.

![Phase response of an inverting second-order transfer function: bode approximation.](image)

**Fig. 3.25.** Phase response of an inverting second-order transfer function: bode approximation.
3.6.2. Lowpass Filter Design Example: DC Gain = 20 dB, \( \omega_{p1} = \omega_{p2} = 100 \text{ Krad/sec.} \)
The key design equation is the desired filter transfer function in a similar form as Eq. 3.44b:

\[
H(s) = \frac{v_2}{v_i} = - \left( \frac{10\omega_{p1}^2}{(s + \omega_{p1})(s + \omega_{p1})} \right) = - \left( \frac{10\omega_{p1}^2}{s + 2\omega_{p1}s + \omega_{p1}^2} \right). \tag{3.47}
\]

Note that the numerator \(10\omega_{p1}^2\) is needed to obtain the desired DC voltage gain of 20 dB. The terms of this equation are equated one by one with the terms in Eq. 3.44b used to obtain the following design constraints:

\[
\frac{R_4}{R_1} = 10, \\
\omega_{p1}^2 = (10^5)^2 = 1/(R_3R_4C_2C_5), \\
2\cdot\omega_{p1} = 2\cdot(10^5) = (1/R_1+1/R_3+1/R_4)/C_2.
\]

Let us design the filter based on power consumption considerations. To avoid the use of very small resistors, which implies very large currents and high power consumption, let us fix the smaller resistor to \(R_1 = 10 \text{ k}\Omega\). Furthermore, we can use \(R_3 = R_4\) for simplicity. Hence,
\[ R_3 = R_4 = 10 \cdot R_1 = 100 \text{k}\Omega , \]
\[ C_2 C_5 = 1 / (\omega_{p1}^2 \cdot R_3^2) = 1 / (10^{10} \cdot 10^{10}) = 10^{-20} \text{ F}^2, \]
\[ C_2 = (1/R_1+1/R_3+1/R_4) / (2 \cdot \omega_{p1}) = (1.2 \cdot 10^{-4}) / (2 \cdot 10^5) = 0.6 \cdot 10^{-9} \text{ F}. \]

It follows that \( C_5 = C_2 C_5 / C_2 = (10^{-20} \text{ F}^2) / (0.6 \cdot 10^{-9} \text{ F}) = 16.67 \cdot 10^{-12} \text{ F}. \) This design is displayed in Fig. 3.26a. The circuit was simulated in PSPICE to evaluate the magnitude and phase responses in Fig. 3.26b and Fig. 3.26c. You can observe that the low-frequency gain is 20 dB and that the phase shift is -90° at the frequency of the two poles (\( \omega_{p1} = \omega_{p2} = 100 \text{ Krad/sec} \rightarrow f_{p1} = f_{p2} = 15,915 \text{ Hz} \)).
(a) Diagram of a circuit with resistors and a capacitor connected to an operational amplifier. The circuit includes a 10 kΩ resistor, a 100 kΩ resistor, a 16.6 pF capacitor, and a 0.6 nF capacitor.

(b) Graph showing the voltage gain (in dB) as a function of frequency (in Hz). The graph has a vertical axis labeled 'Voltage Gain (dB)' and a horizontal axis labeled 'Frequency (Hz).
Fig. 3.26. Second-order lowpass filter example: a) schematic with component values, b) simulated magnitude response, and c) simulated phase response. The bode approximations are the dashed curves.

**Relationship between frequency domain and time domain.** In many cases we are more interested in seeing the response of the circuit in time domain; e.g., impulse and/or step response. An approach for the analysis of a circuit in the time domain is to write the nodal or mesh equations in the time domain using the integro-differential equations for capacitors and inductors. Another approach is to obtain the transfer function in the frequency domain, as shown in the previous examples, and to convert it into a differential
equation by using the properties of the Laplace transform. Among the many other properties of the Laplace transform, one of the fundamental ones is the following:

\[
\ell \left( \sum_{i=0}^{N} a_i (s^i) x(t) \right) = \sum_{i=0}^{N} \frac{d^i x(t)}{dt^i}.
\]  (3.48)

This property of the Laplace transform is used for the conversion of rational linear functions in the s-domain to differential equations in the time domain. To illustrate its use, let us consider the following s-domain (frequency domain) lowpass transfer function:

\[
\frac{v_o(s)}{v_{in}(s)} = \frac{-a_0}{s^2 + b_1 s + b_0}.
\]  (3.49)

The above transfer function can be rewritten as

\[
\left( s^2 + b_1 s + b_0 \right) v_o(s) = -a_0 v_{in}(s).
\]  (3.50)
If the Laplace transform property from Eq. 3.48 is applied to both sides of this equation, the time-domain equivalent is obtained leading to the following second-order differential equation:

$$\frac{d^2}{dt^2} (v_o(t)) + b_1 \frac{dv_o(t)}{dt} + b_0 v_o(t) = -a_0 v_{in}(t).$$

(3.51)

The next step is to solve this equation while taking the type of input signal into account, which could be an impulse, a pulse or a sinusoidal input. It is not a focal point of this chapter to discuss the time domain analysis of linear systems, but you can refer to more specialized books for detailed analysis methods and examples.

3.6.3. Bandpass Transfer Function Implementation. Often the information to be processed is within a given pass band; hence, lowpass or high-pass filtering might not be the most efficient approach for signal detection. A band-pass filter is more suitable for this purpose, which can be obtained if a zero is placed at a low frequency in addition to the two poles of the lowpass transfer function. The zero can be easily implemented with a circuit if it is located at $\omega = 0$. A good example of this is shown in Eq. 3.42 where the multiple feedback transfer function generates a low-frequency zero if one of the two elements $Y_1$ or $Y_3$ is a capacitor and the other one is a conductance. A suitable option for
such a band-pass filter realization is shown in Fig. 3.27. The analysis of the circuit is similar to the one used for the previous lowpass filter, and the transfer function of this band-pass filter is

\[
H(s) = \frac{-sG_1C_3}{s^2C_1C_4 + sG_3(C_3 + C_4) + (G_1 + G_2)G_5} = -\left(\frac{G_1}{C_4}\right)\left\{\frac{s}{s^2 + \frac{sG_3(C_3 + C_4)}{C_3C_4} + \frac{(G_1 + G_2)G_5}{C_3C_4}}\right\}.
\]

(3.52)

The above transfer function has the desired zero at DC. If the poles are at the same frequency, the magnitude and phase responses can be approximated by piece-wise linear functions as depicted in Fig. 3.28.

Fig. 3.27. Multiple feedback band-pass filter.
Fig. 3.28. 2\textsuperscript{nd}-order bandpass filter transfer function: a) magnitude response and b) phase response.

3.7. **Circuits with Partial Positive Feedback.**

3.7.1. **Resistive Amplifiers with Partial Positive Feedback.** Partial positive feedback can also be used for the implementation of high-performance circuits in applications with demanding specifications. For instance, negative resistors have to be used for the design of voltage-controlled oscillators to cancel the effects of resistances associated with inductors and capacitors (due to resistive losses). In circuits with partial positive
feedback, both terminals (inverting and non-inverting) are part of feedback loops, which is exemplified by the circuit in Fig. 3.29 where the voltage at the positive terminal is an example of the output voltage $v_o$ based on the following voltage divider:

$$v_x = \frac{R_3}{R_3 + R_4} v_o. \quad (3.53)$$

The output voltage is influenced by the contribution of $v_i$ (as in an inverting amplifier with a voltage gain $= -\frac{R_2}{R_1}$) and $v_x$ (as in a non-inverting amplifier with a gain of $(1+\frac{R_2}{R_1})$). Thus, the output voltage can be expressed as:

$$v_o = \left(1 + \frac{R_2}{R_1}\right) v_x - \left(\frac{R_2}{R_1}\right) v_i = \left(\frac{R_3}{R_3 + R_4}\right) \left(1 + \frac{R_2}{R_1}\right) v_o - \left(\frac{R_2}{R_1}\right) v_i. \quad (3.54)$$

Rearranging the above equation to relate the input voltage to the output voltage yields:

$$v_o = -\left(\frac{\frac{R_2}{R_1}}{1 - \left(\frac{R_3}{R_1}\right) \left(\frac{R_1 + R_2}{R_3 + R_4}\right)}\right) v_i. \quad (3.55)$$
The positive feedback of the circuit in Fig. 3.29 is reflected in the negative term of the denominator in the above equation. The voltage gain can be very high if \( \frac{R_3 (R_1+R_2)}{(R_1 (R_3+R_4))} \) is slightly less than unity. Notice that the gain can potentially be infinite, which in a practical circuit would cause the output to be stuck at the positive or negative supply voltage level. The situation with a denominator in Eq. 3.55 having a value close to zero is undesirable because a small variation in any of the components has a very high impact on the overall voltage gain. Such variations could be due to component manufacturing tolerances, temperature changes, or component aging effects. Thus, if positive feedback is used, it is good practice to ensure that negative feedback is dominant and that component variations do not drastically affect the circuit’s performance.

![Resistive amplifier with negative and positive feedback.](image)

**Fig. 3.29.** Resistive amplifier with negative and positive feedback.
3.7.2. Realization of Negative Impedances.

The circuit in Fig. 3.30 uses partial positive feedback since the resistor $R_4$ links the output voltage and the non-inverting terminal. To understand the operation of the circuit, let us find the voltage at the non-inverting terminal. Applying the superposition principle, $v_x$ is composed of contributions from $v_i$ and $v_o$. The first component can be obtained by considering $v_i$ and grounding $v_o$ in the analysis, which can be done because the output of the OPAMP is a low-impedance node and $v_o$ is defined by the voltages applied at the OPAMP inputs. The second component is obtained by considering $v_o$ and grounding $v_i$. The combination of these two components is:

$$v_x = \frac{R_4 \parallel Z}{R_3 + R_4 \parallel Z} v_i + \frac{R_3 \parallel Z}{R_3 \parallel Z + R_4} v_o. \quad (3.56)$$

The above expression for $v_x$ can be substituted into the non-inverting gain relationship between $v_x$ and $v_o$:

$$v_o = \left(1 + \frac{R_2}{R_1}\right) v_x = \left(1 + \frac{R_2}{R_1}\right) \left(\frac{R_4 \parallel Z}{R_3 + R_4 \parallel Z} v_i + \frac{R_3 \parallel Z}{R_3 \parallel Z + R_4} v_o\right). \quad (3.57)$$

With some algebra, you can derive the overall transfer function as
\[
\frac{v_o}{v_i} = \frac{1 + \frac{R_2}{R_1} \left( \frac{R_4 || Z}{R_3 + R_4 || Z} \right)}{1 - \left( 1 + \frac{R_2}{R_1} \left( \frac{R_3 || Z}{R_3 || Z + R_4} \right) \right)}.
\]

(3.58)

Once again, the positive feedback is reflected in the negative term of the denominator. An important special case occurs when \( R_1 = R_2 \) and \( R_3 = R_4 \), such that the previous equation simplifies to

\[
\frac{v_o}{v_i} = \frac{2(R_3 || Z)}{R_3 - (R_3 || Z)} = \frac{2Z}{R_3}.
\]

(3.59)

The above transfer function allows non-inverting amplification. The most interesting property of the circuit in Fig. 3.30 is associated with the input impedance. From Eqs. 3.56 and 3.59, the input impedance is obtained for the case where \( R_1 = R_2 \) and \( R_3 = R_4 \) as shown in Eq. 3.60.
\[ v_x = \left( \frac{Z}{R_3 + 2Z} \right) (v_j + v_o) = \left( \frac{Z}{R_3 + 2Z} \right) \left( 1 + \frac{2Z}{R_3} \right) v_i = \left( \frac{Z}{R_3} \right) v_i. \] 

Therefore, the current flowing through \( Z \) is:

\[ i_Z = \frac{v_x}{Z} = \frac{v_i}{R_3}. \] 

3.30. Amplifier with partial positive feedback.

It can be noticed from Eq. 3.61 that the current flowing through \( Z \) depends on \( R_3 \) but is independent of \( Z \). Hence, this circuit can be considered as a voltage-controlled current
source: The current is controlled by the input voltage and the resistors $R_3 = R_4$, and this current is forced to flow through $Z$. On the other hand, you can derive the expression for the impedance at the input port yourself and compare it with this result:

$$Z_i = \frac{v_i}{i_i} = \frac{R_3^2}{R_3 - Z}.$$  

(3.62)

The input impedance is positive for $Z < R_3$, and negative for $Z > R_3$. Thus, if desired, the circuit in Fig. 3.30 can be designed with a negative input impedance.

A useful circuit that is often employed in the design of filters is the negative impedance converter shown in Fig. 3.31, which is a variant of the circuit depicted in Fig. 3.30. The input voltage is applied to the non-inverting terminal of the negative impedance converter, and the output voltage is $v_o = (1+R_2/R_1) \cdot v_i$. The input current is $i_i = (v_i - v_o)/Z$, leading to the following expression of the input impedance:

$$Z_i = \frac{v_i}{i_i} = \frac{v_i}{v_i - v_o} Z = \left( \frac{R_1}{R_2} \right) Z.$$  

(3.63)
Notice that the equivalent impedance at the input is negative. A negative impedance means that, contrary to the case of a positive impedance, the circuit delivers current when positive voltage signals are applied. The reason for this behavior is that the OPAMP circuit with $R_1$ and $R_2$ amplifies the input signal (without inversion) and the output voltage is greater than or equal to $v_i$. Hence positive $v_i$ generates $v_o > v_i$, and since the element $Z$ is connected between the output and input terminals, it generates a current that flows from $v_o$ to $v_i$.

![Negative impedance converter](image)

**Fig. 3.31.** Negative impedance converter.

### 3.7. 3. Sallen-Key Filter.

Positive feedback has been used for the design of filters for a long time. The filter in Fig. 3.32 consists of five admittances and an amplifier with finite gain $K$. Since the amplifier is non-inverting, the feedback produced by $Y_2$ is positive. By
following the analysis procedure discussed earlier in this chapter for the multiple feedback filters, the transfer function can be obtained by writing the admittance matrix as follows:

\[
\begin{bmatrix}
    y_1 + y_2 + y_3 + y_5 & -y_3 & -y_2 \\
    -y_3 & y_3 + y_4 & 0 \\
    0 & -K & 1
\end{bmatrix}
\begin{bmatrix}
    v_x \\
    v_y \\
    v_0
\end{bmatrix} =
\begin{bmatrix}
    y_1 v_{in} \\
    0 \\
    0
\end{bmatrix}
\]

(3.64)

Fig. 3.32. Second-order Sallen-Key filter.

The first two rows in Eq. 3.64 correspond to the nodal equations of nodes \(v_x\) and \(v_y\), respectively. The third row corresponds to the amplifier gain given by \(v_o = K \cdot v_y\). The solution of this system leads to the following transfer function for the filter:
\[ H(s) = \frac{y_1 y_3 K}{(y_1 + y_2 + y_5)(y_3 + y_4) + y_3(y_4 - y_2 K)}. \]  \hspace{1cm} (3.65)

Lowpass, bandpass and highpass filters can be designed based on the above transfer function by selecting the proper elements and component values. The special cases are:

i) Selecting \( Y_1 \) and \( Y_3 \) as conductances, and \( Y_2 \) and \( Y_4 \) as capacitive admittances, which leads to a lowpass transfer function, \( Y_5 \) can be removed in this case, resulting in the filter displayed in Fig. 3.33 with the following transfer function.

\[ H(s) = \frac{K \left( \frac{1}{R_1 R_2 C_2 C_4} \right)}{s^2 + s \left( \frac{1}{R_1 C_2} + \frac{1}{R_2 C_2} + \frac{1}{R_1 C_4} (1 - K) \right) + \frac{1}{R_1 R_2 C_2 C_4}} \]  \hspace{1cm} (3.66)

Similarly, it can be shown that the conditions below lead to band-pass and high-pass transfer functions.

ii) \( Y_1 \) and \( Y_4 \) should be selected as conductances and \( Y_3 \) and \( Y_5 \) as capacitors to realize a band-pass filter with the transfer function in Eq. 3.65.

iii) If \( Y_2 \) and \( Y_4 \) are selected as conductances, and \( Y_1 \) and \( Y_2 \) are capacitors, then a high-pass transfer function is obtained.
To practice, you should write the transfer functions for cases ii) and iii) above, and draw the schematics of the associated circuit implementations. To visualize the results, you can substitute \( s = j\omega \) into the transfer functions and plot \( |H(j\omega)| \) vs. \( \omega \) to observe the magnitude responses.

![Second order Sallen-Key Filter with positive feedback](image_url)

Fig. 3.33. Second order Sallen-Key Filter with positive feedback.

3.8. **Practical Limitations of Operational Amplifiers.**
First at all, we must recognize that practical OPAMPs are not even close to the ideal model with infinite input impedance, infinite gain, infinite bandwidth, and unlimited output current capability and output voltage range. The actual parameters and limitations depend on the OPAMP topology (arrangement and parameters of transistors, resistors and...
capacitors as well as technology used and power consumption). There are many different OPAMPs offered by vendors such as Texas Instruments, Fairchild, National Semiconductor, etc. Although the specific origins of OPAMP design limitations are outside the scope of this book, the effects of these parameters on the overall transfer function are briefly discussed in this section.

38.1. Amplifier Model with Finite DC Gain, Finite Input Impedance and Non-zero Output Impedance. A somewhat more realistic OPAMP macromodel is depicted in Fig. 3.34. Example ranges for some parameter values of commercially available OPAMPs are: $R_i = 1M\Omega - 1G\Omega$, $R_o = 1-100\Omega$, and $A_v = 10^3-10^6 V/V (60 -120 \, \text{dB})$. The gain usually decreases at a rate of -20 dB/decade above the cutoff frequency in the 10 Hz–1 kHz range. These limitations introduce errors in the transfer function. Normally, it is cumbersome to evaluate system degradations with analytical equations, especially for complex circuits. Here, we will obtain some results for a single inverting amplifier stage, but most of the conclusions from the analysis of this circuit are also valid for complex circuits.
Fig. 3.34. An operational voltage amplifier with finite input resistance, finite voltage gain, and non-zero output resistance.

Let us consider the circuit shown in Fig 3.35a and include the effects of both the OPAMP finite input impedance ($Z_i$) and the OPAMP finite gain. Note, $Z_i$ is more general than $R_i$ because the input impedance is typically dictated by both a resistive and a capacitive part. It is assumed that open-loop amplifier gain ($A_v$) is finite but with infinite bandwidth. Please keep in mind that this is not a realistic case. The effect of the finite OPAMP bandwidth is consider later in this chapter. Using the macromodel of Fig. 3.34 where $R_o = 0$ (assuming that $R_o \ll |Z_F|, R_L$), the equivalent circuit can be drawn as shown in Fig. 3.35b. The transfer function can be obtained if the nodal equation at the inverting terminal $v_-$ is written. Since $v_o$ is controlled by the voltage-dependent voltage source [$v_o = A_v(v_+ - v_-)$], the output voltage is entirely defined by the voltage across the OPAMP input terminals and the external impedance elements. The current demanded by $Z_F$ and $Z_L$ is provided by the ideal voltage-controlled voltage source, when can take on any necessary value to solve the equations. However, a real OPAMP has a specified
maximum output current (that is listed in the datasheet), and as a consequence you should be careful when selecting external resistors. Before finalizing a design, it is important to verify with calculations and transient simulations that the resistor values are large enough to avoid an excessive current flow that cannot be sustained at the OPAMP output terminal.

Fig. 3.35a) Inverting amplifier with OPAMP input impedance $Z_i$ and load impedance $Z_L$, and b) its small-signal equivalent circuit where $R_o = 0$.

Let us quantify the effects of $Z_i$ and finite $A_v$ on the transfer function of the circuit in Fig. 3.35. The circuit’s transfer function can be derived by solving the fundamental equation ($i_1 = i_i + i_o$) and taking into account that $v_o = A_v(v_+ - v_-)$ where $v_+ = 0$ due to the connection to ground:
\[
H(s) = -\left( \frac{Z_F}{Z_i} \right) \frac{1}{1 + \frac{1}{A_v} \left( \frac{Z_F}{Z_i} + \frac{Z_F}{Z_i} \right)}.
\]

(3.67)

The effect of the finite open-loop DC gain and finite input impedance on the inverting amplifier can be better appreciated if an error function is defined. From Eq. 3.67 it follows that

\[
H(s) = -\left( \frac{Z_F}{Z_i} \right) \frac{1}{1 + \xi} \approx -\left( \frac{Z_F}{Z_i} \right) (1 - \xi)
\]

(3.68)

where the approximation is valid when the value of the error function $\xi$ is small ($\xi \ll 1$), and $\xi$ is defined as

\[
\xi(s) = \frac{1}{A_v} \left( \frac{Z_F}{Z_i} + \frac{Z_F}{Z_i} \right) \approx \frac{1}{A_v} \left( \frac{Z_F}{Z_i} \right) = \frac{1}{A_v} \left( \frac{Z_F}{Z_i} \right).
\]

(3.69)

If the OPAMP DC gain $A_v$ is limited, the assumption of a virtual ground at the inverting input is no longer valid because any output voltage variation corresponds to a finite variation of the differential input signal given by $v_o/A_v$. The smaller the OPAMP gain, the
larger the voltage variations at the OPAMP input terminals are. Hence, the error should be inversely proportional to $A_v$, as predicted and confirmed by Eq. 3.69. The voltage variations on the non-inverting terminal lead to current errors: First, the input current $i_1 = (v_i - v_-)/Z_1$ has an error proportional to $Z_1$ ($i_{\text{error1}} = -v_-/Z_1$); second, the OPAMP input impedance affects the current generated by $Z_1$, leading to another current error component of $i_{\text{error2}} = v_-/Z_1$. These current errors are converted into voltage errors by the feedback impedance $Z_F$. Notice from Eq. 3.67 that even if the OPAMP input impedance is infinite, a gain error approximately proportional to the magnitude of the intended (ideal) gain $Z_F/Z_1$ and inversely proportional to $A_v$ is present. For a given OPAMP open-loop gain $A_v$, the larger the magnitude of the closed-loop amplifier gain (i.e., the amplification gain you want to implement given by $-Z_F/Z_1$) the larger the error is. The error tolerance is application-dependent. For instance, to keep the transfer function error below 1%, it is required to satisfy the condition:

$$\xi(s) = \left\{ \frac{1}{A_v} \left( \frac{Z_F}{Z_1||Z_i} \right) \right\} < 0.01.$$  

(3.70)

An important limiting factor is the magnitude of the desired amplification gain $Z_F/Z_1$. Notice that Eq. 3.69 can also be rewritten as
The first factor on the right hand side of Eq. 3.71 is the ratio of the magnitude of the intended gain over the OPAMP open-loop gain. The second factor shows that it is desirable to maintain the values of the resistors well below the value of the OPAMP’s input impedance. For instance, if the OPAMP input impedance is $Z_i = 1 \, \text{M}\Omega$ and the closed-loop voltage gain is $-Z_F/Z_1=-10$, and we want to maintain the gain error under 1%. The estimated open-loop voltage gain requirement of the OPAMP according to Eq. 3.71, which is 2000 when $Z_i = 1 \, \text{M}\Omega$. Examples of the OPAMP gain requirements for different $Z_F/Z_i$ ratios are listed in Table 3.1. Notice that the gain requirement decreases as $Z_F$ increases relative to the OPAMP’s input impedance $Z_i$. The realization of high closed-loop gain factors in combination with low feedback resistance values usually demands high-gain OPAMPs.

Table 3.1    Requirements for the OPAMP open-loop gain in the example circuit to maintain a closed-loop gain error below 1% with different $Z_F/Z_i$ ratios.
### Table 3.3.1

<table>
<thead>
<tr>
<th>$Z_F / Z_i$</th>
<th>$A_V$</th>
</tr>
</thead>
<tbody>
<tr>
<td>100 $\Omega$ / 10 $\Omega$</td>
<td>&gt; 1000</td>
</tr>
<tr>
<td>10 k$\Omega$ / 1 K$\Omega$</td>
<td>&gt; 1001</td>
</tr>
<tr>
<td>1 M$\Omega$ / 100 K$\Omega$</td>
<td>&gt; 1100</td>
</tr>
<tr>
<td>10 M$\Omega$ / 1 M$\Omega$</td>
<td>&gt; 2000</td>
</tr>
</tbody>
</table>

### 3.8.2. Effects of Finite OPAMP Bandwidth

Unfortunately the OPAMP bandwidth is usually limited. For example, the -3dB frequency of the $\mu$A741 is only in the 1-10 Hz range while the open-loop DC gain is around $2 \cdot 10^5$V/V. The product of the open-loop DC gain and the bandwidth is defined as the OPAMP’s gain-bandwidth product (GBW). For the OPAMP $\mu$A741, the typical value of GBW is around 1.5 MHz. These parameters and the transfer function of the $\mu$A741 are illustrated in Fig. 3.36.
An OPAMP’s open-loop voltage gain can be modeled with a finite DC gain and a low-frequency pole as follows:

\[
A_V(s) = \frac{A_{DC}}{s} \cdot \frac{1}{1 + \frac{s}{\omega_p}}. \tag{3.72}
\]

Notice that \( \text{GBW} = A_{DC} \cdot \omega_p \). In first-order models, this parameter is also known as the unity-gain frequency \( \omega_u \), defined as the frequency at which the gain magnitude is unity. This frequency is important because it defines the upper limit for the operation of the OPAMP: Beyond this frequency the OPAMP is no longer an amplifier but an attenuator.
Another limitation is that OPAMPs typically have to be operated at frequencies well below $\omega_u$ because a high gain is required. Notice that if you have two or more poles below the unity-gain frequency, then the magnitude response does not match the one in Fig. 3.36 because the roll-off prior to the unity-gain frequency is steeper than -20 dB/decade, such that $\text{GBW} \neq A_{\text{DC}} \cdot \omega_P$.

We learned from the discussion in the previous subsection that an error is introduced if the open-loop gain of the OPAMP is finite. For the inverting configuration, the gain error is determined by Eq. 3.71. If $A_v$ is frequency-dependent, then by making use of Eq. 3.72, we can obtain the general form for the error function including the effects of the finite OPAMP bandwidth:

$$
\xi(s) = \left( \frac{Z_F}{Z_i} \right) \left( \frac{Z_i + Z_i}{A_{\text{DC}}} \right) \left( 1 + \frac{s}{s + \frac{1}{\omega_P}} \right).
$$

Based on the above expression, the pole of the OPAMP leads to a zero in the error transfer function. Fig. 3.37 illustrates the relationship between error function and OPAMP frequency response. The low-frequency error can be estimated from Eq. 3.73 (where $s = 0$). At the frequency of the OPAMP’s pole $\omega_P$, the voltage gain decreases due
to the pole. As a result, the error function increases as predicted by Eq. 3.73. In a first-order approximation, the error function increases by a factor of 10 when the frequency increases by the same factor after the location of the pole. The higher the OPAMP bandwidth (ω_P), the smaller the high frequency error is.

For the example discussed in Section 3.8.1, we have: \( A_{DC} = 10^5 \text{ V/V} \), \( Z_F/Z_1 = 10 \), \( Z_i = 1\text{MΩ} \). If we consider the error measured and different frequencies, the computation of the error function in Eq. 3.73 yields to the results listed in Table 3.2. Notice in the first 5
rows that the error increases with frequency. This is a result of the limited bandwidth of the OPAMP. We have to remember that the open-loop voltage gain reduces approximately proportionally to frequency after $\omega_P$. The error is less than 1% if and only if the frequency of the applied signal meets the condition $\omega/\omega_P < 100$. For the $\mu$A741 OPAMP, $f_P = 6$ Hz and hence the signal’s frequency has to be less than 600 Hz to achieve an amplification factor of -10 with less than 1% error in the example inverting amplifier configuration. It can also be observed from Table 3.2 that the effect of the OPAMP’s finite input impedance is not very critical if the impedances $Z_1$ and $Z_F$ are smaller than $Z_i/10$.

Table 3.2 Closed-loop gain magnitude error of the example amplifier for different $Z_1/Z_i$ and $\omega/\omega_P$ ratios.

<table>
<thead>
<tr>
<th>$Z_1 / Z_i$</th>
<th>$\omega / \omega_P$</th>
<th>Error magnitude</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.001</td>
<td>0.01</td>
<td>$\sim 10^{-4}$</td>
</tr>
<tr>
<td>0.001</td>
<td>1</td>
<td>$\sim 1.4\cdot10^{-4}$</td>
</tr>
<tr>
<td>0.001</td>
<td>10</td>
<td>$\sim 10^{-3}$</td>
</tr>
<tr>
<td>0.001</td>
<td>100</td>
<td>$\sim 10^{-2}$</td>
</tr>
<tr>
<td>0.001</td>
<td>1000</td>
<td>$\sim 10^{-1}$</td>
</tr>
</tbody>
</table>
### 3.8.3. Linear Range Limitations

The operation of an OAPMP is limited by the power supply. For example, the μA741 is usually biased with a dual power supply of ±15 V. In practice, the OPAMP is implemented with interconnected transistors that implement a cascade of gain stages to achieve high gain and over the widest possible bandwidth. It will become evident in Chapters V and VI that these devices require some voltage headroom to operate in a linear mode. The linear range could be limited to ±14 V when an OPAMP is loaded by a resistor of 10 kΩ or larger, and it could reduce to ±13 V when loaded by a resistor of 2 kΩ. Be aware that the operation of the circuits described in the previous sections are effectively implemented provided that one does not exceed the capabilities of the amplifier. As a rule of thumb, the linear range of the amplifiers is limited to around 1 V from the power supply. The OPAMPs also have limitations on the maximum power (and/or current) they can deliver to the load (including the feedback network components) during the processing of signals. When selecting resistors and capacitance values, be aware that small impedances demand significant amounts of current especially when processing signals with large voltage swings. For example, the

<table>
<thead>
<tr>
<th>Value</th>
<th>Gain</th>
<th>Approx. Limit</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.01</td>
<td>100</td>
<td>~10⁻²</td>
</tr>
<tr>
<td>0.1</td>
<td>100</td>
<td>~10⁻²</td>
</tr>
<tr>
<td>1</td>
<td>100</td>
<td>~2·10⁻²</td>
</tr>
</tbody>
</table>
power consumption of the μA741 is in the 50-100 mW range. In comparison, if a DC signal of 10 V is applied to a 100 Ω resistor, the resulting power dissipation is 1000 mW, while a 100 KΩ resistor dissipates 1m W. To avoid using an OPAMP outside of the specified limits, you should look up ratings and specification parameters in the datasheet and compare them with your calculations and transient simulation results. Another result of an OPAMP’s output current limitation is its maximum output voltage rate of change known as slew rate (SR), which is formally defined as

\[ SR = \frac{dv_{out}}{dt} \bigg|_{max}. \]  

(3.74)

The SR units are V/s, and they represent the maximum output voltage variation over time. The μA741 OPAMP has a typical slew rate of 0.5V/μs, implying that it cannot follow very fast signal variations. For a sinusoidal signal with an amplitude of \( V_m \) and a frequency of \( \omega_0 \) radians/s, the maximum rate of change for the signal can be estimated as

\[ \frac{dv_{out}}{dt} \bigg|_{max} = V_m \frac{d}{dt} \left[ \cos(\omega_0 t) \right]_{max} = V_m \omega_0 = (2\pi) (V_m f_0). \]  

(3.75)
Therefore, a real OPAMP with finite slew-rate SR can follow signals that are limited in amplitude and frequency under the following condition:

\[ V_m f_0 \leq \frac{SR}{2\pi}. \]  

(3.76)

For an input signal of 1 V, the maximum frequency the \( \mu A741 \) can follow without significant distortion is limited to around 79.6 KHz. However, if the signal amplitude increases to 10 V, the signal frequency must be limited to 7.96 KHz. The maximum frequency of operation is also limited by the frequency in which the error of realization is within specifications described in Section 3.8.2. The circuit will amplify the signal until the unity-gain frequency, but the system performance may not be acceptable when processing signals with frequency components close to the unity-gain frequency. Practical applications require the consideration of other parameters that are beyond the scope of this book such as DC offset, harmonic distortion (or linearity), tolerance to power supply noise and the noise level due to OPAMP internal components. The analysis of these parameters requires the understanding of OPAMP-internal circuit-level characteristics as well as a thorough understanding of the origin and nature of noise components.
In this chapter, the operational amplifier was introduced as a building block that finds application in a variety of electronic circuits. A simple ideal model was used to convey analysis methods for amplifier and filter circuits. It was demonstrated with examples how the analysis techniques can be employed to derive frequency-dependent transfer functions for OPAMPs with external feedback networks. The analysis approach was extended to account for OPAMP non-idealities such as finite input/output impedance, gain, and bandwidth. Other imperfections such as output current, voltage range and slew rate limitations were also discussed in this chapter. These limitations are consequences of physical properties associated with the devices within OPAMPs where the transistors impose the most stringent performance limits. In the following chapters, the fundamental devices of electronic circuits will be introduced along with device models, analysis methods, and example circuits.