Fundamentals on CMOS Current Mirrors and Amplifiers

ECEN-489
Power Management
MOS Transistor

Subthreshold (weak inversion)

\[ V_{T} > V_G > 0 \]
\[ V_D > 0 \]

Saturation (Strong inversion)

\[ V_G > V_T \]
\[ V_D > 0 \]

N-type transistor

- **Subthreshold** (extremely low-voltage low-power applications)
- **Linear region** (voltage controlled resistor, linear OTA’s, multipliers)
- **Saturation region** (Amplifiers)
Current Mirrors

\[ V_{GS} > V_T \quad \text{and} \quad V_{DS} > V_{GS} - V_T \quad \text{or} \quad V_D > V_G - V_T \]

If

\[ I_D = \frac{\mu_n C_{OX}}{2} \frac{W}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS}) \]

or

\[ V_{GS} = V_T + \sqrt{\frac{2I_D}{\mu_n C_{OX} \frac{W}{L} (1 + \lambda V_{DS})}} \]

M1=M2 =>

\[ I_{D1} = \frac{\mu_n C_{OX}}{2} \frac{W}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{D_{S1}}) \]

\[ I_{D2} = \frac{\mu_n C_{OX}}{2} \frac{W}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{D_{S2}}) \]

\[ I_{D1} \text{ generates the voltage } V_{GS} \]

\[ V_{GS} \text{ generates } I_{D2} \]
Current Mirrors

If $M1 = M2$ and $\lambda = 0$ and mobility degradation is zero $\Rightarrow$

$$I_{D1} = I_{D2} \quad \text{IDEAL CURRENT MIRROR}$$

If $(W/L)_2 = N(W/L)_1$ and assuming $V_{T1} = V_{T2}$ then

$$I_{D2} = \frac{\mu_n C_{OX}}{2} \left( \frac{W}{L} \right)_2 (V_{GS} - V_{T2})^2 = \frac{\mu_n C_{OX}}{2} \left( N \frac{W}{L} \right)_1 (V_{GS} - V_{T2})^2$$

$$I_{D2} = NI_{D1} \quad \text{IDEAL CURRENT AMPLIFIER}$$
Current Mirrors: Accuracy limitations

In general, \((W/L)_2 = N(W/L)_1\), most probably \(V_{T1} \neq V_{T2}\), then

\[
I_{D2} = \frac{\mu_n C_{OX}}{2} \left( \frac{W}{L} \right)_2 (V_{GS} - V_T)^2 (1 + \lambda_2 V_{DS2})
\]

\[
I_{D2} = \frac{\mu_n C_{OX}}{2} \left( \frac{W}{L} \right)_2 (V_{GS} - V_{T2})^2 (1 + \lambda_2 V_{DS2})
\]

\[
I_{D1} = \frac{K_{P2}(V_{GS} - V_{T2})^2 (1 + \lambda_2 V_{DS2})}{K_{P1}(V_{GS} - V_{T1})^2 (1 + \lambda_1 V_{DS1})} \frac{N I_{D1}}{I_{D1}}
\]

Error \(\approx \lambda_2 V_{DS2} \neq \lambda_1 V_{DS1}\)

Error \(\approx K_{P2} \neq K_{P1}\)

Error \(\approx V_{T2} \neq V_{T1}\)

\(\lambda \propto \frac{1}{L}\)  \(\text{Long devices reduce the error; make } V_{DS1} = V_{DS2}\)

Errors can be reduced (but not eliminated) by using replicas of the main device and good layout!

Effective mobility and threshold voltages are sensitive to \(V_{DS}\) and \(V_{dsat}\)

Good solution => use cascode structures
DC Current Mirrors: Second-Order Effects

\[
\frac{I_{D2}}{I_{D1}} = \frac{\mu_{n2}(V_{GS} - V_{T2})^2(1 + \lambda_2 V_{DS2})}{\mu_{n1}(V_{GS} - V_{T1})^2(1 + \lambda_1 V_{DS1})} N
\]

Error \approx V_{T2} - V_{T1}

Error is minimized by using replicas of the basic device

Intra-die \( V_T \) mismatches are inversely proportional to gate area!

After good layout: Tolerances in \( N \) are in the range of 0.5-2 \%. Usually mismatches are inversely proportional to gate area!

\[
\mu = \mu_0 \frac{1}{1 + \theta V_{gs}} \frac{1}{1 + \frac{V_{ds}}{L \varepsilon_{crit}}}
\]

\[ VT \]
\[ VT0 \]

1-3\( \mu \)m

W
Small signal analysis: AC components $i_{d1-2}$

\[ i_{d2} = \frac{g_{m2}}{g_{m1} + g_{01}} i_{d1} + g_{02} v_{02} \]

If the capacitors are considered,

\[ g_{01} = \frac{1}{r_{01}} \Rightarrow g_{01} + sC_{eq} \]
\[ g_{02} \Rightarrow g_{02} + sC_{eq2} \]

Also, you have to consider the overlapping capacitor $C_{GD2}$

Notice:

- $g_{m1}v_{gs1}$ is controlled by its own terminal
  \[ \Rightarrow \] represents an impedance (conductance = $g_{m1}$)

- The output resistance is given by $r_{02}$

\[ i_{d2} = \frac{g_{m2}}{g_{m1} + g_{01}} \frac{i_{d1}}{1 + s} + \frac{(g_{02} + sC_{eq2})v_{02} + ..}{g_{m1} + g_{01}} \]
Small signal analysis: AC components and capacitors

Low-frequency output current

\[ i_{d2} = \frac{g_{m2}}{g_{m1} + g_{01}} i_{d1} + g_{02} v_{02} \]

Medium frequency: Ignoring \( C_{gd2} \)

\[ i_{d2} = \frac{g_{m2}}{g_{m1} + g_{01}} \frac{i_{d1}}{1 + s \frac{C_{x}}{g_{m1} + g_{01}}} + (g_{02} + sC_{y})v_{02} + \ldots \]

Notice that the only component that is mirrored is the one associated with \( g_{m} \! \)!

Exercise: consider the effects of the overlapping (miller) capacitor \( C_{gd2} \)

This issue is more complex since it links the two floating nodes D1 and D2
IMPEDANCE: Basic Configurations

Can you ignore $g_{mb}$?
This question is not for this class!

If $V_d \approx 0$
but be careful when using this approximation
Small signal analysis: Common-source amplifier

Small signal equivalent

\[ AV = \frac{g_{m1}}{g_{01} + g_{02}} \]

If \( V_{OUT} > V_{DSAT1} \), \( V_{OUT} < V_{DD} - V_{SAT2} \)

\[ V_{GS} \]

Operating point

\[ Q \]

\[ v_{TH} \] \[ v_{GSQ} \]

\[ v_{OUT} \]

\[ r_{01} \] \[ r_{02} \]

\[ g_{m1}, g_{01}, \text{and } g_{02} \text{ are function of } Q \]
Small signal analysis: Common-drain (source follower) amplifier

**Small signal equivalent circuit**

**How this is done? Why?**

\[
\begin{align*}
V_{\text{out}} &= g_m V_{\text{in}} \\
V_{\text{in}} &= g_m V_{\text{in}} + g_m V_{\text{gs1}} + g_m V_{\text{bs1}} + \frac{1}{g_m} + \frac{1}{g_{mb}}
\end{align*}
\]
Small signal analysis: Common-gate amplifier (cascode)

\[
\frac{V_{out}}{V_{in}} = \frac{g_{m1} + g_{mb} + g_{01}}{g_{01} + g_{02}}
\]

Impedance seen at Vin and Vout? Are they relevant?
Precise Current Mirrors: Cascode structure

Error $\approx \lambda_2 V_{DS2} - \lambda_1 V_{DS1}$

FUNDAMENTAL PRINCIPLE:

Error can be reduced if and only $\lambda_2 = \lambda_1$ and $V_{DS2} = V_{DS1}$

$\Rightarrow$ Transistors M1 and M2 are used as current mirrors

$\Rightarrow$ Transistors M3 and M4 are used to have $V_{DS1} = V_{DS2}$

$\Rightarrow L_1 = L_2$ and $I_{D1} = I_{D2} \Rightarrow \mu_1 = \mu_2$

$\Rightarrow$ If $M_1 = M_2$ then $\mu_1 = \mu_2$, and $V_{T1} = V_{T2}$
AC Analysis: Cascode structure @ low frequencies

M1 AND M2 ARE THE CURRENT MIRRORS

Solve this circuit for $i_{d2}$ or $v_{02}$ as function of $i_{ia}$!
AC Analysis: Cascode structure @ low frequencies

Thevennin equivalent: Relevant parameters: Zin, Zout and id2

Main parameters are computed as:

\[ Z_{in} = \frac{V_{in}}{i_{in}} \bigg|_{v_{02}=0} \quad ; \quad A_{vf} = \frac{V_{in}}{v_{02}} \bigg|_{i_{in}=0} \]

\[ A_I = \frac{i_{d2}}{i_{in}} \bigg|_{v_{02}=0} \quad ; \quad Y_{out} = \frac{i_{d2}}{v_{02}} \bigg|_{i_{in}=0} \]

\[ v_{in} = Z_{in}i_{in} + A_{vf}v_{02} \]

\[ i_{d2} = A_I i_{in} + Y_{out}v_{02} \]
Output impedance: Cascode structure

\[ Y_{\text{out}} = \left. \frac{i_{d2}}{v_{02}} \right|_{i_{\text{in}} = 0} \]

\[ i_{d2} = (v_{02} - v_{s4})g_{04} - g_{m4}v_{s4} \]

\[ i_{d2} = g_{02}v_{s4} \]

\[ Z_{\text{out}} = r_{02} + r_{04} + g_{m4}r_{02}r_{04} \]

Notice that most of the AC current re-circulate within the cascode device and only \( i_{d2} \) is extracted from \( v_{02} \) !!

Compare \( g_{m4} \) with \( g_{02} \)!
Comparison of current sources: output impedance and headroom

\[ r_{out} = r_{02} \]

\[ V_0 > V_{DSAT2} \]

\[ V_0 > V_{GS1} + V_{DSAT4} = V_{T1} + V_{DSAT1} + V_{DSAT4} \]

\( \approx 100\text{-}400 \text{ mV} \)

\( \approx 0.9\text{-}1.5 \text{ V!} \)
Double Cascode Structure: Advantages and drawbacks!

Small signal output resistance: explain in class this circuit

\[ r_{\text{out}} \approx g_{m4} r_{04} (r_{\text{eq1}}) \approx g_{m4} r_{04} (g_{m3} r_{02} r_{03}) \]

\[ V_0 > V_{\text{DS2}} + V_{\text{DSAT3}} + V_{\text{DSAT4}} \]

- Output resistance is increased
- Voltage swing is reduced
- Parasitic poles could be an issue

How VG3 and VG4 can be generated???

Usually this section is more complex to ensure VDS is similar in both transistors M1 and M2
Voltage references (biasing cascode structures)

Let's consider the case: $V_{DS2} = V_{DSAT2}$

➢ $V_{G3}$ must be $V_{GS3} + V_{DSAT2} = V_{T3} + V_{DSAT3} + V_{DSAT2}$

$$V_{GSR} = V_{TR} + \frac{2}{\mu_n C_{OX}} \frac{L_R}{W_R} I_{D1}$$

Increasing L/W by 4, VDSAT increases by 2

According to $(W/L)_1$, the gate dimensions for MR $(W/L)_R$ must be designed

Problem: $V_{TR} \neq V_{T3}$
Partial solution: $(W/L)_1 = 9(W/L)_R$
Improved (self regulated) current source

\[
\begin{align*}
I_D & \approx g_m (1 + A_V) r_{02} r_{04} \\
r_{out} & \approx g_m (1 + A_V) r_{02} r_{04}
\end{align*}
\]

Similar to double cascode

Key issue: Please understand the concept!!
Other current sources

Wilson Current Source

$$ r_{out} \approx g_m (1 + A_v) \left( r_{eq2} \right) r_{04} $$

$$ r_{eq2} = 1/g_m $$

M1, M3 in triode region
M2, M4 are saturated

$$ r_{out} = ?? $$

$$ V_{out, min} = ?? $$
Other current sources

M1, M3 in triode region
M2, M4 are saturated

\[ i_D = \mu C_{OX} \frac{W}{L_{eff}} \left[ V_{GS} - V_T - 0.5 V_{DS} \right] V_{DS} \]

\[ r_{ds3} = \frac{L_{eff}}{\mu C_{OX} W \left[ V_{GS3} - V_T - V_{DS3} \right]} \]

\[ r_{out} \approx g_m 4 r_{04} \left( r_{ds3} \right) \approx \]

\[ V_0 > V_{DS3} + V_{DSAT4} \]

\[ r_{out} \approx g_m 4 r_{04} \left( \sum r_{dsi} \right) \]
Differential Pair: Linear range is limited to $2 \, V_{\text{DSAT}}$

If both transistors are saturated and IB is ideal ($r_{\text{IB}}=\infty$)

\[
\begin{align*}
    i_{\text{d1}} + i_{\text{d2}} &= IB \\
    i_{\text{d1}} &= \frac{\mu_n C_{\text{OX}}}{2} \frac{W}{L} (V_{\text{gs1}} - V_T)^2 \\
    i_{\text{d2}} &= \frac{\mu_n C_{\text{OX}}}{2} \frac{W}{L} (V_{\text{gs2}} - V_T)^2
\end{align*}
\]

Solving these equations $\Rightarrow$ Valid for $|v_1 - v_2| < 2^{1/2}V_{\text{DSAT1}}$

\[
\begin{align*}
    i_{\text{d1}} &= \frac{\text{IB}}{2} + \frac{g_{\text{ml}}(v_1 - v_2)}{2} \sqrt{1 - \left(\frac{v_1 - v_2}{2V_{\text{DSAT1}}}\right)^2} \\
    i_{\text{d2}} &= \frac{\text{IB}}{2} - \frac{g_{\text{ml}}(v_1 - v_2)}{2} \sqrt{1 - \left(\frac{v_1 - v_2}{2V_{\text{DSAT1}}}\right)^2}
\end{align*}
\]
The diff pair is a nonlinear circuit

\[ i_{d1} - i_{d2} = g_m (v_1 - v_2) \left( 1 - \frac{(v_1 - v_2)^2}{2V_{DSAT1}} \right) \]

Non-linear term

If \( v_d = v_1 - v_2 < V_{DSAT1} \Rightarrow \)

\[ i_{d1} - i_{d2} = \sqrt{\mu_n C_{OX}} \frac{W}{L} I_B (v_1 - v_2) \]

Note:
Linear range increases for large \( V_{DSAT1} \)
\( V_{GS} \) is also increased (limited by VSS)
Basic Operational Transconductance Amplifier

DESIGN CONSIDERATIONS:

- $V_d = v_1 - v_2 < V_{DSAT}$
- $V_{1,2} - VSS > V_{GS1} + V_{DSATB}$

For small signals, ignoring the capacitors:

$$i_{out} = \sqrt{\mu_n C_{OX} \frac{W}{L}} I_B (v_1 - v_2)$$

or

$$i_{out} = g_m (v_1 - v_2) \quad \text{Sensitive to differential signals}$$

$$v_{out} = g_m r_{out} (v_1 - v_2)$$

$$r_{out} = r_{o1} \Pi r_{op}$$

For an ideal current source and ignoring the effects of $g_{mb}$, and transistor mismatches, then $i_{out} = 0$ for $v_1 = v_2$ ==> rejection to common-mode (noise) signals present at the input!
Consider node $V_X$

$$V_X = -\frac{0.5g_m R_X}{1 + SR_X C_X} V_d$$

$$R_X = r_{01} || r_{0P} || \left( \frac{1}{g_{mp}} \right)$$

$$C_X \approx 2C_{gsp} + C_{dbp} + (1 + \text{millerfactor}) C_{dgp} + C_{dbn}$$
Frequency Response

\[ V_0 = - \frac{g_{mp}}{1 + S \frac{C_0}{g_{mp}}} \left( 0.5g_m R_0 \frac{V_d}{1 + S \frac{C_0}{g_{mp}}} - \frac{0.5g_m R_0}{1 + S \frac{C_0}{g_{mp}}} V_d \right) \]

\[ V_0 = \left| 1 + \frac{\left( \frac{g_{mp}}{g_{mp}} \right)}{1 + S \frac{C_0}{g_{mp}}} \right| \left( 0.5g_m R_0 \frac{V_d}{1 + S \frac{C_0}{g_{mp}}} \right) \]
Frequency Response

Poles are associated with both resistors and capacitors

\[ V_X \approx \frac{g_m R_X}{1 + S R_X C_X} V_d \]

**IMPORTANT REMARKS !!!**

- DC-GAIN IS PROPORTIONAL TO R_X
- POLE FREQUENCY IS PROPORTIONAL TO 1/C_X R_X
- GAIN-BANDWIDTH PRODUCT (=gm/C_x) IS CONSTANT

TRADEOFF BETWEEN GAIN AND BANDWIDTH
**Issue** Find the best possible values for $W_n$, $L_n$, $W_p$, $L_p$, $I_B$, $W_b$, $L_b$

Main Specs: 7 unknowns, how many equations?

Fundamental equations: Example

- Small Signal Transconductance $> 1 \text{ mA/V}$
- $A_v > 100$
- $C_{Load} > 0.5 \text{ pF}$
- $GBW > 100 \text{ MHz}$
- Phase margin
- **Slew-rate** $> 0.25 \text{ V/10 nsecs}$
- Noise level $< 10 \mu \text{V} @ \text{BW}=10 \text{ MHz}$
- CMRR (*deals with the tail current*)
- Minimize power
- $V_{GSn}$, $V_{GSp}$ and Compliance voltage have limitations!

*Noise due to the tail current is not very relevant in this case!*
Design ➔ Find the best possible values for \( W_n, L_n, W_p, L_p, I_B, W_b, L_b \)

Direct equations: Example
- Small Signal Transconductance > 1 mA/V
- \( Av > 100 \)
- \( C_{Load} > 0.5 \, \text{pF} \)
- \( GBW > 100 \, \text{MHz} \)
- Phase margin
- Slew-rate > 0.25 V/10 nsecs
- Noise level < 10 \( \mu \text{V} \) @ BW=10 MHz
- CMRR (deals with the tail current)
- Minimize power
- \( V_{GSn}, V_{GSp} \) and Compliance voltage have limitations!

More equations than unknowns
Good design means ➔
• TO SATISFY ALL (or the most critical ones, tradeoffs) THESE CONSTRAINTS AT MINIMUM COST (POWER AND AREA)

Please do not arbitrarily assign values to any of the parameters!

• This is a typical multi-variable system
Design Example: **Check your operating point and parameters!**

* basic circuit

```
m1 v01 vin1 vs vss  nmos  l=2u      w=200u
+ as=300e-12 ad=300e-12 ps=150u  pd=150u
m2 v02 vin2 vs vss  nmos  l=2u      w=200u
+ as=300e-12 ad=300e-12 ps=150u  pd=150u
m3 v01 v01 vdd vdd  pmos  l=2u      w=200u
+ as=300e-12 ad=300e-12 ps=150u  pd=150u
m4 v02 v01 vdd vdd  pmos  l=2u      w=200u
+ as=300e-12 ad=300e-12 ps=150u
```

```
vtest   v02   0     0  dc
******************************************
* biasing
vd vdd  0    dc   1.5
vs vss  0    dc  -1.5
ib1 vs   0      dc  100u
******************************************
* input
vin1 vin1  0    ac
ein2 vin2  0    1    0    -1
******************************************
* analysis
.ac dec 10 1000 1e9
.print ac vdb(v01) i(vtest)
```

```
element  0:m1       0:m2       0:m3       0:m4
model    0:nmos     0:nmos     0:pmos     0:pmos
id       50.8791u   49.1209u   -50.8791u   -52.3328u
ibs      -1.3599f   -1.3599f    0.         0.
ibd      -6.0353f   -4.5000f   5.9294f    9.0000f
vgs      1.0467     1.0467    -988.2359m-988.2359m
vds      1.5585     1.0467    -988.2359m-988.2359m
vbs      -453.2843m-453.2843m  0.         0.
ib1 vs   3.1829u    3.6270u    3.1005u    2.6071u
gam eff  615.7505m  617.1949m  441.0793m  439.6443m
gm       917.2562u  898.5322u  530.5610u  542.4369u
gds      241.1968u  236.4976u  124.0201u  126.5817u
cdtot    168.5315f  174.6577f  190.8988f  197.1777f
cgtot    763.3385f  763.1155f  797.8187f  798.3587f
cstot    786.8845f  786.8845f  872.1273f  872.1273f
cbtot    253.8979f  261.0102f  304.0716f  292.1262f
cgs      660.5874f  660.5874f  707.1273f  707.1273f
cgd      71.8408f   71.2364f   71.2593f   71.9114f
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![Diagram](image-url)
Miller effect: Effects on the poles and the parasitic zero

For a grounded capacitor

\[ V_{out} = (1+A_V)v_2(sC_{GD1}) \]

Consider \( C_{GD1} \)

\[ i = (1+A_V)v_2(sC_{GD1}) \]

\[ i = v_2[s(1+A_V)C_{GD1}] \]

\[ \Rightarrow \text{Voltage drop across capacitor is } (1+A_V)v_2 \]

\[ \Rightarrow \text{Equivalent capacitor} = (1+A_V)C_{DG1} \text{ (Miller effect)} \]

\[ \Rightarrow \text{Same effect for } C_{DG2} \text{ (right hand transistor)} \]
Miller effect: Effects on system output impedance

Equivalent capacitor = $(1+A_V)C_{GD1}$

Large gain

$\rightarrow$ large equivalent capacitors

What is the result if you assume $A_V=+0.9$ or $A_V=+0.99$?

Impedance seen from the output

$\begin{align*}
    v_x &= \frac{C_1}{C_1 + C_2} v \\
    A_V v_x &= \frac{A_V C_1}{C_1 + C_2} v \\
    i_2 &= v + A_V v_x = \left(1 + \frac{A_V C_1}{C_1 + C_2} \right) \frac{r_{out}}{r_{out}} v \\
    Z_{out} &= \left(\frac{r_{out}}{1 + \beta A_V} \right) \left(\frac{1}{s \left(\frac{C_1 C_2}{C_1 + C_2}\right)}\right) \\
    Z_{out1} &= \frac{r_{out}}{1 + \frac{A_V C_1}{C_1 + C_2}} = \frac{r_{out}}{1 + \beta A_V} \\
\end{align*}$

$\beta A_V$ is the loop gain
Miller effect: Effects on the poles

CASCODE STRUCTURES

- Are these effects important for cascode structures??

- $V_y/Vin$ is mainly given by $-g_{m1}/g_{m11}$
  - low-gain amplifier
  - little sensitive to miller effects.

- For $C_{DG11}$, VB is a DC Voltage (AC ground) then this effect is not present.
CASCODE AMPLIFIER WITH CASCODE LOAD: simplified schematic!

Solve in class for $g_m$, $r_{out}$, and poles.

Effect of M5? Advantages and drawbacks?
High - Compliance Current Mirror

\[ M_1 = M_2 = M_3 = M_4 \; ; \; M_1 = 9M5 \Rightarrow I_{out} = I_{ref} \]

Can this topology work properly? Conditions?

Telescopica Amplifier
Small signal analysis: Common-source amplifier

\[ v_{in} + V_{GS} \]

\[ + \]

\[ V_{Y} \]

\[ V_{X} \]

\[ V_{out} \]

\[ I_{D1} \]

\[ I_{D} \]

\[ W \]

\[ 9L \]

\[ W \]

\[ L \]

\[ 1 \]

\[ 1 \]

\[ M1 \]

\[ M2 \]

\[ V_{B1} \]

\[ V_{SB2} \]

\[ V_{B2} \]

\[ V_{DSAT2} \]

\[ V_{T} \]

\[ I_{D1} + i_{d1} \]

\[ DC \] analysis:

\[ V_{SG2} = V_{T} + V_{DSAT2} \]

\[ V_{B2} = V_{T} + 3V_{DSAT2} \]

\[ V_{X} = V_{B2} - V_{SG2} = 2V_{DSAT2} \]

\[ V_{GS1} \] must be designed such that \( I_{D} = I_{D1} \)

\[ V_{B1} \] must be larger than \( V_{GS1} + V_{DSAT1} \) (\( V_{Y} > V_{DSAT1} \))

OUTPUT SWING IS LIMITED BY \( V_{X} \) AND \( V_{Y} \)

\( V_{Y} + V_{DSAT1} < V_{OUT} < V_{X} - V_{DSAT2} \)
Small signal analysis: Common-source amplifier

Telescopic Amplifier with large output swing

AC analysis: 2 POLES: AT $V_Y$ AND AT $V_{OUT}$

⇒ Non-dominant pole: $\approx g_{m1}/C_{PY}$

⇒ CPY=total capacitance at node $V_Y$

⇒ Dominant pole at $g_{OUT}/C_{OUT}$

⇒ $R_{OUT}=1/g_{OUT}=Reqn \parallel Reqp$

⇒ AC transconductance=$g_{m1}$

⇒ Noise components: M1 (driver), and transistors M2 (current mirror). And the cascode transistors???
Small signal analysis: Common-source amplifier

**Small signal circuit**

**AC analysis:**

POLE AT $V_Y$

- Non-dominant pole: \( \approx \)
- \( \omega_{PND} = (g_{m11} + g_{mb11})/C_{PY} \)
- Dominant pole at \( 1/ R_{OUT} C_{OUT} \)
- Transfer function

\[
\frac{v_{out}}{v_{in}} = \left( - \frac{g_{m1}}{g_{out}} \right) \left( 1 + \frac{1}{C_{out} g_{out}} \right) \left( 1 + \frac{1}{C_{PY} \left( g_{m11} + g_{mb11} \right)} \right)
\]
Small signal analysis: Noise level

In general $Z_{01} = R_{01} || 1/sC_{01}$

For $g_{m11}Z_{01} >> 1$

$$v_{eqin,11}^2 = \frac{1}{g_{ml}^2Z_{01}^2}v_{n,11}^2$$

For $g_{m11}Z_{01} << 1$

$$v_{eqin,11}^2 = \left(\frac{g_{m11}}{1 + g_{m11}Z_{01}}\right)^2v_{n,11}^2$$

Input referred Noise:

$$\frac{i_{d11}}{v_{n11}} = -\frac{g_{m11}}{1 + g_{m11}Z_{01}}$$
Main noise sources at low and medium frequencies: M1, and M2

M22 and M11 are cascode transistors

M2B is connected to the input of M22 (cascode)

\[
i_{\text{eq},m2}^2 = \frac{8kT}{3} g_{m2}, \quad v_{\text{eq},m2}^2 = \frac{8kT}{3} \frac{1}{g_{m2}}
\]

Input referred noise:

\[
v_{\text{eqin}}^2 = \frac{8kT}{3} \frac{1}{g_{m1}} \left( 1 + \frac{2g_{m2}}{g_{m1}} \right)
\]

If the load is \(C_L\), typical integrator, then the integrated noise level is:

\[
v_{\text{eqin}}(\text{RMS}) = \sqrt{\frac{8kT}{3} \frac{1}{g_{m1}} \left( 1 + \frac{2g_{m2}}{g_{m1}} \right) \sqrt{BW}}
\]

\[
v_{\text{eqin}}(\text{RMS}) \approx \sqrt{\frac{8kT}{3} \frac{1}{g_{m1}} \left( 1 + \frac{2g_{m2}}{g_{m1}} \right) \frac{g_{m1}}{2\pi C_L}}
\]

\[
v_{\text{eqin}} = \sqrt{\frac{8kT}{3(2\pi)} \frac{1}{C_L} \left[ 1 + \frac{2g_{m2}}{g_{m1}} \right]}
\]
Folded-Cascode OTA: $g_m$, $r_{out}$ and poles?

$V_{B1}$ and $V_{B2}$ must keep $M_1$
- $M_5$ in saturation region

$V_{B2} > V_{sat,4} + V_{GS3}$

$V_{B1} < V_{DD} - V_{sat,5} - V_{SG2}$

Notice that $ID5$ biases both $M2$ and $M1$

$$G_m = g_{m1}; \quad r_{out} \approx \left( \left( r_{ds\ 1} \parallel r_{ds\ 2} \right) g_{m\ 2} r_{ds\ 2} \right) \parallel \left( r_{ds\ 4} g_{m\ 3} r_{ds\ 3} \right)$$
Example: Folded-Cascode OPAMP

Find the gain and the phase from input to output and from input to node 2.

The low frequency gain is 77 dB and the unity gain frequency is around 80 MHz.

The behavior of the gain from the input to node 2 is interesting: above the dominant pole.
**IMPROVED OUTPUT STAGES: Super buffers!**

Performances improved by the use of negative feedback.

\[ i_x = (g_{m1} + g_{ds2})v_x + g_{m4}v_2 \]

\[ v_2 = g_{m1}r_{ds3}v_x \]

\[ R_{out} = \frac{1}{g_{m1}(1 + g_{m4}r_{ds3}) + g_{ds2}} \]
Class AB push-pull

Main concepts:

- Use two buffers in parallel
- P and V transistors must be biased (more complex)
- Output resistance decreases
- Overall transconductance increases (more accurate)
- Linear range?
- Power consumption?
- Noise?
Class AB push-pull with gain stage

Output resistance if CGS is ignored?

Output resistance at high frequencies where CGS can’t be ignored?

Overall transconductance?

Voltage gain?

Output linear range?

Properties of this circuit?
Level Shifters: Needed for signal coupling

- It behaves like a voltage source

\[ \Delta V = V_{DS} = \sqrt{\frac{2L}{kW}} I + V_{Th} \]

\[ \Delta V = V_{GSI} + V_{GS2} = V_{Th1} + V_{Th2} + \sqrt{\frac{2L}{kW}}_1 I_1 + \sqrt{\frac{2L}{kW}}_2 I_2 \]

a) Simple level shifter  b) Shunt feedback level shifter
Additional Examples: The First order filter

\[ v_0^2 = \frac{1}{1 + \omega^2 R^2 C^2} (4kTR) \]

\[ V_0(\text{RMS}) = \sqrt{(4kTR) \int_0^\infty \frac{1}{1 + \omega^2 R^2 C^2} df} = \sqrt{(4kTR) \frac{1}{4RC}} \]

\[ V_0(\text{RMS}) = \frac{kT}{\sqrt{C}} \]

**Extremely important result for SC based Circuits (Filters and ADC)**

Don’t get confuse: Noise is generated by the resistor!

Additional examples:
(see page 205, Johns-Martin)

Page 213 (Amplifier for optical communications)
Noise

Unwanted electrical signals generated in the device or externally and coupled to the output of the system.

Make impossible to detect, with sufficiently quality, signals with an amplitude comparable to the noise level.

Noise

Unwanted electrical signals generated in the device or externally and coupled to the output of the system.

Make impossible to detect, with sufficiently quality, signals with an amplitude comparable to the noise level.

Intrinsic

Thermal Noise

Flicker Noise

Extrinsic

Surrounding Circuitry
(PSRR, CMRR)
Thermal Noise in resistors

Due to the random flow of the carriers, thermal noise (undesired current variations) is produced due to:
- Collisions of carries with the crystal
- Collisions between carriers
- Fluctuations increase with temperature
- Random fluctuations

RMS value of these variations is quasi-uniformly spread up to several GHz

Usually noise is characterized by its Spot power noise (RMS power in bandwidth of 1 Hz) at a given frequency

\[ v_{n1}^2(f_x) = 4kTR_1 \]

\[ v_{n1}^2 = \int_{0}^{\infty} v_{n1}^2 \, df \]

This integral gives infinite total noise, but usually capacitors limit the bandwidth leading to a finite value.
• Lets compute the output voltage: **Apply superposition (noise sources are small signals, you can use small signal models)!**

\[
\begin{align*}
V_0 &= \left( \frac{R_2}{R_1 + R_2} \right) V_{\text{in}} + \left( \frac{R_2}{R_1 + R_2} \right) V_{n1} + \left( \frac{R_1}{R_1 + R_2} \right) V_{n2}
\end{align*}
\]

But noise is a random variable, power noise density have to be used rather than voltage; then the output referred noise density (noise in a bandwidth of 1 Hz) becomes

\[
\begin{align*}
V_{0n}^2 &= \left( \frac{R_2}{R_1 + R_2} \right)^2 V_{n1}^2 + \left( \frac{R_1}{R_1 + R_2} \right)^2 V_{n2}^2 \\
V_{0n}^2 &= \left( \frac{R_2}{R_1 + R_2} \right)^2 4kT R_1 + \left( \frac{R_1}{R_1 + R_2} \right)^2 4kT R_2
\end{align*}
\]
Thermal Noise in resistors

Thermal noise in resistors can be characterized in terms of voltage noise density or current noise density.

\[ v_{n1}^2 = 4kTR_1 \]

\[ i_{n1}^2 = \frac{4kT}{R_1} \]

Units

\[ v_{n1}^2 = \text{Volts}^2 / \text{Hz} \]

\[ i_{n1}^2 = \text{Amps}^2 / \text{Hz} \]

\[ v_{0n}^2 = \left| \frac{1}{1+sRC} \right|^2 \]

\[ v_n^2 = \frac{4kTR}{1 + (\omega RC)^2} \]

and, total noise power is computed as

\[ v_{\text{total}}^2 = \int_0^\infty \left( \frac{4kTR}{1 + (\omega RC)^2} \right) df = \frac{4kT}{C} \]
Noise is generated by R but integrated noise is function of C (??)

\[ v_{total}^2 = \int_0^\infty \left( \frac{1}{1 + (\omega RC)^2} \right) (4kTR) \, df = \frac{4kT}{C} \]

To get more insight, let's have a closer look on the operations!

Notice that:
When R increases thermal noise increases too but the corner frequency decreases, leading to a constant area under the curves!
Thermal Noise

=> Spectral Density of the thermal noise drain current (CMOS transistor biased @ linear region)

\[ i_d^2 = \frac{4kT}{R_{DS}} \]

\[ R_{DS} \approx \frac{1}{\mu C_{ox} \frac{W}{L}(V_{GS} - V_T - V_{DS})} \]
White Noise

@ Triode region

\[ i_d^2 = \left( \frac{4kT}{R_{DS}} \right) \left[ \frac{W}{L} \right] [V_{GS} - V_T - V_{DS}] \]

Low current noise => W/L ↓ => \( g_m \) or \( g_o \) ↓

@ Saturation

\[ g_o = \frac{1}{R_{DS}} \rightarrow \frac{2}{3} g_m \]

\[ i_d^2 = \frac{8}{3} kT g_m \]

\[ \Rightarrow i_d^2 = \left( \frac{8kT}{3} \right) (\mu C_{ox}) \left( \frac{W}{L} \right) (V_{GS} - V_T) \]
Flicker Noise \((1/f)\)

- Due to imperfections in the Si - SiO\(_2\) interface. The traps and imperfections interfere with the charges flowing through the channel.

- Strongly dependent of the technology

\[
\dot{i}_d^2 = \frac{k_F I_{DS}}{C_{ox} L^2 f}
\]

\(k_F\) = fitting parameter
\(f\) = frequency
\(I_{DS}\) = drain current
Output and input referred noise

Current noise is the real one

Thermal Noise
\[ i_d = g_m V_{gs} \]
\[ i_d^2 = g_m^2 V_{gs}^2 \]
\[ \Rightarrow V_{gseq}^2 = \frac{8}{3} \frac{kT}{g_m} \]

Voltage noise representation is an artifact to facilitate system analysis

Flicker Noise
\[ i_d^2 = \frac{k_F I_{DS}}{c_{ox} L^2 f} \]

Referred to the input
\[ v_{eq}^2 = \frac{k_F I_{DS}}{c_{ox} L^2 f g_m^2} \]
\[ v_{eq}^2 = \frac{k_F}{2\mu C_{ox}^2} \left( \frac{1}{WL} \right) \left( \frac{1}{f} \right) \]
Equivalent input referred noise voltage means that all current noise sources are accounted as drain current and represented by an “equivalent” noise voltage at transistor gate.

\[ V_{eq}^2 = \frac{i_{dth}^2 + i_{df}^2}{g_m^2} \]

\[ V_{eq}^2 = \frac{8kT}{3g_m} + \frac{k_F}{2\mu C_{ox}^2} \frac{1}{WL} \frac{1}{f} \]

\[ V_{eq_{total}}^{RMS} = \sqrt{\int_{BW} V_{eq}^2(f) df} \]
Typical noise spectrum

Corner frequency is obtained equating the expression for Flicker and Thermal noise and solving for $f_c$

Signal tones

$\frac{\text{signal}}{\text{noise + THD}} \rightarrow \frac{\text{power of the signal}}{\text{power noise + power THD}}$
NOISE COMPONENTS (values provided are for a 0.8 µm technology)

\[
\begin{align*}
\text{Noise density (V}^2/\text{Hz})
\quad v_{eq}^2 &= v_{th}^2 + v_{1/f}^2 \\
\quad v_{eq}^2 &= \frac{8}{3} \frac{kT}{g_m} \text{df} + \frac{K_F}{WLC_{OX}f} \text{df}
\end{align*}
\]

\[
\frac{K_F}{C_{OX}} = 9.8 \times 10^{-9} \text{V}^2 / \mu\text{m} - \text{Hz (NMOS)}
\]
\[
= 0.5 \times 10^{-9} \text{V}^2 / \mu\text{m} - \text{Hz (PMOS)}
\]

FOR LOW-FREQUENCY APPLICATIONS, WHEREIN 1/F NOISE IS DOMINANT, PMOS DEVICES MUST BE USED.
Output referred noise: Take advantage of SYMMETRIES!

Output referred current noise density

Superposition: Every transistor contributes; consider one at the time.

Analysis: You can use standard circuit analysis techniques but at the end of the day you have to consider POWER.

Output noise density: Each noise component represent the RMS value of random uncorrelated noise! Then add the power noise components

\[ i_{\text{out}}^2 = \frac{8}{3} kT g_{m1} \]
Output referred noise: Take advantage of SYMMETRIES!

Output referred current noise density due to the P-type devices:

Left hand side transistor:

\[ i_{\text{out}2}^2 \approx i_{d2}^2 = \frac{8}{3} kTg_{ml} \]

Right hand side transistor

\[ i_{\text{out}2}^2 = \frac{8}{3} kTg_{ml} \]

Noise injected into the common-source node equally splits into the two branches

Noise due to the current source is mainly common-mode noise
Output and input referred noise

Output referred current noise density

\[ i_{out}^2 = 2\left(\frac{8}{3} kT g_{m1}\right) + 2\left(\frac{8}{3} kT g_{m2}\right) \]

Input referred noise density (V^2/Hz)

\[ v_{in,eq}^2 = 2\left(\frac{8}{3} \frac{kT}{g_{ml}}\right) + 2\left(\frac{8}{3} \frac{kT}{g_{m1}} \frac{g_{m2}}{g_{m1}}\right) \]

In this case, noise due to the current source is mainly common-mode noise

Be careful because this is not always the case!
Integrated Input referred noise

Input referred thermal noise density ($V^2/Hz$)

$$v_{in,eq}^2 = 2\left(\frac{8}{3} \frac{kT}{g_{m1}}\right) + 2\left(\frac{8}{3} \frac{kT}{g_{m1}} \frac{g_{m2}}{g_{m1}}\right)$$

Input referred noise level (volts)

$$\text{Noise}(V_{RMS}) = \sqrt{\int_{BW} v_{in,eq}^2 df}$$

Example: for thermal noise, the noise level becomes

$$\text{Noise}(V_{RMS}) = \sqrt{\frac{16kT}{3} \frac{1}{g_{m1}} \sqrt{1 + \frac{g_{m2}}{g_{m1}}} (\sqrt{BW})}$$

I should advice you to use:

$$\text{Noise}(V_{RMS}) \approx \sqrt{\frac{8kT}{g_{m1}} \sqrt{1 + \frac{g_{m2}}{g_{m1}}} (\sqrt{BW})} \quad 4kT \approx 16 \times 10^{-21} \text{ coul.V}$$