Part II: Recent advances on Oversampled Analog-to-Digital Converters

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Outline

- State of the Art
- Fundamentals of Sigma-Delta Modulators
  - Noise and Signal Transfer Function
  - Error Function
  - Blockers tolerance
- System Limitations
  - Stability
  - Clock Jitter
  - DAC issues
  - Global Tuning
- Cases of Study
  - Sigma-Delta Modulator using TDC Techniques
  - Sigma-Delta Modulator employing Multi-phase approach
- Methodologies to improve ADC resolution
- Conclusions
- Recommended readings
Introduction: Connectivity

- Increasing number of wireless standards
- Support of multiple-standards on the same chip
- Advances in Integrated RF design towards universal devices
- Software Radio: easy addition of new standards
System issues in broadband systems:
High frequency filtering is especially critical in broadband applications
Rejection of Blockers: ADC filtering must be complemented by LP filtering
Neighbor channels are quite relevant even if heavy filtering is used

Trade-offs:
Light filtering in front demands an ADC with higher SNR and higher SDR
Higher SNDR-ADC implies more power and more circuit complexity
**State of the art**

![Graph showing power/frequency vs. signal-to-noise distortion ratio (SNDR) in decibels (dB).](image)

- **ISSCC 2010**
- **ISSCC 1997-2009**
- **VLSI 1997-2009**

**1.0E-01**  **1.0E+00**  **1.0E+01**  **1.0E+02**  **1.0E+03**  **1.0E+04**  **1.0E+05**  **1.0E+06**  **1.0E+07**

- **100mW @10MHz**
- **10mW @10MHz**

**SNDR (dB)**


**Challenge 1: Jitter Tolerance**
Challenge 2: Co-existence
Simultaneous Usage of Radio Bands

RF Interference: Frequency Overlap, Out-of-Band Emissions, Receiver Saturation

* Plot courtesy of Camille Chen/Intel
Roadmap for high-resolution Receivers: Paradigm

Slide courtesy of Prof. Yun Chiu

1. RF Filter → RF → Anti-Aliasing Filter → SCF, $G_mC$ OP-RC → A/D → DSP

2. RF Filter → RF → Anti-Aliasing Filter → A/D → Dig. Filter → DSP

3. RF Filter → LNA → A/D → Dig. Mod. → Dig. Filter → DSP

- How much RF processing should be done before the ADC?
- The front-end must be scalable and configurable to fit multiple standards.
- Better performance at higher frequency.
Impact of SNDR on ADC Power Consumption

- For 4MHz BW a 10dB increase in DR leads to ADC power increment of 50mW at 70dB or 1W at 90dB

- Required:
  Systematic evaluation of filter-ADC interdependence for broadband receivers
Conventional (Nyquist) ADC

SQNR = 6.02*n + 1.76
Basic concepts in $\Sigma\Delta$ Modulators

\[ STF = \frac{H(s)}{1 + H(s)} \]
\[ NTF = \frac{1}{1 + H(s)} \]
Fundamentals of Oversampled A/D Conversion

\[ Y(z) = E(z) \frac{1}{1 + \frac{1}{z - 1}} + X(z) \frac{1}{1 + \frac{1}{z - 1}} \]

Check the input-output trajectories
Original E(z) is shaped by NTF

\[ H_e(z) = 1 - Z^{-1} = 1 - e^{-j\omega T} = e^{-j\omega T/2} \left( e^{j\omega T/2} - e^{-j\omega T/2} \right) \]

\[ H_e(z) = e^{-j\omega T/2} \left( 2 j \sin \left( \frac{\omega T}{2} \right) \right) \]

\[ |H_e(z)| = 2 \sin \left( \frac{\omega T}{2} \right) \]

Original E(z) is amplified here!

\[ SQNR = \frac{|X(z)Z^{-1}|^2}{|E(z)H_e(z)|} \]

Spot SQNR
Oversampled A/D Conversion

Signal to Quantization Noise Ratio (SQNR)

- $N =$ number of bits
- $OSR = \frac{fs}{2fb}$
- SQNR improves by $30\text{dB}$ when OSR increases by 10
- Or $9\text{dB}$ SQNR improvement when doubling OSR

$$SQNR \approx 1.5 \left(2^N - 1\right)^2 \left(3 \cdot \frac{OSR^3}{\pi^2}\right)$$

$$SQNR \approx 1.76 + 6.02 \cdot N - 5.2 + 30 \cdot \log_{10}(OSR) \text{ dB}$$
System Design Considerations

\[ SQNR(dB) = 6.02N + 1.76 + (2L + 1)10 \log_{10} OSR - 10 \log_{10} \frac{\pi^{2L}}{2L + 1} \]

Dashed lines are for 2-bit quantizer
Dashed = Solid + 6.02

Filter order=2
Quantizer Bits=1

Filter order=3
Quantizer Bits=1

Filter order=4
Quantizer Bits=1

Filter order=5
Quantizer Bits=1
Design Considerations: 3\textsuperscript{rd} order loop

\[ SQNR(\text{dB}) = 6.02N + 1.76 + (2L + 1)10\log_{10} OSR - 10\log_{10} \frac{\pi^{2L}}{2L + 1} \]

\[ \text{ENOB} = \frac{\text{SNDR(\text{dB})} - 1.76}{6.02} \]
STF and NTF are definitely not enough to design a robust system; $a_1 \times a_2 = 1; b = 2$

$V(z) = z^{-2}U(z) + \left(1 - z^{-1}\right)^2 E_q(z)$

At the input of the first amplifier we have:

$U(z) - V(z) = \left\{1 - z^{-2}\right\}U(z) - \left(1 - z^{-1}\right)^2 E_q(z)$

At the output of the first integrator we have (saturation?)

$\frac{U(z) - V(z)}{1 - z^{-1}}a_1z^{-1} = \left\{1 + z^{-1}\right\}z^{-1}a_1U(z) - \left(1 - z^{-1}\right)z^{-1}a_1E_q(z)$

If $a_1 > 0.5$, hence the in-band output of the 1st integrator is $>$ than the input!
Sigma-Delta Modulators: Practical Design Issues
Eq stands for the quantization noise
Ed stands for DAC non-idealities (jitter + thermal noise)
Filter’s thermal noise is accounted in Eh

The modulator’s output becomes

\[ Y = STF \ast (X + E_d + E_h) + NTF \ast E_q \]

The error signal (Filter’s input) is

\[ STF = \frac{H(s) \ast ZOH(s)}{1 + H(s) \ast ZOH(s) \ast Z^{-1}} \]
\[ NTF = \frac{1}{1 + H(s) \ast ZOH(s) \ast Z^{-1}} \]
ZOH parameters are defined as

- The lowpass transfer function $H(s)$ provides large loop gain (Noise shaping)
  - DC gain $>>0$ dB
  - Enough phase margin at 0 dB gain
- $Z$ is a complex number (phase)
- Loop stability is fundamental

$$Z = e^{j\omega T_s}$$

$$|ZOH(z)| = \sin c\left(\frac{\omega T_s}{2}\right)$$

Magntitude of loop transfer function
Oversampled A/D Conversion: Effects of ZOH

$$Z^{-1} = e^{-j\omega T_s}$$

$$\text{Phase}(z) = -\omega T_s$$

➢ Notice that

$$|ZOH(f)| = \sin c\left(\pi \left(\frac{f}{f_s}\right)\right)$$
Oversampled A/D Conversion: Stability Issues

- \( L(f) \) is defined as the loop gain
- Phase of \( L(f) \) is quite important for stability
- \( Z \) is quite relevant for phase of \( L(f) \)

\[
\begin{align*}
    Z &= e^{j\omega T_s} = \cos(\omega T_s) + j \sin(\omega T_s) \\
    ZOH(z) &= T_s \cdot \text{sinc} \left( \frac{\omega T_s}{2} \right) \\
    L(f) &= H(z) \cdot ZOH(z) \cdot Z^{-1}
\end{align*}
\]

\[
\begin{align*}
    \text{STF} &= \frac{L(f) \cdot Z}{1 + L(f)} \\
    \text{NTF} &= \frac{1}{1 + L(f)}
\end{align*}
\]
Stability Issues: ΣΔ Modulators

- Check the phase contribution of the filter and the delay element!
- Check the phase of the loop at the unity gain frequency!
- Can’t stabilize the loop employing the conventional filter design approach
- Additional parasitic poles!

\[
\begin{align*}
STF &= \frac{L(f) \ast Z}{1 + L(f)} \\
NTF &= \frac{1}{1 + L(f)}
\end{align*}
\]
Stability Issues: $\Sigma\Delta$ Modulators

- Not very difficult to stabilize the loop if the unity gain frequency is below $\frac{F_s}{4}$! (not very Low OSR); e.g. around 100Mhz if clock frequency is 400MHz
- Notice that larger OSR allow you to reduce the filter gain at high-frequency
- Out-of-Band noise is distributed in wider bandwidth, hence smaller noise density but same integrated noise

- Hard to implement $H(s)$
- Split the filter in 2 parts
- Loop filter and fast path
Remarks on Filter’s operation: Filter’s input signal

- Inband signal is usually very small: Nice property
- Transition band is more critical for filter’s linearity (neighbor channels);
- Filter must be designed for the blockers
- Blocker tolerance is a major issue in broadband applications (LTE)
Typical Quantizer: Flash Architecture

- S/H operates at clock rate
- Huge input capacitance if N>6
  - Kick back noise
- Requires a precise low-impedance resistive ladder:
  - Power-accuracy-Speed tradeoff
- Limited by comparator
  - Speed and accuracy
  - Offset voltage
- Hard to improve its resolution

State of the art: ~ >2.4 GS/s 6 bits resolution
Kick-back noise and coupling capacitors

- Preamp delay is signal-dependent (Metastability)
- Power of the latch could excessive during the resetting phase (M9-ON)
- A major challenge: distributing clock signals across $2^N-1$ comparators with minimum clock skew (routing, PVT effects)
- Input capacitance could be excessive for multi-bit applications
ADC Non-idealities

- **Excess loop delay**: Constant delay between ideal and implemented DAC feedback pulse
  - Decision time required by quantizer affecting latches used for synchronizing DAC inputs
  - Finite response time of DAC to its clock and inputs
  - Filter’s delay is sensitive to PV variations
  - **Excess Loop Delay can be incorporated into**: $Z^{-1} \rightarrow Z^{-1-\Delta}$

- **Inter-symbol interference**: Finite slew rate of DAC outputs with unequal rise and fall times
  - Additional noise and tones fold into baseband

- **Clock jitter in DAC**

- **DAC and Filter Non-linearity**
Oversampled A/D Conversion

- Remarks on DAC non-idealities. Same analysis apply to the input referred filter’s noise

\[ Y_{DAC} = STF * E_d \]

\[ STF = \frac{H(s) * ZOH(s)}{1 + H(s) * ZOH(s) * Z^{-1}} \]

- DAC non-idealities are reflected at the ADC output similarly to the signal
- Baseband noise can be directly mapped to ADC input (\(E_d\) and \(E_h\))
- Non-linearities in DAC that translate HF noise into baseband affects directly SQNR
- DAC is a critical component
Binary-Weighted Current Steering DAC

- Current switching is simple and fast.
- INL and DNL depend on matching, not inherently monotonic.
- Thermometric arrays usually lead to better INL figures
- Large component spread ($2^{N-1}$:1)
This is a major research area in multi-bit sigma-delta modulators. Several alternatives have been reported; main trends are:

- Randomize the errors such that the non-linear errors are converted in noise instead of tones that degrades SNDR
  - Dynamic element matching techniques
  - Pseudo Randomizers such as Rotators
  - Digital signal processors
  - Drawbacks?

- Calibration
  - Usage of large overdrive voltages and large dimensions
  - Pre-calibration of current cells
  - Other options?
Dynamic Element Matching: Simplified scheme

Representing DAC input using a thermometer DAC

- **Data-out= 1** can be represented by any one of $I_{1-8}$
- Averaging all possible combinations produces the ideal output
- Use different combinations to represent a given code
- Errors are randomized, and do not generate harmonics but noise
Implementation of DEM Scheme

- Shifter performs a Rotate-right shift on its inputs
- PN-sequence generator indicates number of shifts
- DEM is operated at higher frequency to minimize its delay
  - Routing and extra cells increase the bill of silicon and power
  - Excessive delay for high frequency applications
  - Noise level increases
A 14 Bit Continuous-Time Delta-Sigma A/D Modulator With 2.5 MHz Signal Bandwidth

Zhimin Li and Terri S. Fiez, Fellow, IEEE

Fig. 5. Output spectrum of the CT modulator for –3 dBFS input.
Analog Self-Calibration of Current Sources


- A reference current source is used
- At the end of a calibration cycle, $C_{\text{CAL}}$ attains the correct $V_{\text{GS}}$ required to generate $I_{\text{ref}}$
Analog Current Calibration Realization

Calibration reference: Shared by all Current Cells

Unit Current Cell
Simulation Results: DEM increases noise level

We found that Calibration (Digital Memory) looks better for wideband applications, but..

OFFLINE!

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<th>Calibration</th>
<th>SNR (dB)</th>
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Clock Jitter Sensitivity (SJNR)

- The main effects of clock jitter is present at the input of the quantizer and DAC.
- Jitter induced noise at DAC output is processed according to the STF, which is a serious problem for continuous-time sigma-delta modulators.
- Clock Jitter in quantizer is not very relevant: processed by NTF.
- Clock jitter introduce uncertainty at the DAC output (jitter induced noise) processed by STF.
Review and advances in delta-sigma DAC error estimation based on additive noise modelling

Ivar Løkken · Anders Vinje · Bjørnar Hernes · Trond

\[ e_{\text{jitter}}(t) = \sum_{n=0}^{N-1} \left[ y_a(nT) - y_a((n-1)T) \cdot \frac{1}{T} \prod_{j(nT)} \left( nT + \frac{j(nT)}{2} \right) \right] \cdot \text{sign}(j(nT)) \]  

Considering a single error pulse on this form, for simplicity denoting its amplitude \( A \) and width \( J \), taking the Fourier transform gives the spectrum:

\[ E_J(f) = \int_{t=0}^{t=J} A \cdot e^{-i2\pi f t} \bigg|_{J \geq 0} = - \int_{t=0}^{t=J} A \cdot e^{-i2\pi f t} \bigg|_{J < 0} = \frac{A \cdot \sin(2\pi Jf)}{2\pi f} \cdot e^{-i\pi Jf} \]

\[ = A \cdot J \cdot \sin c(Jf) \cdot e^{-i\pi Jf}. \]
Jitter Insensitivity of Switched-Capacitor DACs

So far, SC-DAC is the most jitter tolerant approach
• Quite precise and may not require further calibration procedures

**Drawbacks of the SC DAC**
• Peak current in the SC-DAC can be as high as 5 times IDAC used in the current mode DAC!
• Very demanding SR and GBW for the OPAMP: Power consumption; RC discharge is a good trade-off for medium speed architectures!
• Class AB OPAMP may help while dealing with this issue
Phase Modulation: wide frequency spectrum

Phase Modulation:

\[
\cos(\omega_o t + \varphi_n)
\]

\[
\left( \frac{\Delta T}{T} \right)^2 = \left( \frac{\varphi_n}{2\pi} \right)^2
\]

Then

\[
RMS\ J_{\text{per}} = \left( \frac{T}{2\pi} \right) \sqrt{\int_{-\infty}^{\infty} \phi_n^2(f) df}
\]

RMS value of total jitter

\[
RMS\ J_{\text{per}} = \left( \frac{T}{2\pi} \right) \sqrt{2 \int_{0}^{\infty} (L(f)) df}
\]

Typical phase noise measured in the spectrum analyzer

Clock Jitter Sensitivity (SJNR)
The DAC error due to clock jitter:

\[ E_j(n) = (D_{out}(n) - D_{out}(n-1)) \left( \frac{\Delta T(t)}{T} \right) \]

In the frequency domain: Differential of Dout convolves with \( J_n(\omega) \)

\[ E_j(\omega) = \left[ (1 - Z^{-1})D_{out}(\omega) \right] \otimes J_n(\omega) = \left[ 2 \sin \left( \frac{\omega T_s}{2} \right) \right] D_{out}(\omega) \otimes J_n(\omega) \]

In-band signal is shaped by \( 1 - Z^{-1} \), then it is not very critical

Out-of-Band quantization noise and blockers convolve with the clock jitter.
Effect of clock jitter and Quantization noise on SNR

\[ e_j(n) = (V_{out}(n) - V_{out}(n-1)) \frac{\Delta t(n)}{T} \]

then
\[ E_j(Z) = \left\{ (1 - Z^{-1})(V_{out}(Z)) \right\} \otimes (J(Z)) \]

Or
\[ E_j(Z) = \left\{ (1 - Z^{-1})(STF(Z) * V_{in}(Z) + NTF(Z) V_q(Z)) \right\} \otimes (J(Z)) \]

Therefore
\[ E_j(Z) = \left\{ (1 - Z^{-1})STF * V_{in}(Z) \right\} \otimes J(Z) + \left\{ (1 - Z^{-1})NTF * V_q(Z) \right\} \otimes (J(Z)) \]

\[ \left| 1 - Z^{-1} \right| = 2 \sin \left( \frac{\omega T_s}{2} \right) \]

\[ P_{j,S} \approx 2 \int_0^{1/2OSR} \left| E_j(\omega) \right|^2 d\theta \]

\[ P_{j,Q} \approx 2 \int_0^{1/2OSR} \left| \left\{ (1 - Z^{-1})NTF(\omega)V_q(\omega) \right\} \otimes (J(\omega)) \right|^2 d\theta \]

SJNR is function of the convolution of NTF and J(Z)

Quantization noise

Clock Noise Density
Continuous-Time BP-ΣΔ ADC: Jitter effects

\[ SJNR_{NRZ} \approx 60 \text{ dB} \Rightarrow \left( \frac{\text{OSR} \cdot P_{in}}{4} \right) \left( \frac{T_s}{\sigma_j} \right)^2 > 10^6 \]

\[ \sigma_j \approx < 10^{-3} T_s \]

In absence of blockers, assuming white jitter spectrum, the jitter induced noise has been usually approximated as:

\[ SJNR_{NRZ} \approx 10 \log_{10} \left( \frac{P_{in}}{\int_{BW} J_n \otimes (1 - Z^{-1}) V_{Quantization}^2 \, df} \right) = 10 \log_{10} \left( \frac{\text{OSR} \cdot P_{in} \cdot \text{sinc}^2 \left( \frac{\omega \cdot T_s}{2} \right)}{4 \left( \frac{\sigma_j}{T_s} \right)^2} \right) \]
RF clock filtering is an method to partially overcome this issue!

- High frequency blockers convolve with Jn and are folded back in band.

- Considering 
  \[ P_{\text{blocker}} \text{ and } P_{\text{quantization}} \]

\[
SJNR \approx 10 \log_{10} \left( \frac{P_{\text{in}}}{\int_{BW} \left( |J_n \otimes (1 - Z^{-1})V_{\text{Quantization}}|^2 + |J_n \otimes (1 - Z^{-1})V_{\text{Blocker}}|^2 \right) df} \right)
\]

\[
= SJNR_{\text{no Blocker}} - 10 \log_{10} \left( 1 + \frac{\int_{BW} \left( |J_n \otimes (1 - Z^{-1})V_{\text{Blocker}}|^2 \right) df}{\int_{BW} \left( |J_n \otimes (1 - Z^{-1})V_{\text{Quantization}}|^2 \right) df} \right)
\]
Jitter tone around $F_s$ convolve with images of inband signal and produce in-band noise tones.

- Jitter and blocker convolves, producing in-band noise tones.
- Jitter also convolves with OOB quantization noise and downconverts into in-band noise.
Another Major Issue: Loop Saturation

Signal Bandwidth: 20MHz
Oversampling Ratio: 10
Order: 5
No. of Quantizer levels: 9
Peak SQNR: 80dB
Max. NTF Gain: 10dB
Max. Stable Input Amplitude: -3dBFS

Feed-forward and feedback architectures

Internal gain: BP1, BP2 and LP1 are critical nodes
“Blocker and Jitter Tolerant Wideband ΣΔ Modulators” Silva-Karşılayan-Geddada, MWCAS-12

Transient response of the ADC to the 8.7dBFS blocker at 100MHz in the presence of a -6dBFS in-band signal at 5MHz

Effectiveness of the saturation detector: Output spectrum of the ADC with and without the -9dBFS blocker at 40MHz
System-level Optimization

- Order of modulator (L), and OSR set by target SQNR (~80dB) and settling time requirements on 1st integrator stage
  
  \[ L = 5, \text{ OSR} = 10 \]

- Order of modulator (L), and OSR set by target SQNR (~80dB)
  
  \[ L = 5, \text{ OSR} = 10 \]

- A number of tradeoffs involved

- Just picking values is not a good approach

- EDUCATED GUESS!

Order of modulator (L), and OSR set by target SQNR (~80dB)

\[ L = 5, \text{ OSR} = 10 \]

A number of tradeoffs involved

Just picking values is not a good approach

EDUCATED GUESS!
System-level Optimization

- Order of modulator ($L$), and OSR set by target SQNR (~80dB)

- High-Q filters give you better SQNR (due to picking in the gain; better in-band noise)

- Implications on filter’s signal swing and out-of-band noise?
System-level Optimization

- Maximum Signal Amplitude Increase with number of levels and with small NTF values

- Signal at internal nodes could limited even more MSA

- This is a multi-dimensional problem: several tradeoffs involved
System Optimization: Tuning Filter Parameters

Effect of PVT Variations

Filter Tuning; reconfiguration or Master slave techniques could be used

- Calibration of (standalone) building blocks:
  - Does not guarantee loop stability (excess loop delay)
  - Does not guarantee best NTF (Coefficient adjustments)
System Optimization: Global Tuning Scheme

- Linear model used to find NTF
- Model used to calibrate NTF
- Loop response to calibration tones is analyzed in digital domain

Global Tuning Scheme for NTF Parameters: Digital

A set of strategic tones are used to optimize:
- Loop Stability
- Best NTF
- Bandwidth
Digitally assisted calibration scheme

ADC Calibration: Experimental results

![Graphs showing output spectrum vs frequency for ADC calibration](image-url)
Strategy for nanometric technologies

- Make use of time domain signal representation
- Small supply voltage limits the dynamic range of analog signals
- Fast switching gates provide fine time precision, which provide alternate means for high DR signal representation
- Also takes advantage of $CV^2f$

Time domain signal representation

A 20MHz Signal Bandwidth 68dB Dynamic Range Continuous Time $\Delta\Sigma$ ADC Based On Multi-bit Time Domain Quantizer and Feedback Element, V. Dhanasekaran, et.al. ISSCC-2009; JSSC March 2011
Proposed ADC Architecture

- Multi-level quantizer and Digital to Analog Converter (DAC) are replaced by PWM generator and Time to Digital Converter (TDC)
- Width of \( p(t) \) is proportional to the amplitude of the signal in a given clock period
- Output code (Dout) represents “quantized pulse” edges with a quantization step size = \( T_Q \)
PWM Generator

- PWM signal generated by standard method - comparing signal with triangle waveform
- Double-sampled or "asymmetric sampled" PWM is used to minimize distortion and improve OSR
- Performance is relaxed due to noise shaping
**TDC Functionality**

- **Time-to-Digital Converter**
  - Converts pulse timing information to digital codes (Drout & Dfout)
  - Drout & Dfout can be used to reconstruct signal in clocked digital domain
  - Also generates a feedback pulse aligned to the timing edges represented by the dotted lines
Digital output code
- CT PWM output $p(t)$ is latched by delayed versions of the clock
- Flipflop outputs provide “thermometer” coded pulse width
- D input of the flipflops are driven by $p(t)$ to facilitate easy generation of f/b pulse

Feedback pulse - $pq(t)$
- Must match output code
- Edges of $pq(t)$ are always aligned to the delayed clock edges
Time quantized pulse generator

- Pq(t) can be generated using a OR gates and SR latch
- Pq(t) turns ‘High’ when the earliest of CK0-3 goes High after p(t) is High
- Pq(t) turns ‘Low’ when the earliest of CK4-7 goes High after p(t) is Low

- Wired-NOR/NAND gate can be used to ensure uniform delay
- 50 levels of time steps are used in the proposed design for 20MHz ADC
- Clock phases are generated using cascade of delay elements that are tuned using a phase detector
Active-RC Topology Loop Filter

The gain of the filter in the signal bandwidth (20MHz) serves to suppress the quantization noise of the TDC.

The filter has a minimum inband gain of 37dB.

Noise Transfer Function (NTF)

\[ H(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{7.312s^2 + 2.312\times10^7s + 4.223\times10^5}{s(s^2 + 1.414\times10^7s + 1.279\times10^6)} \]
Mitigating Excess loop delay

KFB provides a ‘fast path’ through INT3 => Make AMP3 a minimum phase structure
Two Stage ‘Typical’ configuration

- maximizes gain of the initial stages => Better Q control
- Output pole ~ 4*GBW
- Overall noise limited by input devices
- Rf reduces (degenerate) noise due to NMOS current mirrors

Limitations:
- Parasitic poles result in additional loop delay/excess phase in the filter (could be > 10 deg at 500MHz)
- Limits loop stability and affects the overall performance
Simplified schematic: Amplifier 3

- A simple single stage pseudo-differential ‘inverter based’ amplifier
- Complementary structure with class A-B action
- CM noise (supply etc) is suppressed by biquad gain of 18dB

Limitations:
- Bias point not accurately controlled + % variation across statistical corner & Temp
- Need for ‘Non-conventional’ common-mode control
Amplifier 3 Common Mode control

- Current sources at virtual ground control amplifier’s common mode
- $I_{cm}$ are: small current source, sized to meet transconductance and noise specifications
Chip Micrograph

- Folded layout to minimize delay in feedback
- Digital approach minimizes area requirement
- Occupies 0.15mm²
Output Spectrum: -5dB Input

- Output spectrum for -5dB 4MHz input signal

- SNR=62dB
- THD=65dB
Dynamic Range and SNDR

- DR = 68dB
- Peak SNDR=60dB @ -5dB input
- Peak THD=67dB @ -6dB input
- FoM = 319 fJ/step

Dynamic Range (DR) is defined as the amplitude range with SNR>0dB
The PWM spectrum consists of tones at

- Signal frequency ($\omega_S$) and its odd harmonics,
- Reference tones due to the ramp’s fundamental frequency ($\omega_R$) and its harmonics,
- Intermodulation products of the signal and the reference tones.

\[
v_p(t) = \frac{2V_a}{\pi} \sum_{n=1}^{\infty} \frac{1}{n \frac{\omega_S}{\omega_R}} J_n \left( n \frac{\omega_S}{\omega_R} \frac{\pi}{2} M \right) \sin \left( n \frac{\pi}{2} \right) \cos(n\omega_S t) + \frac{2V_a}{\pi} \sum_{m=1}^{\infty} \frac{1}{m} J_o \left( m \frac{\pi}{2} M \right) \sin \left( m \frac{\pi}{2} \right) \cos(m\omega_R t) + \frac{2V_a}{\pi} \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} J_n \left( \left[ m + n \frac{\omega_S}{\omega_R} \right] \frac{\pi}{2} M \right) \sin \left( \left[ m + n \right] \frac{\pi}{2} \right) \cos(m\omega_R t + n\omega_S t)
\]
Second ADC:
System Architecture: Injection Locking

- 5\textsuperscript{th}-order 3-bit feedforward architecture
- Local feedback is to compensate the excess loop delay
- LC-VCO+CILFD are used to generate clean reference clocks

“25MHz Bandwidth (BW) Continuous-Time Lowpass $\Sigma\Delta$ Modulator with Time-Domain 3-bit Quantizer and DAC” Cho-Ying Lu, et.al., Sept 2010, JSSC
Biquadratic Filter and Amplifier

Two stage amplifier with feedforward compensation

First stage
- No extra CMFB needed

Second stage
- (current re-use)

Large resistors are used

Feed-forward stage

Quiescent current \(\sim 1.0\) mA

GBW > 800MHz
Very linear OPAMP for >100MHz applications

C.-Y. Lu, “A 6th-order 200MHz IF Bandpass Sigma-Delta Modulator With over 68dB SNDR in 10MHz Bandwidth,” JSSC, June 2010
Wide-band Adder with delay compensation

The load resistor is split into 2 pieces and one section replaced by an RC T-network.

\[ R_{feedback} = R_a \parallel (R_b + R_c) \text{ at low frequencies} \]
\[ R_{feedback} = R_a \text{ at low frequencies} \]

\[ \theta(\omega) = \tan^{-1}\left(\frac{\omega}{\omega_z}\right) - \tan^{-1}\left(\frac{\omega}{\omega_p}\right) \]

\[ \tau_{delay} = \frac{d\theta(\omega)}{d\omega} = -\frac{(\omega_z - \omega_p)(\omega^2 - \omega_z \omega_p)}{(\omega^2 + \omega_z^2)(\omega^2 + \omega_p^2)} \]
Pulse Amplitude Modulation

- Traditional Multi-level Digital Signal

Unit element current mismatch generates DAC non-linearity.

\[ Q_{\text{inj}} = (\alpha I)T_s \]

where:

\[ \alpha = [0, \frac{1}{7}, \frac{2}{7}, \ldots, 1] \]
Time-Domain Pulse Width Modulation

- Only inherently linear 1-level DAC achieve multi-bit feedback

- PWM scheme employing multi-phase controller

\[ Q_{inj} = I(\alpha T_s) \]

where:

\[ \alpha = [0, \frac{1}{7}, \frac{2}{7}, \ldots, 1] \]
Systematic (Nonlinearity) errors

- Error Charge from Device Mismatch

### Conventional Multi-Level DAC

\[ Q_{\text{err}} = N \cdot \left( \frac{\Delta I}{I} \right) IT_s \]

Current errors accumulate

### 1-level PWM DAC

\[ Q_{\text{err}} = 2 \cdot \left( \frac{\Delta T}{T} \right) IT_s \]

Timing errors at the pulse edges
INL, DNL and Linearity

- Robustness to device mismatch
  - only affect the edges of the pulse

\[ \delta_\%_I = \frac{\Delta I}{I} = 0.5\% \]
\[ \delta_\%_T = \frac{\Delta T}{T} = 0.16\% \]

\[ \frac{HD_3^{PWM}}{HD_3^{conventional}} \approx \left( \sqrt{\frac{2}{7}} \right) \left( \frac{\delta_\%_T = 0.16\%}{\delta_\%_I = 0.5\%} \right) \]

PWM Linearity could be >10dB better!
Time-Domain Pulse Width Modulation

- Pulse Arrangement
  - To ease the design of interface circuitry between quantizer and level-to-PWM converter

\[ SJNR_{peak} = 10 \log_{10} \left( \frac{T_s^2 \cdot OSR}{2 \cdot \sigma_y^2 \cdot \sigma_\beta^2} \right) \]
Phase noise of VCO is -119dBc/Hz @ 1MHz

CILFD phase noise is -136dBc/Hz @ 1MHz

Jitter among phases is highly correlated
3-bit Algorithmic Quantizer

- The output is composed by **1 MSB + 3LSB**
- The MSB is determined first

- **The output is composed by 1 MSB + 3LSB**
- **The MSB is determined first**

![Diagram](image_url)
Proposed Level-to-PWM Converter

- SR latches generate the pulses
  - AND gates + OR gates decide the required pulses
  - Programmable Delay is used to minimize

5-Input OR Gate

Programmable Delay

to 1-Bit PWM DAC
Chip Microphotograph & Clock Phase Noise
Fabricated in Jazz Semiconductor, 180nm technology

Loop Filter + Summing Amplifier
3-Bit Two-Step Quantizer
VCO & Complementary Injection-Locked Frequency Divider
Level-to-PWM Converter
Buffers
DAC1 & DAC2

Core area = 2.6mm²

RMS jitter = 0.27ps
=> SJNR > 75dB
Output Spectrum of the Modulator

-2.2dBFS @ 5.08MHz

- Peak SNR = 68.5dB @ 25MHz BW
- Peak SNDR = 67.7dB @ 25MHz BW
- SFDR > 70dB
Signal to Distortion Ratio

- Two tones with 2MHz apart and -2dBFS overall power

\[
\text{IM}_3 = -76.3\text{dB}
\]
Can we do better? Fundamentals on MASH architectures

Quite relevant topology:
Quantization noise $E_1$ gets cancelled

Notice that the auxiliary ADC processes the quantization error $E_1$

What about Eq2?

$$Y(z) = H_3(z)Y_1 - H_4(z)V_2$$

$$Y_1(z) = STF_1(z)X + NTF_1(z)E_{q_1}$$

$$Y_2(z) = STF_2(z)E_{q_1} + NTF_2(z)E_{q_2}$$

Then

$$Y(z) = H_3 \{STF_1 * X + NTF_1 * E_{q_1}\} - H_4 \{STF_2 * E_{q_1} + NTF_2 * E_{q_2}\}$$

$$Y(z) = \{H_3 * STF_1\}X + \{H_3 * NTF_1 - H_4 * STF_2\}E_{q_1} - \{H_4 * NTF_2\}E_{q_2}$$

Leslie and Singh
ISCAS-1990
Fundamentals on MASH architectures

Analog Intensive MASH topology

If \( H_3 \ast NTF_1 - H_4 \ast STF_2 = 0 \)

Then

\[ Y(z) = \{ H_3 \ast STF_1 \} X - \{ H_4 \ast NTF_2 \} E_{q2} \]

\[ SQNR = \left( \frac{E_{q1}}{E_{q2}} \right)^2 \left( \frac{STF_2}{NTF_2} \right)^2 \left( \frac{STF_1 \ast X}{NTF_1 \ast E_{q1}} \right)^2 \]
Fundamentals on MASH architectures

Analog Intensive Pseudo-MASH topology

Todd Brooks, et. al., JSSC, Dec 1997
Efficient Pseudo-MASH architecture
Target: SNDR Improvement by 3 bits

- SQNR improvement should be around 18dB (3 bits)
- Power overhead, area overhead < 20%

SNR = 79.516dB
SNR = 105.803dB
Conclusions

- Minimization of filtering functions in the receiver chain demands innovative ADC solutions;
- SNDR > 80 dB will be frequently needed in wireless applications;
- Jitter and Blocker tolerant architectures are needed;
- DAC calibration techniques for fast and high-resolution applications;
- Global tuning strategies (for stability)
- Advanced LTE applications require high-resolution for signal BW as high as 200MHz
Recommended Readings


*Other tutorials: IECE-2012*
A Continuous-Time $\Sigma\Delta$ ADC With Increased Immunity to Interferers

Kathleen Philips, Member, IEEE, Peter A. C. M. Nuijten, Raf L. J. Roovers, Member, IEEE, Arthur H. M. van Roermund, Senior Member, IEEE, Fernando Muñoz Chavero, Macarena Tejero Pallarés, and Antonio Torralba, Senior Member, IEEE.
A 20-mW 640-MHz CMOS Continuous-Time ∑Δ ADC With 20-MHz Signal Bandwidth, 80-dB Dynamic Range and 12-bit ENOB

Gerhard Mitteregger, Member, IEEE, Christian Ebner, Member, IEEE, Stephan Mechnig, Member, IEEE, Thomas Blon, Member, IEEE, Christophe Holuigue, and Ernesto Romani, Member, IEEE
Fig. 10. Four-bit quantizer with 4-bit flash ADC and reference voltage generation plus feedback DAC.

<table>
<thead>
<tr>
<th>TABLE I</th>
<th>PERFORMANCE SUMMARY</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sampling Frequency</td>
<td>640MHz</td>
</tr>
<tr>
<td>Conversion Rate</td>
<td>40MS/s</td>
</tr>
<tr>
<td>Input Range</td>
<td>0-20MHz</td>
</tr>
<tr>
<td>Peak SNR</td>
<td>76dB</td>
</tr>
<tr>
<td>THD</td>
<td>-78dB</td>
</tr>
<tr>
<td>Peak SNDR</td>
<td>74dB</td>
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<tr>
<td>ENOB</td>
<td>12</td>
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<tr>
<td>Process</td>
<td>1.2V 130nm 1P8M CMOS</td>
</tr>
<tr>
<td>Chip Area</td>
<td>8.6mm²</td>
</tr>
<tr>
<td>Power</td>
<td></td>
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<tr>
<td>Modulator</td>
<td>20mW</td>
</tr>
<tr>
<td>Decimator 40MS/s</td>
<td>18mW</td>
</tr>
<tr>
<td>PLL 2.56GHz</td>
<td>12mW</td>
</tr>
<tr>
<td>I/O 1.8V</td>
<td>4mW</td>
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</table>
A 3-mW 74-dB SNR 2-MHz Continuous-Time Delta-Sigma ADC With a Tracking ADC Quantizer in 0.13-μm CMOS

Lukas Dörrer, Franz Kuttner, Patrizia Greco, Patrick Torta, and Thomas Hartig

third-order 4-bit ΔΣ architecture.
The DEM is usually slow and may lead to significant loop delay!

May require loop compensation

Nice feature: Robust against blockers!
A 12-Bit, 10-MHz Bandwidth, Continuous-Time $\Sigma\Delta$ ADC With a 5-Bit, 950-MS/s VCO-Based Quantizer

Matthew Z. Straayer, Student Member, IEEE, and Michael H. Perrott, Member, IEEE
**TABLE II**

**COMPARISON WITH PUBLISHED HIGH-SPEED CT ADCS**

<table>
<thead>
<tr>
<th>Ref.</th>
<th>$F_S$ (MHz)</th>
<th>BW (MHz)</th>
<th>SNR (dB)</th>
<th>SNDR (dB)</th>
<th>Power (mW)</th>
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</thead>
<tbody>
<tr>
<td>[12]</td>
<td>276</td>
<td>23</td>
<td>70</td>
<td>69</td>
<td>43</td>
</tr>
<tr>
<td>[13]</td>
<td>340</td>
<td>20</td>
<td>71</td>
<td>69</td>
<td>56</td>
</tr>
<tr>
<td>[14]</td>
<td>400</td>
<td>12</td>
<td>64</td>
<td>61</td>
<td>70</td>
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<tr>
<td>[16]</td>
<td>640</td>
<td>20</td>
<td>76</td>
<td>74</td>
<td>20</td>
</tr>
<tr>
<td>[17]</td>
<td>1000</td>
<td>8</td>
<td>63</td>
<td>63</td>
<td>10</td>
</tr>
<tr>
<td>This work</td>
<td>950</td>
<td>10</td>
<td>86</td>
<td>72</td>
<td>40</td>
</tr>
</tbody>
</table>
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9.6 A 1.2V 2MHz BW 0.084mm² CT ΔΣ ADC with -97.7dBc THD and 80dB DR Using Low-latency DEM

Sheng-Jui Huang, Yung-Yu Lin

DEM is effectively moved outside the loop, and evolves to a simple counter
• $R_{\text{off}} C_{\text{off}} > 0.1 \, \text{T}$
16.4 A Mostly Digital Variable-Rate Continuous-Time ADC

ΔΣ Modulator

Gerry Taylor\textsuperscript{1,2}, Ian Galton\textsuperscript{1}
A Continuous Time $\Delta\Sigma$ ADC for Voice Coding with 92dB DR in 45nm CMOS

Lukas D"orrer, Franz Kuttner, Andreas Santner, Claus Kropf, Thomas Puaschitz, Thomas Hartig, Manfred Punzenberger