A 10.7-MHz 68-dB SNR CMOS Continuous-Time Filter with On-Chip Automatic Tuning

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Abstract—A maximally flat 10.7-MHz fourth-order bandpass filter with on-chip automatic tuning system is presented. The signal-to-in-band integrated noise ratio (SNR) of the automatically tuned filter is around 68 dB. The third intermodulation distortion (IM3) is lower than $-40$ dB for a two-tone input signal of 3.2 V peak to peak ($V_{pp}$). The complete system operates with supply voltages of ±2.5 V. The power consumption of the system is 220 mW. All this has been achieved due to the use of a low-distortion transconductor, the development of a high-frequency CMOS resistor, and the realization of an advanced on-chip automatic tuning system for both frequency and bandwidth control. The chip has been fabricated in a standard 1.5-μm n-well CMOS process.

I. INTRODUCTION

THE integration in CMOS technologies of filters in the megahertz range is very attractive for video, IF, and other applications. During the last few years, several high-frequency CMOS and bipolar integrated filters have been reported [1]-[9]. Although high-frequency filters have been integrated, these realizations present a relatively small dynamic range. Recently, a 4-MHz low-pass filter performing 61-dB dynamic range has been reported [4]. However, this is a low quality factor ($Q$) realization. For narrow-band filters, the design is more complex because both small and large time constants have to be used in the filter. For these applications, only a few realizations have been reported [3], [5], [7]-[9]. Moreover, the dynamic range of these filters is limited, e.g., less than 50 dB.

In this paper, a maximally flat 10.7-MHz fourth-order CMOS bandpass filter with on-chip automatic tuning system is described. The bandwidth and the ripple of the filter are 300 kHz and 0.5 dB, respectively. The $Q$ of the biquadratic sections is 20. The supply voltages are only ±2.5 V. The third intermodulation distortion (IM3) of the fully differential topology is lower than $-40$ dB for a two-tone input signal up to 3.2 V peak to peak ($V_{pp}$). The signal-to-noise ratio of the filter is in the order of 68 dB while IM3 < $-40$ dB. The center frequency of the filter is controlled with an accuracy of ±1%. The accuracy of the filter bandwidth is within 30%.

The fully differential filter is implemented using the so-called operational transconductance amplifier-Resistor-Capacitor (OTA-RC) technique. For the reduction of the harmonic distortion components, the OTA's use a linearized input stage [6]. The floating resistor is implemented by using the output conductance of the transistor. The large tuning range of the resistor allows one to compensate the excess phase shift effects of the OTA's over a very wide range. For the automatic tuning of the filter, two nonlinked loops, one for the poles frequency ($\omega_0$) and another one for the filter bandwidth ($BW$), are employed. The frequency controller adjusts the transconductance of the OTA's through their bias currents. This controller is based on a new charge comparison principle. In this technique, $\omega_0$ is tracked to an external clock frequency times a ratio of two dc current sources. The ratio of the dc current sources allows one to scale down (or up) the operating frequency of the control loop. For this design, the frequency controller employs a 450-kHz clock frequency. The $BW$ controller tunes the CMOS resistors. For the detection of the filter quality factor, information from the transient response of a biquadratic section is exploited instead of the classical PLL control loop [1]-[5], [8], [18], [19]. Hence, a noncritical low-frequency 150-kHz clock is employed and high-frequency PLL's and VCO's are avoided. Because in the developed tuning circuits both clock references are in the stopband of the filter, a higher dynamic range and lower interference effects have been achieved compared to the other known tuning techniques [3]-[5], [8].

In Section II, the main principles are described. The filter architecture and the building blocks are discussed in Section III. The automatic frequency controller is considered in Section IV. The proposed BW tuning technique is described in Section V. The experimental results are presented in Section VI. In the last section, some conclusions are addressed.

II. THE MAIN PRINCIPLES OF THE SYSTEM

The block diagram of the bandpass filter and the automatic tuning loops are shown in Fig. 1. The tunable fourth-order filter is tuned by the control voltages $V_j$ and $V_{bw}$. The control voltages $V_j$ and $V_{bw}$ tune the poles fre-
The resistance of the tunable resistor. The filter bandwidth is correlated to the filter bandwidth. Thus, the correcting signal is filtered out by the low-pass filter.

For the automatic tuning of continuous-time filters, a clock frequency is the most commonly used reference. The major reasons for that are its high precision, its high stability, and because a clock is commonly available in the system for the digital part of the design. Since the reference is a clock frequency, the typical tuning schemes are based on the phase-locked loop (PLL) principle [1]–[5], [8], [18], [19]. In this paper a different approach is employed [21]. A discussion of the proposed technique follows.

In the Appendix it is shown that the resonant frequency of the biquadratic filter is very insensitive to the finite parameters of the OTA’s, e.g., finite dc gain and parasitic poles and zeros. Hence, the tuning of the poles frequency can be carried out by using a low-frequency $g_m/C$ circuit. Thus, high-frequency PLL’s and phase comparators are avoided. In Fig. 1, the frequency controller is composed of a charge comparator and a low-pass filter. For the charge comparator, two weighted dc current sources, a clock reference, an OTA, and a capacitor are employed. For the processing of the charge, well-known switched-capacitor techniques are employed [10]. In this technique, $g_m/C$ is tracked to the external clock frequency scaled by a factor $N$, with $N$ the ratio of the weighted current sources. The factor $N$ is accurately controlled in currently running CMOS processes [23]–[25]. In this design, a 450-kHz clock frequency and $N = 148$ are employed. Therefore, most of the tuning noise feedthrough falls in the filter stopband. Hence, the signal-to-noise ratio of the main filter is lowly sensitive to the operation of the automatic frequency controller.

For the automatic tuning of the filter bandwidth, a second control loop is employed (see Fig. 1). The $BW$ detection is a complex task because the maximum $BW$ sensitivity of a biquadratic filter is 1. In addition, it occurs just at the filter resonant frequency [14], [15]. At low and high frequencies, the magnitude and the phase response of the biquadratic filter are almost insensitive to the filter bandwidth. Therefore, in the frequency domain the extraction of the $BW$ requires a test signal with frequency at or around the resonant frequency of the filter. The drawback of this approach is an increment of the tuning signal feedthrough [3]–[5], [8]. Here, for the extraction of $BW$ a time-domain analysis is employed.

The $BW$ controller comprises a simple first-order low-pass filter, a second-order filter (replica of a second-order section of the main filter), two envelope detectors, and a low-pass filter. The poles frequency of both reference filter and biquad are tuned by the frequency controller. The main idea of the $BW$ controller is to adjust the $BW$ of the biquad through the adjustment of its pulse response. For $Q > 0.5$, the pulse response of the biquad corresponds to a sinusoidal signal with an oscillating frequency equal to the resonant frequency of the filter and with an exponentially decaying amplitude. The amplitude of the biquad pulse response is determined by the filter bandwidth [20]. In this technique, the $BW$ of the biquad is tracked to the pole frequency of a well-controlled first-order filter. For this purpose, the pulse response of the first-order filter is used as the reference. In the $BW$ controller, the envelope detectors extract and compare the envelope of both filters. The correcting signal is filtered out by the low-pass filter.
and fed back to adjust the tunable resistor in the biquad. Hence, the bandwidth of the biquad is tracked to the pole frequency of the reference filter.

III. THE FOURTH-ORDER BANDPASS FILTER

The filter architecture is based on the cascade of two biquadratic sections as shown in Fig. 2. In order to reduce both the even-order harmonic distortion components and the effects of the power supply noise, a fully differential filter has been implemented. For the following discussion, we refer only to the biquad 1 of Fig. 2. The poles frequency of the biquad, \( \omega_0 = 2\pi f_0 \), is controlled by the transconductance of the OTA2, \( g_{m2} \), and its associated capacitor \( C_1 \) as \( g_{m2}/C_1 \). The frequency of the pulses is adjusted through the control voltage \( V_{cM} \), generated by the frequency controller. The voltage \( V_{cM} \) is also generated by the frequency controller but it is different than \( V_{cF} \) because \( g_{m1} = g_{m2}/Q \). If the OTA’s are ideal (infinite dc gain and absence of parasitic poles and zeros) the quality factor \( Q \) of the filter is determined by the product \( g_{m2}R_1 \), with \( R_1 \) a tunable CMOS resistor. The filter bandwidth \( BW \) is given by \( g_{m1}/C_1 \) (\( g_{m1} = 1/R_0 \)). The BW of the filter is controlled by the tunable resistor through the voltage \( V_{BW} \). This voltage is generated by the automatic BW controller. The peak gain of the biquad is controlled by the transconductance of OTA1, \( g_{m1} \), and the resistor and is given by \( g_{m1}R_1 \). For this design, the peak gain of the second-order bandpass filter is unity. At the resonant frequency, the gain of the low-pass output, \( V_{LP} \), is almost unity as well. As a result, an almost optimum dynamic range around the filter passband is obtained.

For \( C_1 \), polysilicon capacitors of 4 pF have been employed. The total parasitic capacitance at the output of the first biquad is of the order of 0.6 pF. For the second biquad the parasitic capacitor is slightly higher because an extra OTA (not shown in Fig. 2) has been used to buffer out the filter outputs for measurement purposes. Hence, the polysilicon capacitors \( C_2 \) have slightly been modified to compensate this effect.

For the OTA’s a low-distortion voltage-to-current transducer is employed, which is shown in Fig. 3, [6], [16], [22]. The OTA2 transconductance is around 300 \( \mu \)A/V. The transconductance of OTA1 is 20 times lower, 15 \( \mu \)A/V. The dimensions and bias conditions for the transistors of both OTA1 and OTA2 are given in Table I.

For the common-mode stabilization of the OTA’s, one common-mode feedback (CMFB) system per pole is employed instead of using one CMFB per OTA. For each biquad (see Fig. 2), the CMFB is shared by the OTA1 and the right most OTA2. However, the common-mode voltage of the \( V_{cm} \) output is detected at the \( V_{cm} \) voltage of the leftmost OTA2 (see Figs. 2 and 3). Similarly, the common-mode voltage of the \( V_{cp} \) output is detected at the \( V_{CM} \) voltage of the rightmost OTA2. From these common-mode voltages, the CMFB’s are arranged. The result is a very simple CMFB [16], [22].

The huge effects of the active devices (OTA’s and op amps), excess phase shift on the bandwidth and peak gain of the active filters, have been known for long time [1], [8], [14], [26]. In the filter, the theoretical value of the floating resistors is 66 k\( \Omega \). Due to the high \( Q \) of the biquads (\( Q = 20 \)) and the effects of the OTA excess phase shift, it is required to adjust those resistors in a very wide range, e.g., more than 100% (see the Appendix). For this reason, a resistor based on a unity feedback connected OTA, commonly used in OTA-C realizations [1], [2], [4], is avoided. The active resistors are implemented by using the output conductance of two saturated transistors connected in series as shown in Fig. 4. The output conductance of the MOS transistor is almost proportional to its bias current and its harmonic distortion components are fairly insensitive to variations of the resistance [17]. Since the BW of the biquad is inversely proportional.
to the resistance, the BW of the filter can be adjusted in a very wide range without sacrificing either filter dynamic range or frequency response. Due to the reduced number of nodes in this topology, its frequency response is very high. The gate dimensions for the transistors $M_1$ and $M_2$ are $W_1/L_1 = 20 \mu m/1.5 \mu m$ and $W_2/L_2 = 20 \mu m/4.5 \mu m$, respectively.

**IV. THE AUTOMATIC FREQUENCY CONTROLLER**

The resonant frequency of the biquad is fairly insensitive to the OTA finite parameters (see the Appendix). If the parasitic poles and zeros are placed at frequencies higher than $2 \omega_0$, they produce $\omega_0$ errors lower than 0.15%. Using cascode output stages, the effects of the OTA finite dc gain on $\omega_0$ are very small too. If those effects are neglected, the resonant frequency of the biquad (Fig. 2) can be approximated as (referred to the Appendix)

$$\omega_0 = \frac{g_{m2}^{\prime}}{C_1} \sqrt{\frac{g_{m2}}{g_{m2}^{\prime}}} C_1$$

where $g_{m2}^{\prime}$ and $C_1$ are slightly different than $g_{m2}$ and $C_1$, due to the mismatches in the transconductances of the OTA2's and capacitors $C_1$. This equation suggests that the frequency of the poles can be adjusted tuning a simple $g_{m2}/C_1$. The ratio of the transconductances of the same order of magnitude, $g_{m2}/g_{m2}^{\prime}$, can be accurately controlled in current CMOS technologies. The ratio of capacitors, $C_1/C_1^{\prime}$, is quite accurate too, provided that the parasitic capacitors are accounted. The proposed frequency controller is based on a charge comparison principle and tunes a single time constant $C/g_m$.

The charge comparison of discrete packages of charge and continuous-time charge can be carried out with the circuit shown in Fig. 5(a) [21]. $\phi_1$ and $\phi_2$ are two non-overlapping clock frequencies defined in Fig. 5(b). In this controller, the capacitor $C_1$ is charged to $V_{o1}$ during the clock phase $\phi_1$. In the clock phase $\phi_2$, this charge is transferred to the holding capacitor $C_{h}$. Ideally, when the clock $\phi_2$ is closed, $C_1$ is discharged producing a negative jump at $V_{o2}$. The jump is negative because the charge is injected into the negative plate of the capacitor $C_{h}$. At the same time, a constant current $N_{IR}$ is extracted from the same capacitor plate. The current extraction results in a positive slope ramp behavior at $V_{o2}$ (see Fig. 5(b)). Ideally, the $C_{h}$ charge is described by the following charge conservation equation:

$$C_{h} V_{o2}(t) = (t - t_0) N_{IR} - (C_1 V_{C1}(t_0) N_{R2} + C_{h} V_{o2}(t_0))$$

with $V_{o2}(t_0)$ the initial condition of the op-amp output voltage. The first term of (2) corresponds to the extracted charge by the current source $N_{IR}$. The second term is the injected charge, during $\phi_2$, from the capacitor $C_1$ into $C_{h}$. If the time constants are sufficiently large to charge and discharge $C_1$, the total injected charge, $C_1 V_{C1}(t_0)$, is equal to $C_1 V_{o1}(t_0)$. The voltage, $V_{o1}$ is determined by the dc current source, $I_{R}$, and the OTA2 transconductance as $V_{o1} = I_{R}/g_{m2}$. The transconductance $g_{m2}$ is adjusted by the control voltage $V_{f2}$.

In the loop, the dc value of $V_{o2}$ is extracted by the low-pass filter. This value corresponds to the frequency control.
voltage $V_{t2}$. In a steady-state condition the average of $V_{t2}$ is constant. Therefore, in a clock period the injected charge is equal to the extracted charge. This means that $V_{t2}(T + t_0) = V_{t2}(t_0) + T$ being the clock period. If (2) is evaluated at $t = t_0 + T$, the loop steady-state condition can be expressed as

$$\frac{g_{m2}}{C_1} = \frac{1}{N T} = \frac{f_{\text{clock}}}{N} \tag{3}$$

with $N$ being the ratio of the dc current sources. From this relationship, it is evident that $g_{m2}/C_1$ can be tracked to the clock frequency $f_{\text{clock}}$. The factor $N$ is the result of the weighted current sources used. $N$ (the ratio of dc current sources) can be accurately controlled in current CMOS processes [23]-[25]. Using $N > 6.28$, the operating frequency of the loop is lower than the poles frequency. It has to be recognized that the accuracy of the tuning system depends of the precision of the charge comparison instead of the absolute value of the $V_{t2}$ dc voltage. Hence, the accuracy of the system is fairly insensitive to the dc offset voltage of the low-pass filter, but any op-amp offset voltage will reduce the accuracy of the loop.

A fully differential block diagram of the frequency controller is depicted in Fig. 6. The frequency controller is driven by a 450-kHz clock frequency. The ratio of the dc current sources $N$ is 148. For the design of the current sources, unity and interdigitated cascode transistors are employed. The bias current of the unity 6-μm/6-μm transistor is 0.94 μA. The total $I_D$ current is around 0.140 μA (see Fig. 6). For $I_D = 140$ μA and $g_{m2} = 300$ μA/V the differential voltage at the output of the unity feedback connected OTA2 is around 0.93 V. The maximum differential range of the OTA2 is in the order of 2 V before the structure saturates. Hence, the unity feedback OTA2 can support $g_{m2}$ variations as high as 100%.

A major design problem is the mismatch between the filter capacitors and the capacitors associated with the automatic tuning loop. In the filter, there are several parasitic capacitors due to the additional devices connected at the output of the OTA's. A part of these parasitic capacitors are the drain capacitors of the OTA output stage and their values are not very well controlled. Another parasitic component is due to the gate-source and gate-drain capacitors of the OTA input stage. The top capacitors of the polysilicon capacitors have to be considered as well. It is necessary to model carefully these capacitors in order to include their effect in the charge comparator capacitor $C_1$. Unfortunately, this is a manual procedure that requires extensive simulations. Even more, the mismatch can be minimized but cannot be eliminated due to the process parameter variations.

The op amp is a classical fully differential folded cascode structure. The op-amp gain-bandwidth is only 15 MHz and its finite dc gain is around 58 dB. It is not necessary to increase its gain-bandwidth because the clock frequency of the switched-capacitor integrator is only 450 kHz. $C_H$ is a 6-pF capacitor. The differential-to-single-ended converter comprises an OTA and the active load is composed of two series-connected transistors. It should be noted that the signal at the output of the op amp could be very large. Hence, a large input range OTA has to be used. If the sampled-data filter is used then it is not necessary to accurately detect the whole op-amp output voltage. In this case, it is sufficient to convert accurately the op-amp output voltage into current at the end of the clock phase at which the switched-capacitor circuit is sampling the signal. For this design, the OTA is a single-ended version of OTA2. The large input range of the OTA further increases the linear operation of the converter. In addition, the CMFB for the op amp is arranged from the common-mode voltage implicit in the input stage of the OTA (see $V_{CM}$ in Fig. 3).

In Fig. 6, the low-pass filter has been implemented using a switched-capacitor filter. There is no penalty for the use of the switched-capacitor resistor because the clock phases are already available. The silicon area needed for the switched-capacitor resistor is quite small. In switched-capacitor circuits large resistors require minimum silicon area, which is not the case for passive resistors. If the clock phases are arranged as shown in Fig. 6, the sampled voltage (at the end of $\phi_2$) is just the dc voltage of the op-amp output voltage (see Fig. 5(b)). This is the optimum point for the sampling of the dc op-amp output voltage. Furthermore, due to the sampled nature of the low-pass filter, most of the harmonic components due to the charge comparison are eliminated by the switched-capacitor filter. However, the switched-capacitor filter introduces clock-feedthrough offset voltage. This offset voltage is not critical for the accuracy of the system and it can easily be reduced by well-known techniques [10]. At the end of the...
controller, the filtered voltage is level shifted by the voltage divider.

The nonidealities of the charge comparator affect the accuracy of the controller. The differential OTA2 offset voltage introduces a tuning error proportional to the ratio of the offset voltage to the magnitude of the OTA2 differential output voltage [22]. For instance, if the OTA2 differential dc offset voltage is OTA2 differential dc offset voltage is around 5 mV and the OTA2 output voltage is larger than 0.9 V, the tuning error due to this offset is lower than 0.5% [22].

V. AUTOMATIC BANDWIDTH CONTROLLER

Due to the OTA finite dc gain and parasitic poles and zeros, the bandwidth of a biquadratic filter is mathematically composed of two parts as is expressed in (4) (see the Appendix for details):

\[
\text{BW} \equiv \left( \frac{g_{01} + 2g_{02}}{C_1} + 2\frac{\omega_0^2}{\omega_{eq}^2} \right) + \left( \frac{g_1}{C_1} \right)
\]

where \( g_{01} \) and \( g_{02} \) are the finite output conductance's of OTA1 and OTA2, respectively, \( \omega_{eq} \) is the result of the high-frequency parasitic poles and zeros. In (4), the first part of \( \text{BW} \) is due to the OTA finite parameters. The second part, \( g_1/C_1 \), is the tunable part of \( \text{BW} \). In our approach, we did not attempt to improve the performance of the OTA, which should decrease the first term of (4). The proposed tuning system assumes that the parasitic term is present. The only task of the automatic tuning system is to adjust \( g_1/C_1 \) such that the filter bandwidth corresponds to the required value.

In the frequency domain, the response of a first-order filter is totally characterized by two parameters: namely, its dc gain and its -3-dB frequency (pole frequency) [14], [20]. In the time domain, the behavior of the first-order filter can be described by the impulse response of the filter. The step response of a first-order low-pass filter with unity dc gain and -3-dB frequency at \( \omega_{-3dB} \) is given by

\[
u_{OLP}(t - t_0) = (1 - \exp^{-\omega_{-3dB}(t-t_0)})V_{step} + V_{OLP}(t_0)
\]

with \( V_{OLP}(t_0) \) the initial condition of the low-pass filter output. \( t_0 \) is the time at which the step is applied and \( V_{step} \) is the amplitude of the applied step. The step response of a biquadratic low-pass filter with a unity dc gain, a bandwidth equal to \( \text{BW} \), and a \( Q \) factor larger than 0.5 is characterized by the following expression:

\[
u_{OLP_2}(t - t_0) = (1 - h(t - t_0)) V_{step} + V_{OLP_2}(t_0).
\]

The function \( h(t - t_0) \) is called the impulse response of the system [20]. For the biquad, this function becomes

\[
h(t - t_0) = \frac{1}{\sqrt{1 - \frac{1}{4Q^2}}} \exp \left( \frac{-BW(t - t_0)}{2} \right) \sin \left( \sqrt{1 - \frac{1}{4Q^2}} \omega_0(t - t_0) + \phi \right)
\]

where \( \phi \) is a function of \( Q \). For large \( Q \), the first factor of 7 can be approximated as unity. Hence \( h(t - t_0) \) equals a unity sinusoidal function whose amplitude decays exponentially. Comparing (5) and (6) it can be noted that the step response of the first- and second-order low-pass filters are similar. The only difference is the sinusoidal function present in \( h(t - t_0) \). If \( \omega_{-3dB} \) is equal to \( \text{BW}/2 \) then the envelope of both filters are equal. Therefore, the \( \text{BW} \) of a second-order filter can be tracked to the pole of a first-order filter by comparing the step response of both filters. The first-order filter can be considered as the 'reference filter' and the master filter, to be tuned, is the second-order filter. A block diagram implementation of this technique is shown in Fig. 7.

In this diagram, the input signals \( v_p \) and \( \overline{v}_p \) are two complementary pulse trains. The pulsed values for \( v_p \) are 0 and \( V_p \), and for \( \overline{v}_p \) are 0 and \( -V_p \). The loop of the master filter is a replica of a loop of the main filter. Because the same OTA2's are used, the dc gain of the filter is unity. The tunable resistor \( R_1 \) is the element of the master filter to be tuned for the correction of the \( \text{BW} \). The reference filter has been implemented with two OTA1's and the capacitors \( 2C_1 \). The unity feedback connected OTA1 guarantees the unity dc gain of the reference filter. The -3-dB frequency of the reference filter is adjusted with the load capacitor \( 2C_1 \) and \( g_{m1} \). The transconductance factor is \( Q(20) \) times lower than \( g_{m2} \). Because of the absence of resonant loops, the magnitude response of the first-order low-pass filter is rather insensitive to the OTA parasitic poles and zeros.

In the \( \text{BW} \) controller, the envelopes of both filters are extracted by the envelope detectors. The output of the envelopes are compared by the OTA. In the positive transition the detected signal at the output of the first-order filter corresponds to the typical exponential charging response. However, the detected signal from the second-order filter corresponds to an exponential discharge starting from \( 2V_p \). This is a result of the sinusoidal function implicit in (7). Hence, the envelopes have to be compared during the negative transition. For this reason, the low-pass filter has been implemented as a single phase filter. The OTA output current is integrated by the capacitor \( C_i \) only during the clock phase \( \phi_c \). This clock phase is synchronized with the negative transition of the input signals.

The low-pass filter is implemented by the action of the OTA, the op amp and the feedback capacitor \( C_f \). The out-
put of the op amp, \( V_{op} \), is sampled during the clock phase in which the signal is not being injected into \( C_f \). The op amp is a low dc offset symmetrical OTA. Its gain-bandwidth product and its dc gain are 5 MHz and 55 dB, respectively. \( C_f \) is a 10-pF capacitor. For the sample and hold, an external 100-pF capacitor has been employed. The value of this capacitor is not critical, provided that it can hold the sampled voltage during the holding time. For the switches, minimum dimension transistors have been used. The transistors used for the level shifter are similar to the transistor used for the biasing of the floating resistor, \( M_s \).

The envelope detector is shown in Fig. 8. In order to avoid errors due to the common-mode offsets present at the output of the filters, a level shifter has been included. The attenuator and level shifter are implemented by the large-input-range voltage-to-current transducer and the diode-connected transistors \( M_{d} \). This transducer is used because of the large signal present at the output of the filters. The signal is rectified by the differential pair, transistors \( M_{det} \), and the detection is carried out by the current source \( I_{det} \) and the capacitor \( C_{det} \). The current source and the capacitor determine the discharging speed of the detector. The transistor dimensions and the bias currents of the low-distortion input stage of the envelope detector are the same as for the OTA2. The transistor dimensions \( W/L \) of \( M_{d} \) and \( M_{det} \) are 150 \( \mu \)m/4 \( \mu \)m and 200 \( \mu \)m/1.5 \( \mu \)m, respectively. The discharging current of the detector, \( I_{det} \), and the capacitor of the envelope detector, \( C_{det} \), are 4 \( \mu \)A and 4 pF, respectively.

There are several second-order effects that limit the accuracy of the BW tuning system. A discussion of some of them follows. For the design high-\( Q \) filters large OTA transconductance ratios are required in both the filter and the BW controller. Unfortunately, large OTA transconductance ratios are not very well controlled in current CMOS processes, e.g., accuracy is \( \approx 1 \) to 3%. The OTA transconductance ratios depend on both effective transistor width ratios and effective transistor length ratios. For small transistor dimensions, the uncertainties of both effective lengths and effective widths (due to lateral diffusion, birds beak, depletion regions, etc.) are two of the most limiting factors in the accuracy of these ratios. This is a limitation of this approach.

The BW tuning loop is based on a comparison of the envelopes of both the reference and master filter. The envelopes are compared by the OTA (see Fig. 7). Hence, any offset voltage in the OTA will result in a comparison error. As a result, the OTA offset voltage produces a tuning error [22]. The tuning error is a function of both the product \( T \cdot BW \) and the ratio of the OTA offset voltage to the amplitude of the envelopes \( V_{out} \) in Fig. 8. For the detection of the envelopes it is desirable to use a clock period at least 8 times higher than \( BW \). In the case where the OTA offset \( \approx 10 \) mV and \( V_{out} \approx 0.3 \) V and considering \( T \cdot BW = 8 \), the theoretical BW tuning error is of the order of 8.8% [22]. Therefore, a major design constraint for the OTA is a low dc offset voltage, i.e., lower than 5 mV. The gain-bandwidth of the OTA is not critical because it is only a low-frequency loop. The transconductance of this OTA is 32 \( \mu \)A/V. For this OTA transconductance, HSPICE simulations have shown BW tuning errors of about 8%.

VI. EXPERIMENTAL RESULTS

The circuit has been fabricated in a standard n-well double-metal 1.5-\( \mu \)m CMOS process. The microphotograph of the chip is shown in Fig. 9. The filter outputs are buffered out by an additional OTA2. Hence, the data presented in this section includes the effects of this OTA2.

The frequency response of the automatically tuned 10.7-MHz bandpass filter is depicted in Fig. 10. The peak gain of the bandpass filter is around \(-3 \) dB and the bandwidth is 300 kHz. For several chips measured, the variations of the filter center frequency are around \( \pm 1 \)% as has been expected. However, the variations of the filter bandwidth are around \(+20\%\) to \(+30\%\). The reasons are assumed to be the following. Firstly, a larger systematic offset in the OTA of the Fig. 7 is present, mainly due to the differential-to-single-ended output conversion. Secondly, there are inaccuracies in the detection of the envelopes. Thirdly, the \( \omega_0 \) tuning errors produce bandwidth errors due to the high \( \omega_0 \) sensitivity (proportional to \( Q \)) of the high-\( Q \) realizations [14], [15], [22]. The systematic errors, such as the one in the OTA, have resulted in a systematic shift in the \( Q \) value of about 20%. The random error accuracy from chip to chip is about 10%. For several measured chips, the attenuations at 5 and 20 MHz are
around $-55$ to $-62$ dB. At very low frequencies the attenuation is in the order of $-68$ dB.

The very large BW (or $Q$) programmability of the filter, manually tuned, is shown in Fig. 11. The filter bandwidth has been varied from 250 kHz up to 2 MHz. Furthermore, the peak gain of the filter can be controlled by more than 30 dB. For those results, the bias currents of the floating resistors are 10, 50, and 250 $\mu$A.

The measured two-tone intermodulation distortion for the filter is shown in Fig. 12. In this plot, a 3.2-V$_{pp}$ two-tone input signal has been applied to the filter. In this plot, it can be noted that the third-harmonic two-tone intermodulation distortion is slightly lower than $-40$ dB. The other harmonic distortion components, for instance at 10.675 MHz, are more than 6 dB smaller. These additional harmonic distortion components are mainly due to the limited common range of the OTA input stage. This spectrum shows the low distortion of the OTA's but also the low-distortion behavior of the active resistor. The reason can be explained as follows. In the fourth-order filter, the resonant frequency of the biquads are very close to the center frequency of the filter. At the center frequency, the loops of the OTA2's and the capacitors $C_I$ are almost in resonance. At resonance the OTA2's of each loop are transferring the charge between the $C_I$ capacitors of that loop, but they do not interfere with the current injected by the OTA1's. The situation is the same as for the parallel connection of a capacitor, an inductor, and a resistor. At the resonant frequency, the total impedance of the RLC circuit is equal to $R$. Hence, any injected current in the RLC circuit with a frequency equal to the resonant frequency of the LC tank is converted into a voltage only by the resistor. At the center frequency of the filter, the OTA1 currents are almost totally injected into the resistors $R_I$. As a result, at the passband the filter distortion is dominated by the nonlinearities of the OTA1's and the active resistors. The OTA1 structure is a very low-distortion circuit [6]. As a result, the distortion of this filter is mainly assumed to be due to the floating resistors.

The output-referred noise density of the automatically tuned filter, including both the buffer and the setup, is depicted in Fig. 13. This noise density has been scaled up by 3 dB (the peak gain of the filter is around $-3$ dB). In this plot, some small spikes can be recognized. The presence of these frequency components is mainly due to the BW controller. They are a result of the oscillating frequency of the master filter (see (7)). It can be noted in Fig. 13 that the amplitudes of the spikes are basically at the filter noise level. This demonstrates that the noise feedthrough of the proposed automatic tuning system is very small, especially if it is compared with previously published systems [3]-[5], [8]. For the automatically
tuned filter, the in-band input-referred noise of the filter is calculated around 450 μV \text{rms}. The linear input range of the filter is around 1.2 V \text{rms}. These values lead to a filter signal-to-noise ratio of 68 dB, with the IM3 < -40 dB. A summary of the filter experimental results is given in Table II.

The functionality of the frequency controller is shown in Fig. 14. In this plot, the clock frequency has been varied from 375 up to 525 kHz. In general, the center frequency of the filter tracks the clock over a clock frequency range from 300 up to 600 kHz (center frequencies in the range of 7 up to 14 MHz). For very high clock frequencies, the major limitation of the system accuracy is the offset voltages of the voltage-to-charge converter. For low clock frequencies the accuracy of the frequency controller is limited by the linear range of the charge comparator.

VII. CONCLUSIONS

A 10.7-MHz fourth-order bandpass filter with on-chip automatic tuning has been described. The bandwidth of the filter is 300 kHz and the Q of the biquadratic sections is 20. The continuous-time filter has been implemented using the OTA-RC technique. For the automatic tuning of the filter two nonlinked control loops have been employed. These loops are operated at lower frequencies than the main filter resonant frequencies. Hence, the filter signal-to-noise ratio is little affected by the operation of the filter controllers. As a result, a filter realization performing a 68-dB signal-to-noise ratio has been obtained. The third intermodulation distortion is lower than −40 dB for a two-tone signal as large as 3.2 V p-p. The chip uses supply voltages of only ±2.5 V. All experimental results of the 10.7-MHz filter described in the paper are a consequence of the use of linearized OTA's, tunable and linear floating resistors, and the development of two low-noise feedthrough controllers.

The functionality of the automatic tuning system has been shown. The low-noise feedthrough behavior of the proposed automatic tuning system has also been demonstrated. The center frequency of the fourth-order bandpass filter is controlled within a 1% accuracy. The accuracy of the filter bandwidth is within 30%. The external clock controls the filter center frequency in a range of 7 to 17 MHz.

APPENDIX

It is well known that the OTA has a finite dc gain and several high-frequency poles and zeros \[1, 8, 14, 26\]. The OTA finite dc gain is a result of the nonzero transistor output conductance. The high-frequency poles and zeros are due to the parasitic nodes in both input and output OTA stages. Typically, the frequencies of the parasitic poles and zeros are at least 10 times higher than the resonant frequencies of the main filter. Hence, at the passband of the filter they can be approximated by a single pole-zero pair. The equivalent pole-zero pair can be included in the OTA transconductance leading to a frequency-dependent \( g_m \) given by

\[
g_m(s) = g_m \frac{1 + \frac{s}{\omega_z}}{1 + \frac{s}{\omega_p}} \approx g_m \left( 1 + s \left( \frac{1}{\omega_z} - \frac{1}{\omega_p} \right) \right)
\]

where \( g_m \), \( \omega_z \), and \( \omega_p \) are the OTA transconductance, the equivalent parasitic zero, and the equivalent parasitic pole, respectively. A simple OTA macromodel is shown in Fig. 15(a).
the OTA finite dc gain is higher for low-Q factors. If small
zero of the OTA’s can be expressed as

\[ g_m \left( s + g_o \right) \]

\[ C_1 \]

\[ s^2 + BWs + \omega_0^2 \]

\[ 1 + \frac{s}{\omega_{eq1}} \] (A2)

with \( \omega_{eq1} = 1/(\omega_0^{-1} - \omega_p^{-1}) \). Note that \( \omega_{eq1} \) may be positive (zero is dominant) or negative (pole is dominant) or infinite (pole and zero cancel each other). \( \omega_0 \) and \( BW \) are the pole frequency and the filter bandwidth, respectively. They are approximately given by

\[ \omega_0 \approx \sqrt{\frac{g_{m2} g_{m2}'}{C_1 C_1'}} \left[ 1 + \frac{1}{A_{2}} \left( \frac{g_1}{A_{2}} + \frac{g_2}{g_{m2}} \right) - \frac{g_{m2}^2}{C_1^2 \omega_{eq1}^2} \right] \]

\[ BW \approx \frac{g_1}{C_1} + \frac{g_{o1} + 2g_{o2}}{C_1} + 2 \frac{\omega_0^2}{\omega_{eq1}} \] (A3)

where \( g_{m1} \) and \( A_{m1} = g_{m1}/g_{o1} \) are the transconductance and the dc gain of the \( i \)th OTA, respectively, and \( g_1 = 1/R_1 \). The transconductances of OTA2 and OTA2’ and also \( C_1 \) and \( C_1' \) are slightly different due to the unavoidable mismatches. From (A3), the effect of the OTA parasitic poles and zeros is an additional zero at \( \omega = \omega_{eq1} \). However, the OTA1 pole-zero does not affect neither the poles frequency nor the filter bandwidth.

According to (A3), the frequency of the poles is marginally sensitive to both OTA2 parasitic effects: finite dc gain and excess phase shift due to the high-frequency parasitic zero and pole. After some approximations on (A3), it can be shown that the normalized deviation of the poles frequency due to both finite dc gain and parasitic pole-zero of the OTA’s can be expressed as

\[ \Delta \omega_0 \left( \frac{\omega_0}{\omega_{eq1}} \right) \approx \frac{1}{2A_{V2}} \left( \frac{g_1}{A_{2}} + \frac{2}{A_{2}} \right) \]

\[ - \frac{1}{2} \frac{\omega_0}{\omega_{eq1}}^2 \approx \frac{1}{2} \left( \frac{1}{Q_{A_{V2}}} - \frac{\omega_0}{\omega_{eq1}} \right)^2 \] (A5)

According to this expression, the \( \omega_0 \) deviation due to the OTA finite dc gain is higher for low-Q factors. If small \( \omega_0 \) deviations are required, large OTA dc gains have to be used. The effect of the OTA2 parasitic pole-zero on the resonant frequency of the loop is also evident in (A5). According to this equation, \( \omega_0 \) is marginally sensitive to the parasitic poles and zeros of the OTA’s. If the equivalent parasitic frequency \( \omega_{eq2} \) is 20 or more times higher than \( \omega_0 \), the normalized \( \omega_0 \) deviation is lower than 0.15%.

The filter bandwidth is also affected by the finite parameters of the OTA’s. From (A4), the \( BW \) deviation due to the effect of these parameters can be approximated by

\[ \frac{\Delta BW}{BW} \left( \frac{\omega_0}{\omega_{eq1}} \right) \approx \frac{g_{o1} + 2g_{o2}}{g_1} + 2 \frac{g_{m2}}{g_1} \frac{\omega_0}{\omega_{eq2}} \]

\[ \approx \frac{g_{o1} + 2g_{o2}}{g_1} + 2Q \frac{\omega_0}{\omega_{eq2}} \] (A6)

The effects of the output conductance of the OTA’s on \( BW \) are accounted in the first term of (A6). In order to reduce this error, it is desirable to reduce the output conductance of the OTA’s as small as possible. For high-frequency and high-Q applications, the \( BW \) deviation is dominated by the effect of the excess phase of the OTA’s [8], [26]. It can be noted that the \( BW \) deviation is extremely important when \( 2 Q \omega_0/\omega_{eq2} \) is close to \(-1\) (\( \omega_{eq2} < 0 \) implies that the parasitic pole is dominant). The case \( 2 Q \omega_0/\omega_{eq2} = -1 \) (for instance, \( Q = 20 \) and \( \omega_{eq2}/\omega_0 = 40 \)) implies a \( BW \) deviation of 100%. Therefore, the actual \( BW \) is equal to zero or equivalently the quality factor of the biquad is infinite. For the compensation of these errors, huge adjustments on the conductance \( g_1 \) are required.

REFERENCES

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