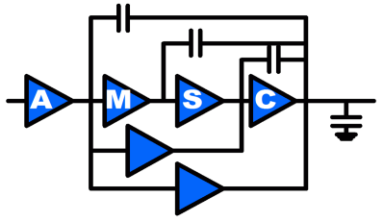
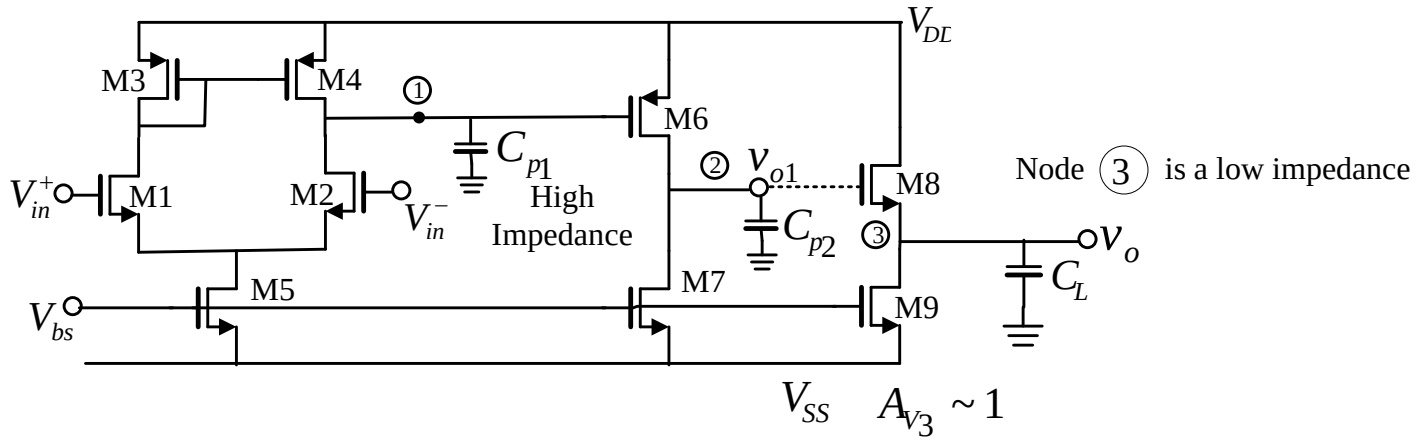


Op Amps Conventional Topologies

Edgar Sánchez-Sinencio
TI J. Kilby Chair Professor

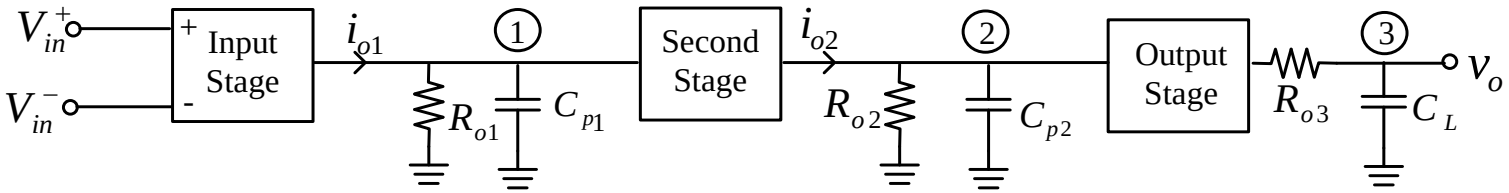
Next we review the *conventional Op Amp Design frequency response compensation* techniques and also we introduced a simple LV Current-Mode based Op Amp using resistors as transconductors. Difference Differential Amplifiers are also introduced.

UNCOMPENSATED CMOS OPERATIONAL AMPLIFIER



M1=M2; M3=M4

Ignoring zeros we can model this topology as:



$$A_{V_1}(0) \cong \frac{g_{m1}}{g_{o1}+g_{o3}} \quad ; \quad A_{V_2}(0) = \frac{-g_{m6}}{g_{o6}+g_{o7}} \quad ; \quad \omega_{p1} = \frac{g_{o2}+g_{04}}{C_{p1}} \quad ; \quad \omega_{p2} = \frac{g_{o6}+g_{o7}}{C_{p2}}$$

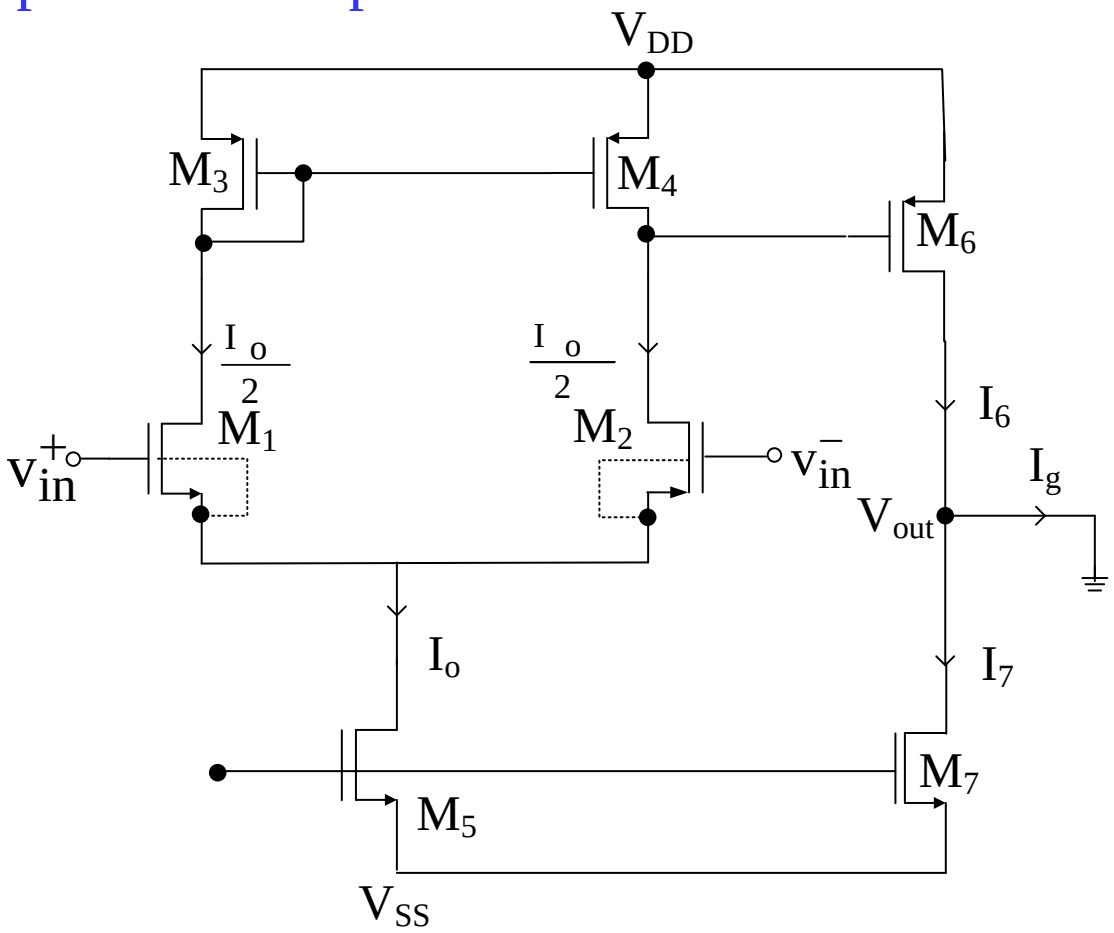
$$A_{V_T}(s) \cong \frac{A_{V1}(0)A_{V2}(0)A_{V3}(0)}{(1+s/\omega_{p1})(1+s/\omega_{p2})(1+s/\omega_{p3})} \quad ; \quad \omega_{p3} \cong \frac{g_{m8}}{C_L}$$

3

UNCOMPENSATED CMOS OPERATIONAL AMPLIFIER STABILITY ISSUES

- The low frequency voltage gain is high enough for a number of applications. 
- The open loop poles are far from the origin, this can cause stability problems for closed loop applications. 
- Closed loop poles might end very close to the jw axis and some in the RHP. 
- How to tackle this stability problem will be discussed next.

Two-Stage Uncompensated Amplifier



Uncompensated Operational Amplifier

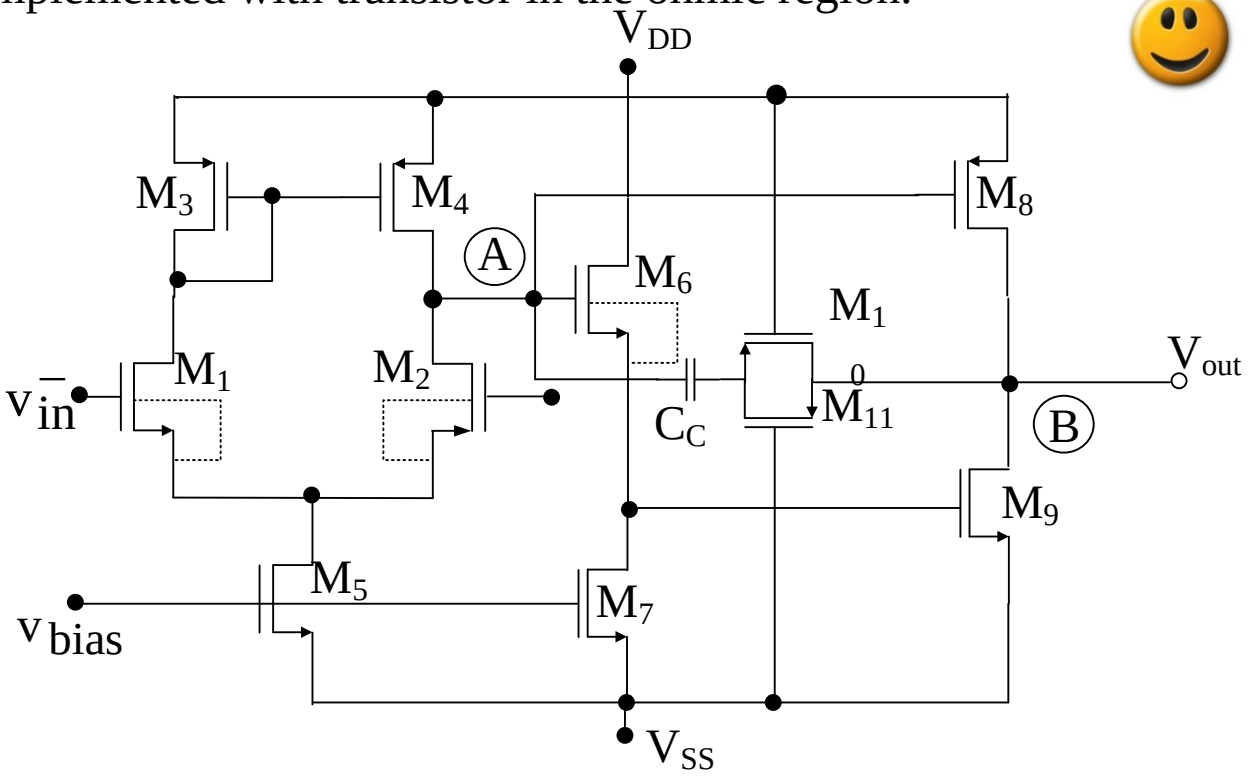
– $A_V = A_{V1}A_{V2} = \dfrac{g_{m2}}{g_{02} + g_{04}} \dfrac{g_{m6}}{g_{06} + g_{07}}$ Large voltage gain

– Poles are close to the jω axis causing stability problems

5

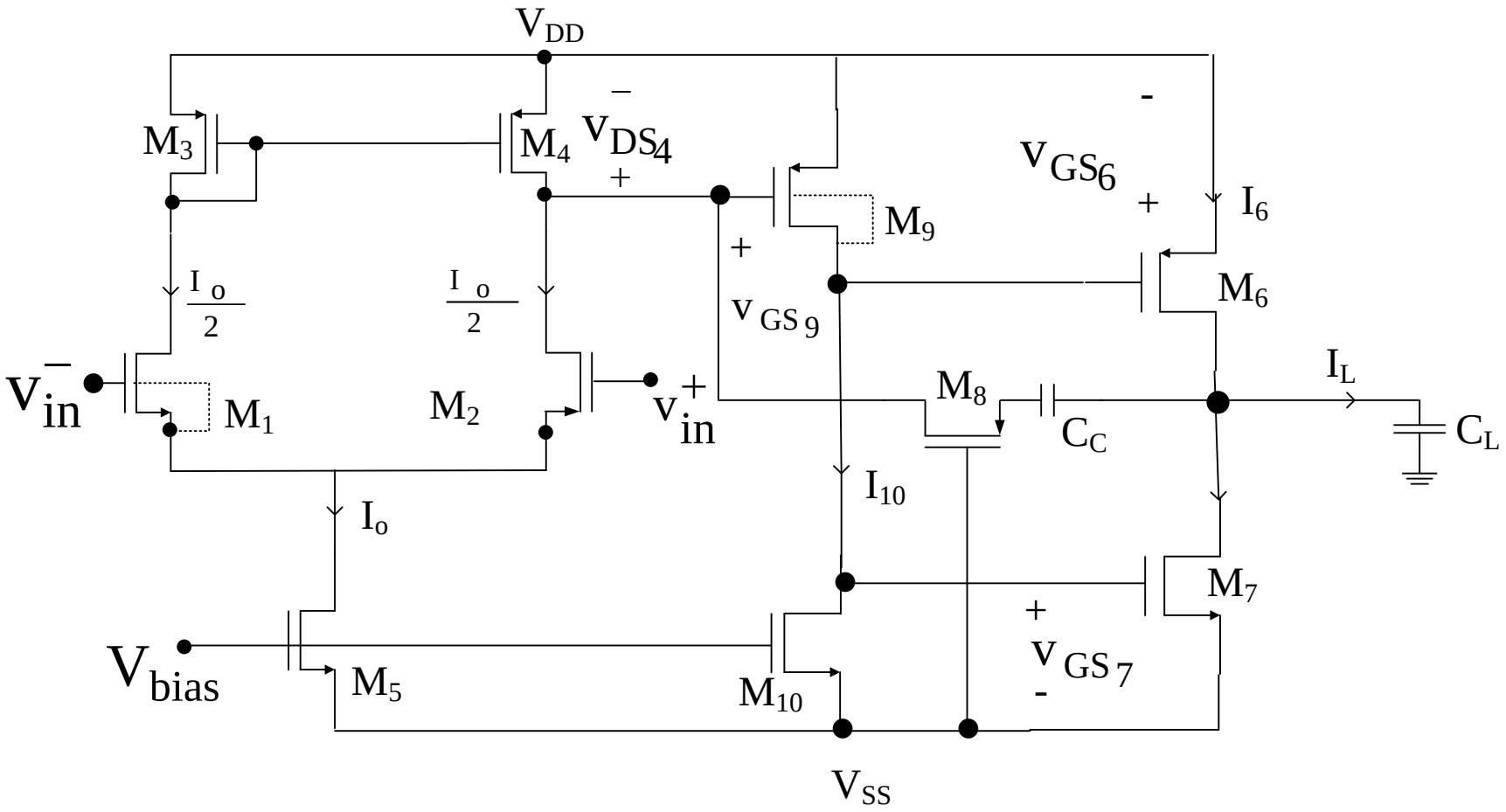
Employing a simple capacitor will split correctly the poles but will generate a Zero in the RHP.

Using an RC compensation can eliminate the zero and split poles. The resistor can be implemented with transistor in the ohmic region.



Improved internally compensated CMOS operational amplifier. Better bias for the output stage (M8 and M9)

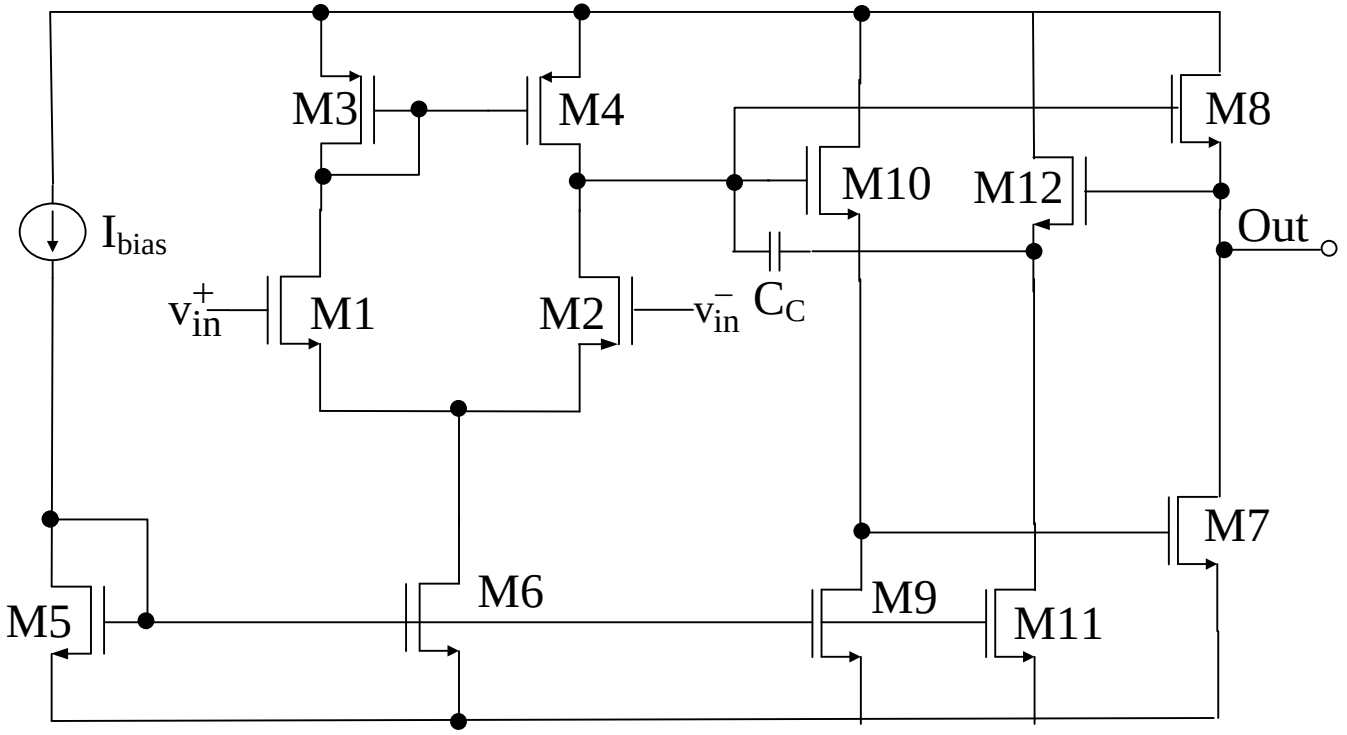
A variation at the output stage with class – AB is shown below.



CMOS op-amp with class-AB output stage and RC pole splitting.

7

"Pole Splitting" can be carried out with a compensation capacitor feedback and a voltage buffer as shown below



Two-Stage amplifier with source follower compensation scheme

- Without M12 and M11 a zero in the PRH
- With buffer (voltage follower), zero is eliminated and pole sp
  (due to C_C) is kept.

8

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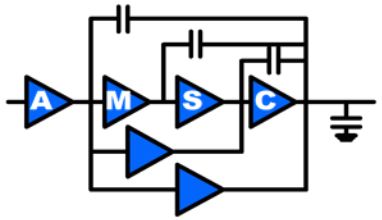


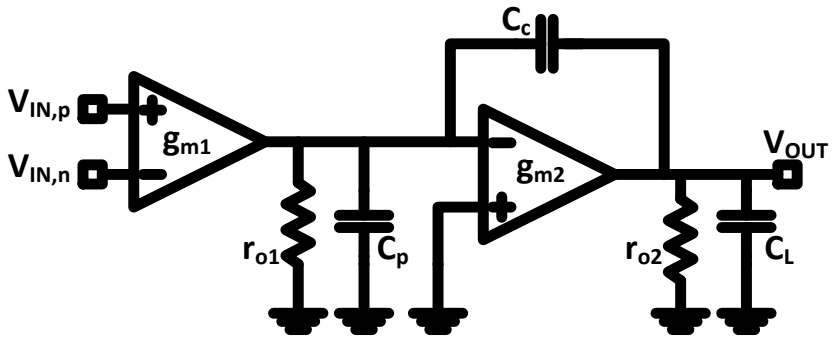
An Improved Frequency Compensation Technique for CMOS Operational Amplifiers using Current Buffers

ECEN 607 (ESS)

Courtesy of Hatem Osman

Background.-
Two-Stage Op-amp with Miller compensation

- The first stage is a differential-input/single-ended output stage, and the second stage is a class A or class AB inverting output stage.



- **DC Gain**

$$A_{v,0} = -A_{v1}A_{v2}$$

$$A_{v1} = g_{m1}r_{o1}$$

$$A_{v2} = g_{m2}r_{o2}$$

- Transfer Function

$$A_v = \frac{1-\frac{C_c}{g_{m2}}s}{1+(r_{o1}C_p+A_{v2}r_{o1}C_c+r_{o2}C_L)s+r_{o1}r_{o2}(C_pC_c+C_pC_L+C_cC_L)s^2}$$

- Pole/zero locations

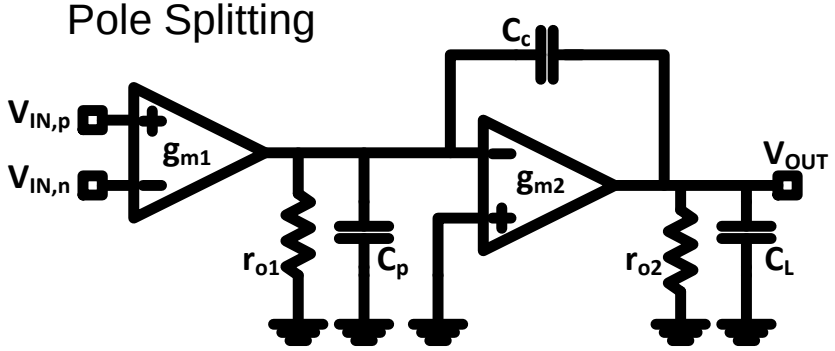
$$s_z = \frac{g_{m2}}{C_c}$$ RHP zero

$$s_{p1} = -\frac{1}{r_{o1}C_p+A_{v2}r_{o1}C_c+r_{o2}C_L} \approx -\frac{1}{A_{v2}r_{o1}C_c}$$ Dominant Pole

$$s_{p2} = -\frac{r_{o1}C_p+A_{v2}r_{o1}C_c+r_{o2}C_L}{r_{o1}r_{o2}(C_pC_c+C_pC_L+C_cC_L)} \approx -\frac{g_{m2}}{C_L}$$ Non-dominant Pole

Two-Stage Op-amp with Miller compensation

- Pole Splitting



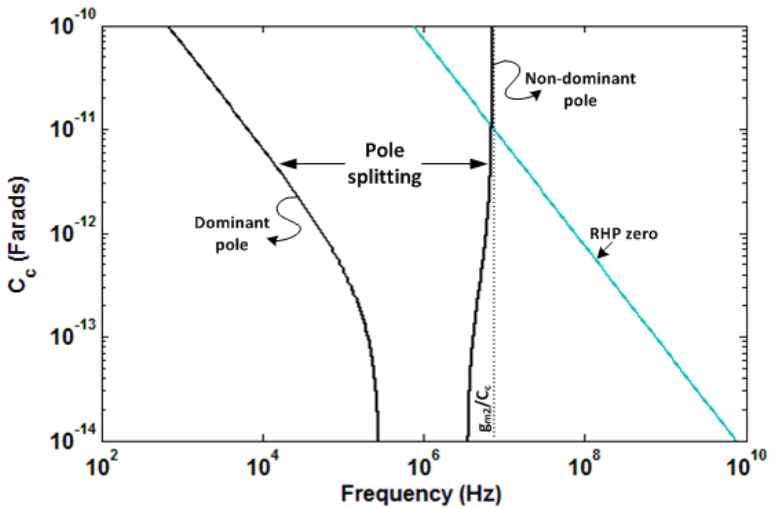
- **Pole/zero locations**

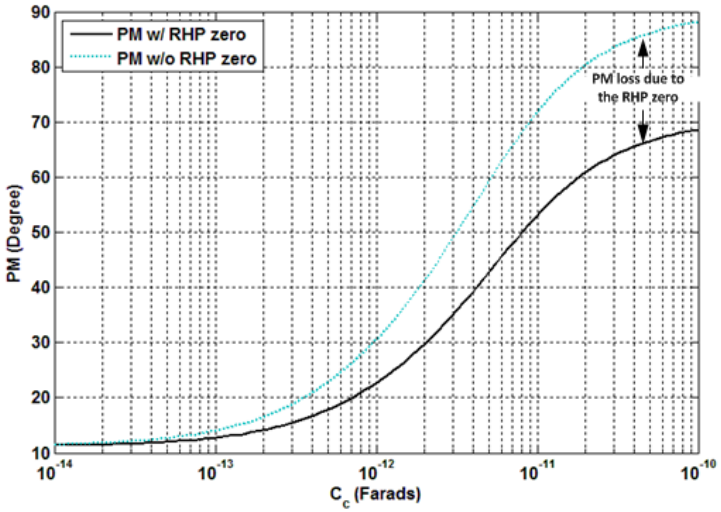
$$S_z = \frac{g_{m2}}{C_c}$$

$$S_{p1} = -\frac{1}{A_{v2} r_{o1} C_c}$$

$$S_{p2} = -\frac{g_{m2}}{C_L}$$

- Pole-zero position diagram

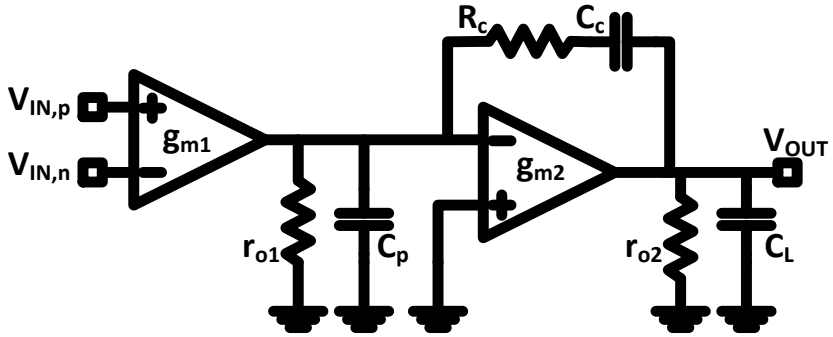




Increasing C_c achieves sufficient pole-splitting thus improving the PM. However, the larger C_c shifts the RHP zero to lower frequencies thus ruining the PM.

Miller Op-amp with Nulling Resistance

- Introducing a small series resistance in series with C_c may cancel the RHP zero or shift it to the LHP.



- **Pole/zero locations**

$$s_z = \frac{1}{\left(\frac{1}{g_{m2}} - R_c\right)C_c}$$

$$s_{p1} = -\frac{1}{A_{v2} r_{o1} C_c}$$

$$s_{p2} = -\frac{g_{m2}}{C_L}$$

$R_c = 1/g_{m2}$	No zero
$R_c > 1/g_{m2}$	LHP zero – Can be used to cancel the first non-dominant pole.

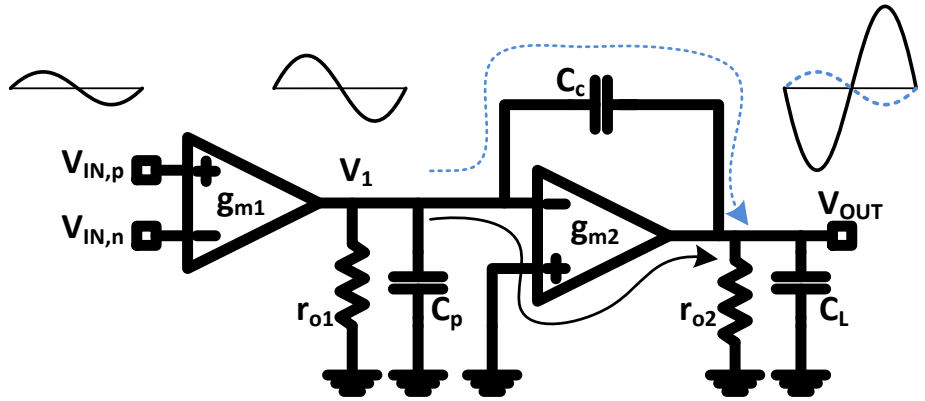
- Disadvantages:
  - To achieve a sufficient phase margin, second pole cross-over of the unity gain frequency should be avoided.

$$f_{p2} \gg GBW \quad \rightarrow \quad C_L \ll \frac{g_{m2}}{g_{m1}} C_c$$

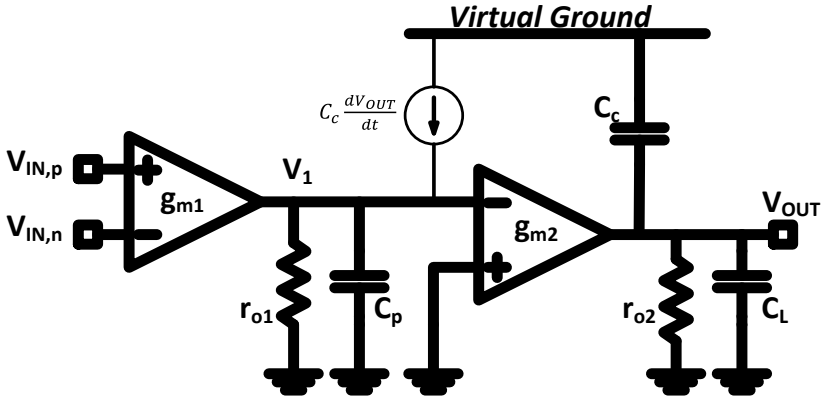
Thus, the Op-amp stability is severely degraded for capacitive loads of the same order as compensation capacitor.

Improved compensation technique

- **The RHP zero is a result of the feed-forward path through C_c.**



- **The RHP zero can be eliminated if we cut the feed-forward path and make the compensation capacitor unidirectional.**

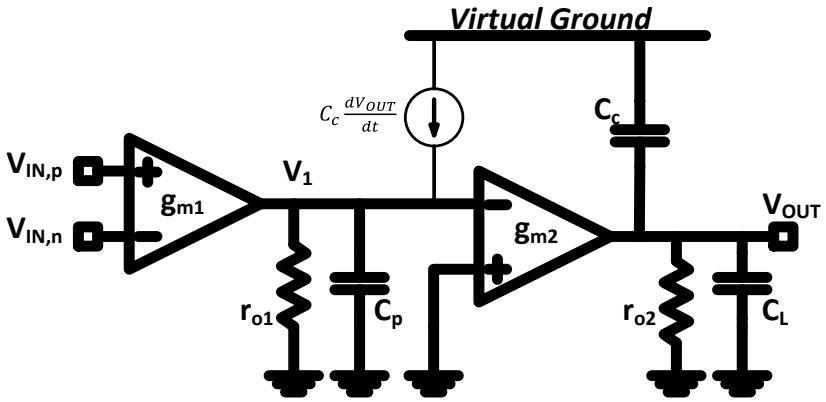


An Improved Frequency Compensation Technique for CMOS Operational Amplifiers

BHUPENDRA K. AHUJA

Improved compensation technique

- The controlled current source injects AC current of $C_c \frac{dV_{OUT}}{dt}$ to the output of the first stage.



- **DC Gain**

$$A_{v,0} = -A_{v1}A_{v2}$$
$$A_{v1} = g_{m1}r_{o1}$$
$$A_{v2} = g_{m2}r_{o2}$$

- **Transfer Function**

$$A_v = \frac{A_{v,0}}{1+(r_{o1}C_p+A_{v2}r_{o1}C_c+r_{o2}(C_c+C_L))s+r_{o1}r_{o2}C_p(C_c+C_L)s^2}$$

- **Pole/zero locations**

$$s_{p1} = -\frac{1}{r_{o1}C_p+A_{v2}r_{o1}C_c+r_{o2}(C_c+C_L)} \approx -\frac{1}{A_{v2}r_{o1}C_c}$$ Dominant Pole

$$s_{p2} = -\frac{r_{o1}C_p+A_{v2}r_{o1}C_c+r_{o2}(C_c+C_L)}{r_{o1}r_{o2}C_p(C_c+C_L)} \approx -\frac{g_{m2}C_c}{C_p(C_c+C_L)}$$ Non-dominant Pole

- **To achieve sufficient PM**

$$f_{p2} \gg GBW \quad \rightarrow \quad C_L \ll \frac{g_{m2}}{g_{m1}}\frac{C_c^2}{C_p}$$

Improved compensation technique

- **Numerical example**

Miller compensation with nulling resistance	Improved compensation technique
Dominant pole $\omega_d = \frac{1}{g_{m2} r_{o1} r_{o2} C_c}$	**Dominant pole** $\omega_d = \frac{1}{g_{m2} r_{o1} r_{o2} C_c}$
Non-dominant pole $\omega_{nd} = \frac{g_{m2}}{C_L}$	**Non-dominant pole** $\omega_{nd} = \frac{g_{m2} C_c}{C_p (C_c + C_L)}$
Gain-bandwidth product $GBW = \frac{g_{m1}}{C_c}$	**Gain-bandwidth product** $GBW = \frac{g_{m1}}{C_c}$
Phase margin $PM = 90 - \tan^{-1}\left(\frac{GBW}{\omega_{nd}}\right)$	**Phase margin** $PM = 90 - \tan^{-1}\left(\frac{GBW}{\omega_{nd}}\right)$

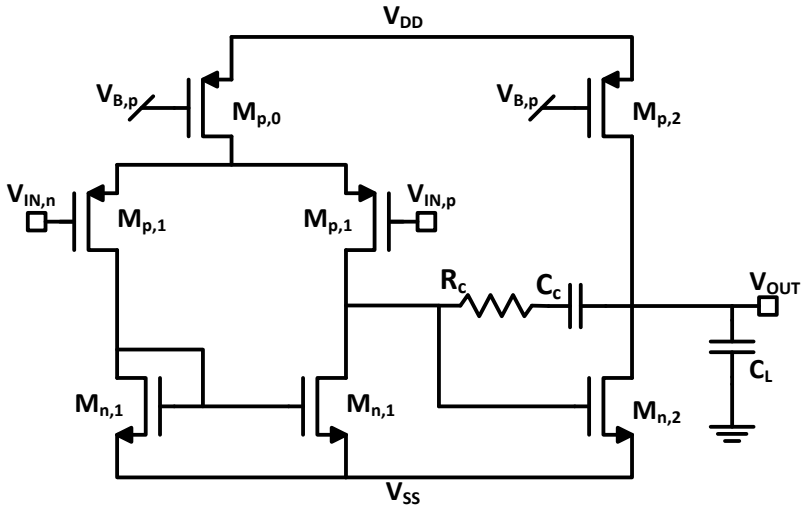
- If $\frac{g_{m2}}{g_{m1}} = 10, C_c = 5\ pF, C_p = 0.5\ pF, and\ \frac{\omega_{nd}}{GBW} \geq 4$ for $PM > 75°$

$C_L \leq \frac{GBW}{\omega_{nd}} \frac{g_{m2}}{g_{m1}} C_c \rightarrow C_L \leq 12.5\ pF$	$C_L \leq \frac{GBW}{\omega_{nd}} \frac{g_{m2}}{g_{m1}} \frac{C_c^2}{C_p} \rightarrow C_L \leq 125\ pF$

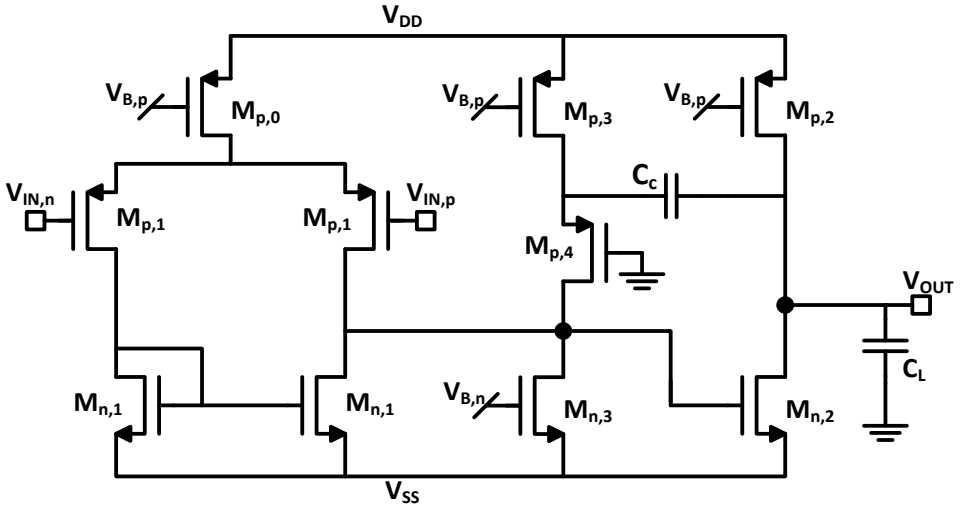
- The improved technique offers an order of magnitude improvement in capacitive load capability for the same performance.

Circuit Implementation

- **Miller compensation with nulling resistance.**

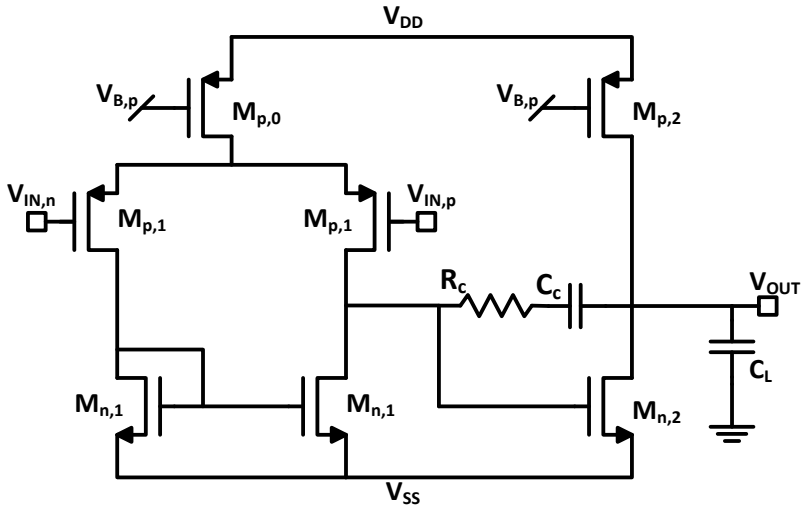


- **Improved compensation technique.**

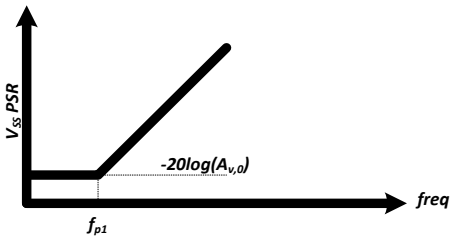


Other performance parameters- PSR

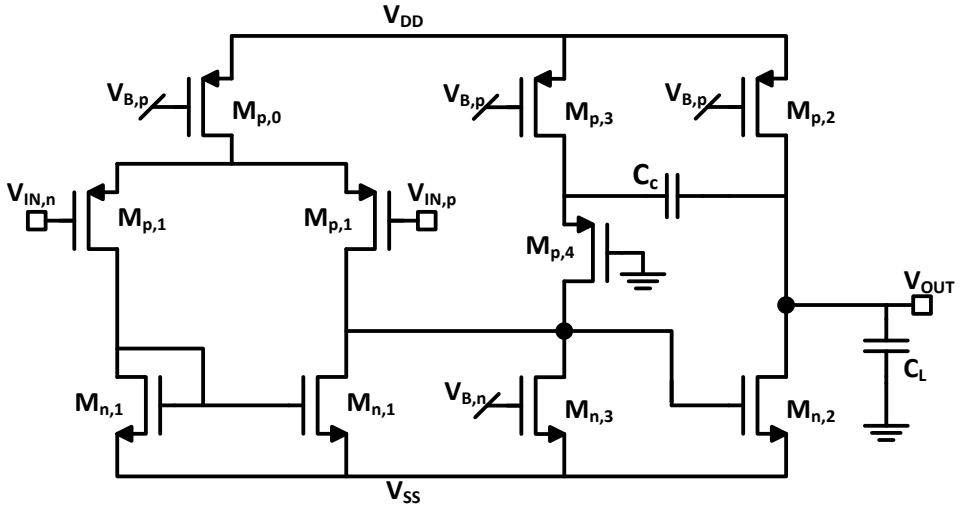
- **Miller compensation with nulling resistance.**



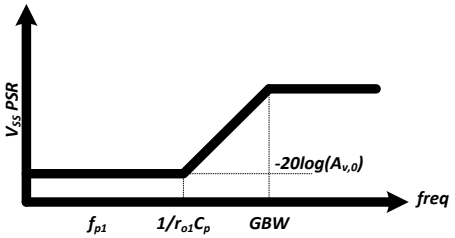
$$\frac{V_{OUT}}{V_{SS}} = \frac{1 + sA_{v2}C_c r_{o1}}{g_{m1}g_{m2}r_{o1}r_{o2}}$$



- **Improved compensation technique.**



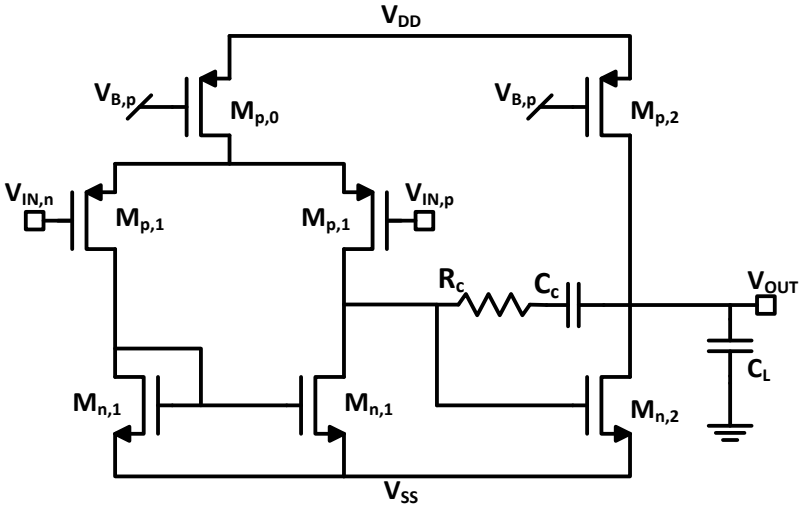
$$\frac{V_{OUT}}{V_{SS}} = \frac{1 + sC_p r_{o1}}{g_{m1}g_{m2}r_{o1}r_{o2}\left(1 + \frac{s}{GBW}\right)}$$



- **Better PSR at high frequencies.**

Design Example – Miller Compensation

- **Design an OTA with GBW > 5MHz, C_L=10pF, PM>70, and SR> 2 V/µs.**



- Choose C_c=C_L/2= 5 pF.
- GBW > 5MHz

$$GBW = \frac{g_{m1}}{C_c} \rightarrow g_{m1} \geq 157\ \mu S$$

- SR > 2 V/µS

$$SR = \frac{I_{p,0}}{C_c} \rightarrow I_{p,0} \geq 20\ \mu A$$

- PM > 70°

$$PM = 90 - \tan^{-1}\left(\frac{GBW}{\omega_{nd}}\right) \rightarrow \omega_{nd} \geq 2.7GB$$

Let

$$\omega_{nd} = 3 \times GBW = \frac{g_{m2}}{C_L} \rightarrow \frac{g_{m2}}{g_{m1}} = 3\frac{C_L}{C_c} = 6$$

Then

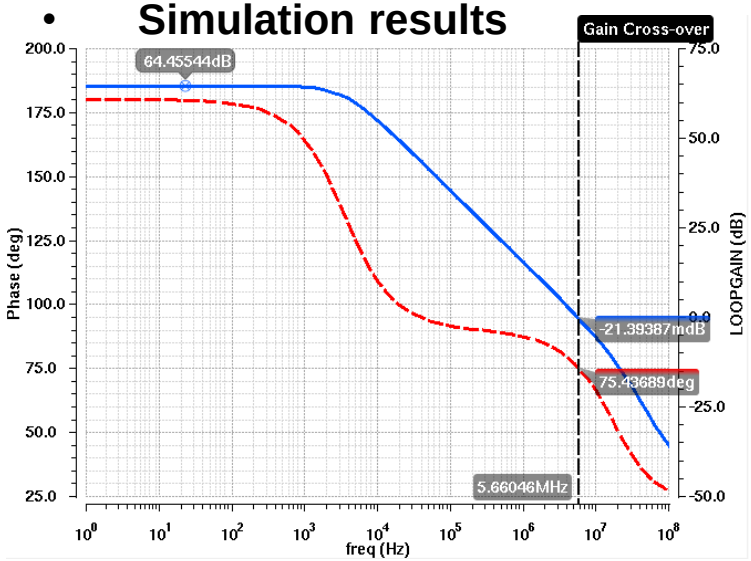
$$g_{m2} = 6g_{m1} \cong 1\ mS \rightarrow I_{p,2} = 3I_{p,0}$$

- Choose $R_c > 1/g_{m2}$

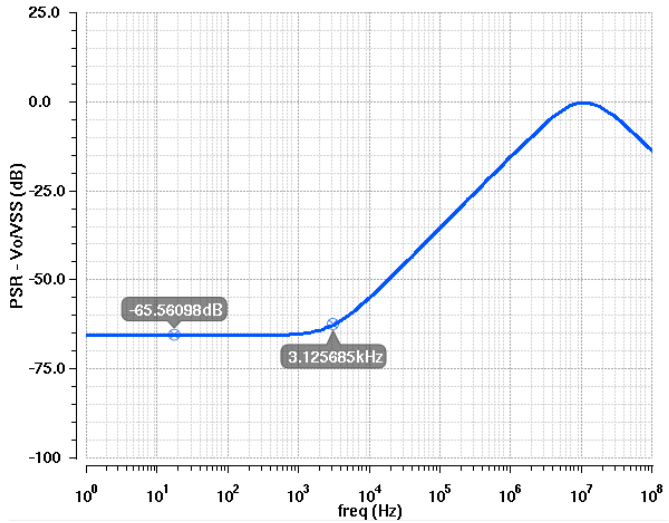
$$R_c \geq 1\ K\Omega$$

Design Example – Miller Compensation

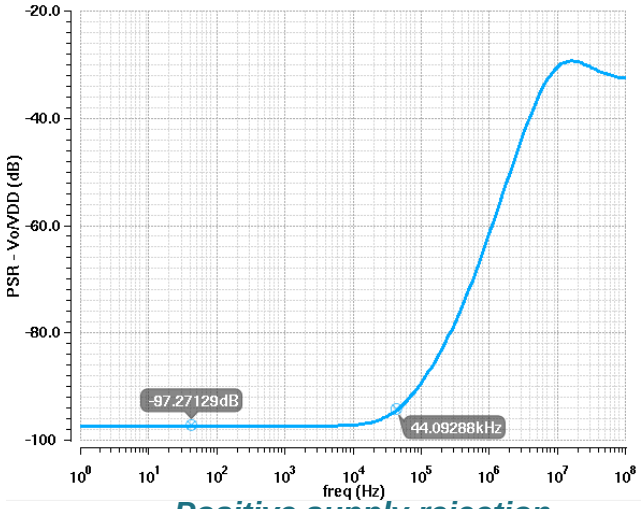
- **Simulation results**



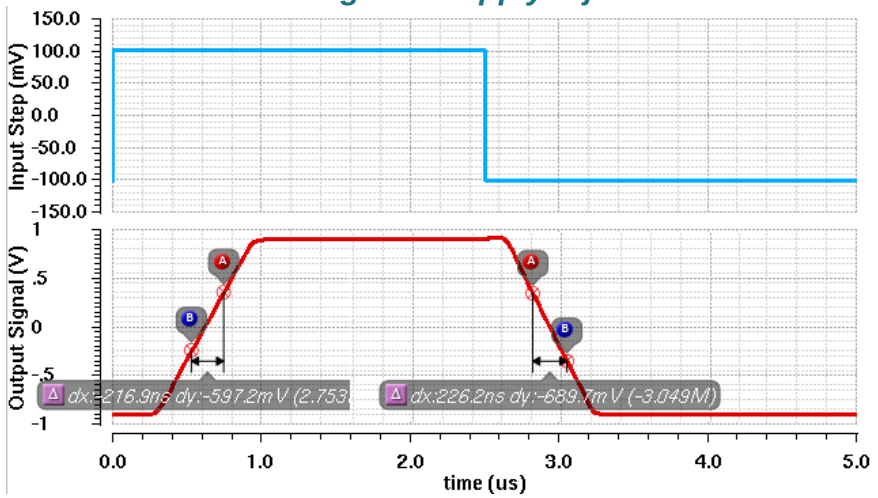
OL Transfer function



Negative supply rejection



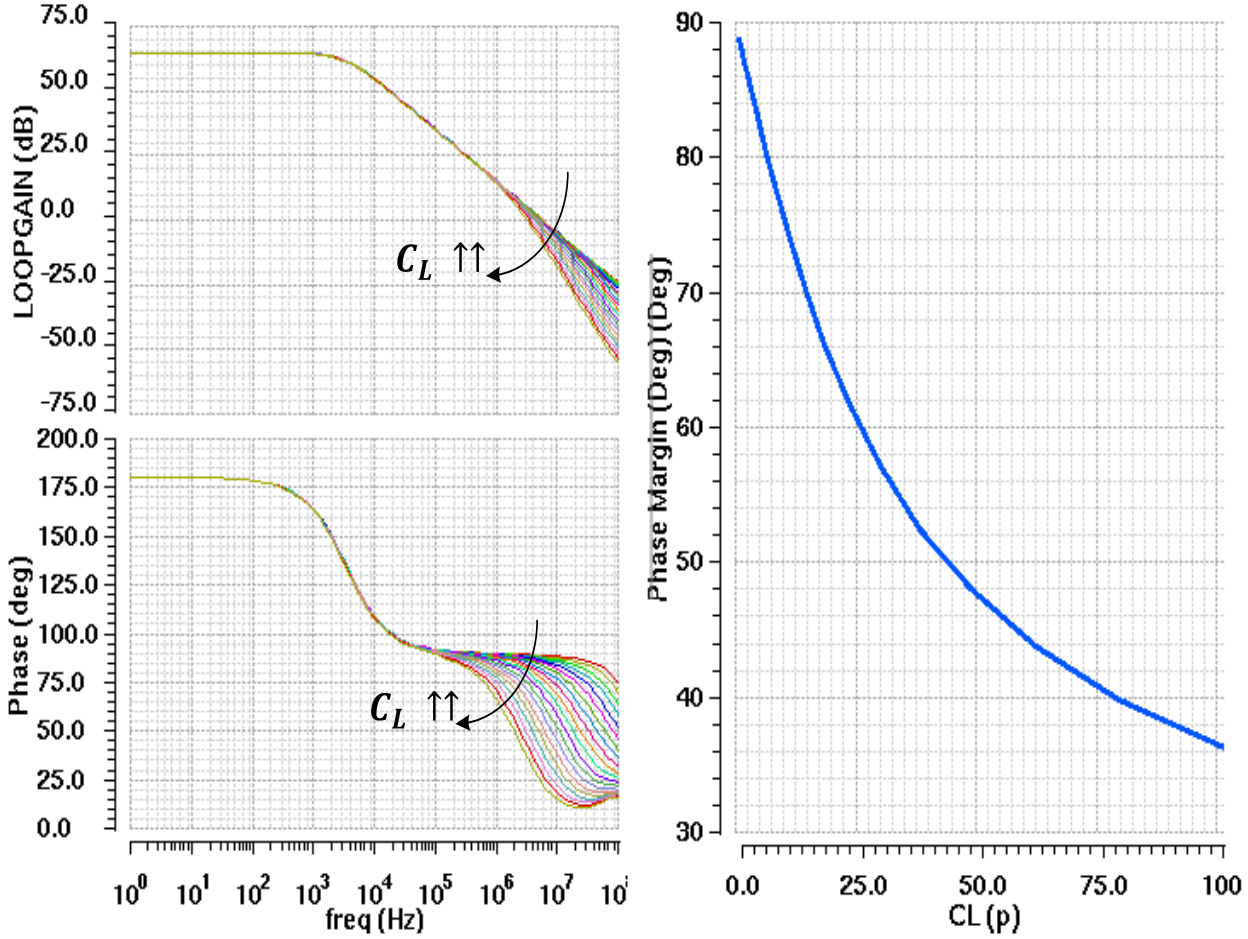
Positive supply rejection



Transient step response

Design Example – Miller Compensation

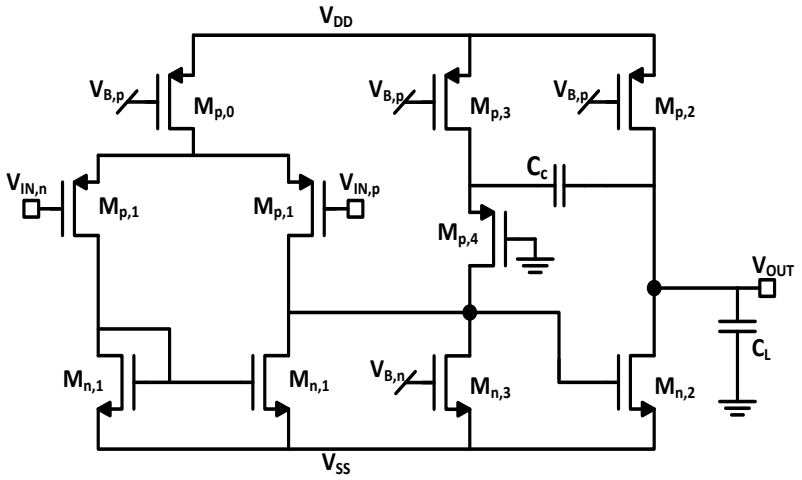
- **Capacitive load driving capability**



- PM > 70° for C_L < 15 pF.

Design Example – Improved Compensation

- **Design an OTA with GBW > 5MHz, C_L=10pF, PM>70, and SR> 2 V/µs.**



- Choose $C_c=C_L/2$= 5 pF.
- GBW > 5MHz

$$GBW = \frac{g_{m1}}{C_c} \rightarrow g_{m1} \geq 157\ \mu S$$

- SR > 2 V/µS

$$SR = \frac{I_{p,0}}{C_c} \rightarrow I_{p,0} \geq 20\ \mu A$$

In order to make the current transformer biased during slewing interval

$$I_{p3} > I_{p0} \rightarrow I_{p,3} = 30\ \mu A$$

- PM > 70°

$$PM = 90 - \tan^{-1}\left(\frac{GBW}{\omega_{nd}}\right) \rightarrow \omega_{nd} \geq 2.7GBW$$

Let

$$\omega_{nd} = 3 \times GBW = = \frac{g_{m2}C_c}{C_p(C_c+C_L)} \rightarrow \frac{g_{m2}}{g_{m1}} = 0.3$$

Then

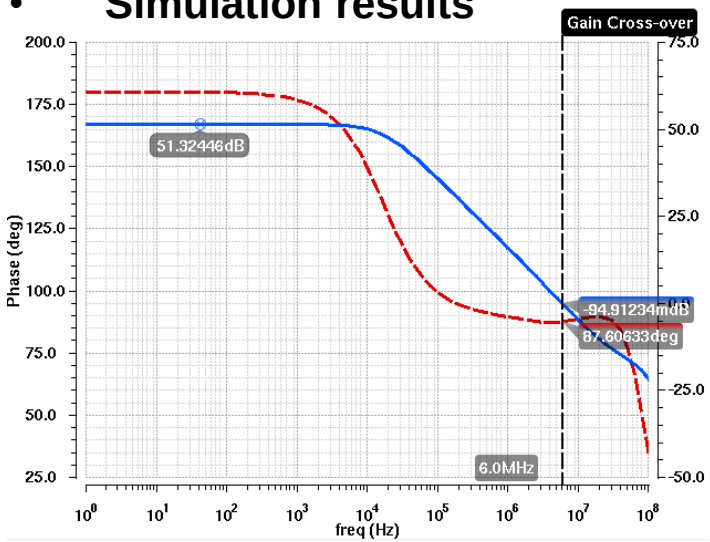
$$g_{m2} = 0.3g_{m1} \cong 52\ \mu S \rightarrow I_{p,2} = 0.3I_{p,0}$$

✓ Let's use g_{m2}=6gm1 like the miller Op-amp to make a comparison between the capacitive driving capability.

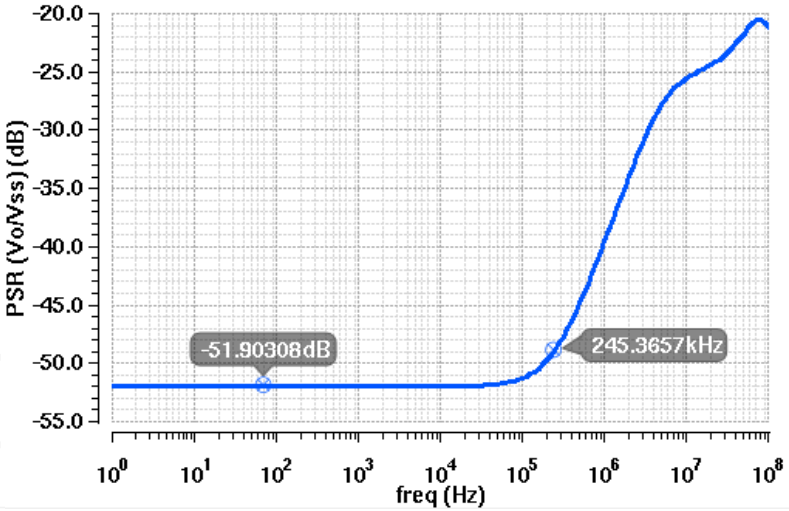
✓ For the same capacitive load driving capability, the second stage will consume less current making it suitable for low power applications

Design Example – Improved Compensation

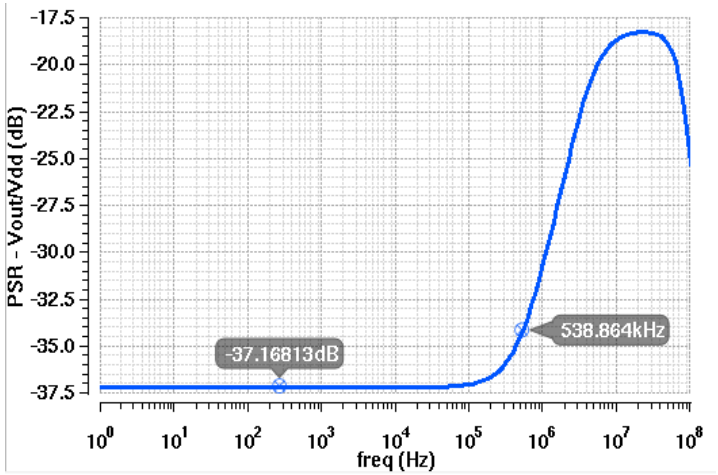
- **Simulation results**



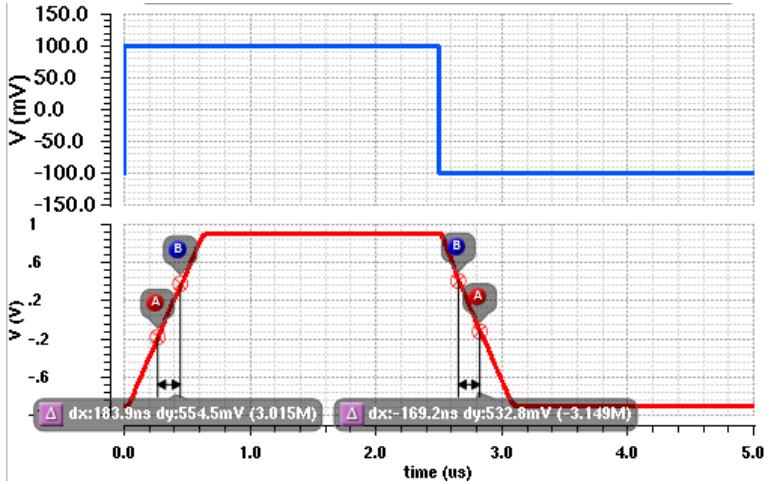
OL Transfer function



Negative supply rejection



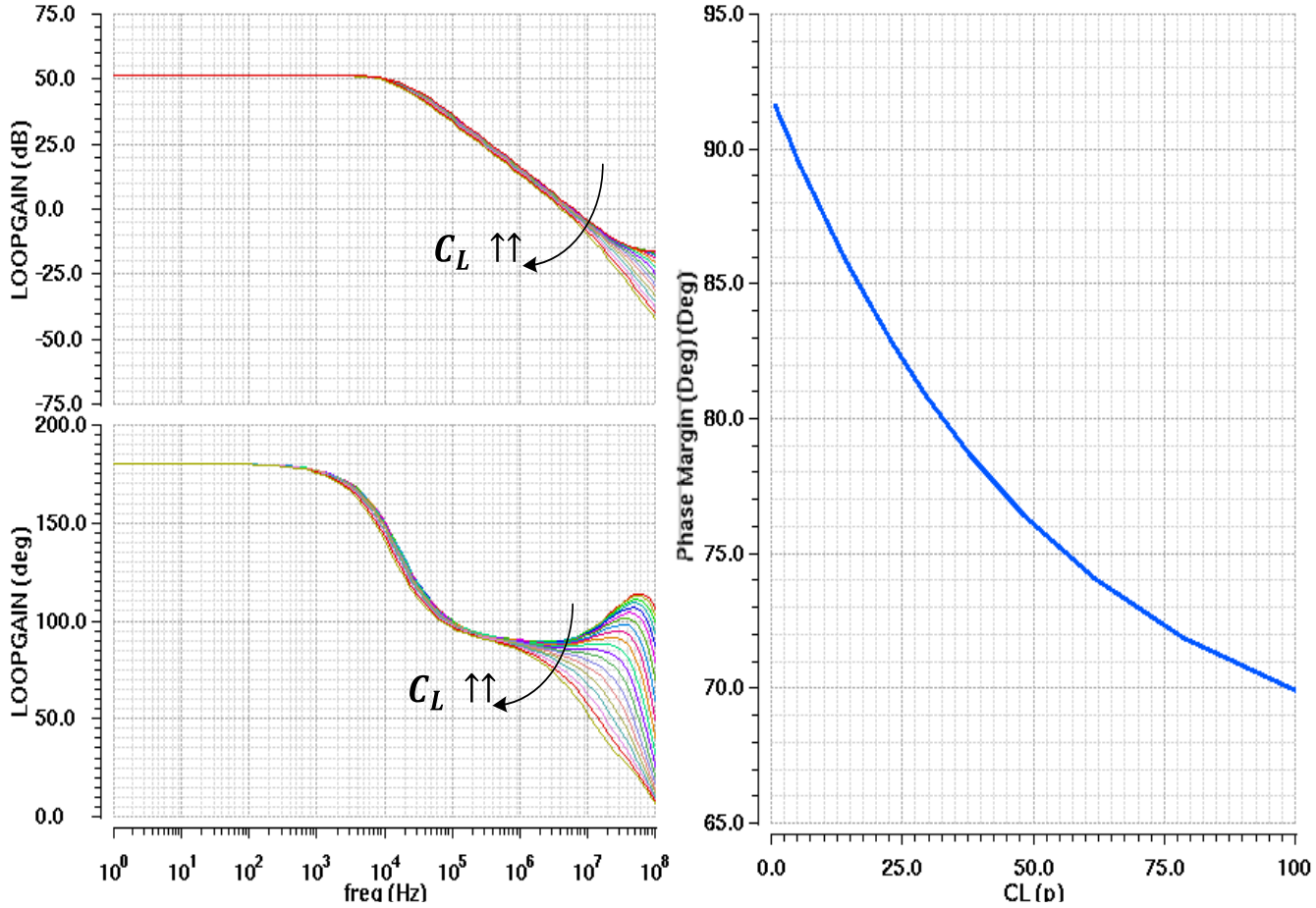
Positive supply rejection



Transient step response

Design Example – Improved Compensation

- **Capacitive load driving capability**



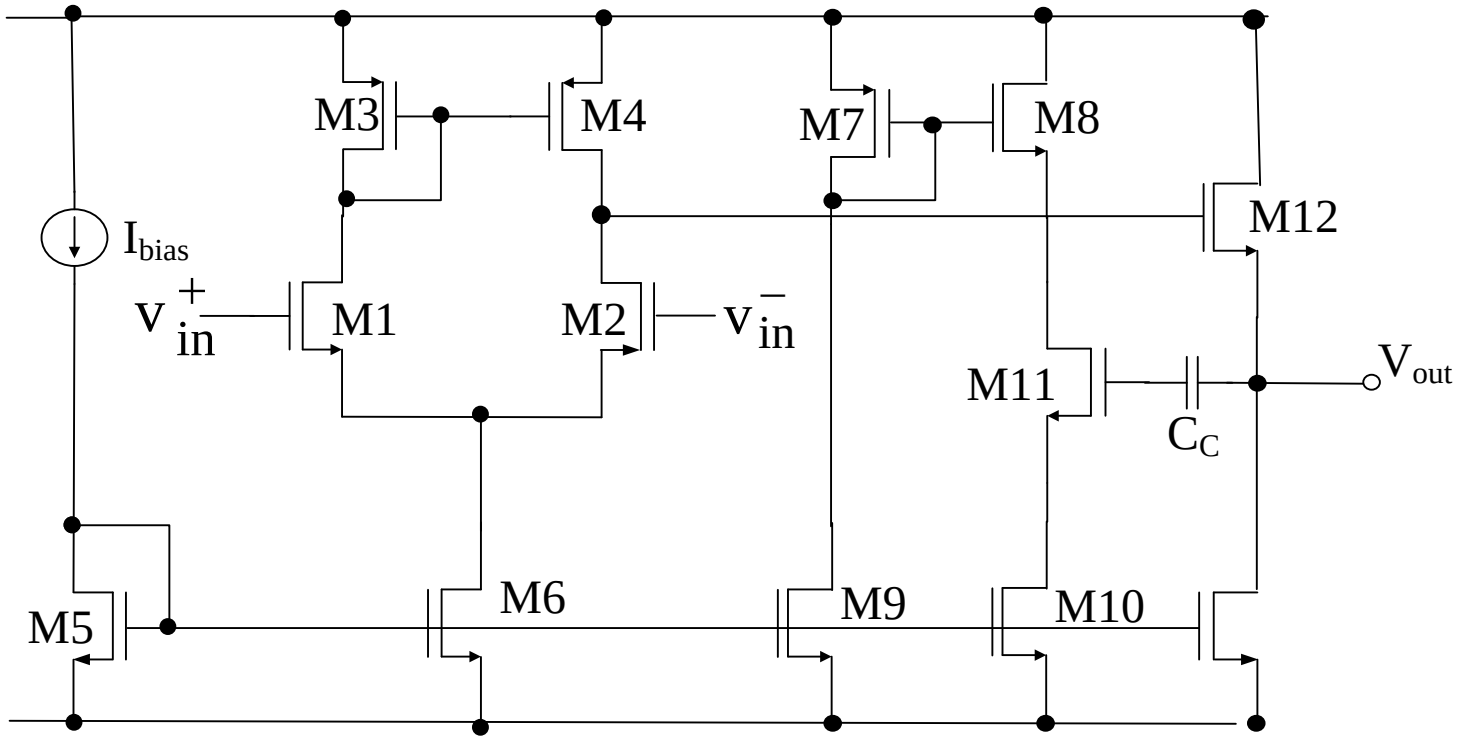
- PM > 70° for C_L < 100 pF.

Design Example – Improved Compensation

- **Summary of Simulation results**

Parameter	Spec	Miller Compensation	Improved Compensation
GBW	> 5MHz	5.5 MHz	6 MHz
PM	> 70°	75°	87.6°
SR^+	> 2 V/µs	2.75 V/µs	3 V/µs
SR^-	> 2 V/µs	3 V/µs	3.15 V/µs
PSR^-	-	-65.6 dB At (0-3.1 kHz)	-51.9 dB At (0-245.4 kHz)
PSR^+	-	-97.2 dB At (0-44 kHz)	-37.2 dB At (0-538.9 kHz)
DC gain	-	64.5 dB	51.3 dB
Current consumption	-	80 µA	110 µA
Capacitive load driving capability	-	PM > 70° for C_L < 15 pF	PM > 70° for C_L < 100 pF

Using another current buffer Op Amp topology.

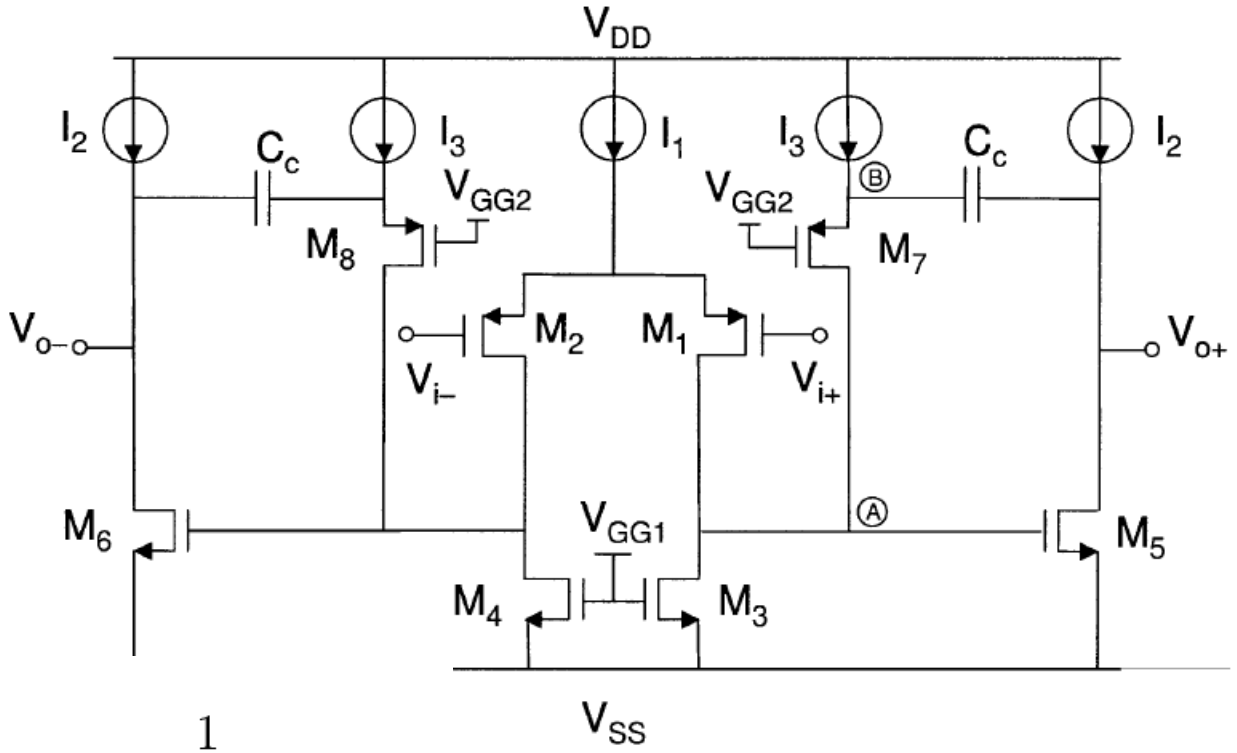


Two-Stage amplifier with Current Buffer compensation scheme.

• Improve SR at the expense of power consumption.

25

Differential Output Two Stage Amp with a capacitor compensation with a current Buffer (Common Gate)



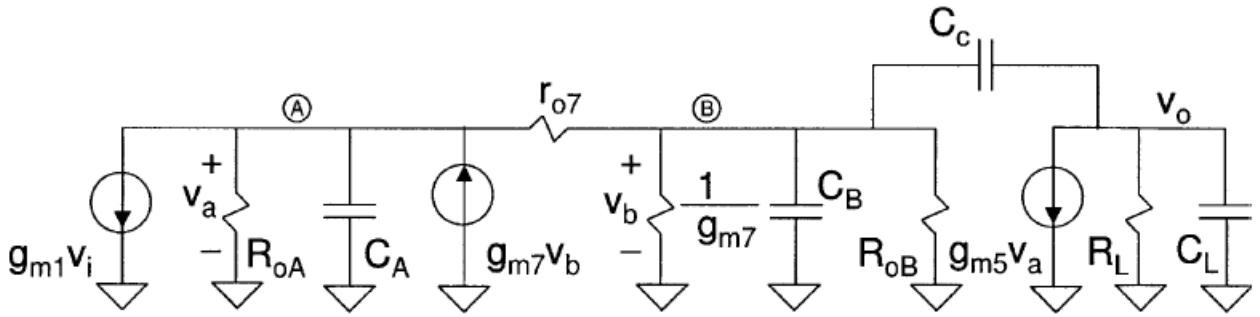
$$p_1 \approx -\frac{1}{g_{m5} R_L R_{oA} C_c} \ .$$

$$p_2 \approx -\frac{g_{m5}}{(C_L + C_c)} \frac{C_c}{C_A}$$

$$z \approx -\frac{g_{m7}}{C_B + C_c} \ .$$

$\mathrm{gm7} \to \infty$ then $\mathrm{p3} \to \infty$

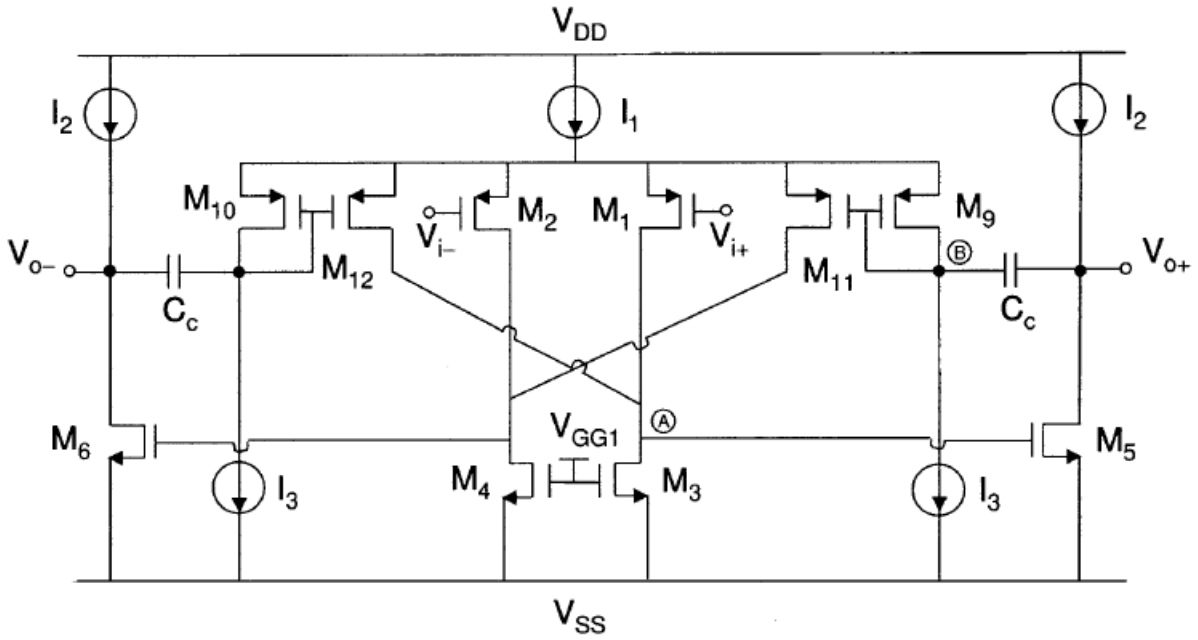
Differential mode half circuit of previous topology



Element	Fig. 1(a)
R_{oA}	$r_{o1}\|\|r_{o3}$
C_A	$C_{gs5}+C_{db1}+C_{db3}+C_{db7}$
R_{oB}	∞ *
C_B	$C_{gs7}+C_{sb7}$ **
R_L ***	r_{o5}
C_L ****	C_{db5}

Note that this and previous structure are fully differential but this approach could be used for single output topologies.

Compensation using a current buffer (current gain)



Note that the current-mirror introduces an extra inversion which must be taken into consideration for the single ended version.

P.J. Hurst, Lewis, S.H. ; Keane, J.P. ; Aram, F. ; Dyer, K.C.
" Miller compensation using current buffers in fully differential CMOS two-stage operational amplifiers" *IEEE Transactions on Circuits and Systems I*, Volume: 51 , Issue: 2, Feb. 2004

Element	
R_{oA}	$r_{o1}\|\|r_{o3}\|\|r_{o11}$
C_A	$C_{gs5}+C_{db1}+C_{db3}+C_{db11}$
R_{oB}	r_{o9} *
C_B	$C_{gs9}+C_{gs11}+C_{db9}$ **
R_L ***	r_{o5}
C_L ****	C_{db5}

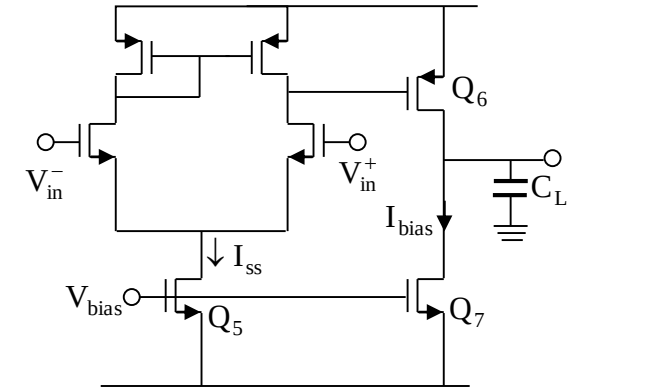
$$z \approx -\frac{g_{m11}}{C_B + C_c}.$$

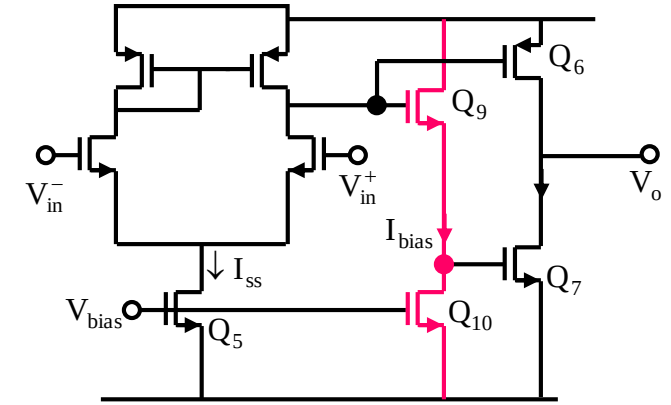
Besides the above zero the amp has three poles

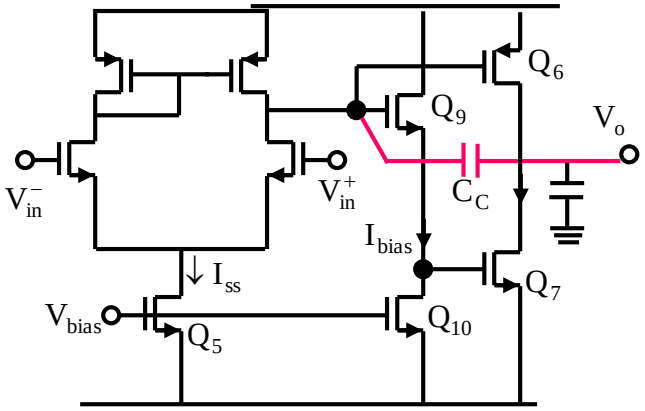
Elements of Current-Mirror Cc compensated

Note that the common-gate and current mirror topologies under ideal case are almost identical, however in practice the one using current-mirrors is more power hungry and has a larger parasitic capacitance C_B

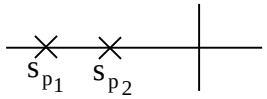
Summary for Two Stage Op Amp Architecture Designs







- Roots close to the jω axis for uncompensated



- Potentially unstable for some values of C_L

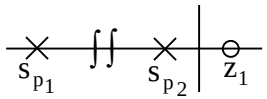
  $I_{bias} = C_L S_R * 2.5$

- Improved output stage optimal bias of Q_6 and Q_7
- No significant change of pole locations.

  A_v (0) -> +

  A_v (ω) -> -

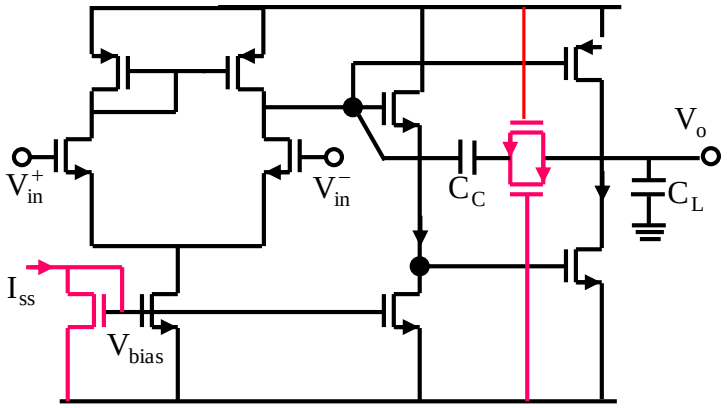
Pole splitting => one dominant pole



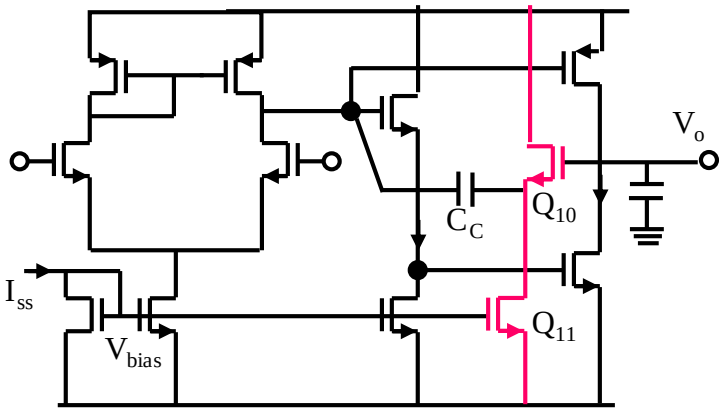
z_1 Phase deteriorates phase margin

The good and the bad news

Two possible solutions to cancel z_1 and keeping $s_{p2} > \omega_t$ =GBW and s_{p1} small



Internally Compensated with R_C C_C



Internally Compensated with unity gain buffer (Q_{10}, Q_{11})

Operational Amplifier (conventional) Architectures.

Reader.- See the internally Op Amp compensated with current gain buffer in previous pages

Folded Cascode Op Amp

- Compared to two-stage Op Amp, **folded cascode Op Amp** has:
  - Improved input common-mode range (ICMR)
  - Improved power supply rejection (PSR)
  - Push-pull output stage
  - Self compensation

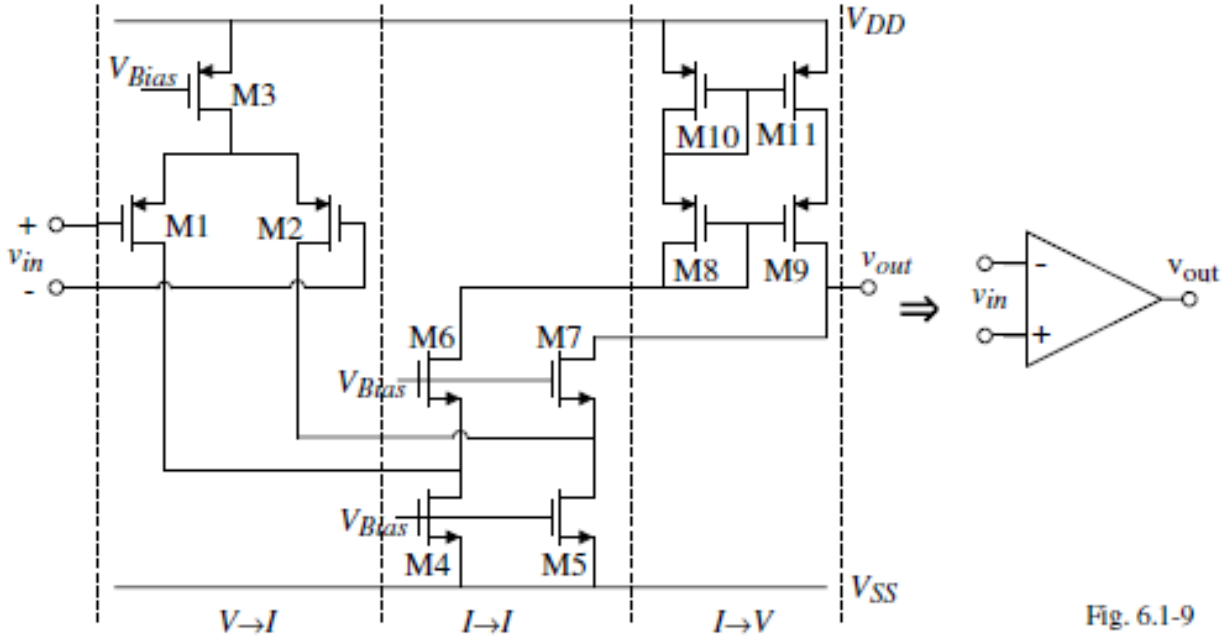
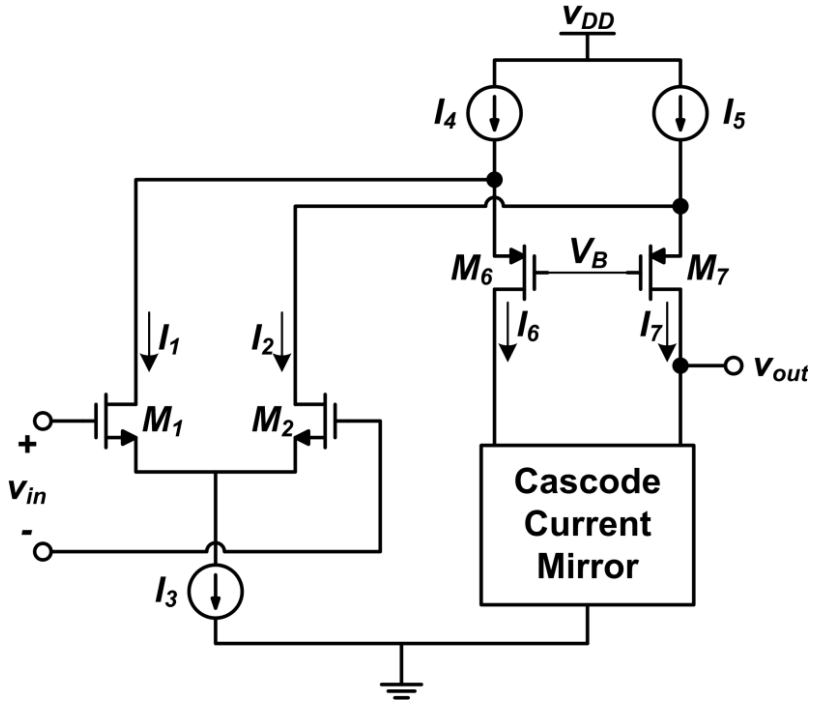
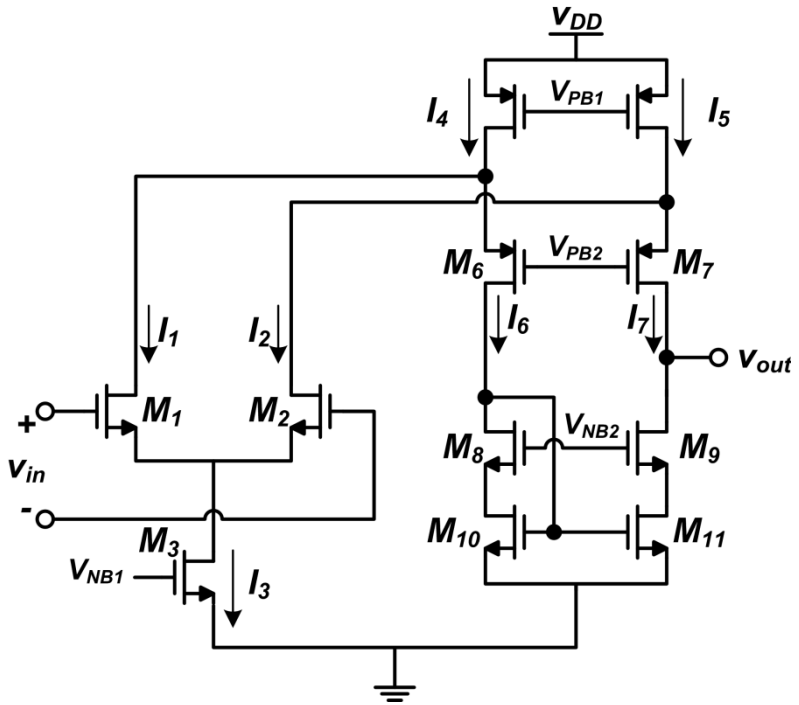


Fig. 6.1-9

Folded-cascode Op Amp broken into stages [Allen]

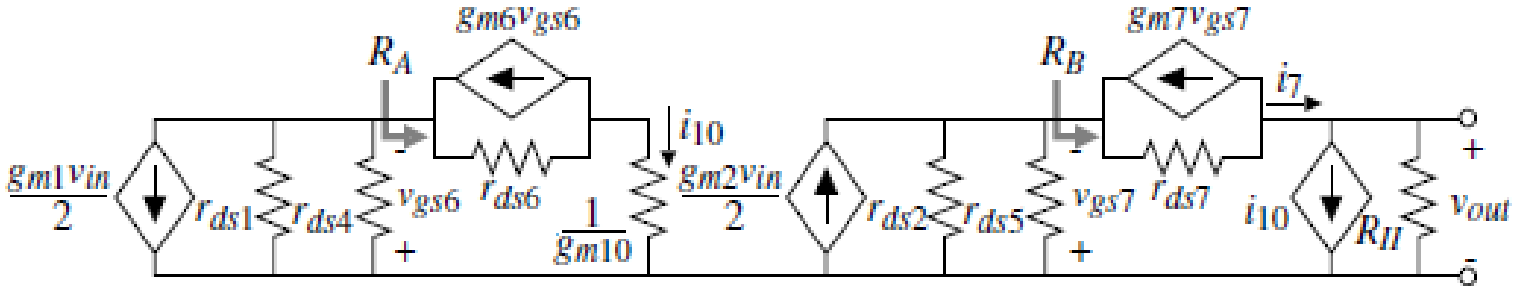
Folded Cascode OpAmp





- The extended ICMR is achieved
- The bias currents I4 and I5 should be designed such that I6 and I7 never goes to zero (i.e. $I_{4,5} = 1.2I_3 \rightarrow 1.5I_3$)
- Poor noise performance: In addition to the input transistors, transistors $M_{4,5}$ and $M_{10,11}$ generate significant current noise

Small Signal Analysis



R_A and R_B are the resistances looking into the sources of M_6 and M_7

$$R_A = \frac{r_{ds6}+1/g_{m10}}{1+g_{m6}r_{ds6}} \approx \frac{1}{g_{m6}} \text{ and } R_B = \frac{r_{ds7}+R_{II}}{1+g_{m7}r_{ds7}} \approx \frac{R_{II}}{g_{m7}r_{ds7}} \text{ where } R_{II} = g_{m9}r_{ds9}r_{ds11}$$

The currents i_7 and i_{10} is expressed as

$$i_7 = \frac{g_{m2}(r_{ds2}\|r_{ds5})}{R_B+(r_{ds2}\|r_{ds5})}\frac{v_{in}}{2} = \frac{g_{m2}}{k+1}\frac{v_{in}}{2} \quad \text{where} \quad k = \frac{R_B}{r_{ds2}\|r_{ds5}}$$

$$i_{10} = -\frac{g_{m1}(r_{ds1}\|r_{ds4})}{R_A+(r_{ds1}\|r_{ds4})}\frac{v_{in}}{2} \approx -g_{m1}\frac{v_{in}}{2}$$

Thus, the transfer function can be found as follows

$$\frac{v_{out}}{v_{in}} = \left(\frac{g_{m1}}{2} + \frac{g_{m2}}{2(k+1)}\right)R_{out} = \left(\frac{2+k}{2+2k}\right)g_{m1}R_{out}$$

Where

$$R_{out} = g_{m9}r_{ds9}r_{ds11}\left\|g_{m7}r_{ds7}\left(r_{ds2}\right\|r_{ds5}\right)$$

Where k is the low-frequency unbalance factor

Frequency Response

- The frequency response is dominated primarily by the output pole due to the high output impedance

$$P_{out} = \frac{-1}{R_{out}C_{out}}$$

- In order to have sufficient phase margin, all other pole should be located will above the GBW

Pole at source of M_6 (Folding node) $\quad P_A = -\frac{1}{R_A(C_{gs}+2C_{bd})} \approx -\frac{g_{m6}}{C_{gs}+2C_{bd}}$

Pole at source of M_7 (Folding node) $\quad P_B = -\frac{1}{R_B(C_{gs}+2C_{bd})} \approx -\frac{g_{m7}}{C_{gs}+2C_{bd}}$

Pole at drain of M_6 $\quad P_6 = -\frac{g_{m10}}{2C_{gs}+2C_{bd}}$

Pole at source of M_8 $\quad P_8 = -\frac{g_{m8}r_{ds8}g_{m10}}{C_{gs}+C_{bd}}$

Pole at source of M_9 $\quad P_9 = -\frac{g_{m9}}{C_{gs}+C_{bd}}$

- **Remarks:**

We assumed $R_B \approx 1/g_{m7}$ because at high frequency, where this pole has influence, C_{out} shunts the drain of M_7 to ground.

Power Supply Rejection

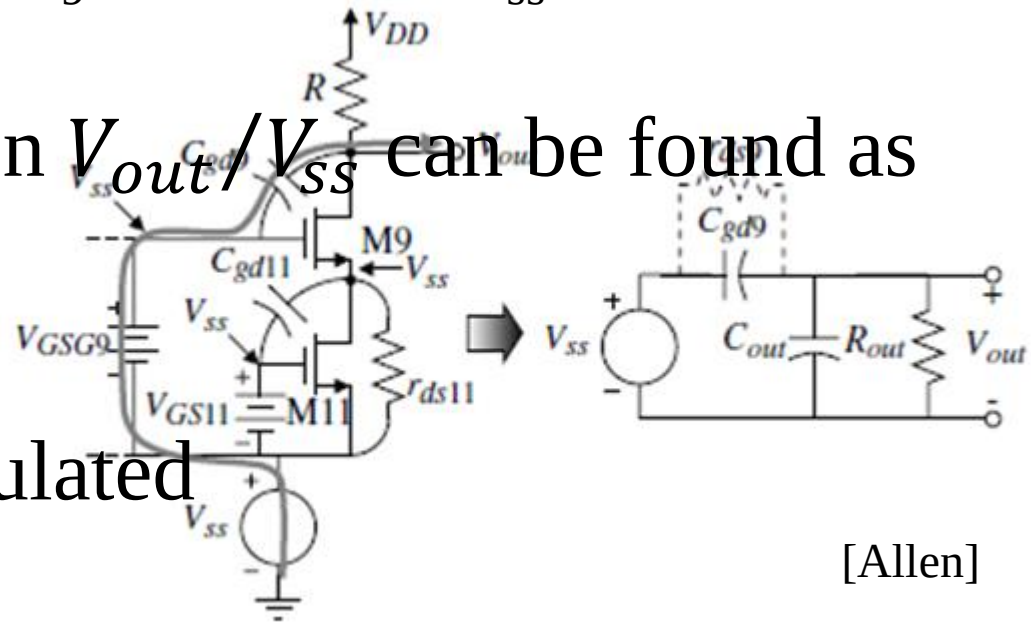
- The following model is used to calculate the negative PSR
  - The gate, source and drain of M_{11} varies with V_{SS}
  - The gate, source of M_9 varies with V_{ss}

- The transfer function V_{out}/V_{ss} can be found as

$$\frac{V_{out}}{V_{ss}} = \frac{sC_{gd9}R_{out}}{sC_{out}R_{out}+1}$$

- $PSRR^-$ can be calculated

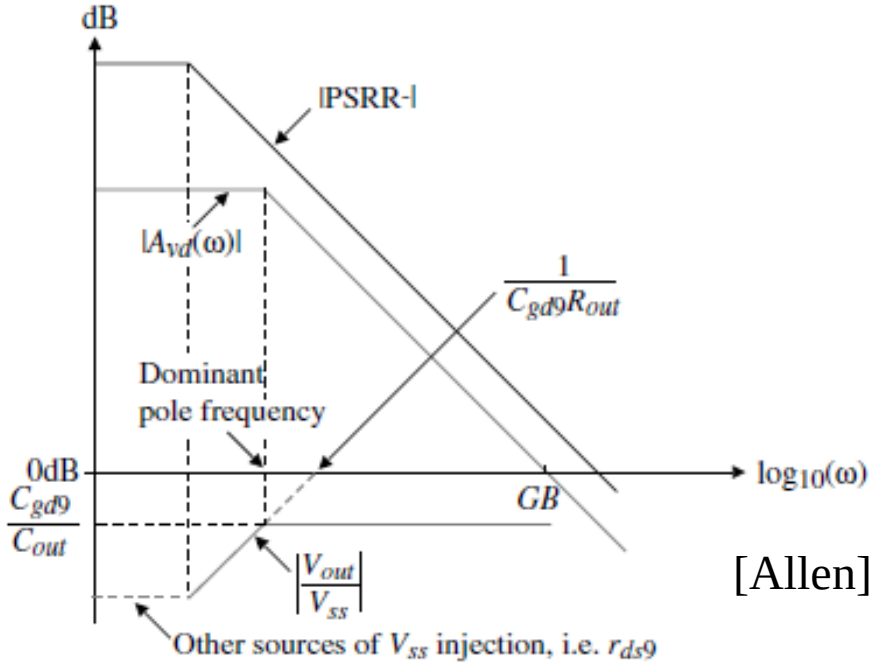
$$PSRR^- = \frac{A_v}{|V_{out}/V_{ss}|}$$



[Allen]

Output stage of folded cascode OpAmp

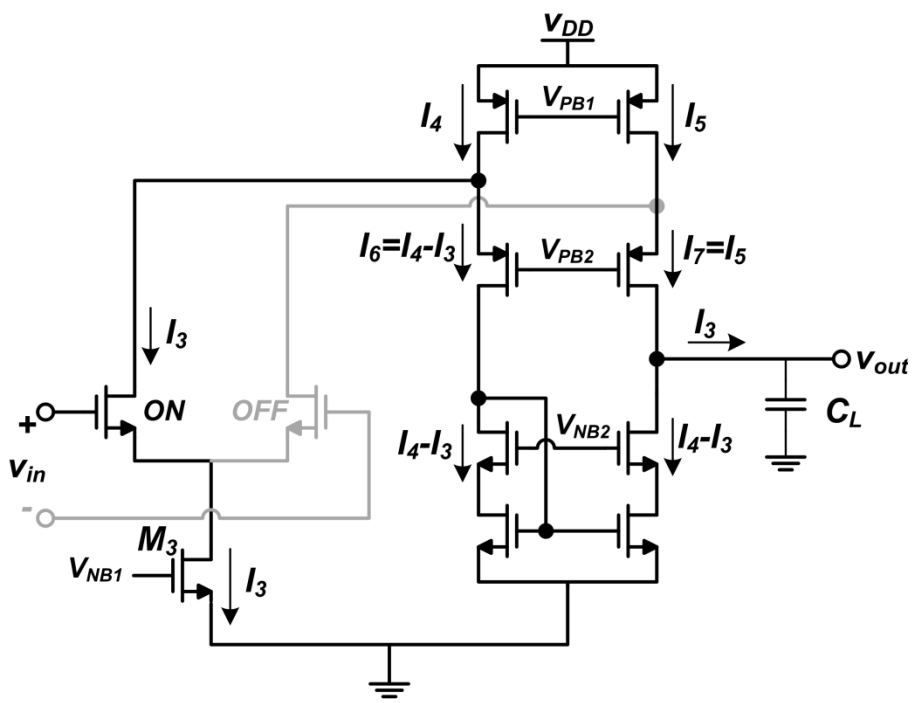
Power Supply Rejection

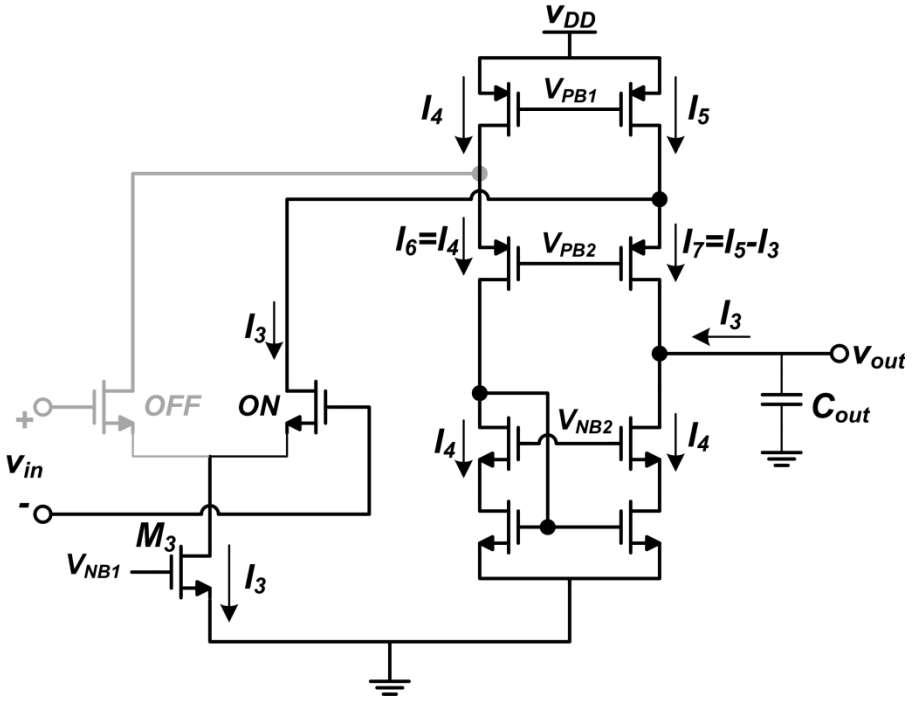


[Allen]

- At low frequency, we assume that other source of V_{ss} injection becomes significant
- Low frequency PSRR$^-$ is at least as large as the magnitude of the differential voltage gain A_v
- PSRR$^+$ can be derived similarly: the primary source of injection is through

Slew Rate



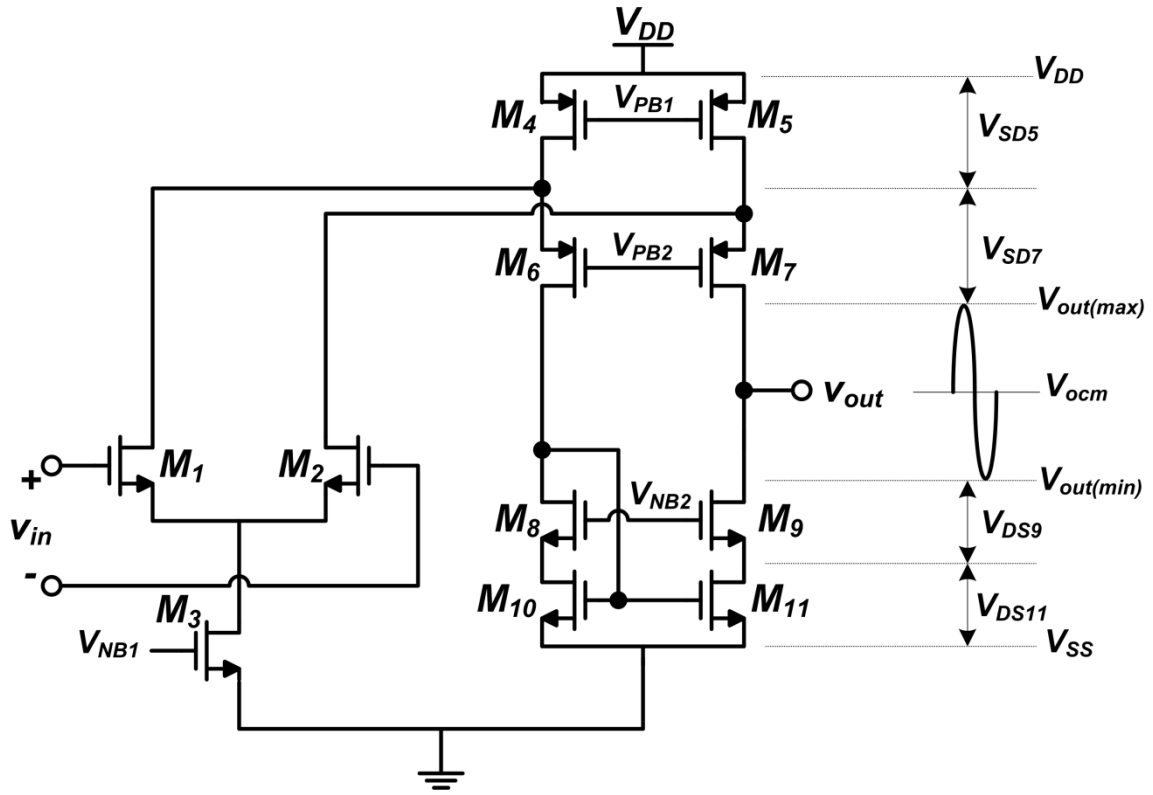


$$SR^+ = SR^- = \frac{I_3}{C_L}$$

- The bias currents $I_{4,5}$ should be designed such that $I_{6,7}$ never goes to zero

$$I_{4,5} = 1.2I_3 \rightarrow 1.5I_5$$

Maximum Available Output Swing



$$V_{out(max)} = V_{DD} - V_{SD5} - V_{SD7}$$
$$V_{out(min)} = V_{ss} + V_{DS9} + V_{DS11}$$

- The output common mode level V_{ocm} is often dictated by the circuit that interface with the amplifier (e.g. $V_{ocm} = V_{DD}/2$)

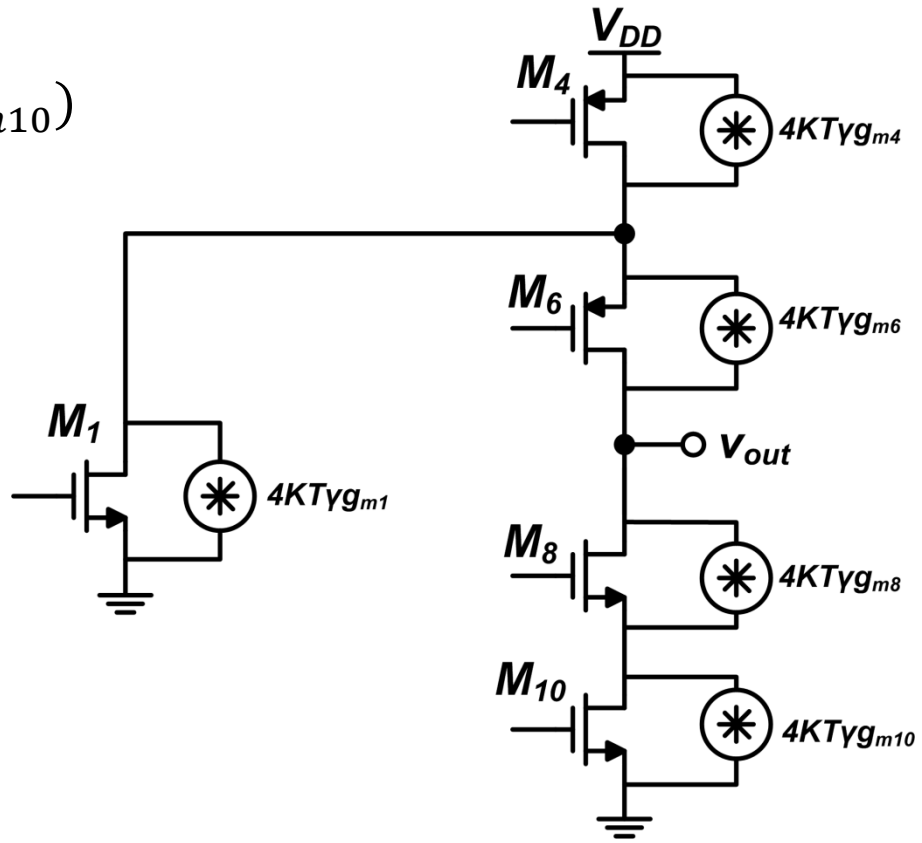
Noise Analysis

- The noise current of M_1, M_4 and M_{10} goes directly to the output
- At low and medium frequencies, noise contribution of the cascode transistors (M_6 and M_8) can be neglected
- Total output noise current becomes

$$\overline{i_{out}^2} = 8KT\gamma(g_{m1} + g_{m4} + g_{m10})$$

- Input referred noise density

$$\overline{v_{n,in}^2} = \frac{8KT\gamma}{g_{m1}}\left(1 + \frac{g_{m4}}{g_{m1}} + \frac{g_{m10}}{g_{m1}}\right)$$



Half circuit model

Folded Cascode Op Amp Design Procedure

- Design approach for the folded cascode Op Amp using long-channel model

Step	Relationship	Design Equation/Constraint	Comments
1	Slew Rate	$I_3 = SR \cdot C_L$	
2	Bias currents in output cascodes	$I_4 = I_5 = 1.2I_3$ to $1.5I_3$	Avoid zero current in cascodes
3	Maximum output voltage, $v_{out}(\max)$	$S_5 = \frac{2I_5}{K_P' V_{SD5}^2}$, $S_7 = \frac{2I_7}{K_P' V_{SD7}^2}$, ($S_4 = S_5$ and $S_6 = S_7$)	$V_{SD5}(\text{sat}) = V_{SD7}(\text{sat}) = 0.5[V_{DD} - V_{out}(\max)]$
4	Minimum output voltage, $v_{out}(\min)$	$S_{11} = \frac{2I_{11}}{K_N' V_{DS11}^2}$, $S_9 = \frac{2I_9}{K_N' V_{DS9}^2}$, ($S_{10} = S_{11}$ and $S_8 = S_9$)	$V_{DS9}(\text{sat}) = V_{DS11}(\text{sat}) = 0.5[V_{out}(\min) - V_{SS}]$
5	$GB = \frac{g_{m1}}{C_L}$	$S_1 = S_2 = \frac{g_{m1}^2}{K_N' I_3} = \frac{GB^2 C_L^2}{K_N' I_3}$	
6	Minimum input CM	$S_3 = \frac{2I_3}{K_N' \left(V_{in}(\min) - V_{SS} - \sqrt{(I_3/K_N' S_1)} - V_{T1}\right)^2}$	
7	Maximum input CM	$S_4 = S_5 = \frac{2I_4}{K_P' \left(V_{DD} - V_{in}(\max) + V_{T1}\right)^2}$	S_4 and S_5 must meet or exceed value in step 3
8	Differential Voltage Gain	$\frac{v_{out}}{v_{in}} = \left(\frac{g_{m1}}{2} + \frac{g_{m2}}{2(1+k)}\right) R_{out} = \left(\frac{2+k}{2+2k}\right) g_{m1} R_{out}$	$k = \frac{R_{II}(g_{ds2} + g_{ds4})}{g_{m7} r_{ds7}}$
9	Power dissipation	$P_{diss} = (V_{DD} - V_{SS})(I_3 + I_{10} + I_{11})$	

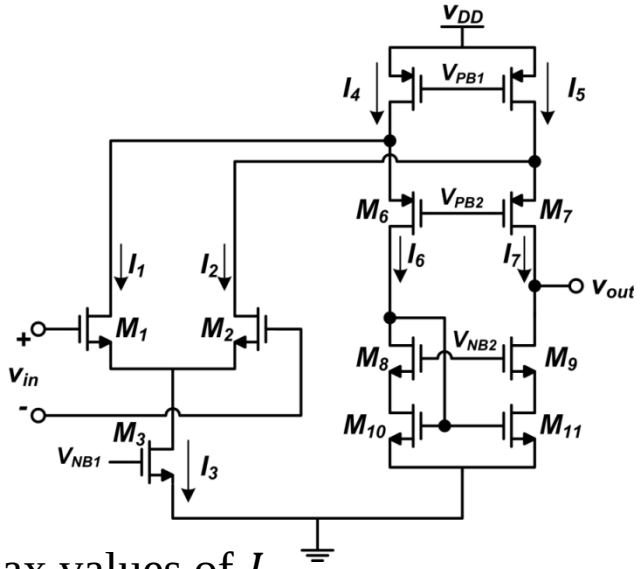
[Allen]

Design Example

- Design a folded cascode Op Amp to comply with the following specifications using 0.18µm CMOS technology

Parameter	Spec
Slew rate	$> 10\ \mathrm{V/\mu s}$
Load Capacitor	10pF
Power Supply	$\pm 1\ \mathrm{V}$
Max/Min Output Voltage	$\pm 0.5\ \mathrm{V}$
GBW	$> 10\ \mathrm{MHz}$
Min Input CM Voltage	$-0.3\ \mathrm{V}$
Max Input CM Voltage	$1\ \mathrm{V}$
Differential Voltage Gain	$> 60\ \mathrm{dB}$
Power Dissipation	$< 2\ \mathrm{mW}$

Design Example (Cont.)



❑ **Solution:**

➢ From the value of the slew rate we can get I_3

$I_3 = SR \times C_L > (10 \times 10^6)(10 \times 10^{-12}) \rightarrow I_3 \geq 100\mu A$

Select $I_3 = 120\mu A$

➢ $I_{4,5}$ will be designed such that $I_{6,7}$ never goes to zero

$I_4 = I_5 = 1.2I_3$ to $1.5I_3$

Select $I_4 = I_5 = 1.25I_3 = 150\mu A$

➢ Knowing I_4 and I_3, we can get the quiescent, min, and max values of $I_{6,7}$

$I_{6,Q} = I_{7,Q} = I_4 - 0.5I_3 = 90\mu A$

$I_{6(min)} = I_{7(min)} = I_4 - I_3 = 20\mu A$

$I_{6(max)} = I_{7(max)} = I_4 = 150\mu A$

➢ From the min and maximum output voltages we can get overdrive voltage of transistors M_{4-11}

$V_{SDsat(4-7)}\big|_{max} = 0.5\left(V_{DD} - V_{out(max)}\right) = 0.25\ V$

$V_{DSsat(8-11)}\big|_{max} = 0.5\left(V_{out(min)} - V_{SS}\right) = 0.25\ V$

Design Example (Cont.)

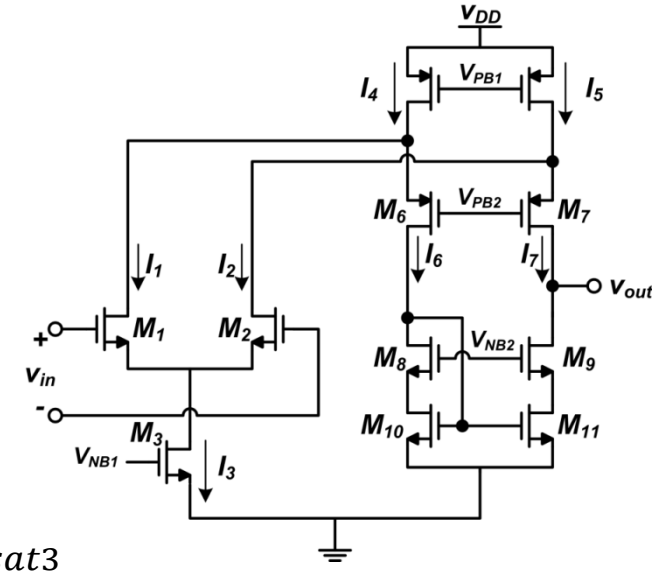
- The value of GB gives $g_{m1,2}$

$g_{m1,2} = GB \times C_L \geq 628.3\ \mu A/V$

Thus, choose $g_{m1,2} = 700\ \mu A/V$

From $g_{m1,2}$ and $I_{1,2}$, we can obtain $V_{DSsat(1,2)}$

$$V_{DSsat(1,2)} = \frac{2I_1}{g_{m1}} = \frac{I_3}{g_{m1}} = 0.17\ V$$



- The minimum input common mode voltage defines V_{DSsat3}

$V_{icm(min)} = V_{SS} + V_{DSsat(3)} + V_{Tn} + V_{DSsat(1)}$

Thus, $V_{DSsat(3)} = 0.13\mu A$ for $V_{Tn} = 0.4\ V$

- We need to check that the maximum input common mode voltage is satisfied

$V_{icm(max)} = V_{DD} - V_{SDsat(4)} + V_{Tn} = 1.15\ V$ → Meets the spec

Design Example (Cont.)

- Now, we have the bias currents I_D and overdrive voltage V_{DSsat} of all the transistors. Thus, we can obtain W/L of all the transistors from the ACM model or square-law model if long-channel transistors are used.

- The channel length of the transistors should be chosen to satisfy the specified voltage gain.

- The current flowing in transistors M_{6-11} can have any value from $20\,\mu A$ to $150\,\mu A$ depending on the amplitude and polarity of the differential input voltage. Therefore, they should be sized such that the worst case V_{DSsat} of each transistor meets the specified limits on the output voltages.

- Bias voltages of the cascode transistors V_{PB2} and V_{NB2} are chosen such that

V_{PB2}

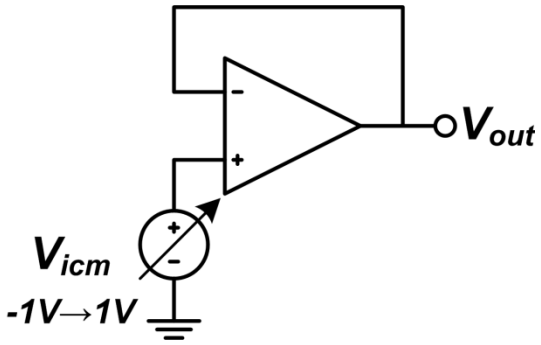
Simulation Results

❑ DC operating point

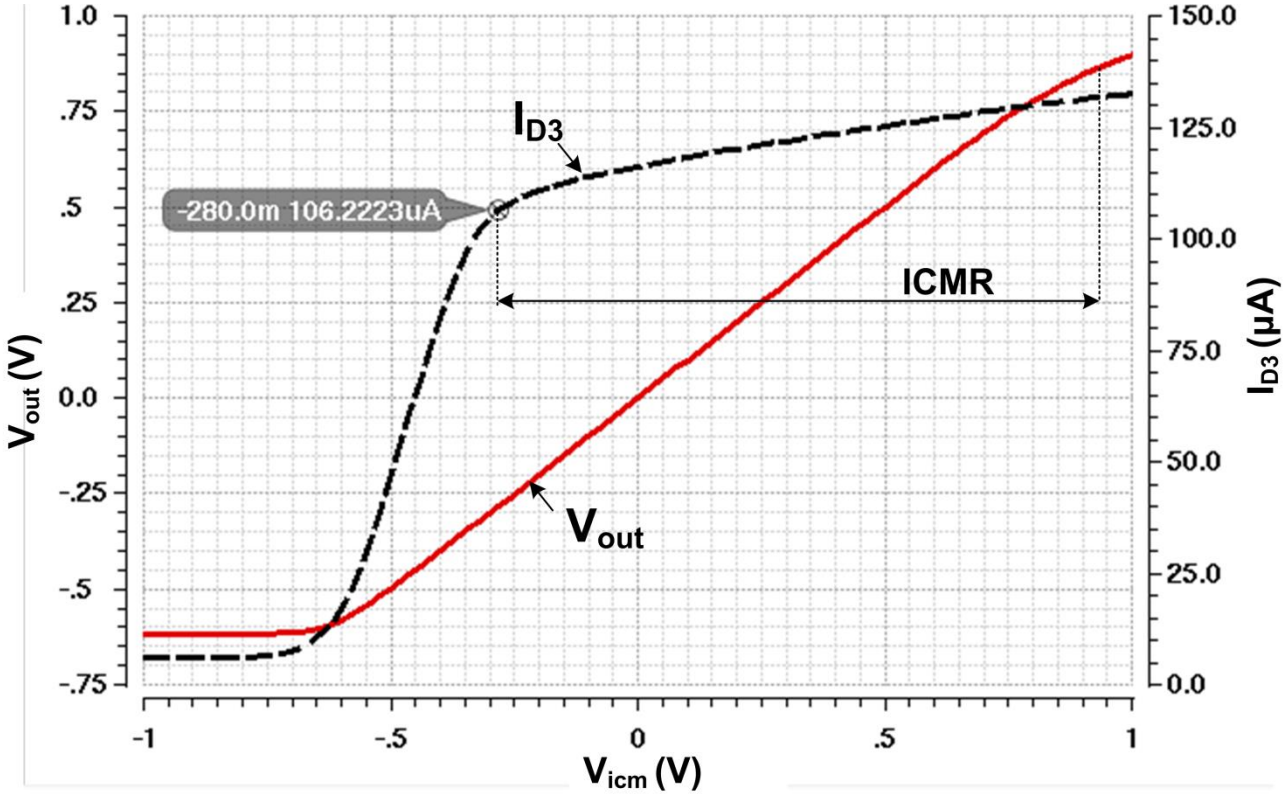
Transistor	W/L	$I_D\ (\mu A)$	V_{DSsat}
$M_{1,2}$	18/1	120	0.13
M_3	24/1	60	0.16
$M_{4,5}$	72/1	150	0.23
$M_{6,7}$	72/1	90	0.23
$M_{8,9}$	12/1	90	0.24
$M_{10,11}$	12/1	90	0.24

Simulation Results

❑ Input common-mode range



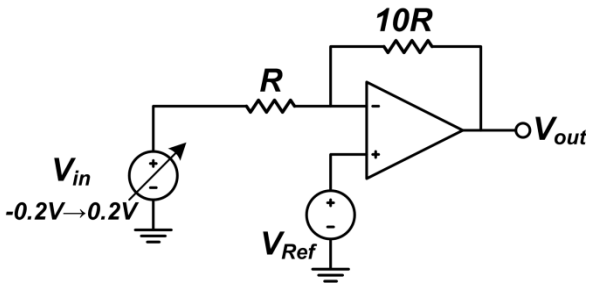
ICMR testbench



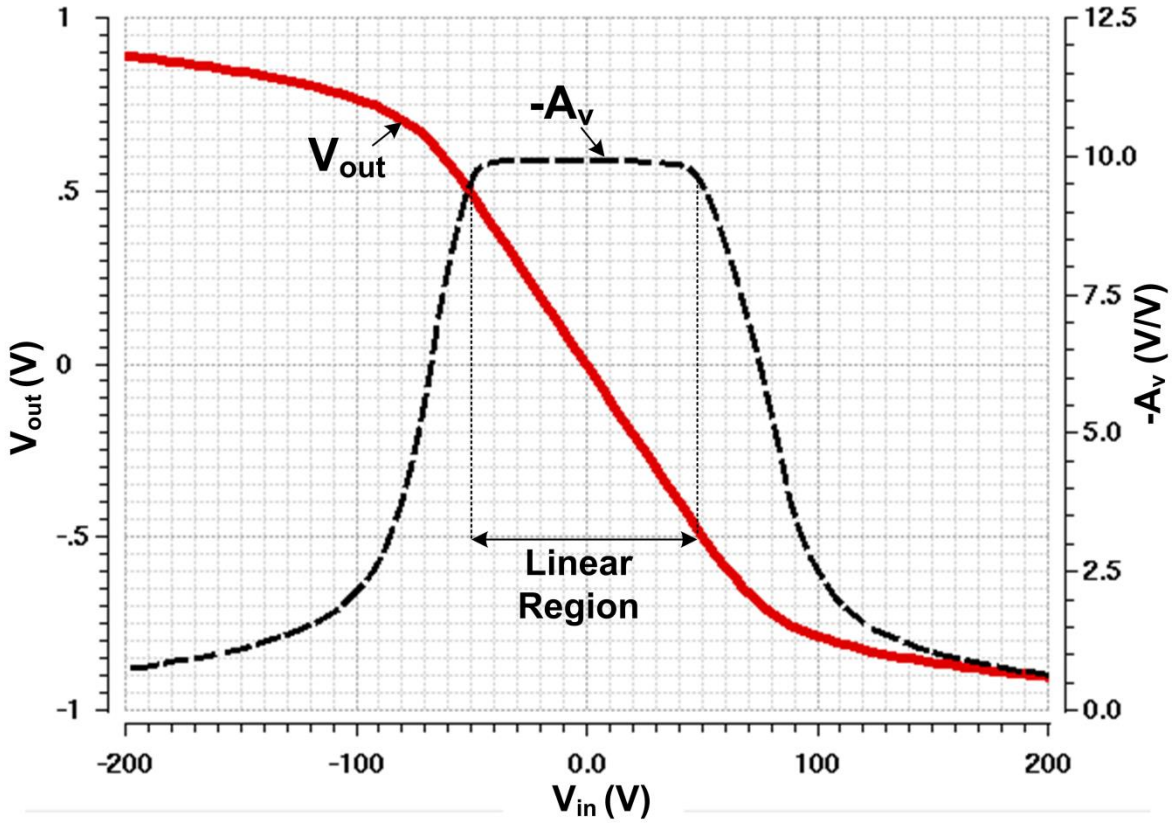
Minimum input common mode voltage is 0.28 V

Simulation Results

❑ Output Swing



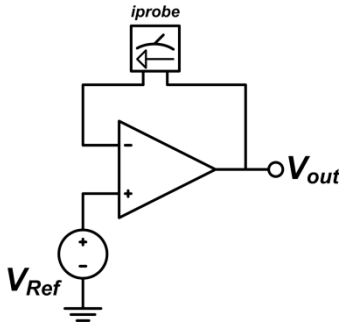
Output Swing Testbench



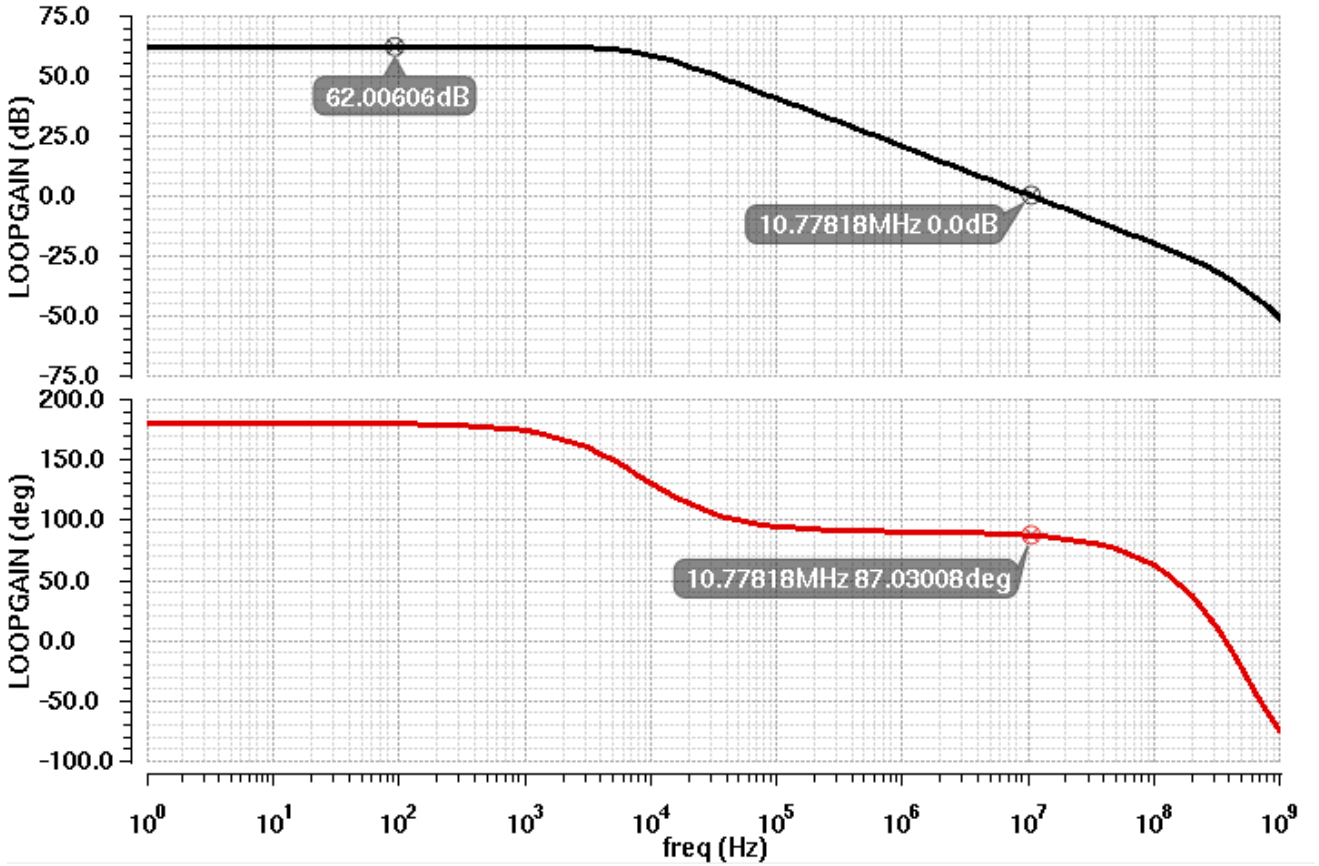
The gain is perfectly linear for $-0.5 \leq V_{out} \leq 0.5$

Simulation Results

❑ Open loop response



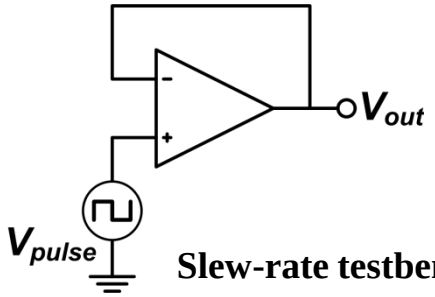
Open loop response testbench



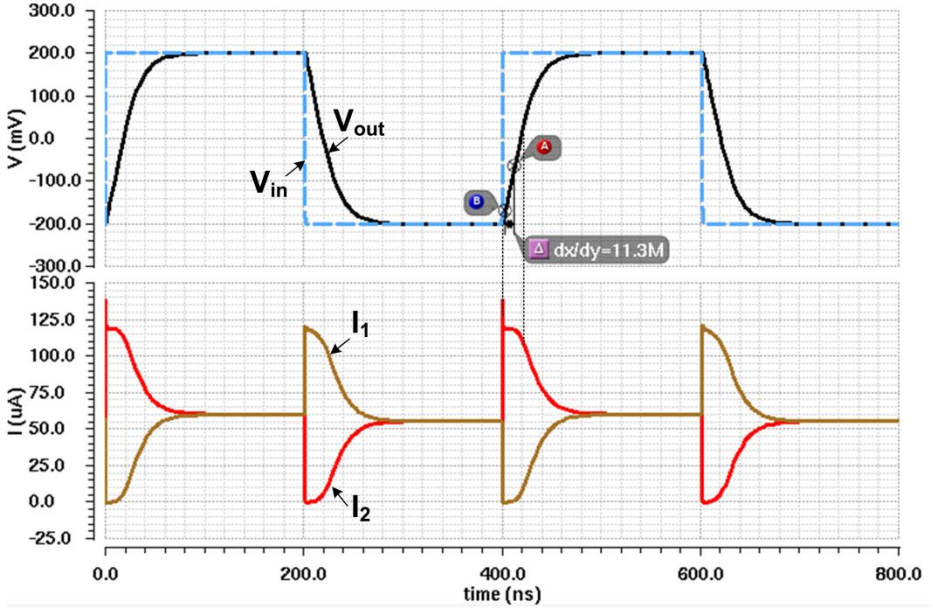
$$A_v > 60\ dB$$
$$GB > 10\ MHz$$

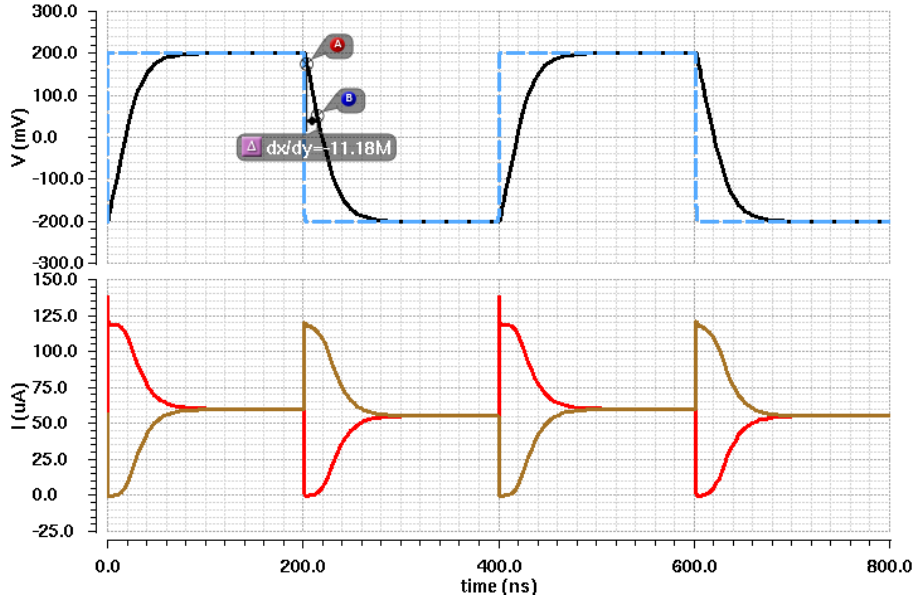
Simulation Results

❑ Slew Rate



Slew-rate testbench

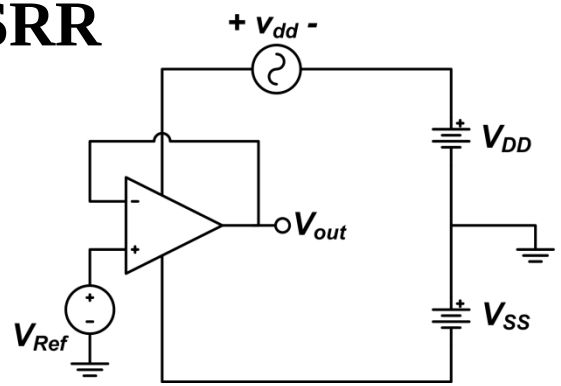




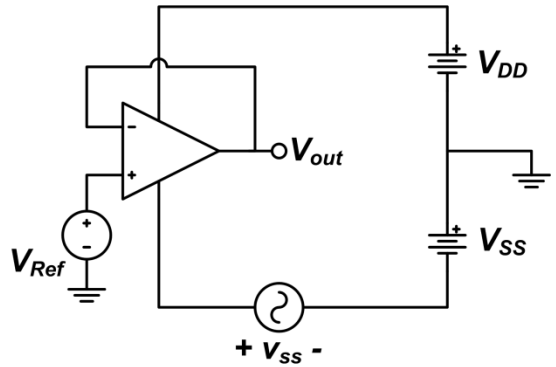
$$SR^+, SR^- > 10\ V/\mu s$$

Simulation Results

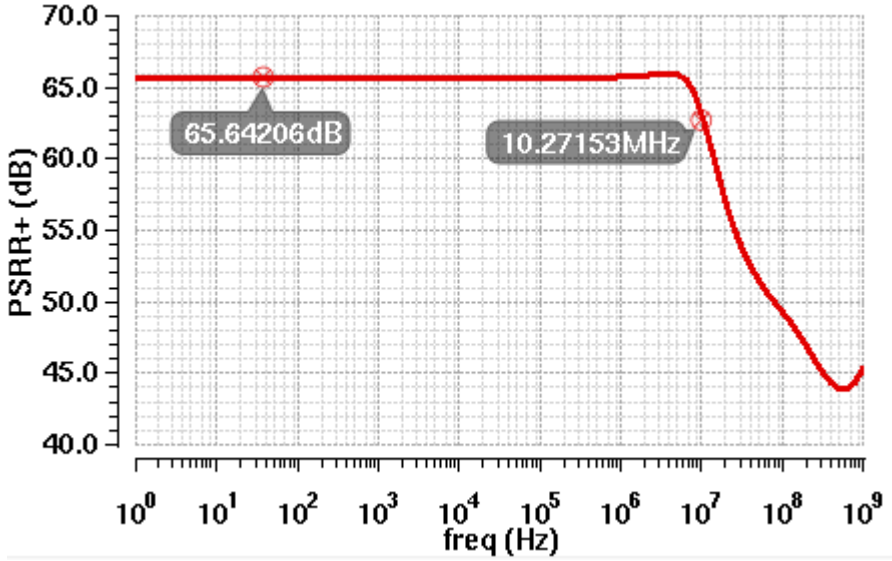
❑ PSRR

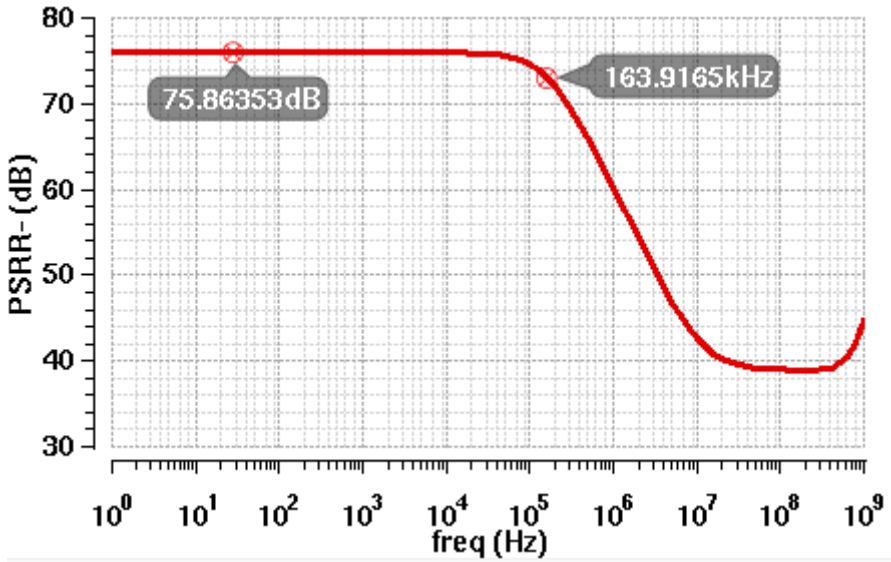


PSRR⁺ testbench



PSRR⁻ testbench



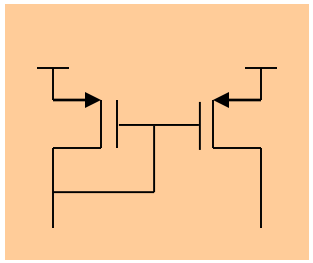


Summary of Results

- The following simulation results for $C_L = 10pF$, $V_{DD} = 1\ V$ and $V_{SS} = -1V$

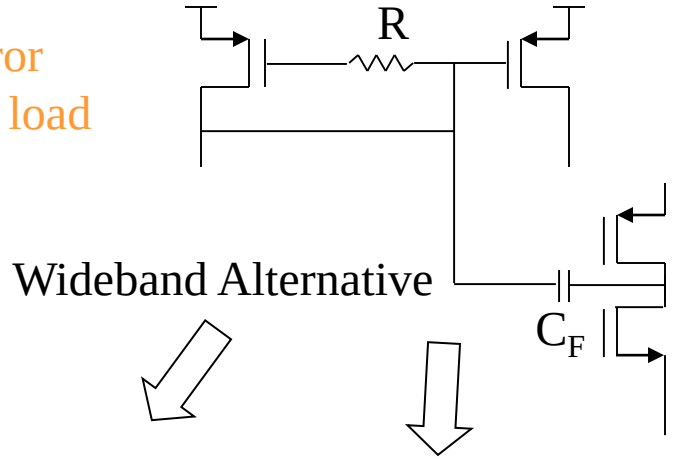
Parameter	Spec	Simulation
SR^+	$> 10\ \mathrm{V/\mu s}$	$11.3\ \mathrm{V/\mu s}$
SR^-	$> 10\ \mathrm{V/\mu s}$	$11.18\ \mathrm{V/\mu s}$
Max/Min Output Voltage	$\pm 0.5\ \mathrm{V}$	$-0.65 \rightarrow 0.61\ V$
GBW	$> 10\ \mathrm{MHz}$	$10.7\ MHz$
Min Input CM Voltage	$-0.3\ \mathrm{V}$	$-0.28\ V$
Max Input CM Voltage	$1\ \mathrm{V}$	$1\ V$
Differential Voltage Gain	$> 60\ \mathrm{dB}$	$62\ dB$
$PSRR^+$	-	$65.64\ dB$
$PSRR^-$	-	$75.86\ dB$
Power Dissipation	$< 2\ \mathrm{mW}$	$840\ \mu W$

Techniques for Wideband Amplifiers
Focus the improvement in the load of the differential pair



Conventional

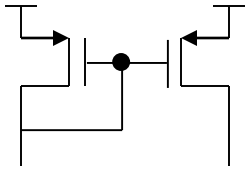
Current Mirror
at the output load



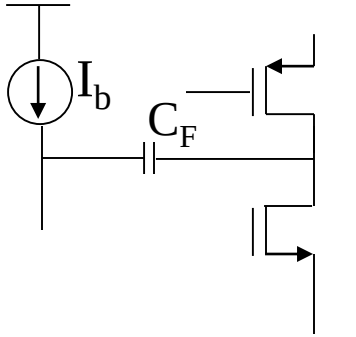
Frequency Dependent
Current Mirror (FDCM)

$C_F >> Cgs$

$0.1K < R < 1K$



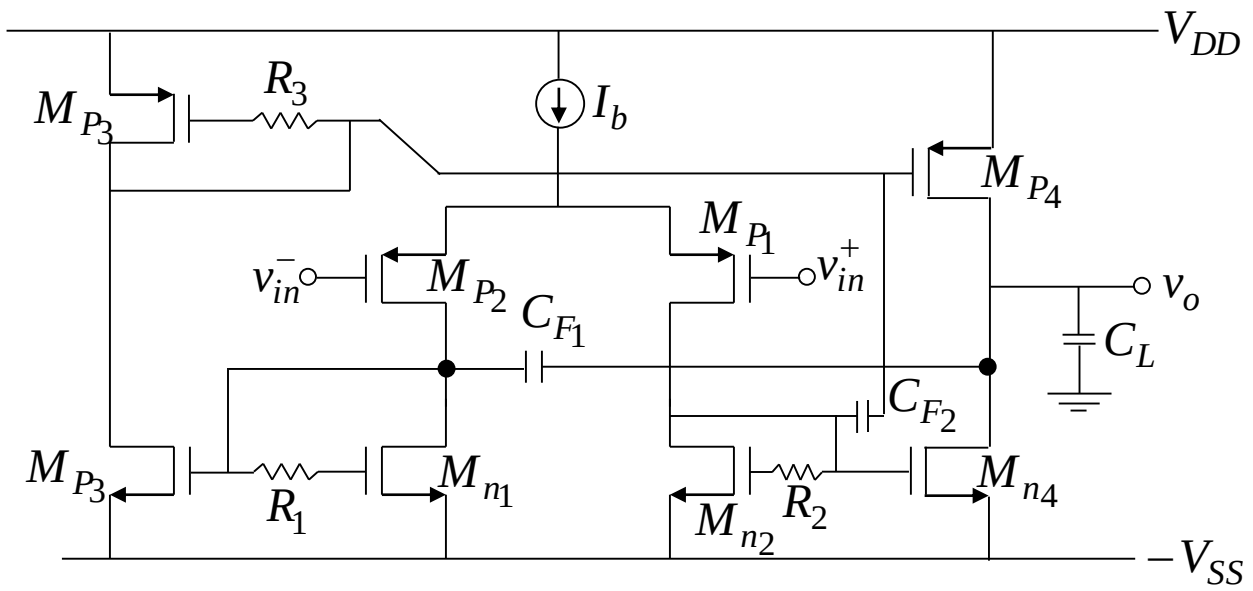
Low Frequency
Behavior



High Frequency
Behavior

T. Itakura and T. Iida, "A Feedforward Technique with Frequency-Dependent Current Mirrors for a Low-Voltage Wideband Amplifier," *IEEE J. Solid-State Circuits*, Vol. 31, No.6, pp. 847-849, June 1996.

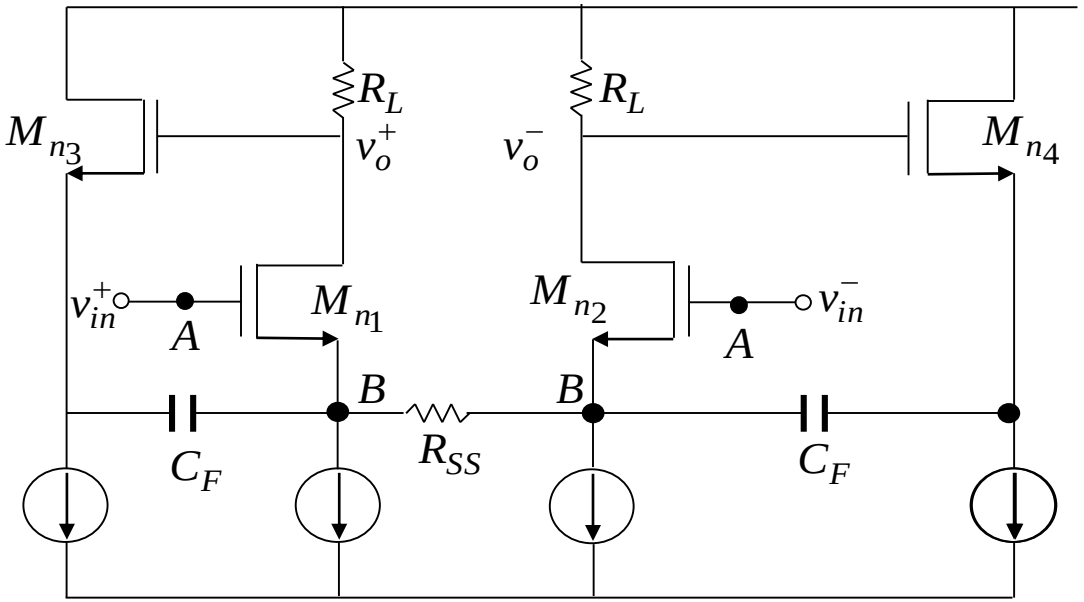
An example of its use:



Wideband Amplifier with Feedforward Technique

- What is the optimal value of R1 as a function og G_{mP3} ?
- C_{F1} by passes two current mirrors.
- C_{F2} is fed forward to the input of another FDCM and signal is amplified.

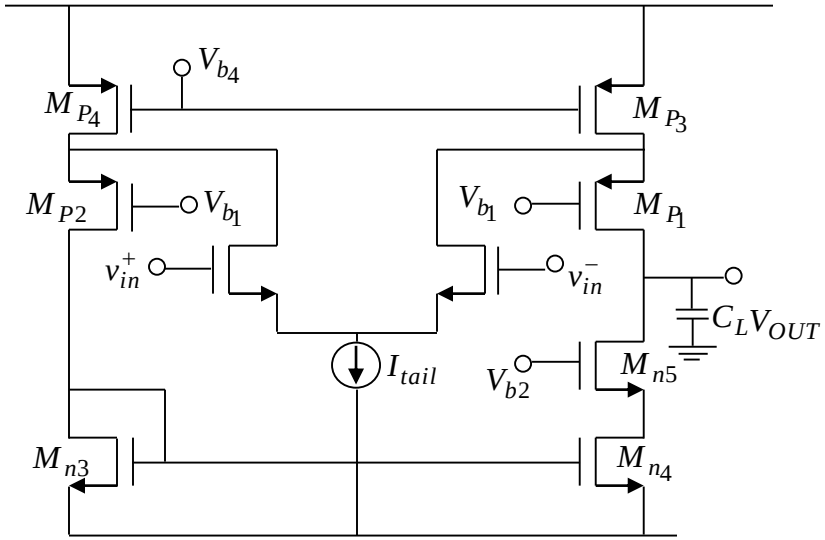
Next, we discuss different families of wideband reported in the literature.



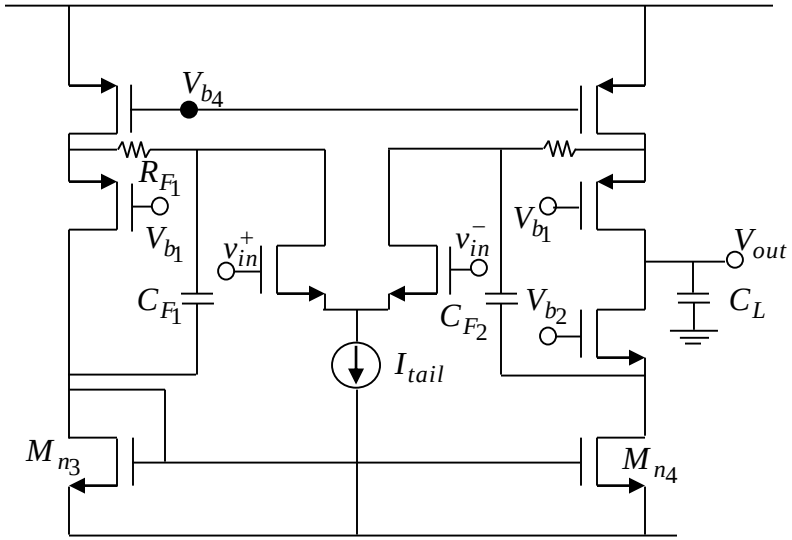
- An alternative is to connect C_F instead to nodes B to nodes A

F. Centurelli et al, "A Bootstrap Technique for Wideband Amplifiers," *IEEE Trans. on Circuits And Systesm – I,* Vol. 49, No. 10, pp. 1474-1480, October 2002

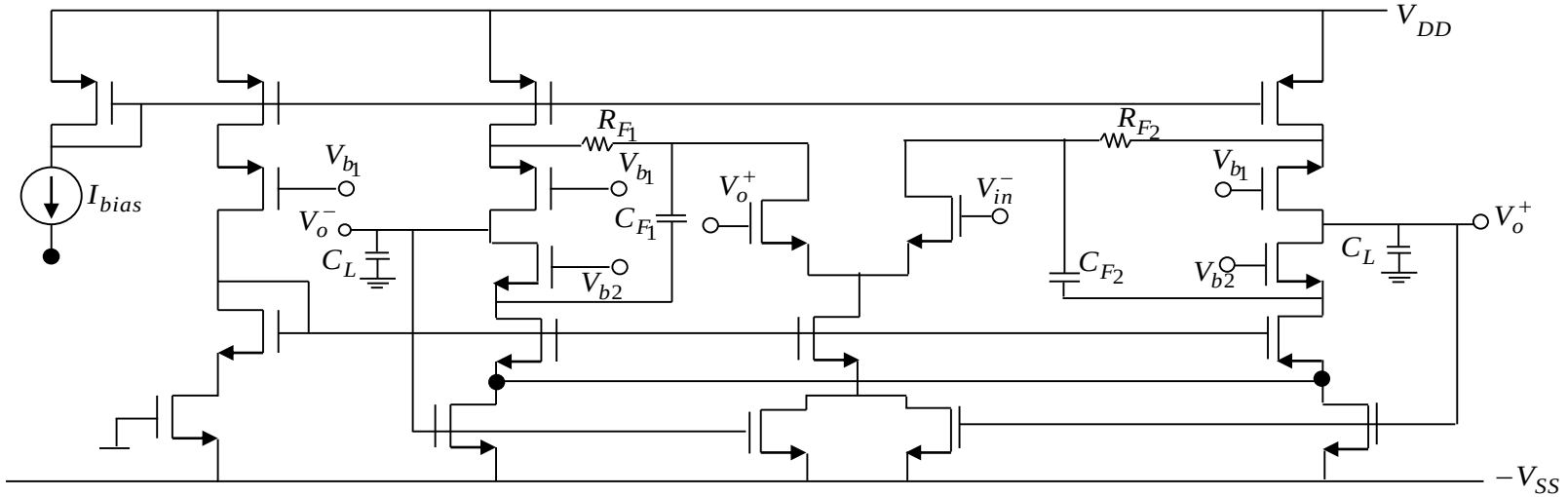
FOLDED-CASCODE WIDEBAND AMPLIFIER (See page 11 for cascode)



Conventional Folded-Cascode (FC)



FC with Capacitive Feedforward



Differential Wideband Amplifier

F. Opt Eynde, W. Sansen, "A CMOS Wideband Amplifier with 800MHz Bandwidth," *IEEE Custom Integrated Circuits Conf.*, pp. 9.1.1-9.1.4, 1991

An example of LV techniques: Current-Mode based LV Op Amp

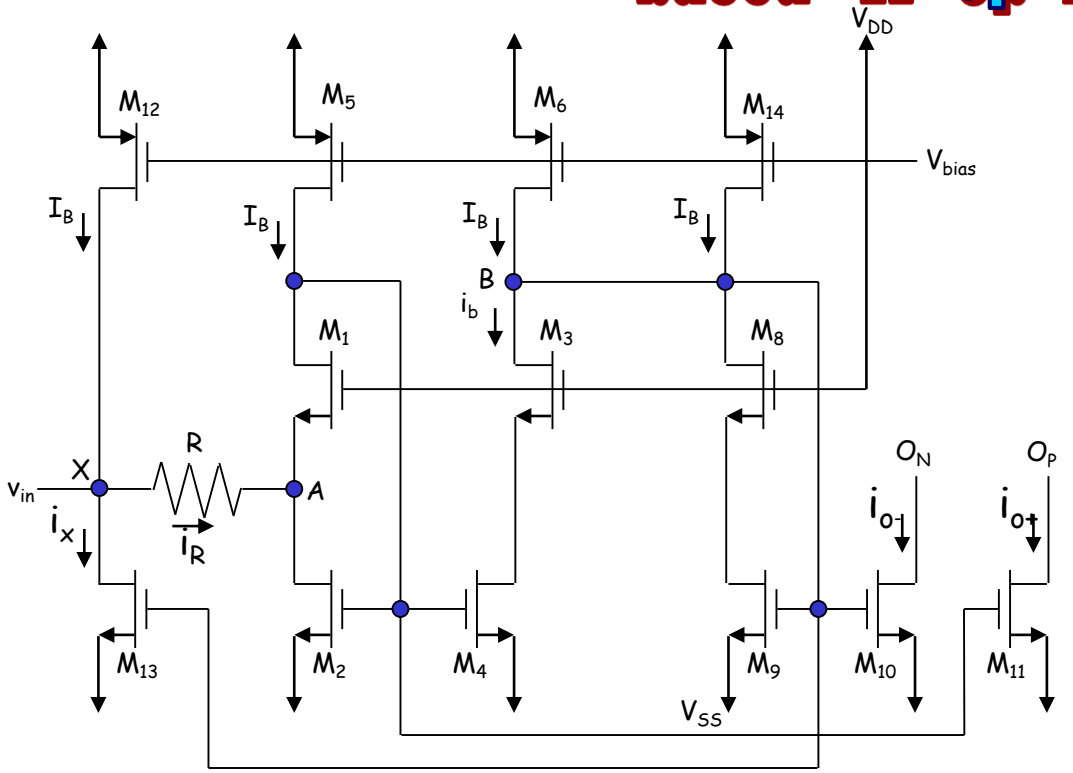


Fig. 1 Transconductance Amp
Basic Structure based on current-mode

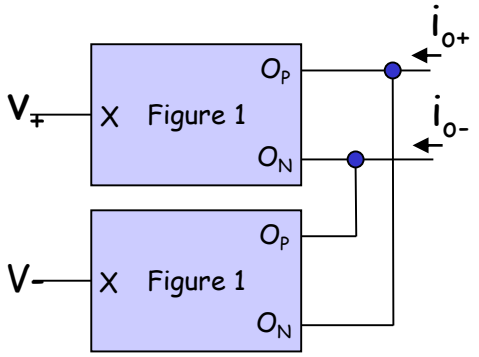


Fig 2
Pseudo Differential Op Amp

$i_R = Vin/R$

$i_X = - i_R$

$I_B > i_R$

E.K.F. Lee, " Low-Voltage Opamp Design and Differential Difference Amplifier Design Using Linear Transconductor with Resistor Input , " IEEE Trans. Circuits and Systems II,vol. 47, pp 776-778, Aug. 2000

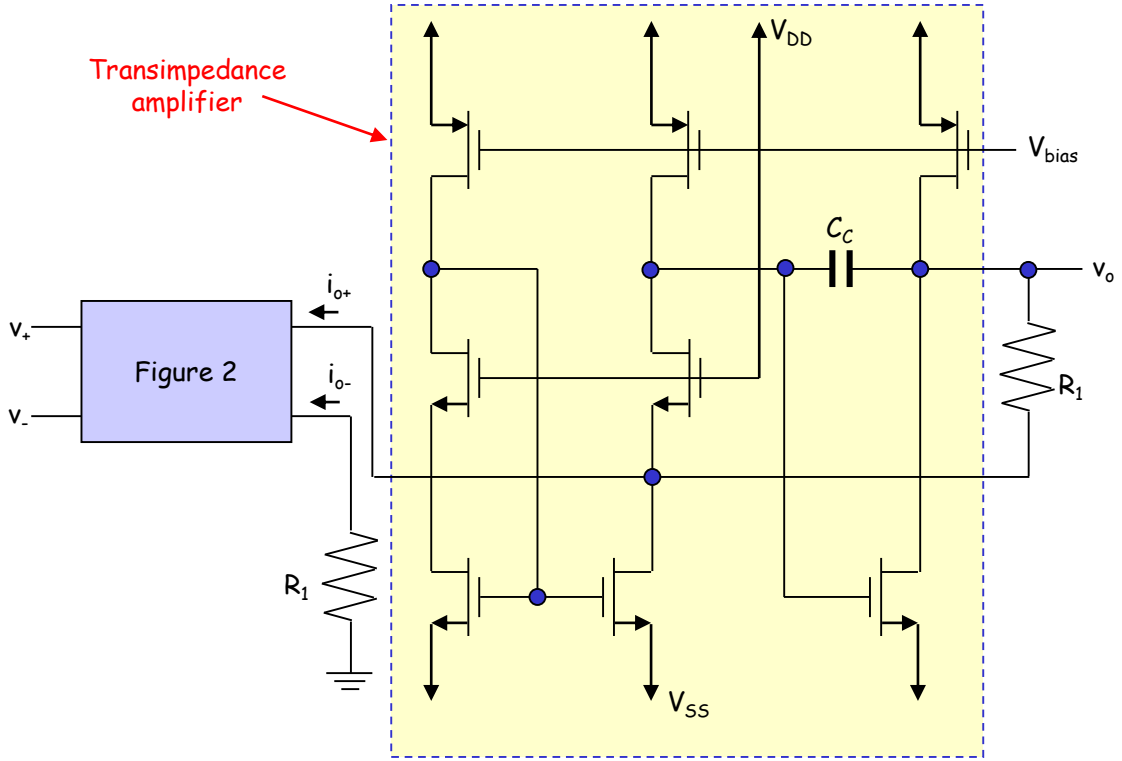
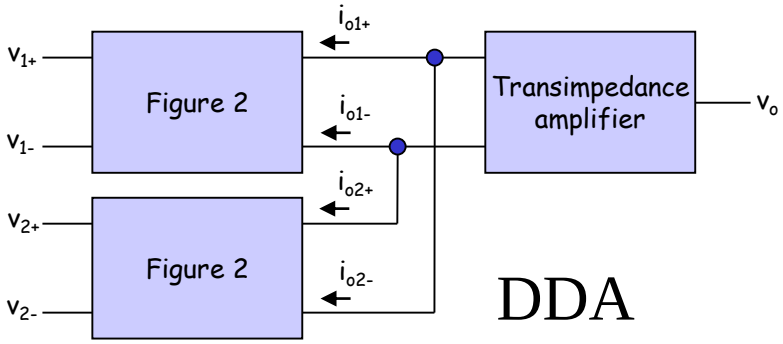


Fig 3 VCVS Amplifier: Op Amp



DDA

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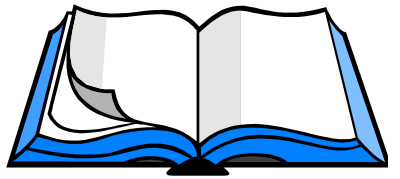

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S. Yan and E. Sánchez-Sinencio, Low Voltage Analog Circuit Design Techniques: A Tutorial, *IEICE Trans. Fundamentals*, Vol. E83-A, No. 2, pp 179-196, February 2000

E. Sánchez-Sinencio and Andreas G. Andreou, Eds. " *Low-Voltage/Low-Power Integrated Circuits and Systems* ", IEEE Press, Piscataway, NJ 1999

X. Xie, M.C. Schneider, E. Sanchez-Sinencio and S.H.K. Embabi, " Sound Design of Low Power Nested Transconductance-Capacitance Compensation Amplifiers", *IEE Electronics Letters*, Vol. 35, pp.956-958, June 1999.

A. Rodriguez-Vazquez and E. Sánchez-Sinencio, Eds., Special Issue on Low-Voltage and Low-Power Analog and Mixed-Signal Circuits and Systems, *IEEE Trans. on Circuits and Systems I*, vol. 42, No. 11, November 1995

J. Crols, J.; Steyaert, M.; Switched-opamp: an approach to realize full CMOS switched capacitor circuits at very low power supply voltages" *IEEE Journal of Solid-State Circuits*,, Volume: 29 , Issue: 8 , Aug. 1994 Pages:936 - 942

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Stan, M.R. Low Power Electronics and Design, 1998. Proceedings. 1998 International Symposium on , 10-12 Aug. 1998 Pages:97 - 99

A dynamic threshold voltage MOSFET (DTMOS) for ultra low voltage operation *Assaderaghi, F.; Sinitsky, D.; Parke, S.; Bokor, J.; Ko, P.K.; Chenming Hu;*
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Galup-Montoro, C.; Schneider, M.C.; Coitinho, R.M.;
Design & Test of Computers, IEEE ,Volume: 19 , Issue: 2 , March-April 2002 Pages:50 - 58

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Series-parallel association of FET's for high gain and high frequency applications
***Galup-Montoro, C.; Schneider, M.C.; Loss, I.J.B.;* Solid-State Circuits, IEEE Journal of ,Volume: 29 , Issue: 9 , Sept. 1994 Pages:1094 - 1101**

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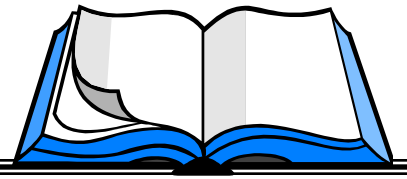

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S. Rabii and B. A. Wooley, " A 1.8V-V Digital Audio Sigma-Delta Modulator in 0.8-um CMOS", *IEEE J. of Solid-State Circuits*, Vol. 32, N0. 6, pp. 783-796, June 1997

CMOS Analog Circuit Design, P.E. Allen, D.R. Holberg, Oxford University Press, 3rd Edition, 2012