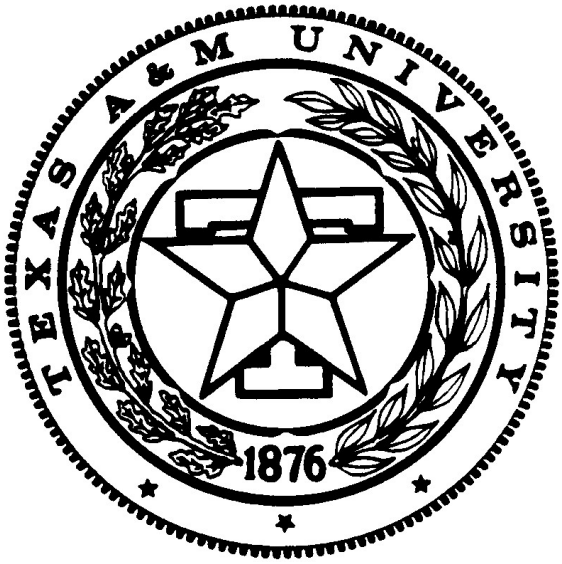
ECEN607 Advanced Analog Circuit Design Techniques

Homework Set#6



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Problem 1 Negative Impedance and Low Voltage Current Source:

Design a negative impedance circuit for V_{DD} = -V_{SS} = 1.00 V with 0.35 μ m CMOS technology. The load is 1 Mohm and 20 pF. Use this differential negative resistor to design an Op amp with Ao=110 db, GB> 5MHz, maximize input voltage swing, also employ a LV tail current source, i.e., F. You et all IEEE JSSC, Vol. 32, pp. 1173-1180, August 1997. Discuss the reason for using a PMOS or NMOS driver for each building block of your amplifier. Provide a Table summarizing your results; also include S/N, PSSR, CMR, CMRR, 1% settling time, offset voltage, power consumption, phase and gain margins.

The key procedure to solve this problem is to design the negative impedance amplifier using ideal current source first and then sub-design the low voltage current source to provide the same amount of current used in the ideal current source in Step 1. If the design is turned backwards, there will be no guarantee that the designed LV current source will actually work for the amplifier design. Once it does not work, we will have go back and start the design all over again, which is not a desirable experience for us. Therefore, the following design process will be gone through for this case:

i. Design the amplifier using ideal current source.
ii. Establish the LV current source accordingly.
iii. Plug the finished LV current source into the amplifier and do some fine tuning if there is any performance mismatch caused by the plugged-in LV current source circuit.

1. Negative Impedance Amplifier Design using Ideal Current Source:

(1) Schematic:

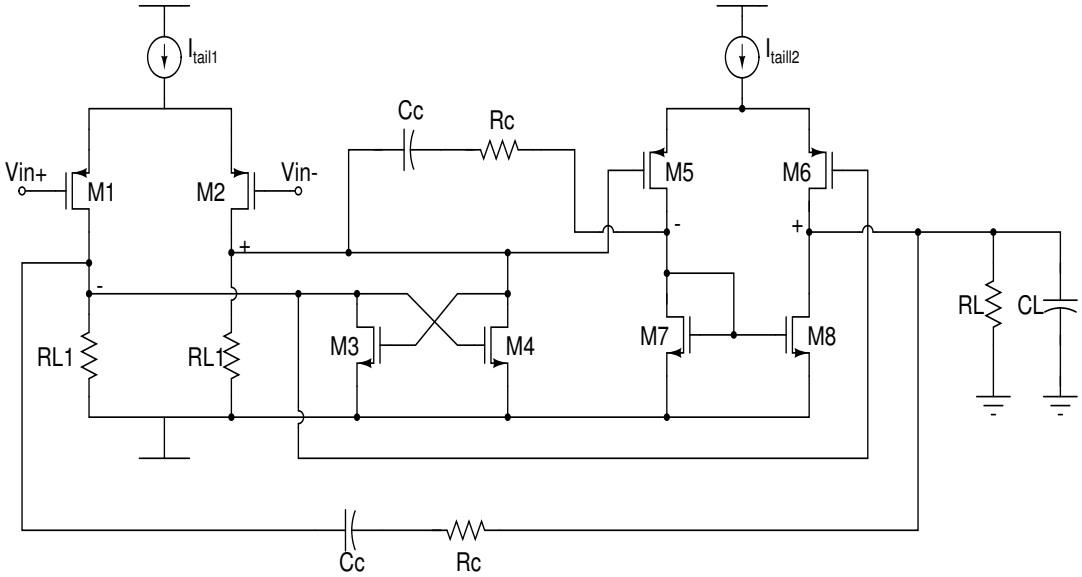


Figure 1: Schematic of Negative Impedance Amplifier with Ideal Current Source

(2) Design Specifications:

Specs	Values
Av (dB)	>110
GBW (MHz)	>5.0
Rload (Mohms)	1
Cload (pF)	20
Vsup (V)	+/- 1

Table 1: Required Design Specifications of Negative Impedance Amplifier

(3) Design Procedure:

For the negative impedance amplifier, the pMOS driver will be used to optimize the noise performance. The design of transistor parameters is somehow random since the gain will be boosted once the negative resistance is compensated by R_{L1}.

A. Choose Cc:

Since there are going to be high impedance at the output nodes of the second stage, therefore to make enough compensation, the compensation capacitor needs to be really large. Here, randomly pick up $Cc=6C_L=60pF$.

B. Design of g_{m1} and g_{m2} of M1 and M2 from GBW spec:

$$GBW=\frac{g_{m1}}{2\pi\cdot Cc}>5MHz \Rightarrow g_{m1}=2\pi\cdot Cc\cdot GBW>2\pi\cdot 60\times 10^{-12}\cdot 5\cdot 10^{6}=1.884mS$$

Here, we pick up $g_{m1}=g_{m2}=2mS$.

C. Choose the channel length of M1 and M2:

To ensure a good DC gain, we want to make the length a little large, say 0.6um.

D. Choose g_m/I_D of M1 and M2:

Normally, to make balance between circuit speed and power dissipation, simply pick up $(g_m/I_D)_1=(g_m/I_D)_2=10$.

E. Select tail current for the first stage:

Though there is no power spec, still to save power consumption, set the tail current to be 550uA.

F. Decide channel width of M1 and M2:

According to the I_D/W *vs.* g_m/I_D plot, we have $I_{D1}/W=8.258$. Since $I_{D1}= I_{D2}=275uA$, the channel width of M1 and M2 will be 33.3um.

G. Design of M3 and M4:

Choose g_{m3} and g_{m4} to be 400uS.

Choose $(g_m/I_D)_3=(g_m/I_D)_4=10$.

Choose channel length to be 0.8um.

H. Design of g_{m5} and g_{m6} of M5 and M6:

Though there is no phase margin spec, to have a stable amplifier. Set the spec to be 50°. Therefore, we have:

$$\frac{g_{m5}}{C_L} > 3\text{GBW} \cdot 2\pi \Rightarrow g_{m5} > 2\pi \cdot 3\text{GBW} \cdot C_L = 1.884\text{mS}$$

Here, simply pick up $g_{m5}=g_{m6}=2$mS.

I. Choose the channel length of M5 and M6:

Since the DC gain of the first stage will have already finished most part of the DC gain spec for the entire two stage amplifier, therefore, we only need the DC gain of this stage to be around 20dB, therefore, continue on with 0.6um.

J. Choose g_m/I_D of M5 and M6:

Similarly, set the value to be 10.

K. Select tail current for the second stage:

To save some labor and simplify the circuit, continue on with 550uA here, otherwise two LV current source will have to be designed, which will also introduce more current mismatches. This will bring more difficulties to implement the LV current source.

L. Decide channel width of M5 and M6:

According to the I_D/W *vs.* g_m/I_D plot, we have $I_{D1}/W=8.258$. Since $I_{D1}= I_{D2}=275uA$, the channel width of M1 and M2 will be 33.3um.

M. Design of M7 and M8:

M7 and M8 are just used to provide large output impedance in the fully differential pair. Therefore, only a properly-working M7 and M8 are desired. This means that a smaller transistor size and strong saturated working status are more desirable here.

N. Hand Design Summary:

W1(W2)	33.3um	gm1(gm2)	2mS	Itail1	550uA
L1(L2)	0.6um	gm3(gm4)	400uS	Itail2	550uA
W3(W4)	16um	gm5(gm6)	2mS	Rc	100ohms
L3(L4)	0.8um	gm7(gm8)	1mS	Cc	60pF
W5(W6)	33.3um	ID1(ID2)	275uA	RL1	3.5Kohms
L5(L6)	0.6um	ID3(ID4)	50uA	RL	1Mohms
W7(W8)	16um	ID5(ID6)	275uA	CL	20pF
L7(L8)	0.8um	ID7(ID8)	275uA	Vi(dcbias)	0V

Table 2: Hand Design Summary of Negative Impedance Amplifier with Ideal Current Source

(4) Cadence Design Parameters:

Transistor	W (um)	L (nm)	Multiplier#	gm (mS)	gm/ID	ID (uA)
M1	15	600	12	2.676	9.733	-274.9
M2	15	600	12	2.677	9.732	-275.1
M3	10	800	1	0.357	8.628	41.38
M4	10	800	1	0.363	8.495	42.73
M5	15	600	12	2.616	9.49	-275.7
M6	15	600	12	2.634	9.602	-274.3
M7	10	800	1	0.8321	3.018	275.7
M8	10	800	1	0.8282	3.019	274.3

Table 3: Transistor Parameters of Negative Impedance Amplifier with Ideal Current Source

Itail1	550uA
Itail2	550uA
Rc	380ohms
Cc	45pF
RL1	3269ohms
RL	1Mohms
CL	20pF
Vi(dcbias)	-0.2V

Table 4: External Parameters of Negative Impedance Amplifier with Ideal Current Source

(5) Circuit Performance:

Specs	Required	Achieved
Av (dB)	>110	122.1
GBW (MHz)	>5.0	6.303
Phase Margin (◦)		58.43
Rload (Mohms)	1	1
Cload (pF)	20	20

Table 5: Circuit Performance of Negative Impedance Amplifier with Ideal Current Source

(6) Performance Plots (refer to Appendix A for complete pack of simulation plots):

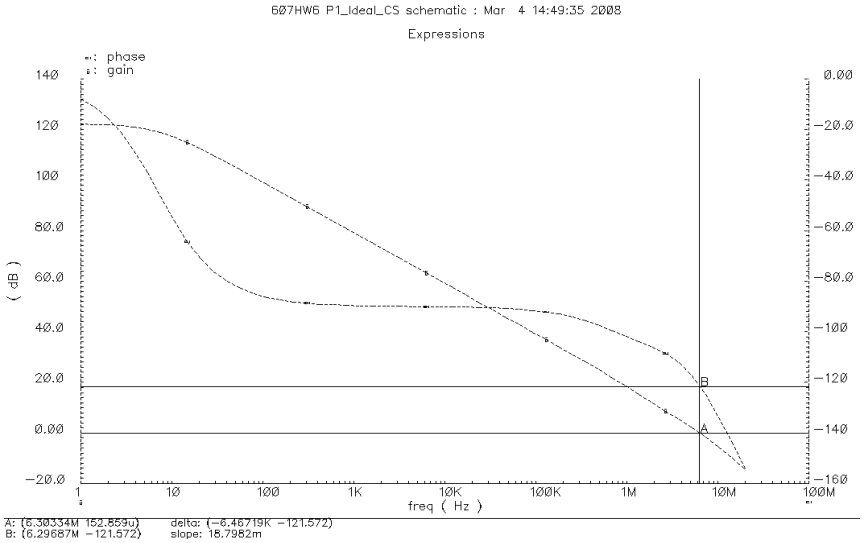


Figure 2: GBW=6.303MHz and Phase Margin=58.43◦
(Negative Impedance Amplifier with Ideal Current Source)

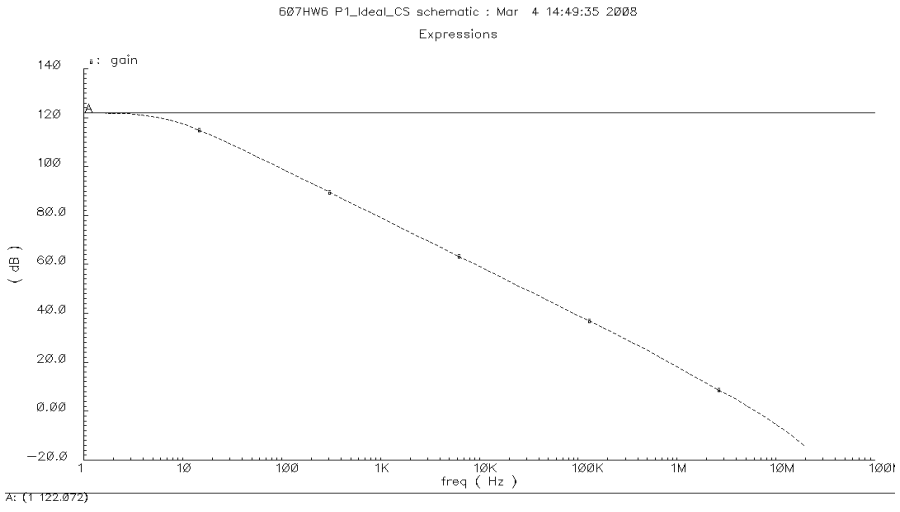


Figure 3: DC Gain=122.1dB (Negative Impedance Amplifier with Ideal Current Source)

2. Low Voltage Current Source:

(1) Schematic:

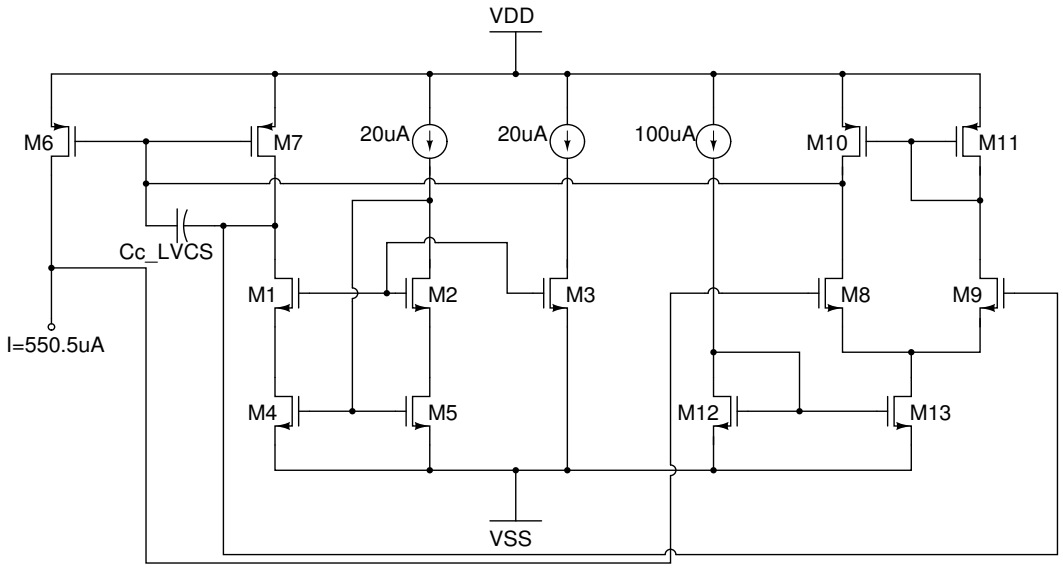


Figure 4: Schematic of Low Voltage Current Source

(2) Introduction:

It turned out to be that this low voltage current source is the main design issue for this problem. According to [1] in the Reference Section, since all kinds of cascade current sources will not be a good choice for low voltage applications due to their high compliance voltage, the following low voltage current source is explored. The basic idea here is that: A constant current is injected into M7 which is mirrored to the output transistor M6. A change in the current output node will force a similar change at the drain of M7 because of the virtual short circuit provided by the error amplifier A. This implies that the drain-to-source voltage of M7 tracks that of M6. Since the drain current of M7 is fixed and is equal to the constant current measured above, the error amplifier adjusts the gate voltage to compensate for the change in the drain-to-source voltage of M7 and M8. The output current remains fairly constant, which implies that the effective resistance of M6 has been enhanced.

A large output resistance is desired here to maintain a small output current variation. According to the following LV current source model, its output resistance can be obtained:

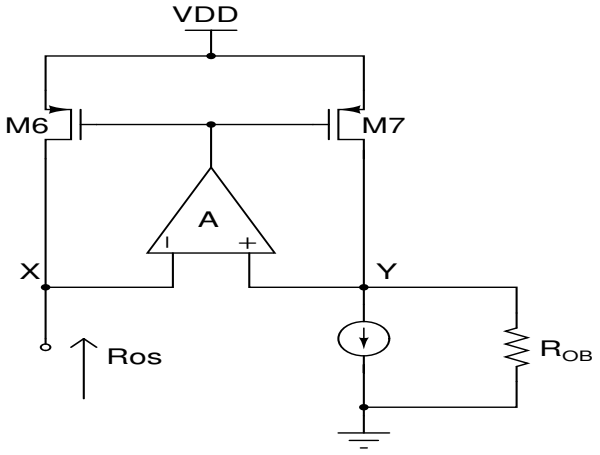


Figure 5: Low Voltage Current Source Model

Therefore, we can get the small signal model for this circuit (assume M7 and M6 have a same transconductance of g_{m0} and same drain-to-source resistance):

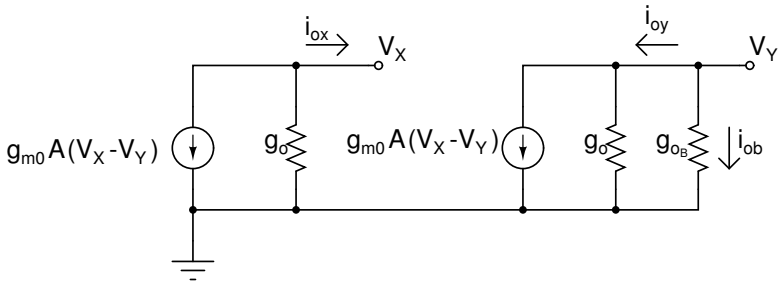


Figure 6: Small Signal Model of the LV Current Source

From Figure 4 and Figure 5, we can see that $i_{oy}=i_{ob}$. Hence, we are going to have the following KCL equation group:

$$\begin{cases} g_{m0}A(V_X-V_Y)+V_Y g_o = V_Y g_{OB} \\ -i_{ox} = g_{m0}A(V_X-V_Y)+V_X g_o \end{cases}$$

$$\Rightarrow \begin{cases} V_Y = \dfrac{g_{m0}A}{g_{OB}+Ag_{m0}-g_o} V_X \\ -i_{ox} = \left(g_{m0}A+g_o\right)V_X - g_{m0}AV_Y \end{cases}$$

$$\Rightarrow -i_{ox} = \left(g_{m0}A+g_o\right)V_X - g_{m0}AV_Y = \left(g_{m0}A+g_o - \frac{{g_{m0}}^2A^2}{g_{OB}+Ag_{m0}-g_o}\right)V_X$$

$$\Rightarrow R_{os} = \frac{V_X}{i_{ox}} = -\left(g_{m0}A+g_o - \frac{{g_{m0}}^2A^2}{g_{OB}+Ag_{m0}-g_o}\right)^{-1} = -\left(\frac{Ag_{m0}g_{OB}+g_o g_{OB}-{g_o}^2}{g_{OB}+Ag_{m0}-g_o}\right)^{-1}$$

Since g_o and g_{OB} are much smaller than Agm0, therefore, $g_o g_{OB}$ and ${g_o}^2$ in the numerator as well as g_{OB} and g_o in the denominator can be ignored here. Thus, the

output resistance could be derived as following:

$$R_{os}=-\left(\frac{Ag_{m0}g_{OB}}{Ag_{m0}}\right)^{-1}=-\frac{1}{g_{OB}}=-R_{OB}$$

Therefore, for design consideration, we want R_{OB} to be large. This is what a good current source should be. Imagine the designed current source is used as a tail current source of a differential pair. When there are rising common-mode signal at the inputs of the differential pair, since the drain current will change only a little bit, therefore, the V_{gs} will go up to maintain a close drain current and hence V_s will go up too. For this occasion, if the output resistance of the current source is not large enough, there would be a large current variation in the tail current. On the contrary, with a large output resistance, a large amount of voltage change across the current source will only leads to a small current fluctuation.

For the amplifier used in the LV current source, a large DC gain is desired because this would make the approximation introduced during the derivation of output resistance.

According to [1], there would be three poles in this current source system. Two of them are very close to each other. This will introduce instability into the system. The compensation capacitor is used to push one of the two poles to a higher frequency. Now, we are ready for the hand design.

(3) Design Procedure:

A. The design objective is to design a LV current source with a current drive ability of 550uA.

B. Design of the fully differential amplifier:

i) A low frequency gain of 35dB is aimed.
ii) The tail current is set to be 100uA.

According to the g_m/I_D design mechanism, we have the following hand design for the amplifier summarized in table:

W_8,W_9	56um	g_{m8},g_{m9}	750uS
L_8,L_9	900nm	g_{m10},g_{m11}	650uS
W_{10},W_{11}	140um	g_{m12},g_{m13}	1.2mS
L_{10},L_{11}	1um	I_{D8},I_{D9}	50uA
W_{12},W_{13}	58um	I_{D10},I_{D11}	50uA
L_{12},L_{13}	800nm	I_{D12},I_{D13}	100uA

Table 6: Hand Design of Low Voltage Current Source

C. Design of the current mirror and R_{OB}:

The designs here are somehow flexible. To me, there seems no way to manage the exact transistor size design. However, several design rules are better to be followed:

i) The cascode structure composed of M1 and M2 is used here to generate a large R_{OB}.
ii) M2 is added above M5 to make sure the VDS of M4 and M5 stay roughly the same. Thus, an accurate current for M7 will be provided.
iii) The values of g_m/I_D of M7 and M6 are better to be around 12.
iv) Large g_m/I_D values for M1, M2, M4 and M5 as well as a relatively small transistor size of M3 are desired to make sure all the transistors working in the saturation region.

(4) Cadence Design Parameters:

Transistor	W (um)	L (nm)	Multiplier#	gm (mS)	gm/ID	ID (uA)
M1	4	800	930	11.34	20.59	551
M2	4	800	26	0.4018	20.09	20
M3	4	800	1	155.7	7.784	20
M4	4	800	384	10.11	18.34	551
M5	4	800	14	0.3667	18.33	20
M6	3.2	800	390	7.112	12.91	-551
M7	3.2	800	390	7.113	12.91	551
M8	3.6	900	16	0.7631	15	50.86
M9	3.6	900	16	0.7622	15.03	50.72
M10	6	1	24	0.671	13.19	-50.86
M11	6	1	24	0.6693	13.2	-50.72
M12	3.2	800	20	1.278	12.78	100
M13	3.2	800	20	1.293	12.73	101.6

Table 7: Transistor Parameters of Low Voltage Current Source

(5) Discussion:

There might be a start-up problem of this circuit. Assume a very low voltage is presented at the output node of the LV current source. Since M6 and M7 form a current mirror, the drain voltage of M7 will track this low voltage and keep going down all the way to a voltage level which will not be large enough to supply enough drain-to-source voltage drop for the transistors on the same branch with M7, which are M1 and M4, to work in the saturation region. Hence, if this is the case that V_{D6} is so low at the very beginning that not enough voltage margin is left for M1 and M4, the circuit may not even start functioning.

(6) Current Source Performance:

After both DC and AC testing, the current can provide a stable current of 551uA, which is very close to the value used in the design of the negative impedance amplifier with ideal current source.

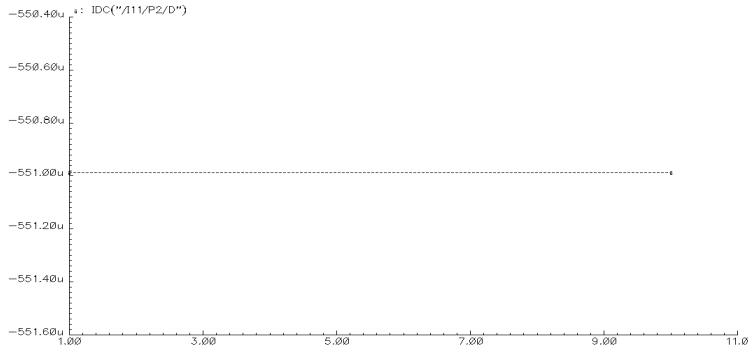


Figure 7: Output DC Current of the Low Voltage Current Source=551uA

3. Negative Impedance Amplifier with the Low Voltage Current Source Designed in Step 2:

This testing procedure is done by substitute the two ideal current sources used in Step 1 with the LV current source designed in Step 2. For the circuit parameters, there is no difference from those used in the ideal current source case except RL1 has to switch to 3.264kohms. This circuit is very sensitive to the load resistance variation.

(1) Cadence Simulation Results Summary:

Specs	Required	LV CS
Av (dB)	>110	110.5
GBW (MHz)	>5	6.118
Phase Margin (◦)		60.59
SNR (dB)		74.71
PSRR+ (dB)		196.4
PSRR- (dB)		182.3
CMR (V)		1.04
CMRR (dB)		244
1% Settling Time (ns)		694.23
Input Offset (nV)		395.2
PD (mW)		5.347
Gain Margin (dB)		6.44

Table 8: Circuit Performance Summary of Negative Impedance Amplifier with Low Voltage Current Source

(2) Detailed Simulation Plots (see Appendix A).

4. Circuit Comparison between Ideal Current Source Case and Low Voltage Current Source Case:

Specs	Required	Ideal CS	LV CS
Av (dB)	>110	122.1	110.5
GBW (MHz)	>5	6.303	6.118
Phase Margin (◦)		58.43	60.59
SNR (dB)		76.73	74.71
PSRR+ (dB)			196.4
PSRR- (dB)		186.9	182.3
CMR (V)			1.04
CMRR (dB)		287.6	244
1% Settling Time (ns)		249.6	694.23
Input Offset (nV)		85.69	395.2
PD (mW)		2.2	5.347
Gain Margin (dB)		28.85	6.44

Table 9: Circuit Performance Comparison between Ideal and LV Current Source Cases

5. Discussion about Maximizing Input Voltage Swing:

There are two possible methods here to achieve this design goal: 1. Rail-to-Rail; 2. Bulk Driven. Because of the limited job cycle, they have not been simulated. There might be a DC operation point problem for the Rail-to-Rail idea since the negative impedance amplifier is very sensitive to DC bias variations while the main idea of Rail-to-Rail is to have a constant transconductance over a large range of input DC voltage.

Problem 2 Fully Differential Op Amp Design using CMFB:

Using 65nm technology design a Fully Differential Op Amp whose topology you can select and justify, discuss at least two different CMFB circuit implementations. The load is 1.2 Mohms and 10 pF. The main specifications to satisfy include Ao > 130 db, GB > 2.0GHz, and phase margin > 55 degrees. Summarize your results and discuss the design procedure you propose for this design.

1. Schematic:

For this problem, the negative-impedance amplifier circuit used in Problem 1 will be implemented again to save time.

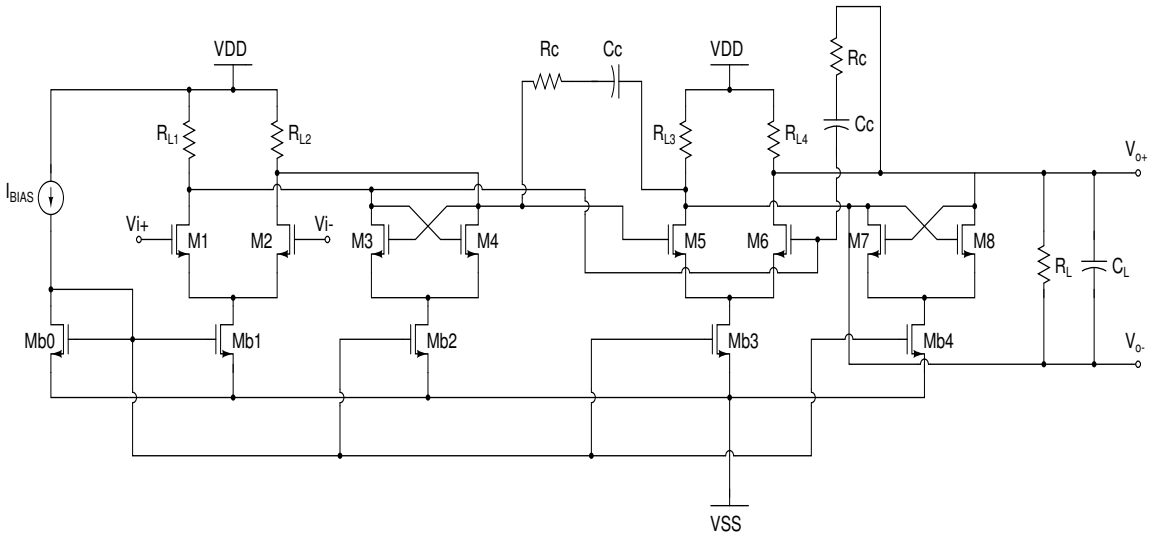


Figure 8: Two-Stage Negative Impedance Amplifier

2. Design Specification:

Specs	Values
Av (dB)	>130
GBW (GHz)	>2.0
Phase Margin (°)	>55
Rload (Mohms)	1.2
Cload (pF)	10

Table 10: Design Specifications of the Two-Stage Differential Pair Amplifier

3. Design Procedure:

(1) Choose Cc:

Usually, pick up Cc=2pF.

(2) Design g_{m1} and g_{m2} from GBW spec:

$$\because \frac{g_{m1}}{C_C} = 2\pi \times GBW > 2\pi \times 2 \times 10^9 Hz ,$$

$$\therefore g_{m1} = 2\pi \cdot GBW \cdot C_C > 2\pi \times 2 \times 10^9 \times 2 \times 10^{-12} = 25.12mS .$$

Here, we simply pick up $g_{m1}=g_{m2}$=30mS.

(3) Choose the channel length of M1 and M2:

According to the tuning experience, the channel length of M1 and M2 does not have too much effect on the AC responses Therefore, to minimize the parasitic components, set it to be the minimum channel length: 65nm.

(4) Choose g_m/I_D of M1 and M2:

Since once M1 and M2 is working in the saturation region, they will not quite affect the circuit performance. Therefore, just simply choose the value to be 12.

(5) Decide the drain current for M1, M2 and tail current of the first stage different pair:

$\because g_{m1}/I_{D1}=g_{m2}/I_{D2}=12$

$\therefore I_{D1}=g_{m1}/12=30mS/12=2.5mA=I_{D2}$

$\therefore I_{tail1}=5mA$

(6) Choose the channel width of M1 and M2:

According to the I_D/W *vs.* g_m/I_D plot, we have $I_{D1}/W=7.5$. Therefore, the channel width of M1 and M2 will be 333um.

(7) Design of R_{L1}, g_{m3}, g_{m4} and I_{tail2}:

Set I_{tail2}=6mA, $I_{D3}=I_{D4}$=3mA.

According to the $g_m \cdot r_o$ *vs.* g_m/I_D plot, to have a large gain, a large g_{m3} (g_{m4}) is desired. Therefore, we want a large g_m/I_D value for M3 and M4. Set it to be 15. Hence we are going to have $g_{m3}= g_{m4}$=45mS.

To cancel the negative impedance for gain boosting, we want $R_{L1}=1/g_{m3}$. =22.22ohms.

(8) Design of the channel length and width for M3 and M4:

Choose the length to be 80nm.

Then according to the I_D/W *vs.* g_m/I_D plot, we have $I_{D3}/W=3.5$. Therefore, the channel width of M3 and M4 will be 857um.

(9) Design of g_{m5}, g_{m6} and I_{tail3} from the phase margin spec:

$$\because PM > 55^\circ$$

$$\therefore \frac{g_{m5}}{C_L} = 3 \cdot 2\pi \cdot GBW$$

$$\therefore g_{m5} > 3 \times 2\pi \times 2 \times 10^9 \times 10 \times 10^{-12} = 376.8mS$$

Here, just simply choose the $g_{m5}= g_{m6}$ to be 400mS.

If set the g_m/I_D to be 12, then we are going to have $I_{D5}=I_{D6}=33.33$mA. Then I_{tail3} will be around 70mA.

(10) Design of the channel length and width for M5 and M6:

Choose the length to be 65nm.

Then according to the I_D/W *vs.* g_m/I_D plot, we have $I_{D5}/W=7.5$. Therefore, the channel width of M5 and M6 will be 4.44mm.

(11) Design of R_{L2}, g_{m7}, g_{m8} and I_{tail4}:

Set I_{tail4}=40mA. Then $I_{D7}=I_{D8}$=20mA.

According to the $g_m \cdot r_o$ *vs.* g_m/I_D plot, to have a large gain, a large g_{m7} (g_{m8}) is desired. Therefore, we want a large g_m/I_D value for M7 and M8. Set it to be 15. Hence we are going to have $g_{m7}= g_{m8}$=300mS.

To cancel the negative impedance for gain boosting, we want $R_{L1}=1/g_{m7}$ =3.333ohms.

(12) Design of the channel length and width for M7 and M8:

Choose the length to be 80nm.

Then according to the I_D/W *vs.* g_m/I_D plot, we have $I_{D7}/W=3.5$. Therefore, the channel width of M7 and M8 will be 5.71mm.

(13) Design Summary:

W1(W2)	333um	gm1(gm2)	30mS	RL1	22.2ohms
L1(L2)	65nm	gm3(gm4)	45mS	RL2	3.3homs
W3(W4)	857um	gm5(gm6)	400mS	Itail1	5mA
L3(L4)	80nm	gm7(gm8)	300mS	Itail2	6mA
W5(W6)	4.44mm	ID1(ID2)	2.5mA	Itail3	70mA
L5(L6)	65nm	ID3(ID4)	3mA	Itail4	40mA
W7(W8)	5.71mm	ID5(ID6)	33.33mA	Rc	70ohms
L7(L8)	80nm	ID7(ID8)	20mA	Cc	2pF

Table 11: Hand Design Summary of the Two_Stage Amplifier

4. Simulation Results:

(1) Transistor Parameters:

Transistor	W (um)	L (nm)	gm (mS)	gm/ID	ID (mA)
M1	333	65	50.6	20.24	2.5
M2	333	65	50.6	20.24	2.5
M3	860	80	63.62	21.21	3
M4	860	80	63.62	21.21	3
M5	1000	65	764.6	12.74	60
M6	1000	65	764.6	12.74	60
M7	1000	80	337.8	16.89	20
M8	1000	80	337.8	16.89	20

Table 12: Simulation Design Summary of Transistor Parameters of the Two-Stage Amplifier

RL1 (ohms)	18.462
RL2 (ohms)	4.72
Itail1 (mA)	5
Itail2 (mA)	6
Itail3 (mA)	120
Itail4 (mA)	40
Rc (ohms)	20
Cc (pF)	4

Table 13: Simulation Design Summary of External Parameters of the Two-Stage Amplifier

(2) Circuit Performance Summary:

Specs	Required	Achieved
Av (dB)	>130	137.42
GBW (GHz)	>2.0	2.345
Phase Margin (°)	>55	71.24
Rload (Mohms)	1.2	1.2
Cload (pF)	20	20

Table 14: Circuit Performance Summary of the Two-Stage Amplifier

(3) Simulation Plots:

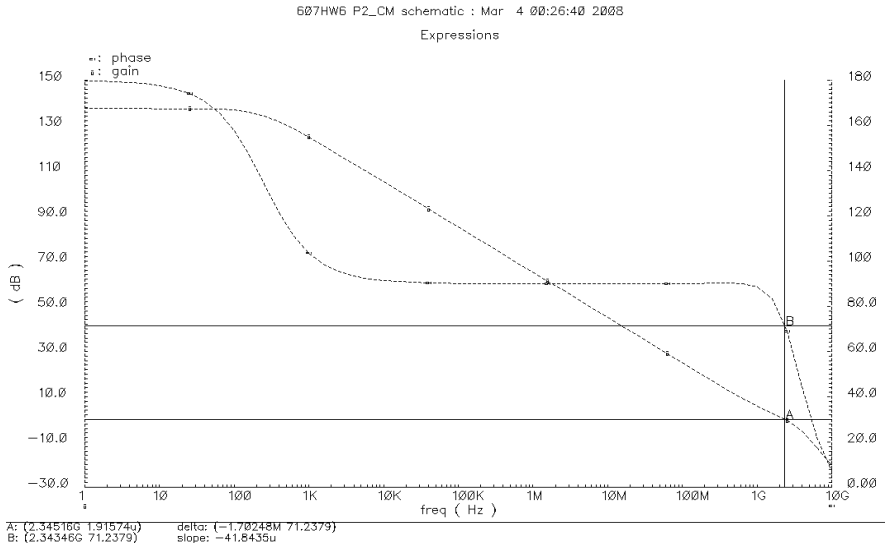


Figure 9: GBW=2.34516GHz > 2.0GHz and Phase Margin=71.2379° > 55°

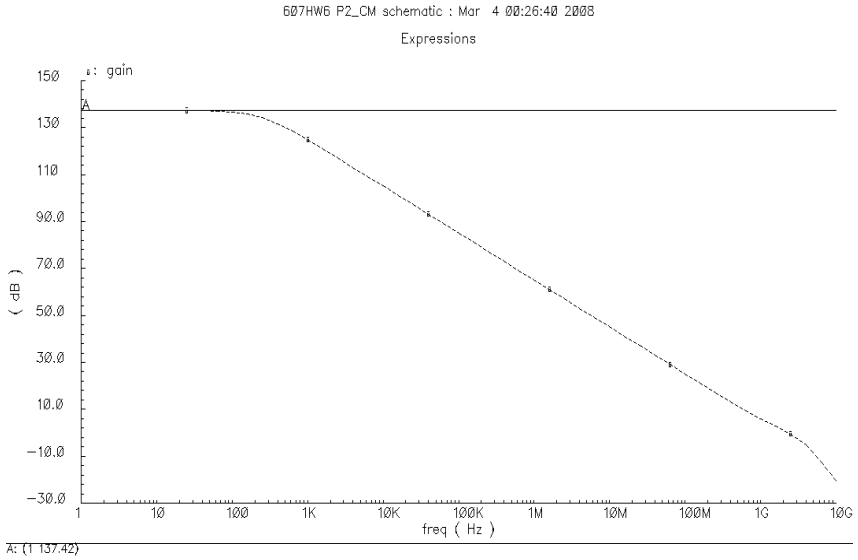


Figure 10: DC Gain=137.42dB > 130dB

5. Discussion of Two CMFB Circuit Implementations:

(1) Fully-Differential Filter CMFB Circuit:

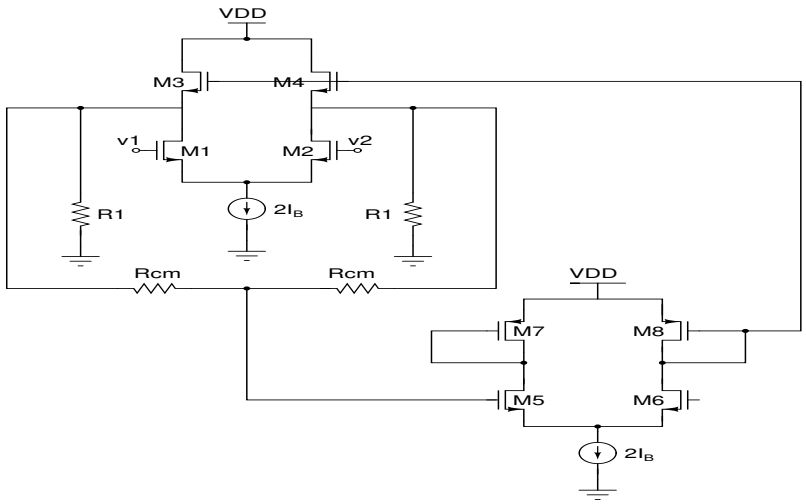


Figure 11: Schematic of Fully-Differential Filter CMFB Implementation

The basic idea here is that: once there is a rising common-mode signal at the inputs of the differential pair, the outputs voltage level will go up too. The voltage at the node between two R_{cm}s rises. The voltage increase will be fed into the CMFB circuit and a corresponding feedback signal will be transmitted back to the differential pair through the output node of the CMFB circuit to scale down the output node voltage of the differential pair. The major problem of this structure is the R_{cm}s are reducing the DC gain of the OTA.

(2) Low Voltage OTA CMFB Implementation:

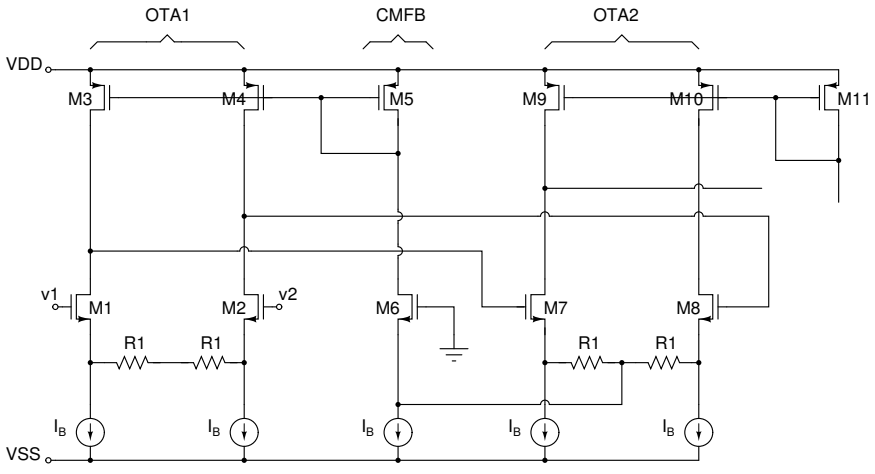


Figure 12: Low Voltage OTA CMFB Implementation

The basic idea here is that when there are common-mode signals at the inputs of the OTA1, the outputs of it will be fed into the inputs of the second OTA to generate a CMFB enable signal at the node between the two R_1s in the second OTA stage. This signal will be plugged into the CMFB structure to finally generate the CMFB signal, which will be returned to the first OTA stage to compensate the output variations caused by the common-mode signal. This cascade structure turns out more popular for low voltage applications.

Problem 3 Input Offset Voltage Analysis:

Consider a NMOS differential pair with an ideal tail current Is and two R_L resistive loads. Prove that the corresponding input offset voltage for the three cases is as shown below. Then determine the values of Voff when the resistive mismatch is 2.5%, the K mismatch is 2.5% and ΔV_T=3mV.

1. $V_{OFF}=\left(\frac{V_{gs}-V_T}{2}\right)\frac{\Delta R_L}{R_L}$, **when** $R_{L1}=R_L+\frac{\Delta R_L}{2}$ **and** $R_{L2}=R_L-\frac{\Delta R_L}{2}$;

2. $V_{OFF}=\left(\frac{V_{gs}-V_T}{2}\right)\frac{\Delta K}{K}$, **when** $\left(\frac{W}{L}\right)_1=\frac{W}{L}+\frac{\Delta\left(\frac{W}{L}\right)}{2}$, $\left(\frac{W}{L}\right)_2=\frac{W}{L}-\frac{\Delta\left(\frac{W}{L}\right)}{2}$ **and**

$K=\mu C_{ox}\frac{W}{L}$;

3. $V_{OFF}=\Delta V_T$, **when** $V_{T1}=V_T+\frac{\Delta V_T}{2}$ **and** $V_{T2}=V_T-\frac{\Delta V_T}{2}$.

Proof:

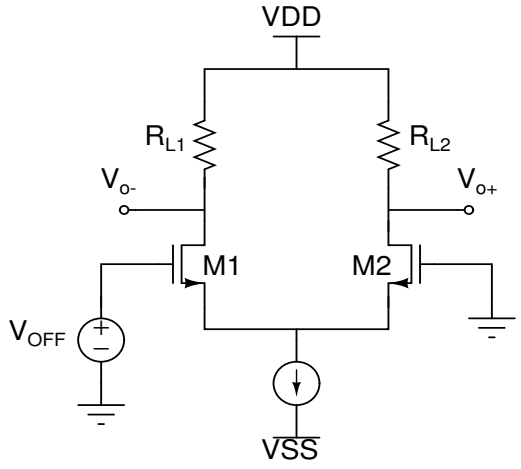


Figure 13: Schematic of a NMOS Differential Pair

Without any circuit mismatches, we will have the following ideal DC analysis:

(1) $R_{L1}=R_{L2}=R_L$;

(2) $\left(\frac{W}{L}\right)_1=\left(\frac{W}{L}\right)_2=\frac{W}{L}\Rightarrow\left\{\begin{matrix}I_{D1}=\frac{1}{2}\mu C_{ox}\frac{W}{L}\left(V_{gs}-V_T\right)^2\\I_{D2}=\frac{1}{2}\mu C_{ox}\frac{W}{L}\left(V_{gs}-V_T\right)^2\end{matrix}\right\}\Rightarrow I_{D1}=I_{D2}=I_D$;

(3) $V_{o+}=V_{o-}=V_{DD}-I_DR_L$.

However, input offset will be introduced into the circuit if there is some kind of circuit mismatch:

1. Load Resistance Mismatch ΔR_L:

The mismatched load resistance will be expressed as following:

$R_{L1}=R_L+\frac{\Delta R_L}{2}$ and $R_{L2}=R_L-\frac{\Delta R_L}{2}$

Since the drain current still remains the same, V_{o+} will be different from V_{o-}:

$$V_{o+}-V_{o-}=\left(V_{DD}-I_DR_{L2}\right)-\left(V_{DD}-I_DR_{L1}\right)=I_D\left(R_{L1}-R_{L2}\right)=I_D\left[\left(R_L+\frac{\Delta R_L}{2}\right)-\left(R_L-\frac{\Delta R_L}{2}\right)\right]=I_D\cdot\Delta R_L$$

Since V_{OFF} caused by ΔR_L will generate an equivalent ΔI_D in I_{D1} when there were no resistive mismatch, we will have:

$$V_{OFF}=\Delta I_D\cdot R_L=V_{o+}-V_{o-}=I_D\cdot\Delta R_L$$

, where ΔI_D can be presented like:

$$\begin{aligned}\Delta I_D&=I_{D1(OFFSET)}-I_{D1}\\&=\frac{1}{2}\mu C_{ox}\frac{W}{L}\left(V_{gs}+V_{OFF}-V_T\right)^2-\frac{1}{2}\mu C_{ox}\frac{W}{L}\left(V_{gs}-V_T\right)^2\\&=\frac{1}{2}\mu C_{ox}\frac{W}{L}\left[\left(V_{gs}+V_{OFF}-V_T\right)^2-\left(V_{gs}-V_T\right)^2\right]\\&=\frac{1}{2}\mu C_{ox}\frac{W}{L}\left[\left(V_{gs}+V_{OFF}-V_T+V_{gs}-V_T\right)\left(V_{gs}+V_{OFF}-V_T-V_{gs}+V_T\right)\right]\\&=\frac{1}{2}\mu C_{ox}\frac{W}{L}V_{OFF}\left(2V_{gs}+V_{OFF}-2V_T\right)\end{aligned}$$

$$\because \quad \Delta I_D = I_D \cdot \frac{\Delta R_L}{R_L}$$

$$\therefore \quad \frac{1}{2}\mu C_{ox}\frac{W}{L}V_{OFF}\left(2V_{gs}+V_{OFF}-2V_T\right) = I_D \cdot \frac{\Delta R_L}{R_L} = \frac{1}{2}\mu C_{ox}\frac{W}{L}\left(V_{gs}-V_T\right)^2 \cdot \frac{\Delta R_L}{R_L}$$

$$\therefore \quad V_{OFF}\left(2V_{gs}+V_{OFF}-2V_T\right) = \left(V_{gs}-V_T\right)^2 \cdot \frac{\Delta R_L}{R_L} \quad ,$$

$$\therefore \quad V_{OFF} = \frac{\left(V_{gs}-V_T\right)^2 \cdot \frac{\Delta R_L}{R_L}}{2\left(V_{gs}-V_T\right)+V_{OFF}}$$

Since V_{OFF} is usually much smaller than $2(V_{gs}-V_T)$, we are going to get:

$$V_{OFF} = \frac{\left(V_{gs}-V_T\right)^2 \cdot \frac{\Delta R_L}{R_L}}{2\left(V_{gs}-V_T\right)+V_{OFF}} \approx \frac{\left(V_{gs}-V_T\right)^2 \cdot \frac{\Delta R_L}{R_L}}{2\left(V_{gs}-V_T\right)} = \left(\frac{V_{gs}-V_T}{2}\right)\cdot\frac{\Delta R_L}{R_L}$$

$$\Rightarrow V_{OFF} \approx \left(\frac{V_{gs}-V_T}{2}\right)\cdot\frac{\Delta R_L}{R_L}$$

, when V_{OFF} is small enough.

Proof finished.

2. Transistor Size Mismatch Δ (W/L):

The transistor mismatch will lead to drain current mismatch between the two differential arms. Since there is no resistive mismatch, the current mismatch could be expressed as following:

$$\begin{aligned}\Delta I_D &= I_{D1}-I_{D2}\\ &= \frac{1}{2}\mu C_{ox}\left(\frac{W}{L}\right)_1\left(V_{gs}-V_T\right)^2 - \frac{1}{2}\mu C_{ox}\left(\frac{W}{L}\right)_2\left(V_{gs}-V_T\right)^2\\ &= \frac{1}{2}\mu C_{ox}\left(V_{gs}-V_T\right)^2\left[\left(\frac{W}{L}\right)_1-\left(\frac{W}{L}\right)_2\right]\\ &= \frac{1}{2}\mu C_{ox}\left(V_{gs}-V_T\right)^2\cdot\Delta\left(\frac{W}{L}\right)\end{aligned}$$

Since the equivalent ΔI_D generated by V_{OFF} caused by Δ (W/L) in this case is also:

$$\Delta I_D = I_{D1(OFFSET)} - I_{D1} = \frac{1}{2}\mu C_{ox}\frac{W}{L}V_{OFF}\left(2V_{gs} + V_{OFF} - 2V_T\right)$$

$$\therefore \quad \frac{1}{2}\mu C_{ox}\frac{W}{L}V_{OFF}\left(2V_{gs} + V_{OFF} - 2V_T\right) = \frac{1}{2}\mu C_{ox}\left(V_{gs} - V_T\right)^2 \cdot \Delta\left(\frac{W}{L}\right)$$

$$\therefore \quad \frac{W}{L}V_{OFF}\left(2V_{gs} + V_{OFF} - 2V_T\right) = \left(V_{gs} - V_T\right)^2 \cdot \Delta\left(\frac{W}{L}\right)$$

$$\therefore \quad V_{OFF} = \frac{\left(V_{gs} - V_T\right)^2 \cdot \Delta\left(\frac{W}{L}\right)}{\left[2\left(V_{gs} - V_T\right) + V_{OFF}\right] \cdot \left(\frac{W}{L}\right)}$$

Similarly, since V_{OFF} is usually much smaller than $2(V_{gs}-V_T)$, we are going to have:

$$V_{OFF} = \frac{\left(V_{gs} - V_T\right)^2 \cdot \Delta\left(\frac{W}{L}\right)}{\left[2\left(V_{gs} - V_T\right) + V_{OFF}\right] \cdot \left(\frac{W}{L}\right)} \approx \left(\frac{V_{gs} - V_T}{2}\right) \cdot \frac{\Delta\left(\frac{W}{L}\right)}{\frac{W}{L}}$$

$$= \left(\frac{V_{gs} - V_T}{2}\right) \cdot \frac{\frac{1}{2}\mu C_{ox} \cdot \Delta\left(\frac{W}{L}\right)}{\frac{1}{2}\mu C_{ox} \cdot \left(\frac{W}{L}\right)} = \left(\frac{V_{gs} - V_T}{2}\right) \cdot \frac{\Delta K}{K}$$

$$\Rightarrow V_{OFF} \approx \left(\frac{V_{gs} - V_T}{2}\right) \cdot \frac{\Delta K}{K}$$

, when V_{OFF} is small enough.

Proof finished.

3. Threshold Voltage Mismatch Δ V_T:

The threshold voltage mismatch will lead to drain current mismatch between the two differential arms. Since there is neither resistive mismatch nor transistor size mismatch, the current mismatch could be expressed as following:

$$\Delta I_D = I_{D2} - I_{D1}$$

$$= \frac{1}{2}\mu C_{ox}\frac{W}{L}\left(V_{gs} - V_{T1}\right)^2 - \frac{1}{2}\mu C_{ox}\frac{W}{L}\left(V_{gs} - V_{T2}\right)^2$$

$$= \frac{1}{2}\mu C_{ox}\frac{W}{L}\left[\left(V_{gs} - V_{T2} + V_{gs} - V_{T1}\right) \cdot \left(V_{gs} - V_{T2} - V_{gs} + V_{T1}\right)\right]$$

$$= \frac{1}{2}\mu C_{ox}\frac{W}{L}\left[\left(2V_{gs} - V_{T1} - V_{T2}\right) \cdot \Delta V_T\right]$$

Since the equivalent ΔI_D generated by V_{OFF} caused by ΔV_T in this case is also:

$$\Delta I_D = I_{D1(OFFSET)} - I_{D1} = \frac{1}{2}\mu C_{ox}\frac{W}{L}V_{OFF}\left(2V_{gs} + V_{OFF} - 2V_T\right)$$

Therefore, we have:

$$\frac{1}{2}\mu C_{ox}\frac{W}{L}V_{OFF}\left(2V_{gs}+V_{OFF}-2V_T\right)=\frac{1}{2}\mu C_{ox}\frac{W}{L}\left[\left(2V_{gs}-V_{T1}-V_{T2}\right)\cdot\Delta V_T\right]$$

$$\therefore\quad V_{OFF}\left(2V_{gs}+V_{OFF}-2V_T\right)=\left(2V_{gs}-V_{T1}-V_{T2}\right)\cdot\Delta V_T$$

$$\therefore\quad V_{OFF}=\frac{\left(2V_{gs}-V_{T1}-V_{T2}\right)\cdot\Delta V_T}{2V_{gs}+V_{OFF}-2V_T}$$

Since V_{OFF} is usually much smaller than $2(V_{gs}-V_T)$, $V_{T1}=V_T+\frac{\Delta V_T}{2}$ and $V_{T2}=V_T-\frac{\Delta V_T}{2}$, we are going to have:

$$V_{OFF}=\frac{\left(2V_{gs}-V_{T1}-V_{T2}\right)\cdot\Delta V_T}{2V_{gs}+V_{OFF}-2V_T}=\frac{\left(2V_{gs}-2V_T\right)\cdot\Delta V_T}{2V_{gs}+V_{OFF}-2V_T}\approx\Delta V_T$$

$\Rightarrow V_{OFF}=\Delta V_T$, when V_{OFF} is small enough.

Proof finished.

4. Determine VOFF when resistive mismatch is 2.5%, transistor size mismatch is 2.5% and ΔV_T=3mV:

(1) When there is resistive mismatch:

$$V_{OFF}\approx\left(\frac{V_{gs}-V_T}{2}\right)\cdot\frac{\Delta R_L}{R_L}$$

Since the mismatch rate should be measured like this:

$$ER=\frac{R_{L1}-R_L}{R_L}\times100\%=\frac{R_L+\frac{\Delta R_L}{2}-R_L}{R_L}\times100\%=\frac{\Delta R_L}{2R_L}\times100\%$$

Therefore,

$$\frac{\Delta R_L}{2R_L}\times100\%=2.5\%\Rightarrow\frac{\Delta R_L}{R_L}=1.25\%$$

Hence,

$$V_{OFF}\approx\left(\frac{V_{gs}-V_T}{2}\right)\cdot\frac{\Delta R_L}{R_L}=\left(\frac{V_{gs}-V_T}{2}\right)\cdot1.25\%$$

Usually, we take $\frac{V_{gs}-V_T}{2}$ between 0.1V and 0.2V, here suppose $\frac{V_{gs}-V_T}{2}=0.15V$, then:

$$V_{OFF} \approx \left(\frac{V_{gs}\text{-}V_T}{2} \right) \cdot 1.25\% = 0.15V \times 1.25\% = 1.875mV$$

(2) When there is transistor size mismatch:

$$V_{OFF} \approx \left(\frac{V_{gs}\text{-}V_T}{2} \right) \cdot \frac{\Delta K}{K}$$

Since similarly, we take $\frac{V_{gs}\text{-}V_T}{2} = 0.15V$ and $\frac{\Delta K}{K} = 1.25\%$, the input offset voltage will be:

$$V_{OFF} \approx 0.15V \times 1.25\% = 1.875mV$$

(3) When there is threshold voltage mismatch:

$$V_{OFF} = \Delta V_T$$

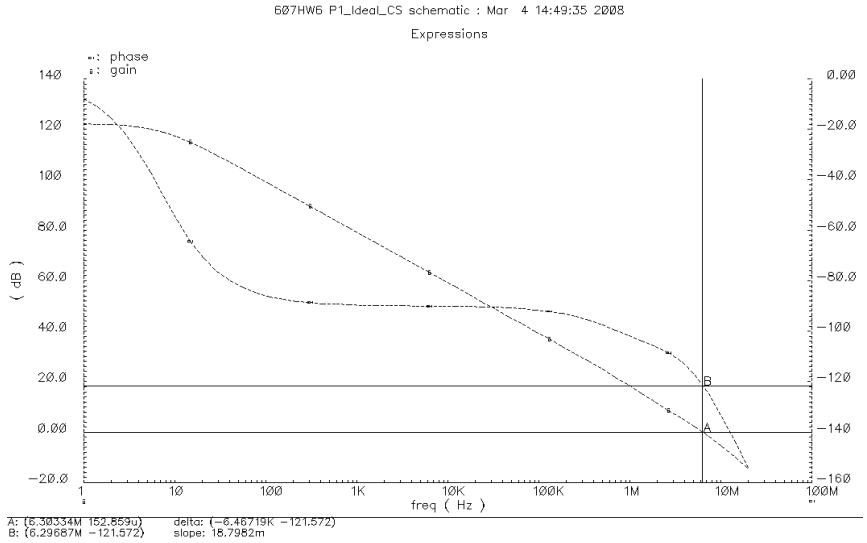
Since $\Delta V_T = 3mV$, V_{OFF}=3mV.

Reference

[1] Fan You, Sherif H. K. Embabi, J. Francisco Duque-Carrillo and Edgar S´anchez-Sinencio, “An Improved Tail Current Source for Low Voltage Applications” JSSC, VOL. 32, NO. 8, AUGUST 1997.

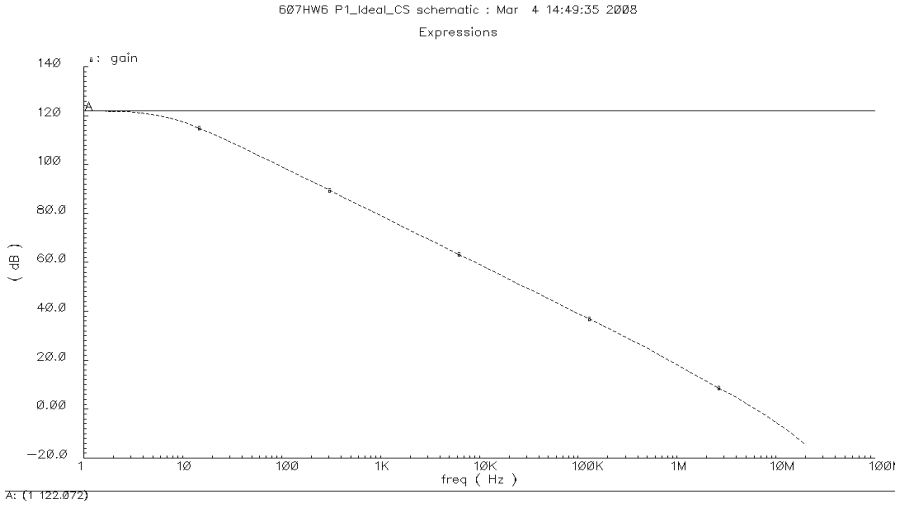
Appendix A: Cadence Simulation Plots for Negative Impedance Amplifier with Ideal Current Source

1. GBW and Phase Margin:



GBW=6.303MHz>5MHz and Phase Margin=58.43°>50°

2. DC Gain:



DC Gain=122.072dB>110dB

3. SNR:

Device	Param	Noise Contribution	% Of Total
/P0	id	4.15912e-09	38.62
/P1	id	4.15632e-09	38.60
/N11	id	6.01921e-10	5.59

Integrated Noise Summary (in V^2) Sorted By Noise Contributors
Total Output Noise = 1.07682e-08
Total Input Referred Noise = 1.06217e-10
The above noise summary info is for noise data

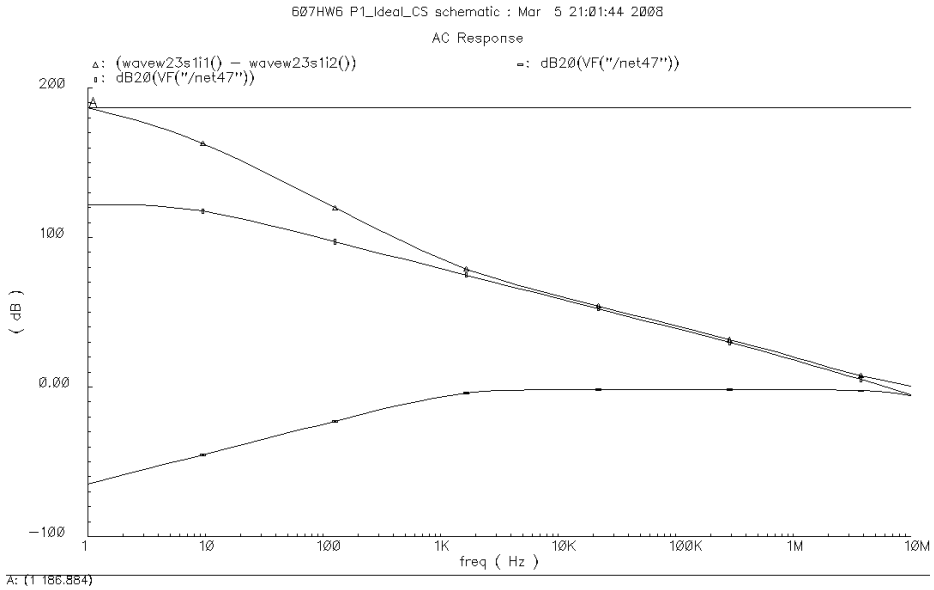
Input Referred Noise=10.62pV^2/Hz (from 0.1MHz to 6MHz)

Therefore, the SNR of the amplifier will be (with a 1Vpp):

$$SNR = 10\log\frac{1^2/2}{1.062\times10^{-8}} = 76.73dB$$

4. PSRR:

No PSRR+ in this case because the noise cannot pass through the ideal current source.

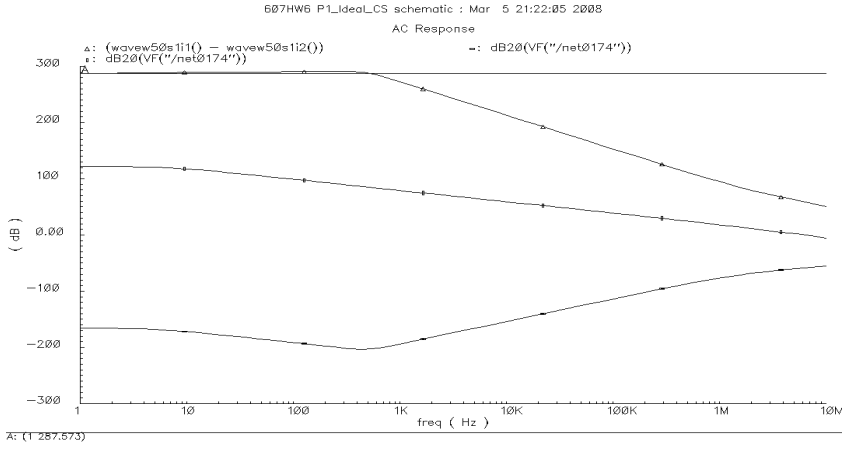


PSRR- = 186.9dB

5. CMR:

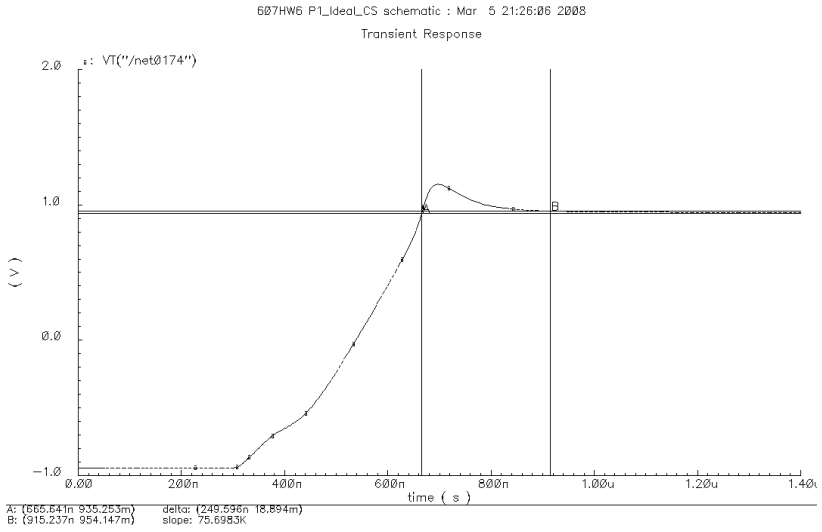
Because of the ideal current source is used, there will be no CMR.

6. CMRR:



CMRR=287.6dB

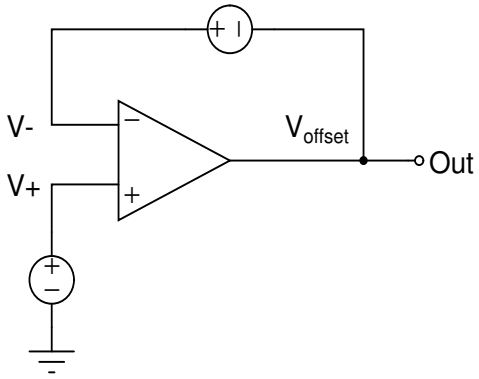
7. 1% Settling Time:



1% Settling Time=249.60ns

8. Input Offset Voltage:

For the negative impedance case, we cannot use DC sweep to do the testing. The reason is that the circuit is very sensitive to the input DC bias and therefore once the DC bias varies, the DC performance of the circuit will be destroyed. The input offset tested from the DC sweep method will not be an accurate value. Hence, the following method will be followed to do this measurement:



According to the definition of input offset voltage, Voffset= V_{-}-V_{+}. As for this proposed method, the DC bias of the circuit is not changed, which means during the testing, V_{+} remains the same. On the other hand, V_{-} will be equal to the summation of V_{out} and the voltage drop of the upper DC voltage source, which will be set equal to V_{+}. Therefore, Vout here will be our input offset voltage once you finish the simple math.

The input offset voltage for this case is:

VDC("/net0174"
85.69e-9

Input Offset Voltage=85.69nV

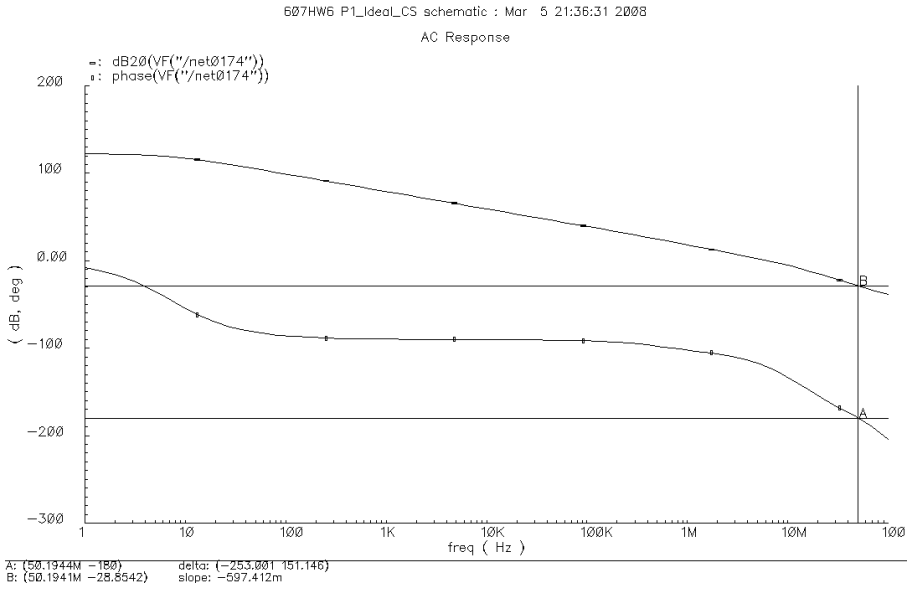
9. Power Consumption:

signal	OP("V1" "??")
i	-1.1m
pwr	-1.1m
v	1

signal	OP("V2" "??")
i	-1.1m
pwr	-1.1m
v	1

Power Consumption=2.2mW

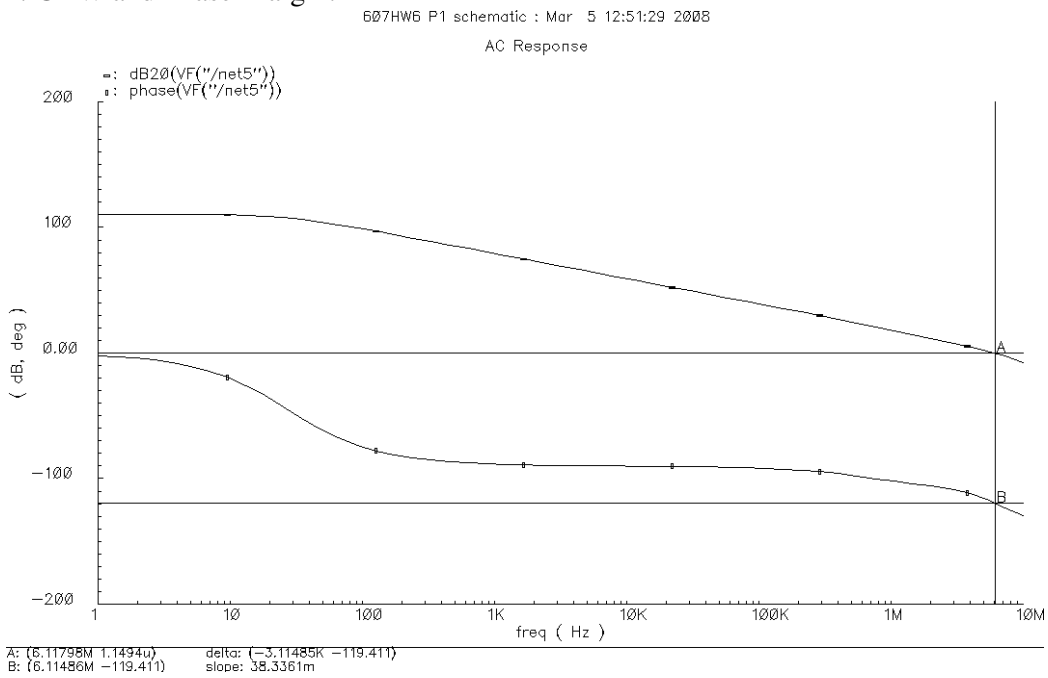
10. Gain Margin:



Gain Margin=28.85dB

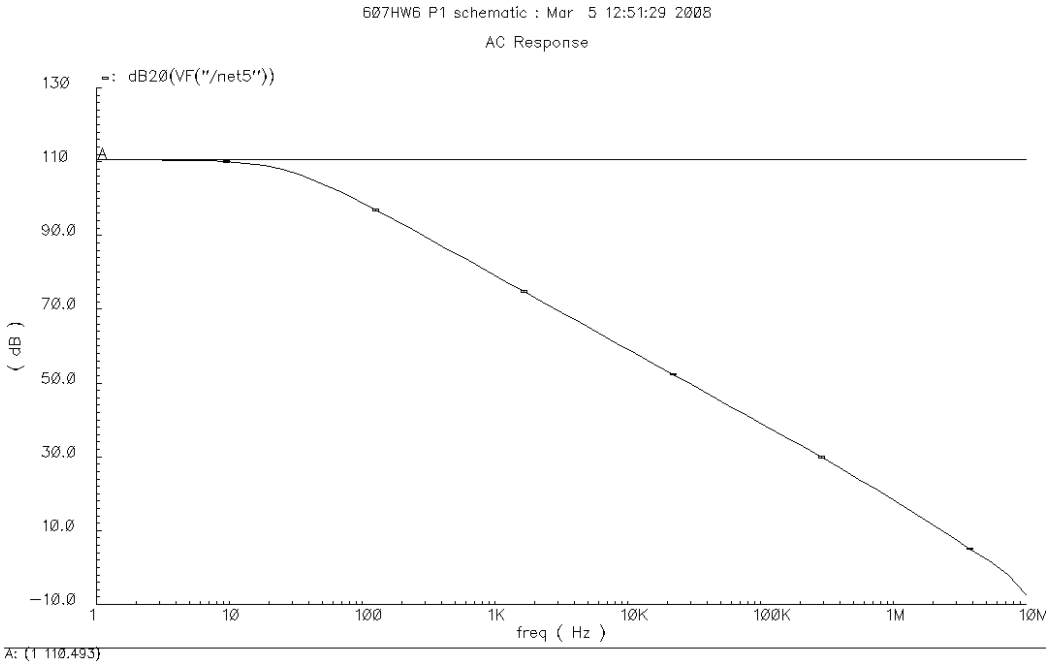
Appendix B: Cadence Simulation Plots for Negative Impedance Amplifier with Low Voltage Current Source

1. GBW and Phase Margin:



GBW=6.118MHz>5MHz and Phase Margin=60.59°>50°

2. DC Gain:



DC Gain=110.493dB>110dB

3. SNR:

Device	Param	Noise Contribution	% Of Total
/P1	id	4.16039e-09	24.63
/P0	id	4.15589e-09	24.60
I12.N10	id	3.9106e-09	23.15

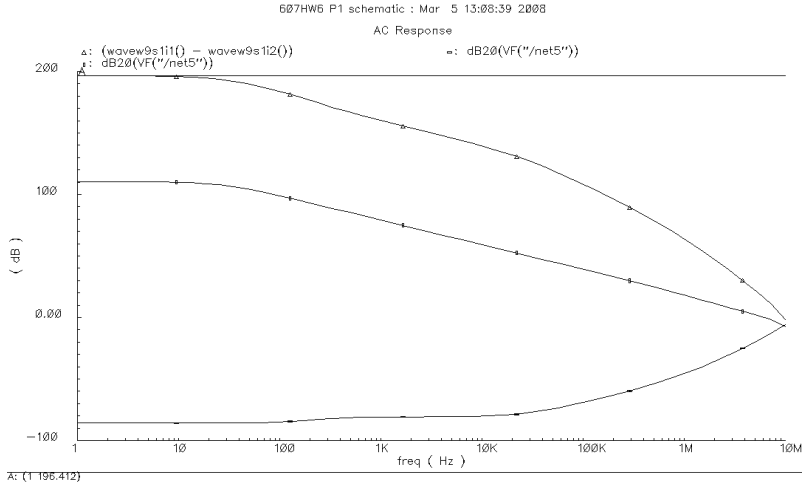
Integrated Noise Summary (in V^2) Sorted By Noise Contributors
Total Output Noise = 1.6891e-08
Total Input Referred Noise = 1.69168e-08
The above noise summary info is for noise data

Input Referred Noise=16.92pV^2/Hz (from 0.1MHz to 6MHz)

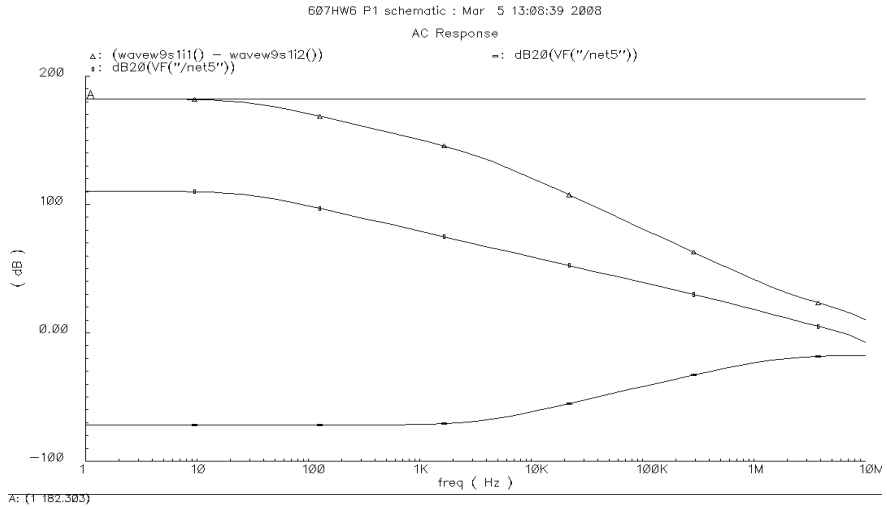
Therefore, the SNR of the amplifier will be (with a 1Vpp):

$$SNR = 10\log\frac{1^2/2}{1.692\times10^{-8}} = 74.71dB$$

4. PSRR:

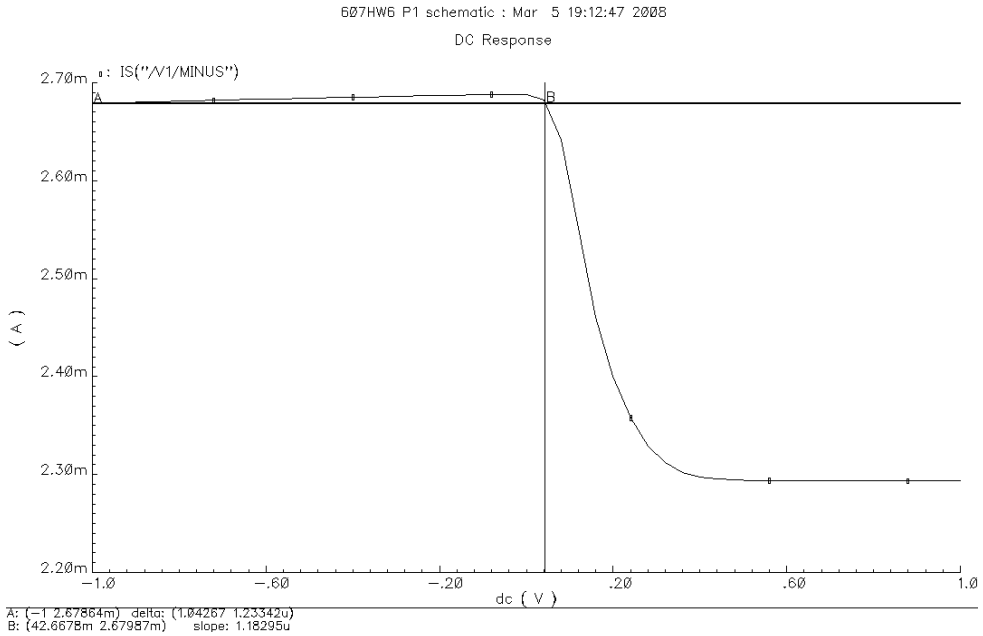


PSRR+ = 196.4dB



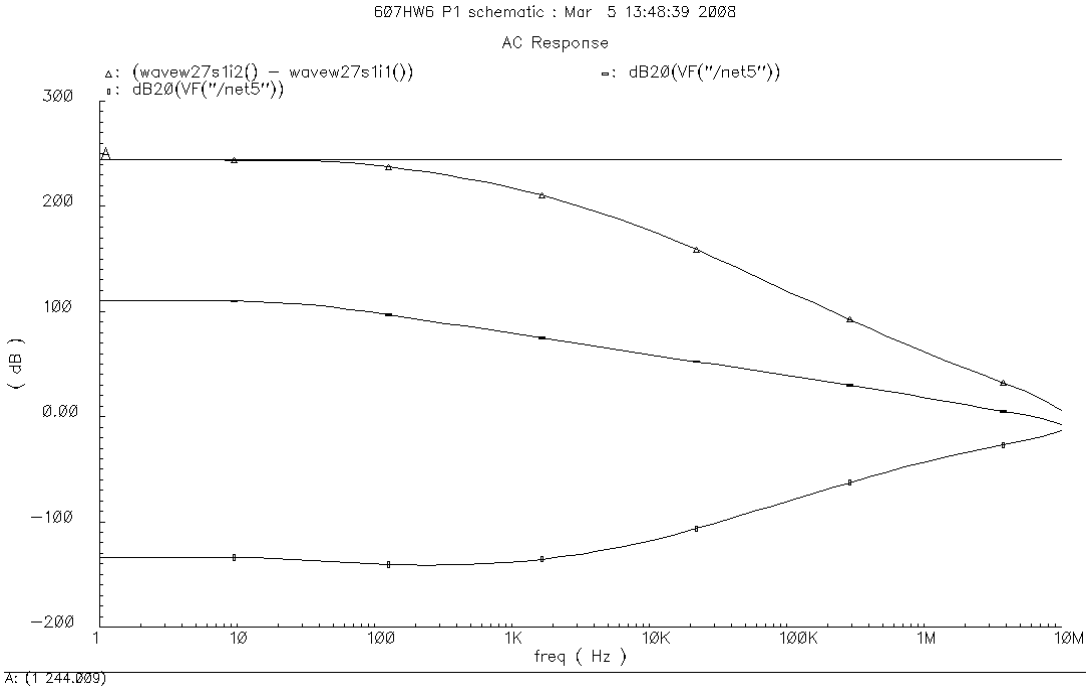
PSRR- = 182.3dB

5. CMR:



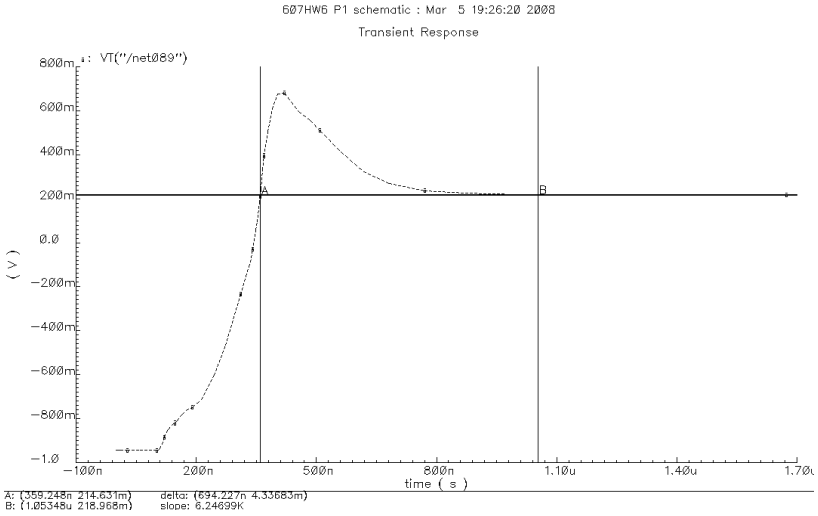
CMR=1.04V

6. CMRR:



CMRR=244dB

7. 1% Settling Time:



1% Settling Time=694.23ns

8. Input Offset Voltage:

VDC("/net089")
395.2e-9

Input Offset Voltage=395.2nV

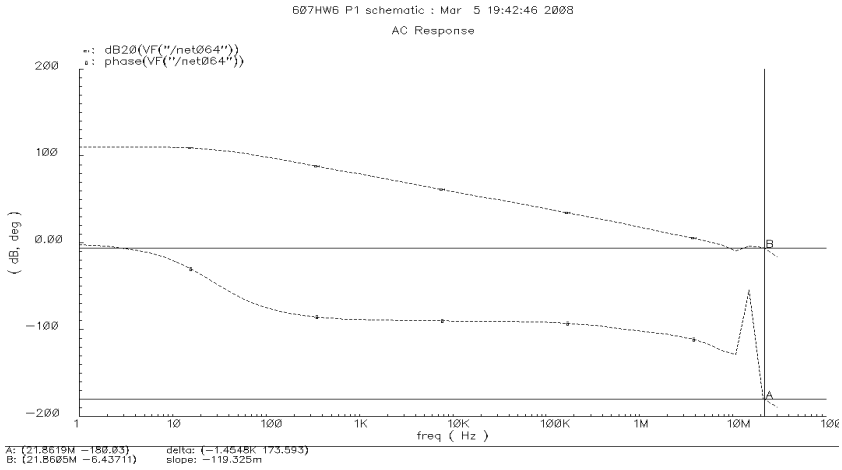
9. Power Consumption:

signal	OP("V1" "??")
i	-2.687m
pwr	-2.687m
v	1

signal	OP("V2" "??")
i	-2.687m
pwr	-2.687m
v	1

Power Consumption=5.374mW

10. Gain Margin:



Gain Margin=6.44dB