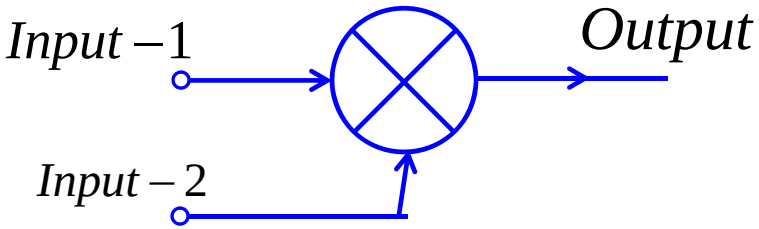


CMOS Multipliers: Architectures and Transistor level Implementations

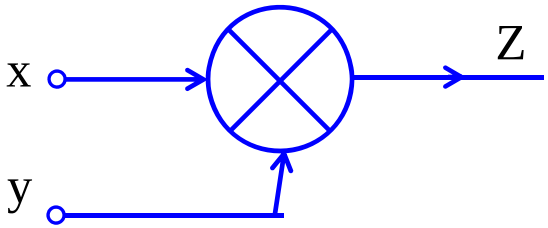
By Edgar Sánchez-Sinencio

Analog and Mixed-Signal Center, TAMU

607 Spring'12

Multipliers

What is a multiplier?



$Z = Kxy$

Where

x and y are the input signals, Z is the output and K is a constant with suitable dimensions.

How do you obtain a multiplier?

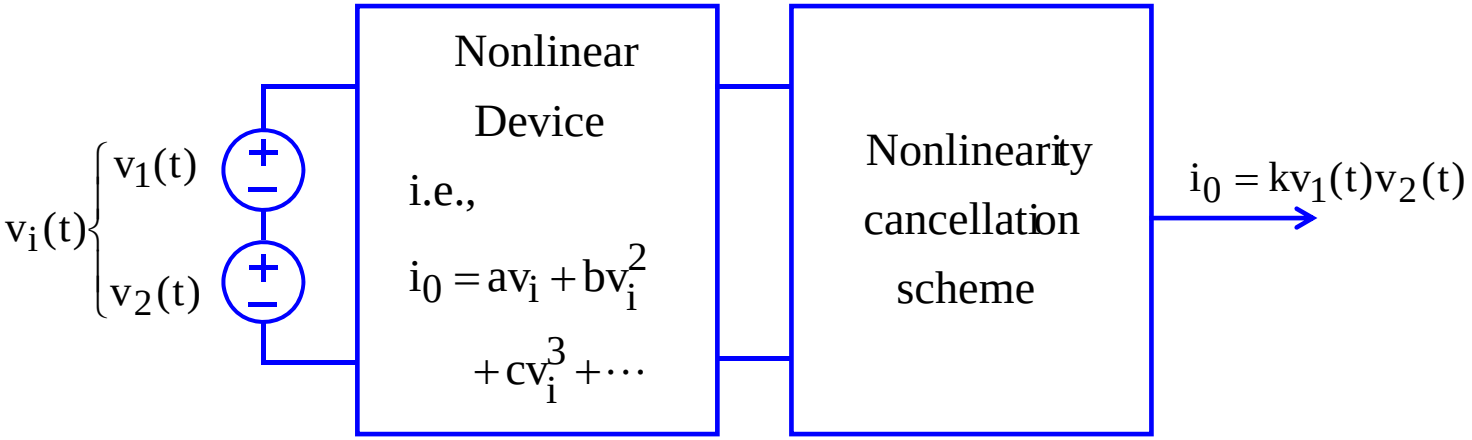


Fig. 1 Basic idea of multiplier

Transconductance-Mode Multiplier

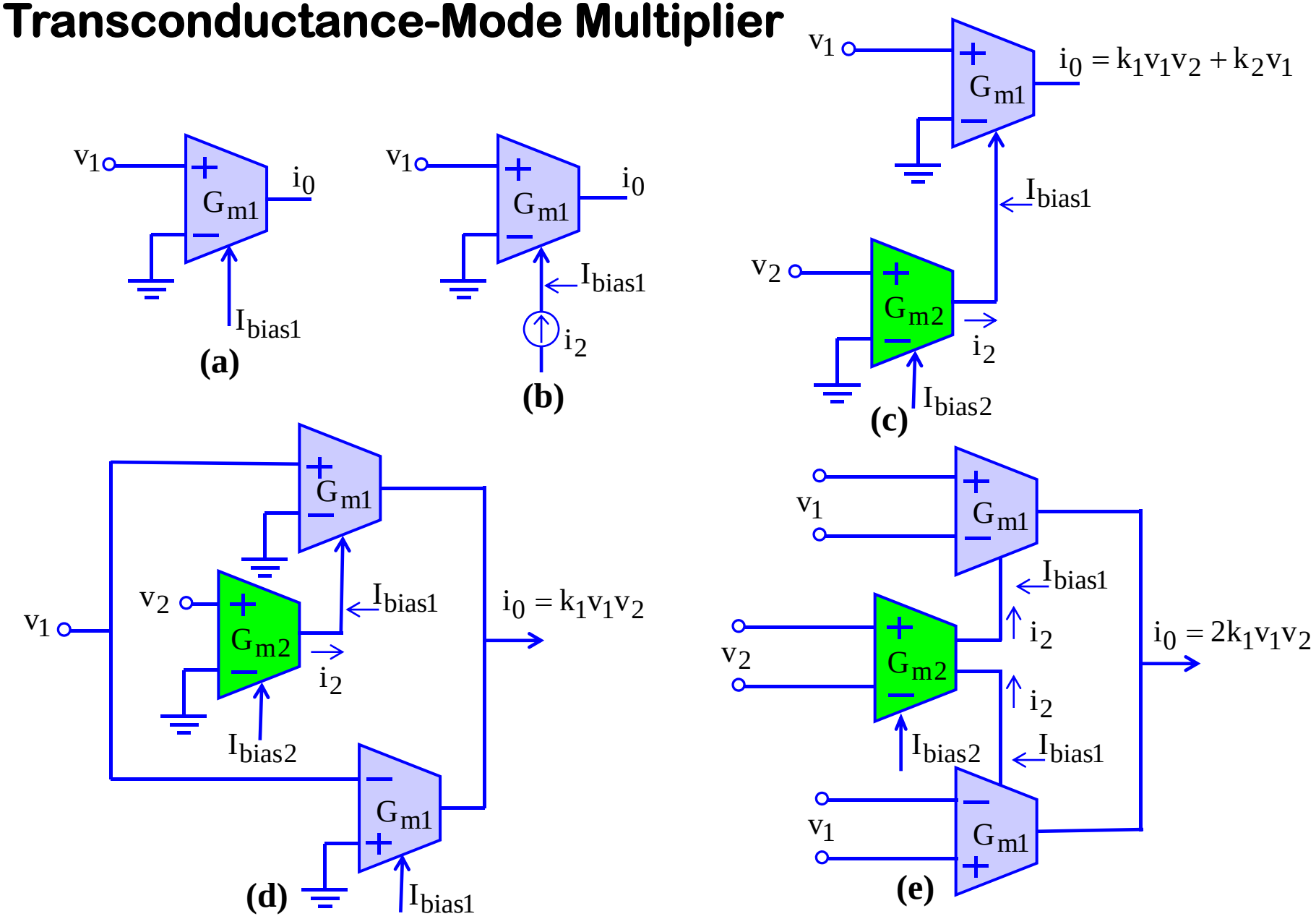


Fig. 2 Multiplication operation using programmable transconductor

How Does It Work?

$$i_0 = G_{m1} v_1 \tag{1}$$

where

$$G_{m1} = G_{m1}(I_{bias1}) \tag{2a}$$

For a bipolar transconductor, G_{m1} becomes

$$G_{m1} = \frac{I_{bias1}}{2V_t} \tag{2b}$$

$$i_0(t) = G_{m1} v_1 = \frac{I_{bias1} + G_{m2} v_2(t)}{2V_t} v_1(t) \tag{3a}$$

$$i_0(t) = \frac{G_{m2} v_1(t) v_2(t)}{2V_t} + \frac{I_{bias1}}{2V_t} v_1(t) = \frac{I_{bias2} v_1(t) v_2(t)}{2V_t 2V_t} + \frac{I_{bias1} v_1(t)}{2V_t} \tag{3b}$$

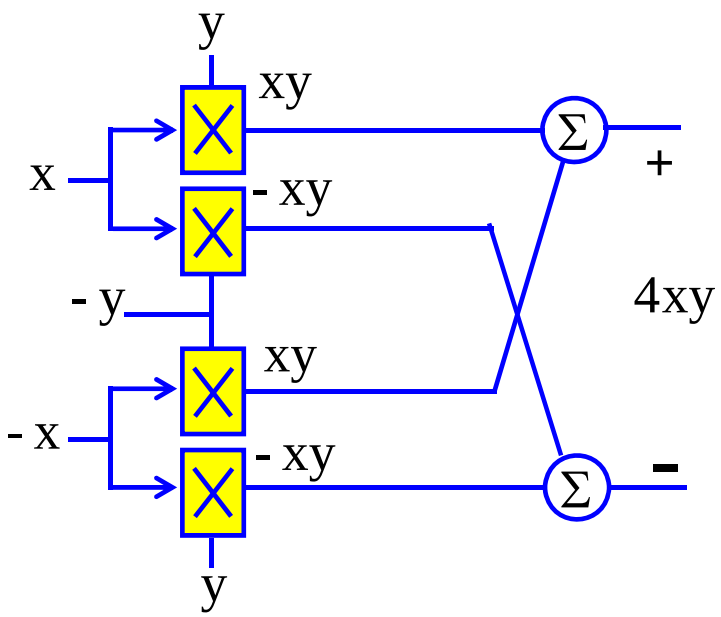
or

$$i_0(t) = k_1 v_1(t) v_2(t) + k_2 v_1(t) \tag{3c}$$

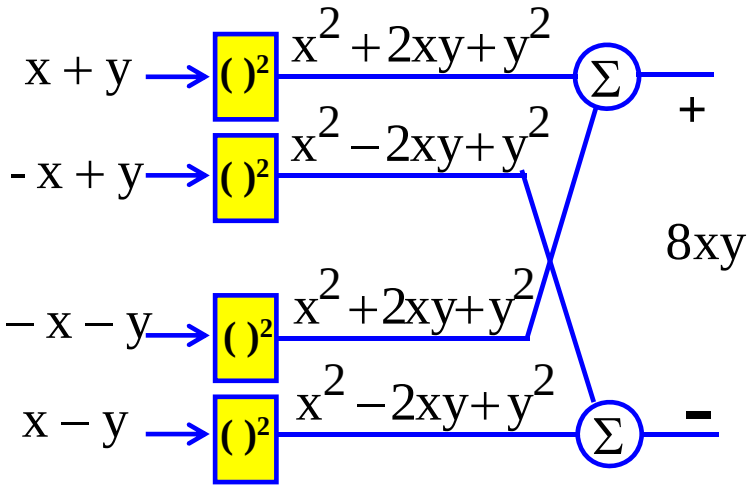
Thus, $i_0(t)$ represents the multiplication of two signals $v_1(t)$ and $v_2(t)$, and an unwanted component, $k_2 v_1(t)$. This component can be eliminated as shown in Fig. 2(d). Better cancellation is achieved when the third transconductor (G_{m2}) becomes a fully differential transconductor, and v_1 and v_2 are fully differential inputs as illustrated in Fig. 2(e).

$$i_0(t) = 2k_1 v_1(t) v_2(t) \tag{4}$$

Basic Multiplier Architectures



(a) using single-quadrant multipliers



(b) using square divices

Where capital (low case) letters represent DC (time domain) signals.

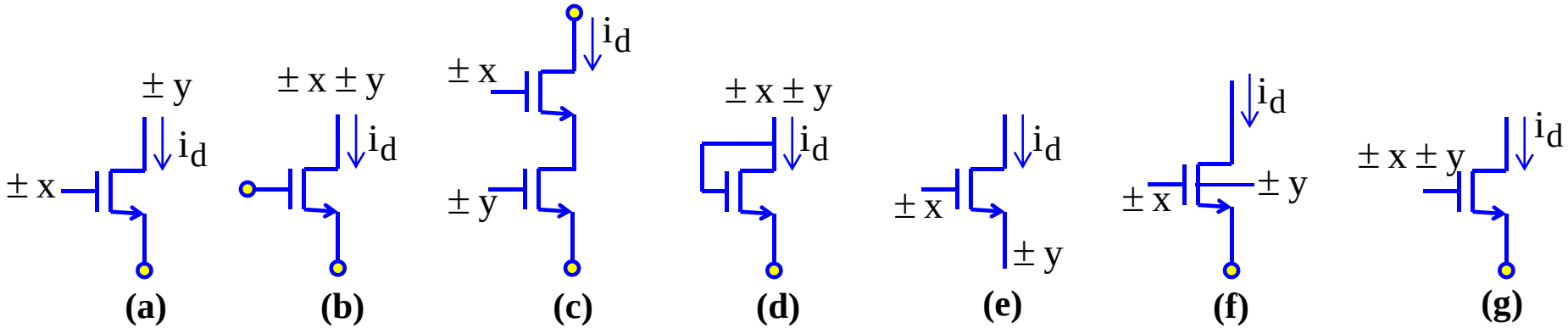
$$\left[(X+x)(Y+y)+(X-x)(Y-y)\right]$$
$$-\left[(X-x)(Y+y)+(X+x)(Y-y)\right]=4xy$$

or

$$\left\{\{(X+x)+(Y+y)\}^2+\{(X-x)+(Y-y)\}^2\right\}$$
$$-\left[\{(X-x)+(Y+y)\}^2+\{(X+x)+(Y-y)\}^2\right]=8xy$$

How the x and y Inputs can be Applied?

Consider a one transistor case first.



Voltage signal injection methods

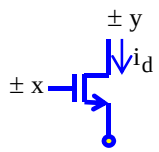
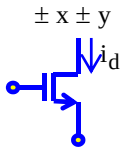
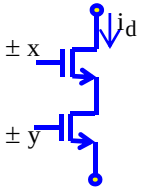
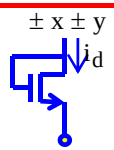
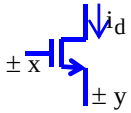
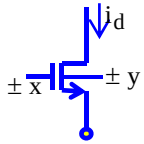
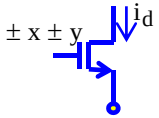
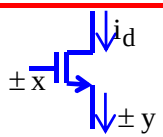
The simple MOS transistor model is expressed as :

$$I_d = K\left[V_{gs} - V_T - \frac{V_{ds}}{2}\right]V_{ds} = K\left[V_{gs}V_{ds} - V_T V_{ds} - \frac{V_{ds}^2}{2}\right] \quad \text{for } V_{gs} > V_T,\ V_{ds} < V_{gs} - V_T$$

$$I_d = \frac{K}{2}\left[V_{gs} - V_T\right]^2 = \frac{K}{2}\left[V_{gs}^2 - 2V_{gs}V_T - V_T^2\right] \quad \text{for } V_{gs} > V_T,\ V_{ds} > V_{gs} - V_T$$

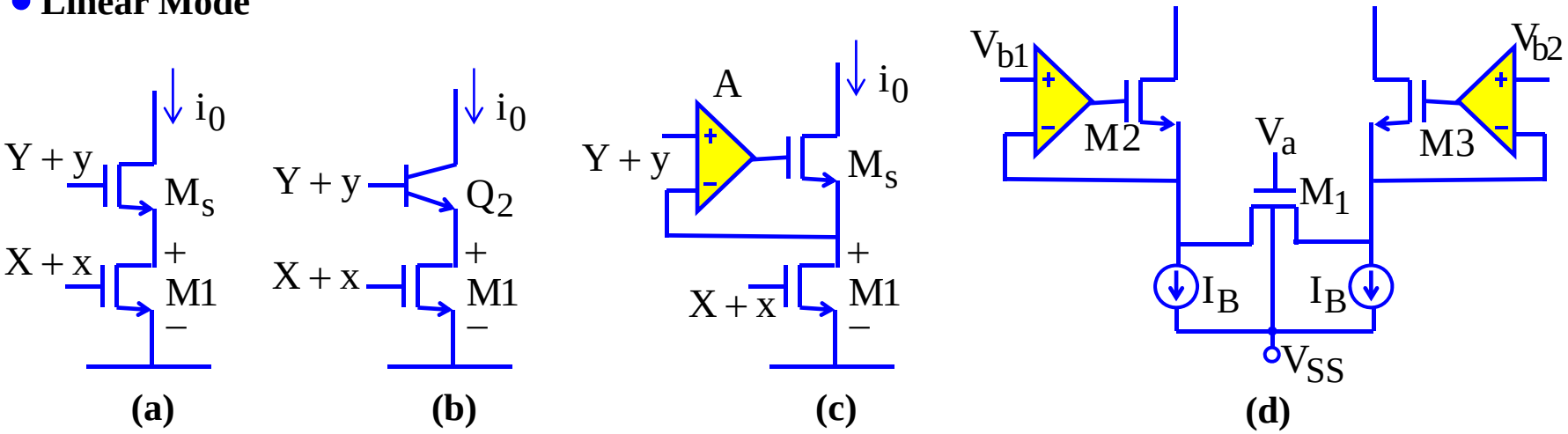
Results are summarized next.

Table 1. Summary of multiplier operating modes

Operating region	Input signal injection method	Active term	Cancellation method	Type	Comment
Linear		$V_{gs}V_{ds}$	single-quadrant	I	
		V_{ds}^2	square device	II	Not practical
		$V_{gs}V_{ds}$	single-quadrant	III	Not practical
Saturation		V_{gs}^2	square device	IV	Not practical
		V_{gs}^2	square device	V	
		V_{gb}^2	square device	VI	Not practical
		V_{gs}^2	square device	VII	
		V_{gs}^2	Gilbert cell (single-quadrant)	VIII	

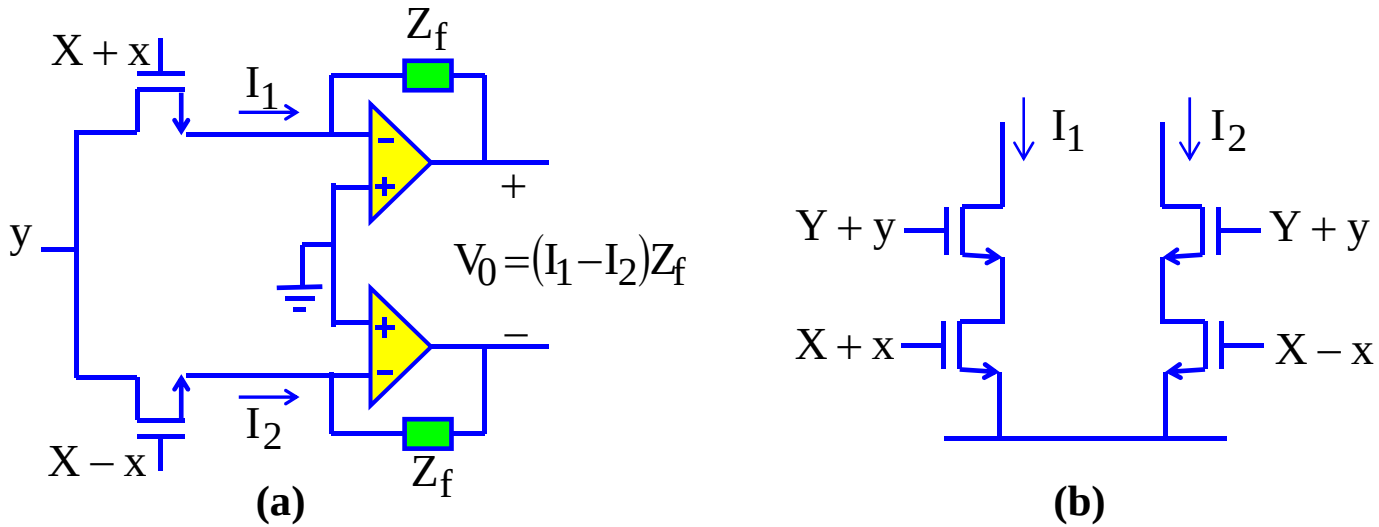
Let us describe multipliers as functions of their mode of operations

- **Linear Mode**



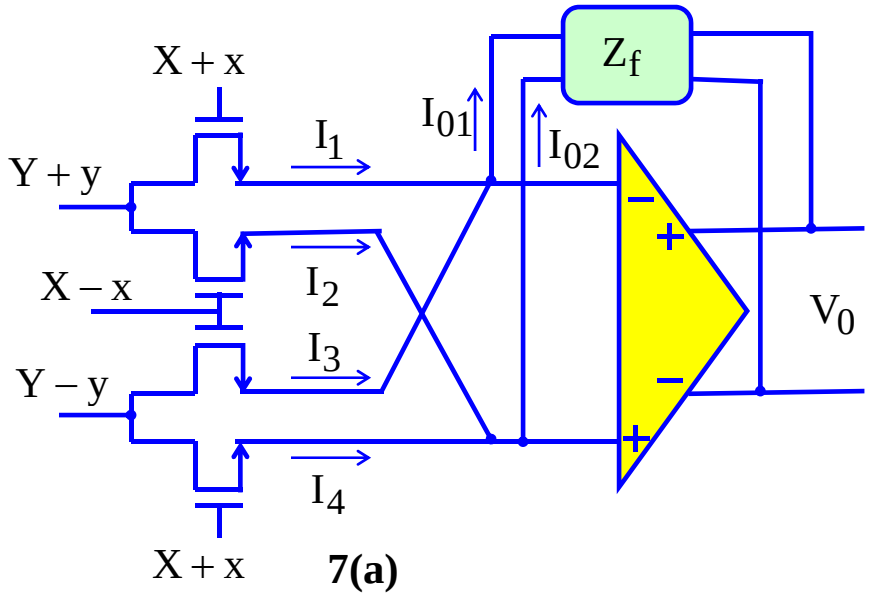
Programmable transconductor in ohmic operation

Using $V_{gs}V_{ds}$ (Type I)

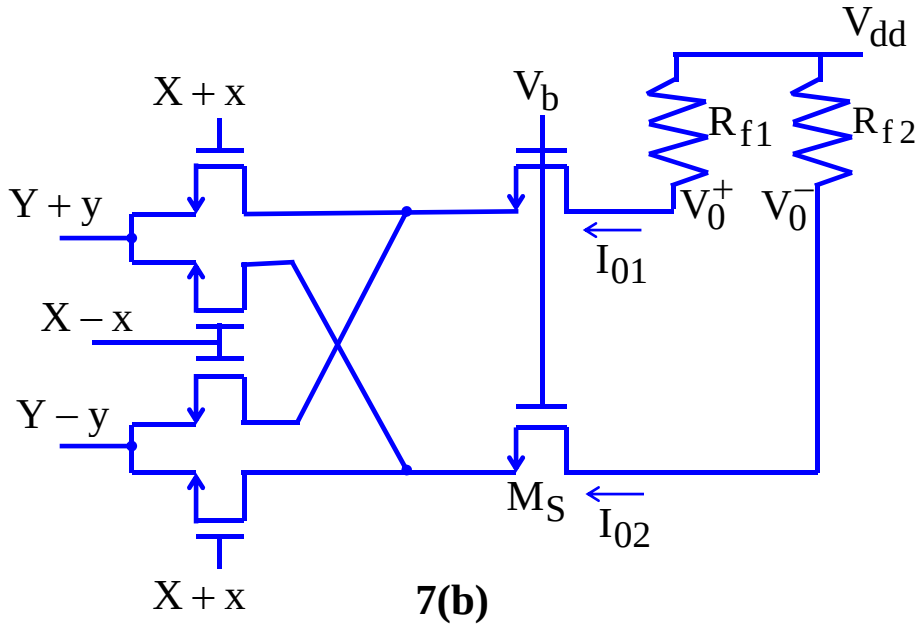


Four-quadrants multipliers with two transistors operating in linear region

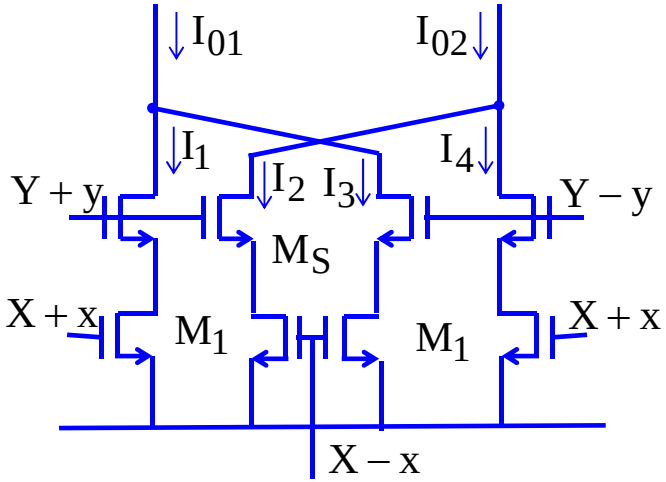
Multiplier Implementations Using $V_{gs}V_{ds}$ (Type I)



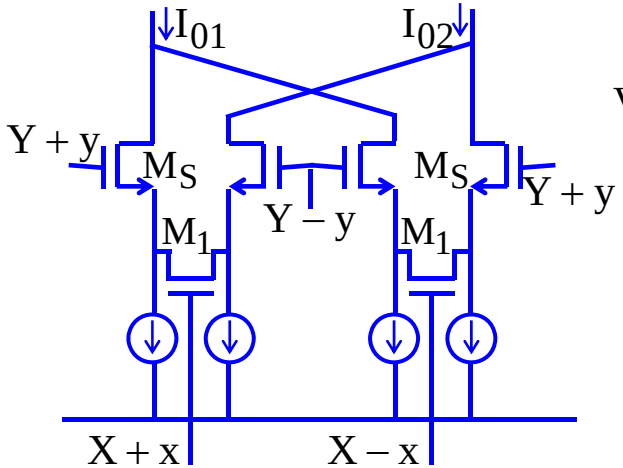
7(a)



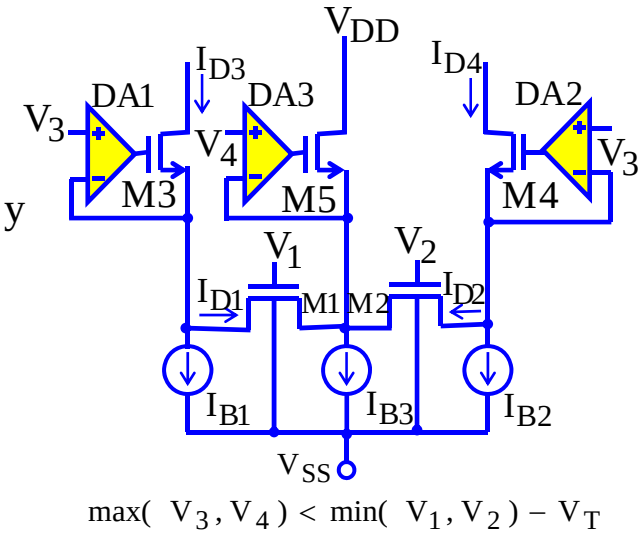
7(b)



7(c)



7(d)



$\max(V_3, V_4) < \min(V_1, V_2) - V_T$

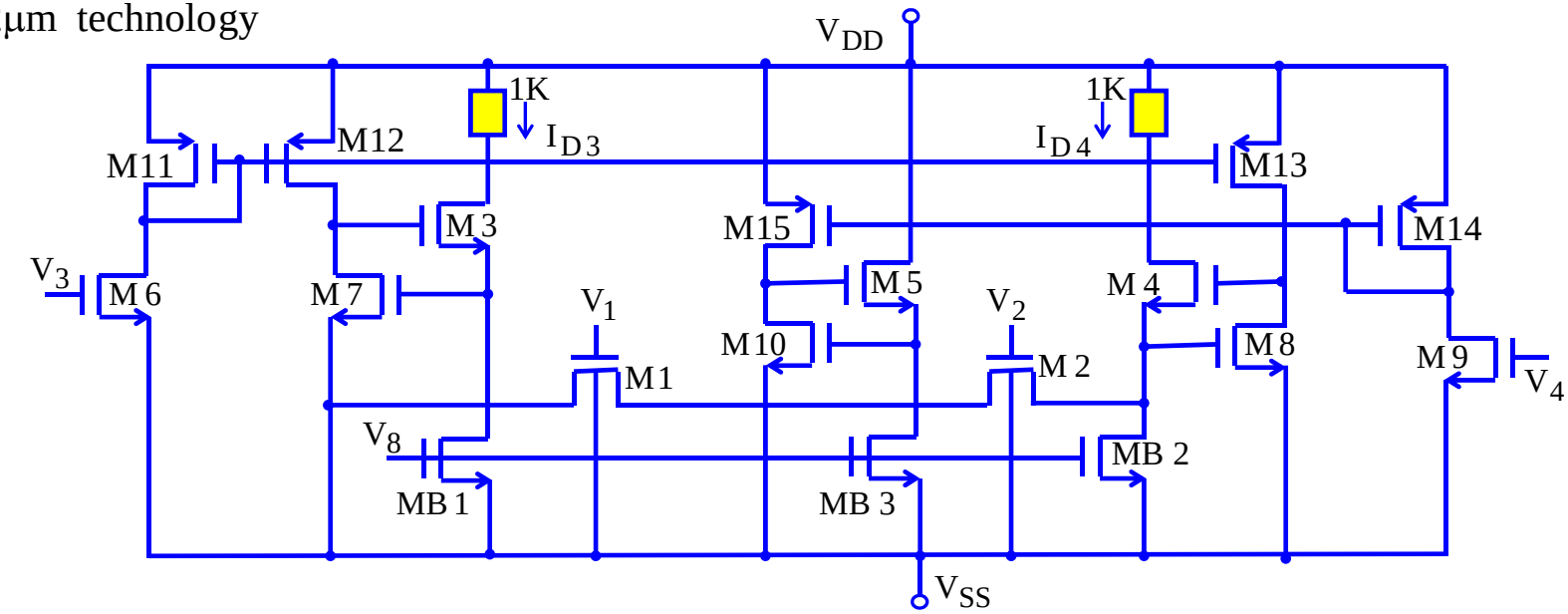
7(e)

Fig. 7 Fully-differential four-quadrant multipliers using VgsVds term (Type I)

Example of a Complete Implementation of Multiplier $V_{gs}V_{ds}$ Type I. {From Fig. 7(e)}

± 3V supply voltages

2μm technology



Transistors	M1 – M2	M3 – M5	M6 – M10	M11 – M15	MB1 – MB3
W[μm]/L[μm]	10/50	100/5	10/10	50/5	10/10

$$I_{D3} = I_{B1} + I_{D1} = I_{B1} + 2K_1\left[(V_{GS1} - V_{T1})V_{DS1} - \frac{1}{2}V_{DS1}^2\right] \qquad (1)$$

and

$$I_{D4} = I_{B2} + I_{D2} = I_{B2} + 2K_2\left[(V_{GS2} - V_{T2})V_{DS2} - \frac{1}{2}V_{DS2}^2\right] \qquad (2)$$

It is evident th at M1 and M2 have the same drain and source voltages. Thus $V_{DS1} = V_{DS2}$ and $V_{T1} = V_{T2}$ Now, let $K_1 = K_2 = K$ and $I_{B1} = I_{B2} = I_B$. The output current I_{out} can then be written as :

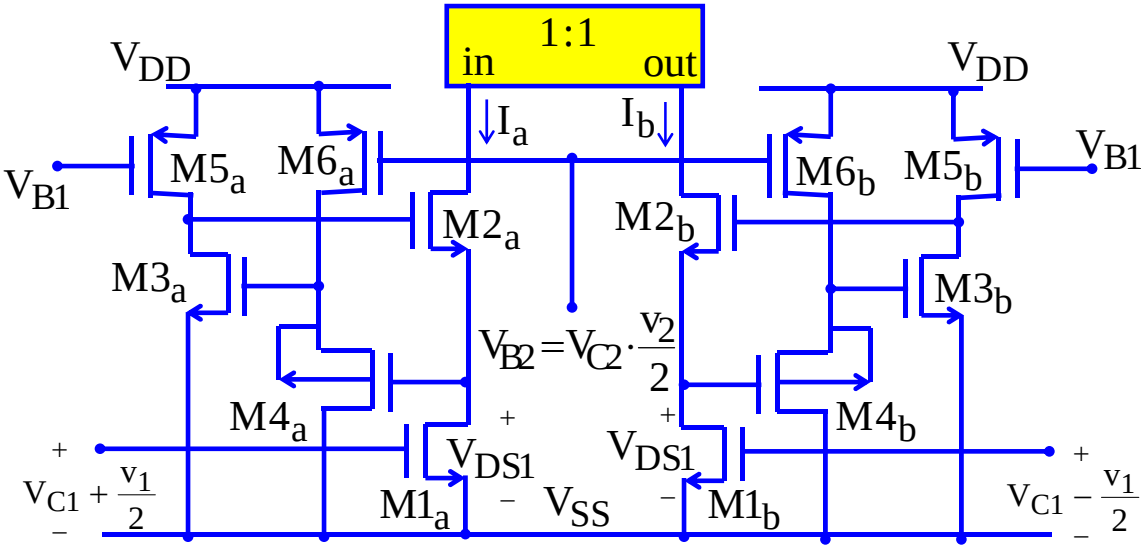
$$I_{out} = I_{D3} - I_{D4} = I_{D1} - I_{D2} = 2K(V_1 - V_2)(V_3 - V_4) \qquad (3)$$

Low voltage multiplier working with transistors in linear region. (Coban & Allen)

- One single 1.5V supply
- $M1_a$ and $M1_b$ in linear range. $I_1 \cong K_1 v_1 V_{DS}$

  $I_0 = I_1 - I'_1 = K v_1 v_2$ requires two of the following transconductors.

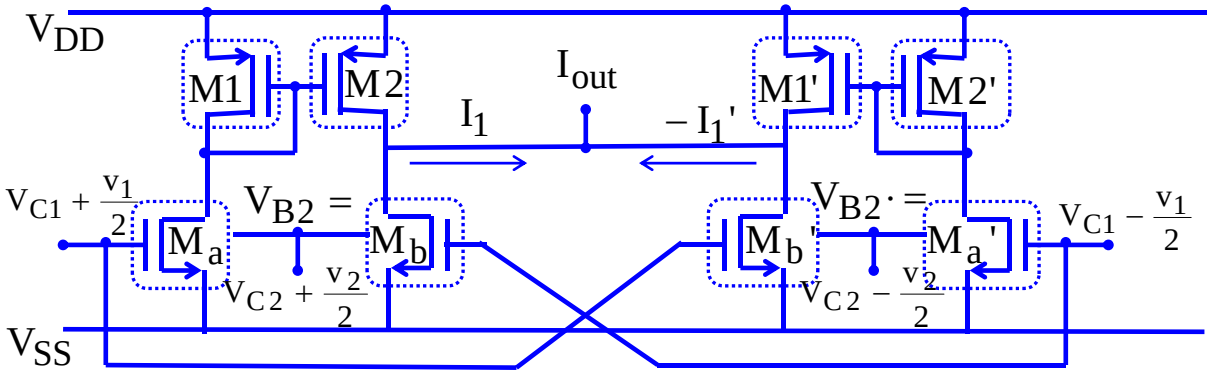
  with $K = K_1\sqrt{K_6 / K_4}$



Low voltage transconductor block

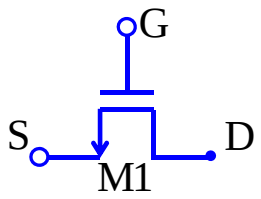
- Use composite transistor.
- Based on the regulated cascode circuit.

- The complete circuit with composite transistors drawn as single transistors.



Proposed low voltage four quadrant multiplier

Multiplier Using a Transistor in the Linear Range



M1 Operating in the linear (OHMIC) region

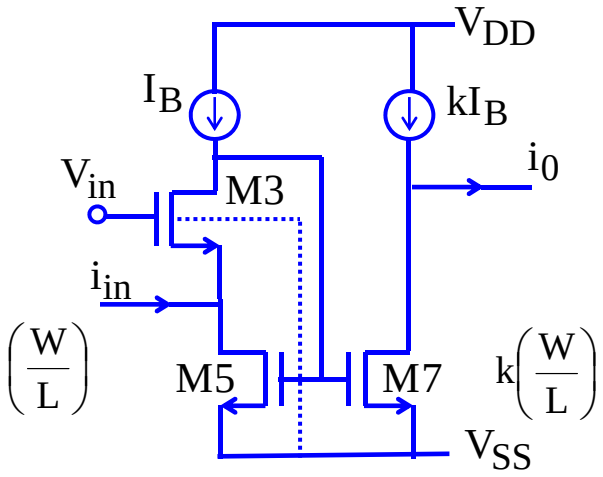
$$I_D = K_P\left(\frac{W}{L}\right)\left[V_{GS} - V_T - \frac{V_{DS}}{2}\right]V_{DS}$$

$$I_D = K_P\left(\frac{W}{L}\right)\left[V_{GS}V_{DS} - \left(V_T + \frac{V_{DS}}{2}\right)V_{DS}\right]$$

For $V_{DS} << V_{GS}$, I_D Becomes:

$$I_D \cong K_P\left(\frac{W}{L}\right)V_{GS}V_{DS} + \Delta I_D, \quad \Delta I_D \sim 0$$

How to sense the drain current while at the same time provide the input voltage at the same node?



$$\frac{f_{nd}}{GBW} \cong \frac{V_{GS3} - V_{T3}}{V_{GS5} - V_{T5}} \cdot 2$$

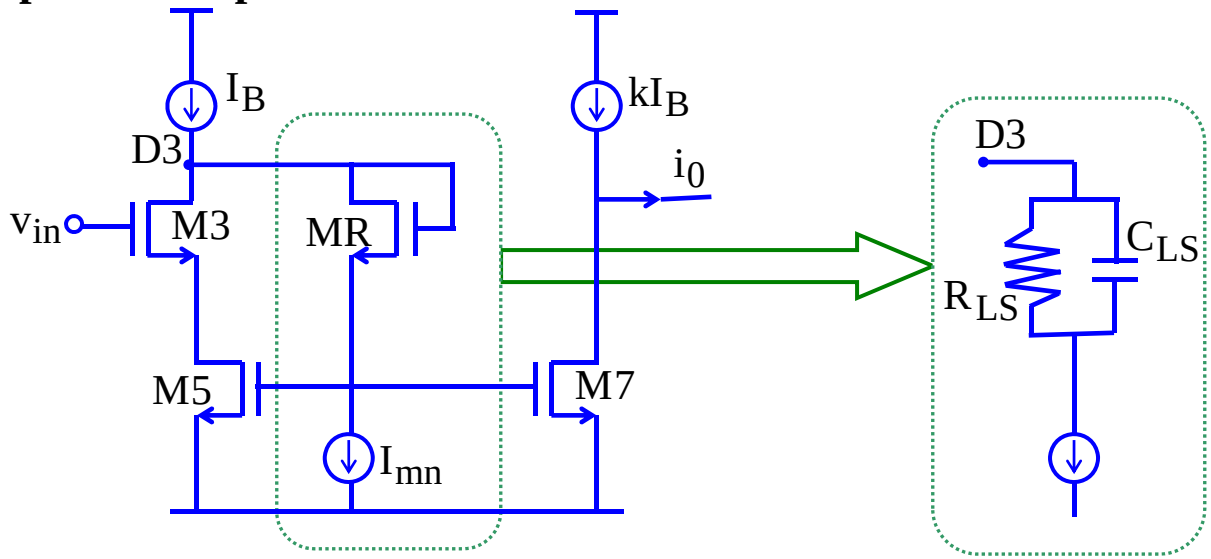
$i_0 = ki_{in}$

M3 acts as a voltage follower, i.e.

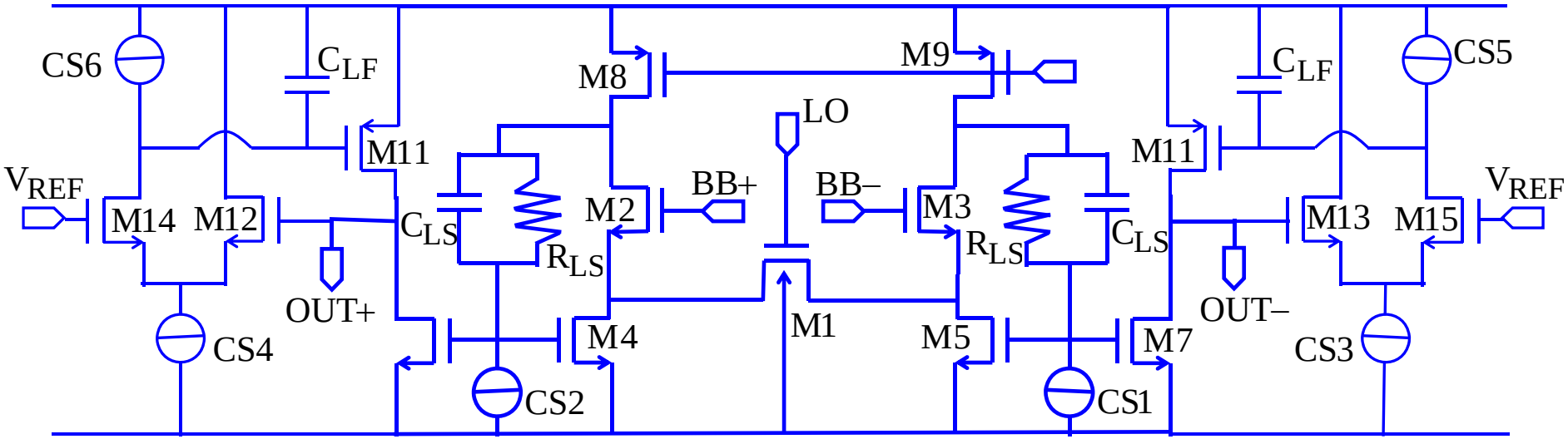
$$A_{V3} = \frac{1}{1 + g_{mb3}/g_{m3}}$$

M3 input voltage range is limited due to the feedback connection of M7, therefore it is needed to be boosted with a level shifter.

A possible implementation follows:

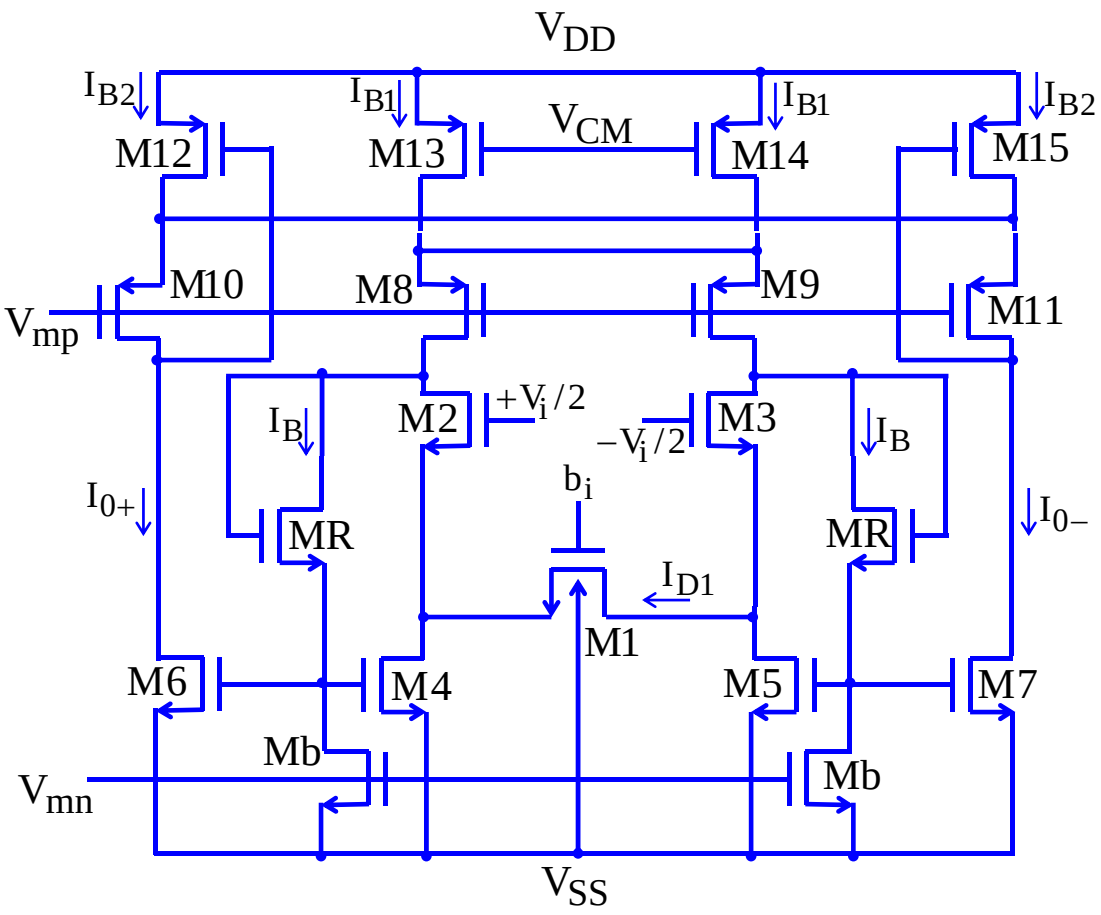


Version 1 of a complete multiplier (mixer)



The differential linear up-conversion mixer; the single ended carrier signal is applied at the LO terminal and the differential baseband signal is applied at the BB terminals. The baseband modulation feedthrough in the output signal is suppressed through the output circuits (thin lines) which act as active coils

Version 2: Multiplier Using Cascode Current Source.



Switching Modulator Based on Linear MOS

For $M2 = M3$

$$+V_1^+ - V_{S1} = V_{T0} + \sqrt{\frac{I_{B1}}{K_p (W/L)_2}}$$

$$V_1^- - V_{D1} = V_{T0} + \sqrt{\frac{I_{B1}}{K_p (W/L)_3}}$$

Thus for $V_1^+ = V_i / 2$ and $V_1^- = -V_i / 2$

$$V_{DS1} = -\frac{V_i}{2} - \frac{V_i}{2} = -V_i$$

Neglecting ΔI_D, it yields:

$$I_{D1} = K_p (W/L)_1$$

M4, M6 and M5, M7 act as CM, then

$$I_0^+ = K_p (W/L)_1 \frac{(W/L)_6}{(W/L)_4} \left[V_i \left(b_i - \frac{V_i}{2} \right) \right]$$

$$I_0^- = -K_p (W/L)_1 \frac{(W/L)_7}{(W/L)_5} \left[V_i \left(b_i - \frac{V_i}{2} \right) \right]$$

$$I_{0d} = \frac{I_0^+ - I_0^-}{2} = K_p \left(\frac{W}{L} \right)_1 \frac{(W/L)_{6,7}}{(W/L)_{4,5}} \left[2 V_i b_i - V_i^2 \right]$$

$$I_{0d} \cong K_p \left(\frac{W}{L} \right)_1 \frac{(W/L)_{6,7}}{(W/L)_{4,5}} \left[V_i \cdot b_i \right] \quad \text{for } V_i << b_i$$

Linear Operation using V^2_{ds} (Type II)

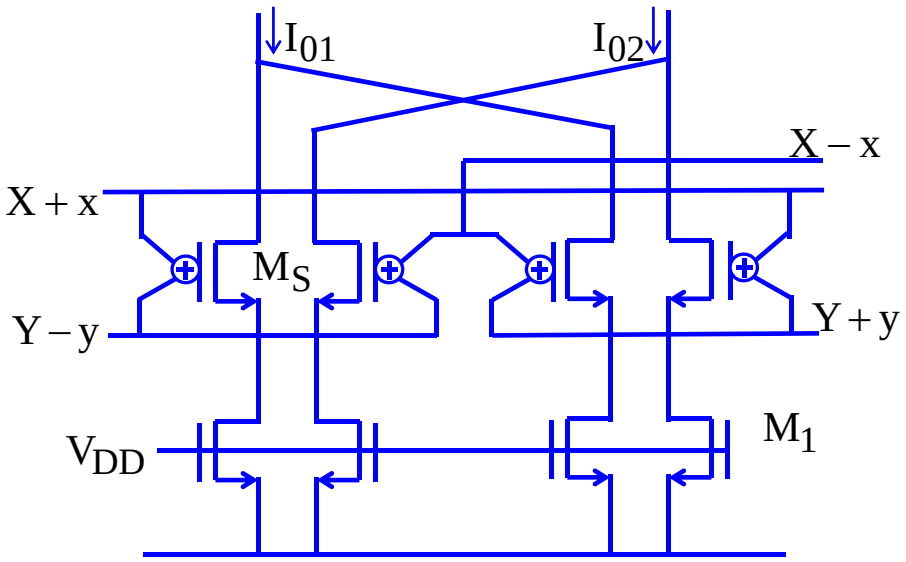
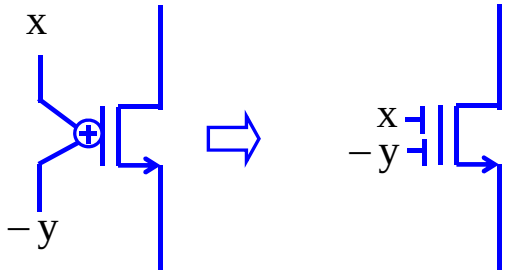


Fig. 8 Multiplier using V^2_{ds} (Type II)



A possible summer implementation

$$I_0 = I_{01} - I_{02} = Kxy$$

Dual Gate in Linear Range (Type III)

$M_{d1} = M_{d2}$ in saturation region

M1 & M2 in Linear Region. Where $V_{pol} \cong \sqrt{\frac{I_{pol}}{K_d}}$ for $I_d << I_{pol}$

and $C = V_{com} - V_S - V_T - V_{pol}$ and $C >> x, y$

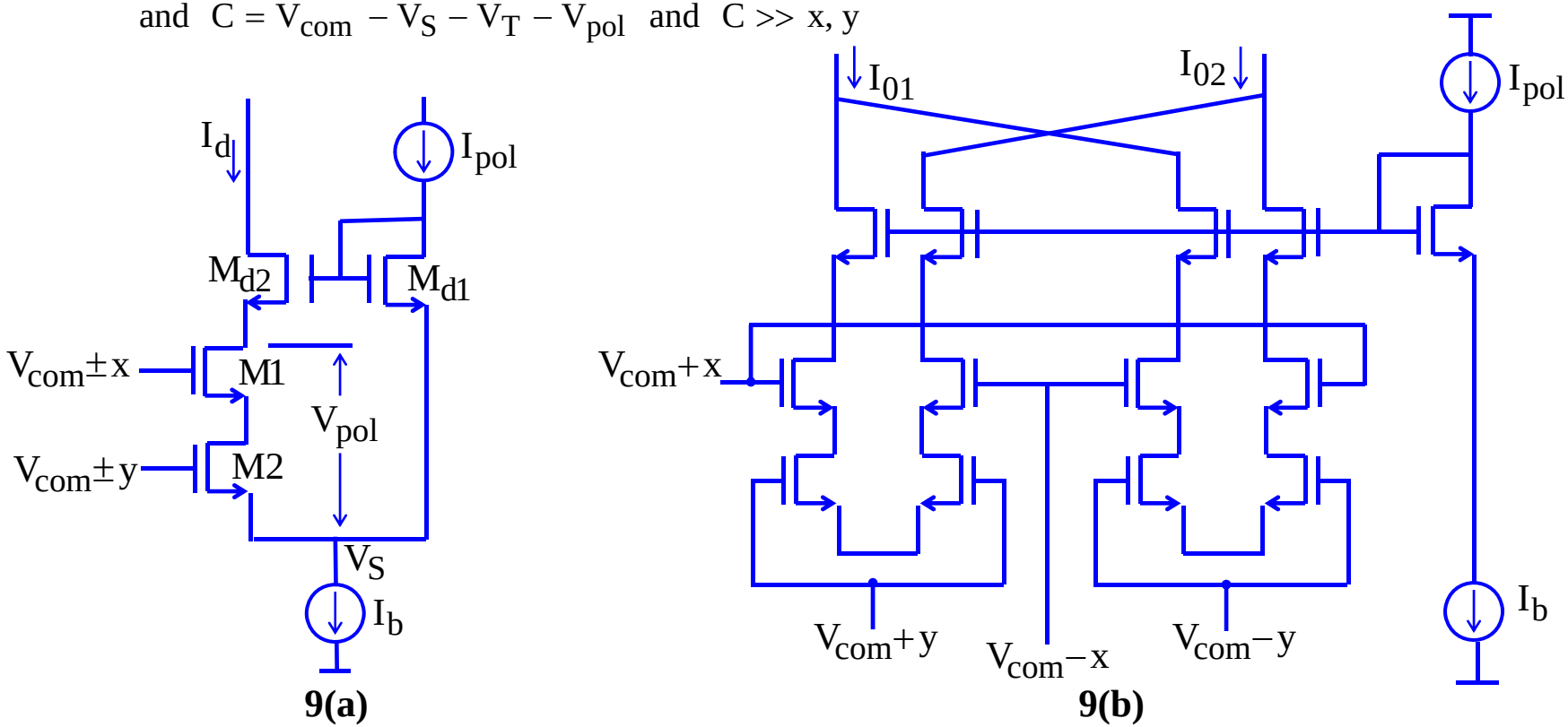
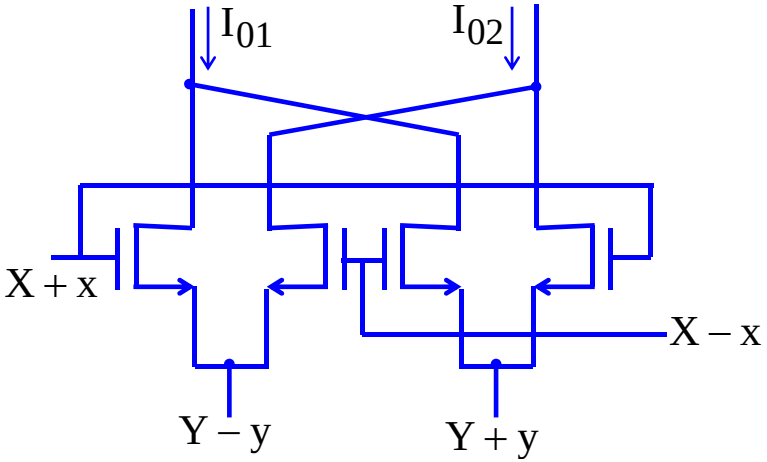


Fig. 9 Four quadrant multiplier using dual gate (Type III)

$$I_0 = I_{01} - I_{02} = 8KV_{pol}cxy\frac{x^2 + y^2 - 2c^2}{(4c^2 - (x+y)^2)(4c^2 - (x-y)^2)}$$

$$I_0 \cong \frac{KV_{pol}}{c}xy$$

MOS Multipliers Operation in Saturation Region



Four cross coupled FETs multiplier using V_{gs}^2 term. (Type V)

Based on the 4xy architecture

$$I_0 = I_{01} - I_{02} = 4Kxy$$

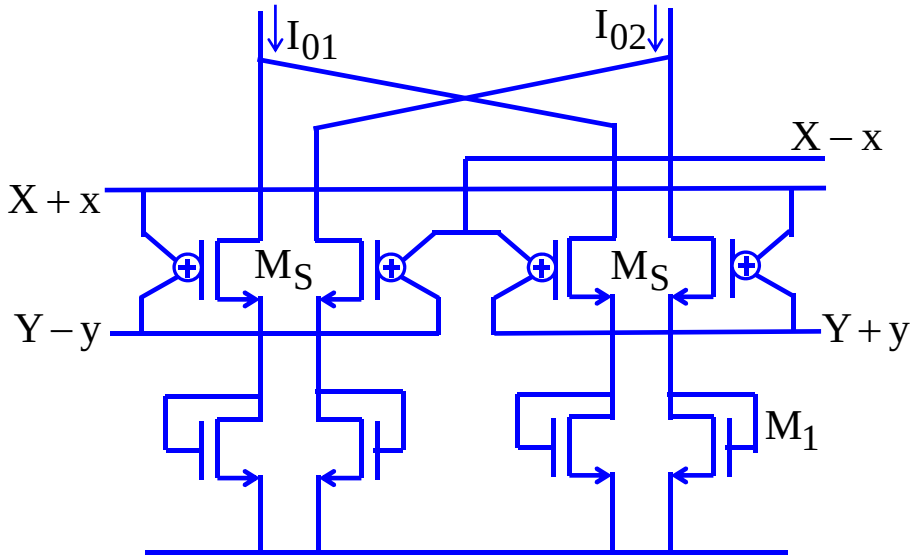
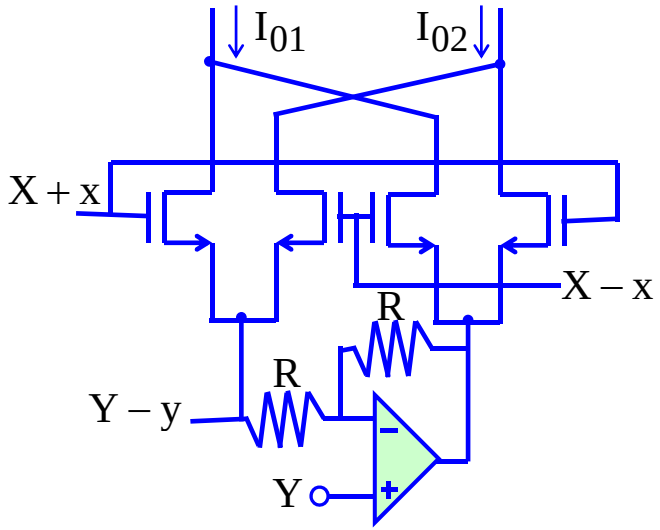
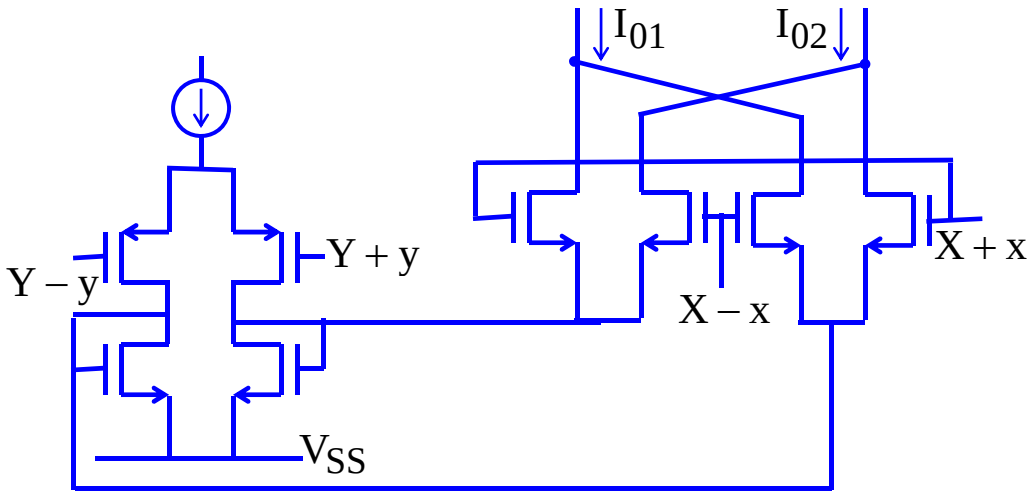


Fig.10 Multiplier using V_{gs}^2 with diode connection (Type IV)

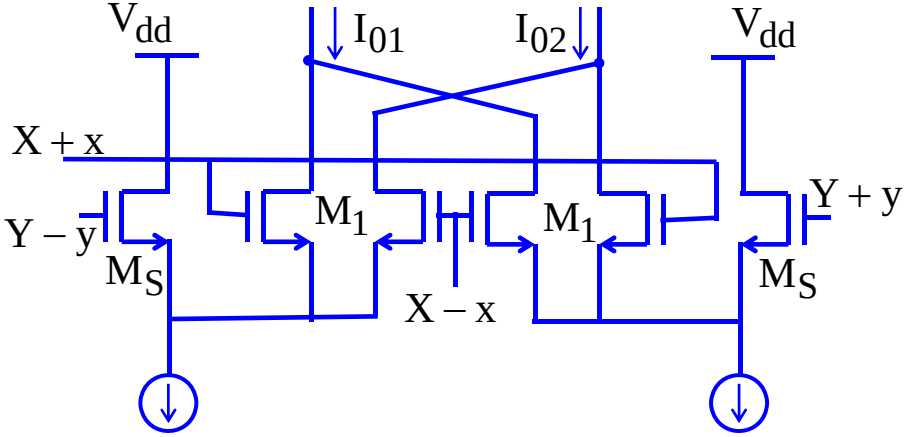
Alternative Signal Injection Implementations using V^2_{GS}



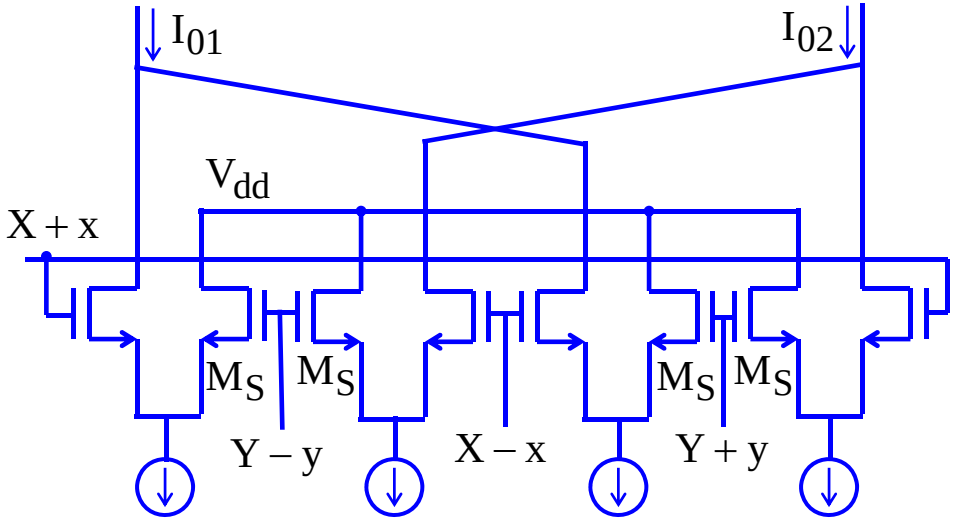
12(a) Using OP Amp



12(b) Using a linear differential amp



12(c) Using source followers



12(d) A separate follower for each cross-coupled transistor

Fig. 12 Source signal injection methods for multiplier using V^2_{gs} term (Type V)

Bulk-Driven Transistor Using V^2_{gs} (Type VI)

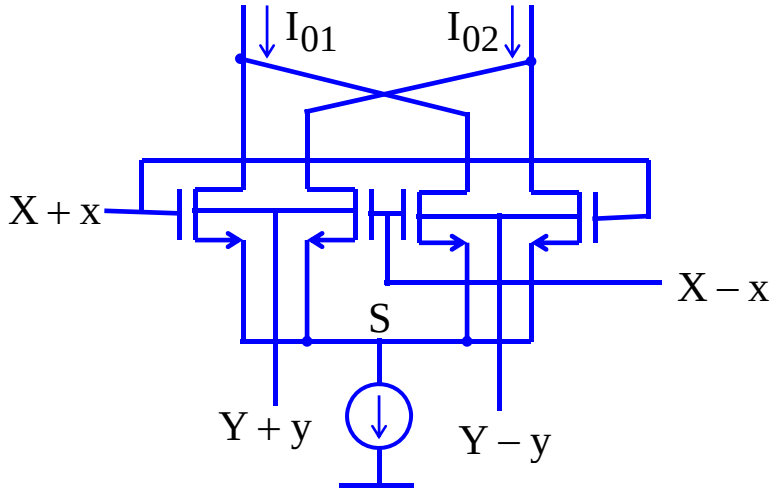


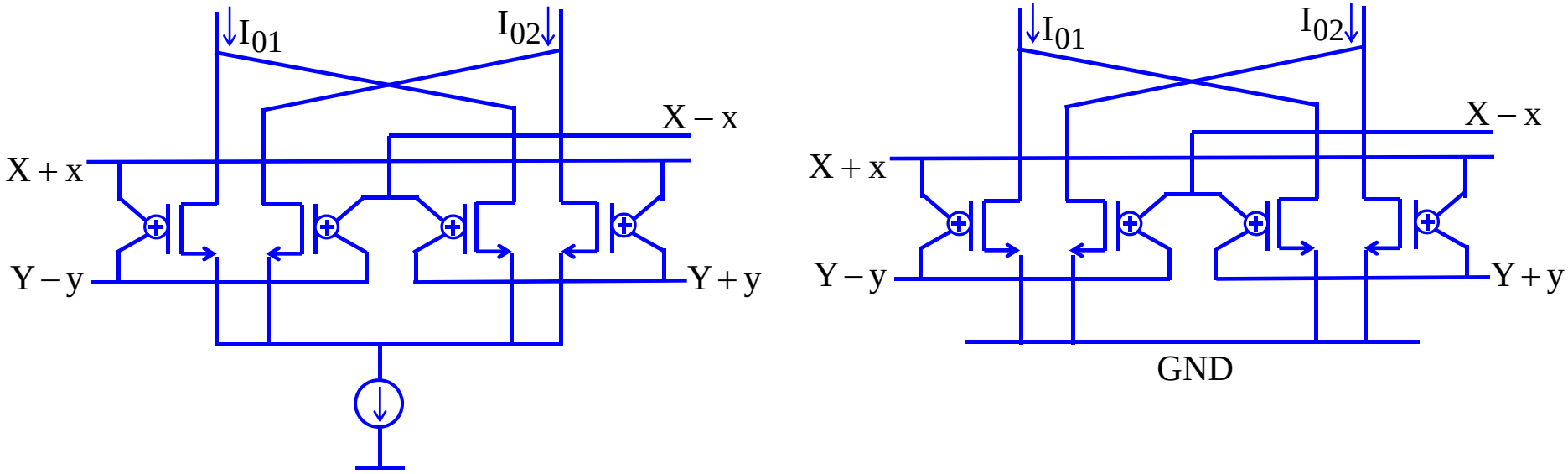
Fig. 13 Using substate signal injection (Type VI)

$$V_T = V_{T0} + \gamma\sqrt{2|\phi_F| - V_{bs}} - \sqrt{2|\phi_F|}$$

$$I_0 = I_{02} - I_{01} = \frac{4K\gamma}{2|\phi_F| - Y + s}\left[y\sqrt{2|\phi_F| - Y + s} + \left\{ \frac{y}{2\left(2|\phi_F| - Y + s\right)} \right\}^3 \right] x$$

$$I_0 \cong \frac{4K\gamma}{\sqrt{2|\phi_F| - Y + s}}\, xy \qquad \text{for } 2|\phi_F| - Y + s >> y$$

Voltage Adder (Type VII) using V^2_{gs}



14(a) with tail current **14(b) without the tail current**

Fig. 14 Multipliers using voltage adder (Type VII)

This implementation is based on the $(\,)^2$ cancellation scheme. Summers can be implemented with (i) resistors, (ii) capacitors, or (iii) active adders.

Floating Voltage Source (Type VII) Using V^2_{gs}

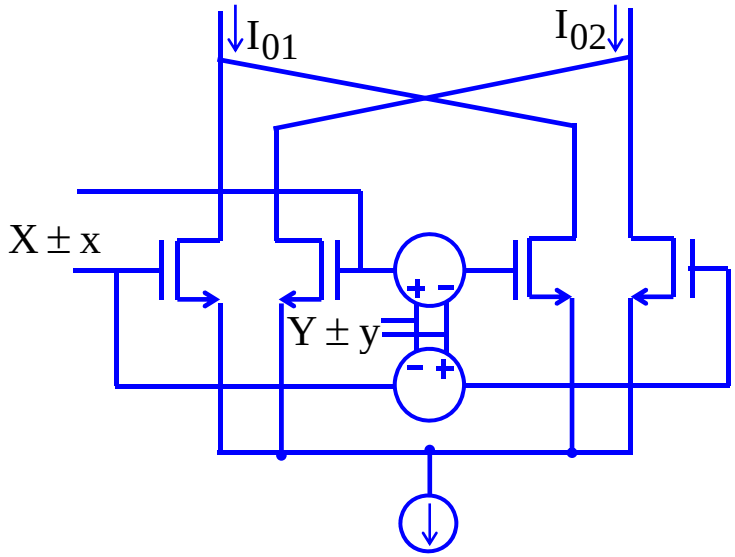


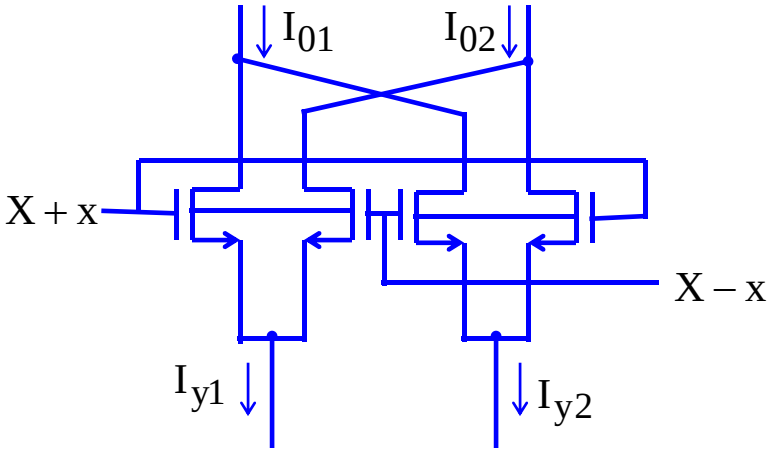
Fig. 15 Multiplier using floating voltage source (Type VII)

MOS Gilbert Cell (Type VIII)

Analysis:

One MOS differential pair yields $I_{0d} = I_{01} - I_{02} = 2\sqrt{KI_s}\,x\left(1 - \frac{Kx^2}{I_s}\right)^{\frac{1}{2}}$

In what follows x is a voltage signal and y(I_y) is a current signal



Current steering circuit

For the two differential pairs, we obtain :

$I_0 = I_{01} - I_{02} = 2\sqrt{K}x\left(\sqrt{I_{y1}} - \sqrt{I_{y2}}\right)$

Note that $\sqrt{I_{y1}} - \sqrt{I_{y2}}$ is generated by a third differential pair as shown next. Thus

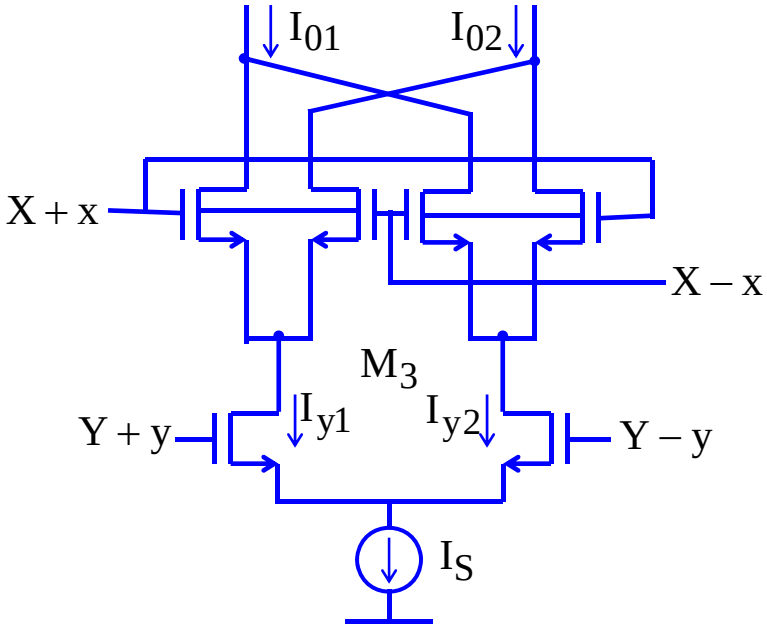
$$\sqrt{I_{y1}} - \sqrt{I_{y2}} = y\sqrt{2K_3}$$

Thus

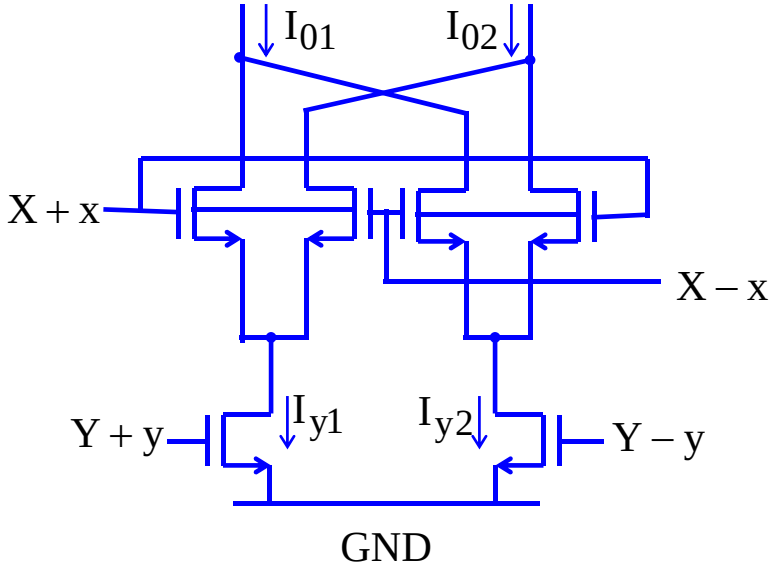
$$I_0 = I_{01} - I_{02} = 2xy\sqrt{2KK_3}$$

Here both x and y are voltage signals.

MOS Gilbert Multiplier Implementations



17(a) with tail current



17(b) without tail current

Fig. 17 MOS Gilbert multipliers (Type VIII)

- Improvement of this cell involve linearization of the differential pairs, folded architectures or active attenuators.
- This structure might not be suitable for low power supplies.

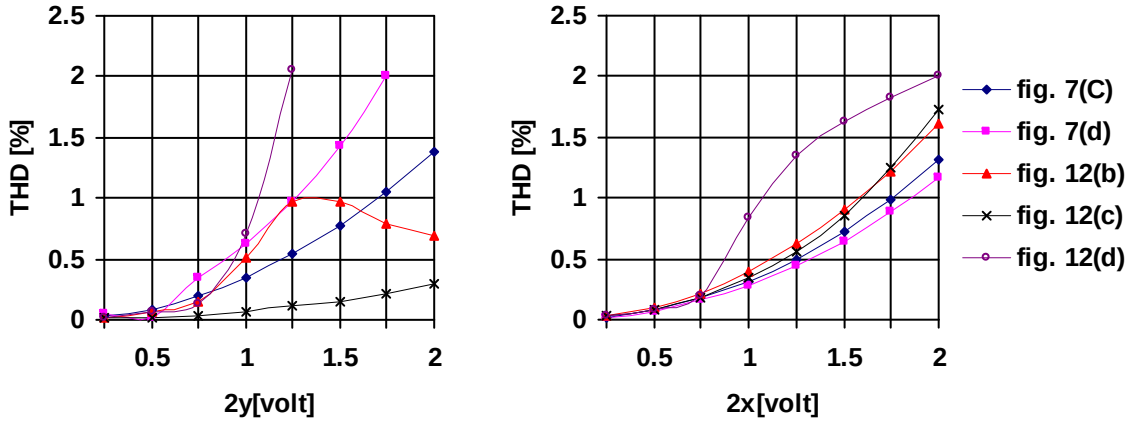
Comparisons

A specific comparison is application dependent. A limited qualitative and through simulation are discussed next.

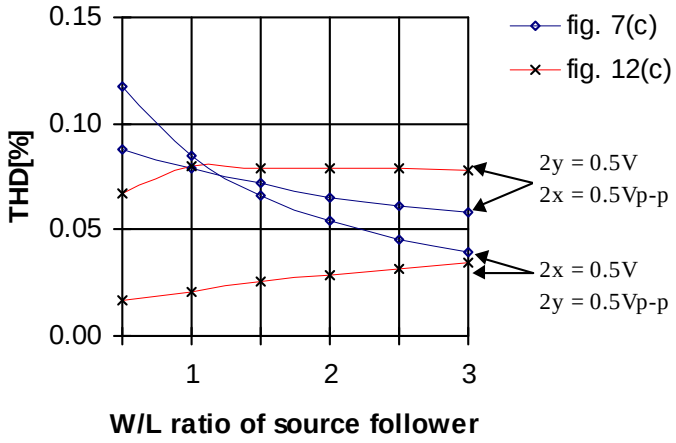
Table 2. Summary of general qualitative comparison of 15 multiplier topologies.

NO.	Type	Circuit Diagram Figure	Worse than	Remark
1	I	7(a), 7(b)	2	Require additional circuitry.
2	I	7(c),7(d)		
3	II,III,IV	8, 9, 10	2	Require additional circuitry. Poor linearity.
4	V	12(a)	5	Require OP Amp
5	V	12(b), (c), (d)		
6	VI	13	5	Poor linearity
7	VII	14, 15	5	Require additional circuitry.
8	VIII	17	2	High power supply voltage. Poor linearity.

THD Comparisons

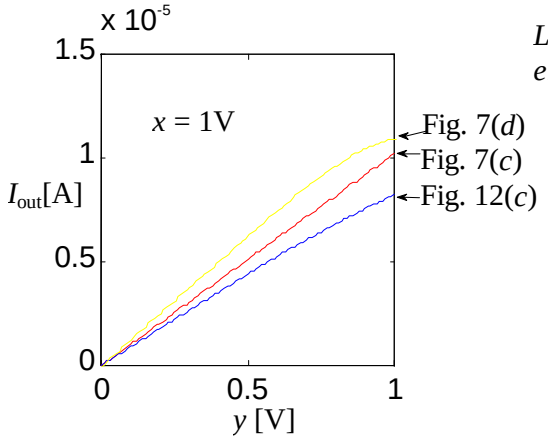


Simulated Total Harmonic Distortion(THD) for W/L= 10μm/10μm for all transistors.

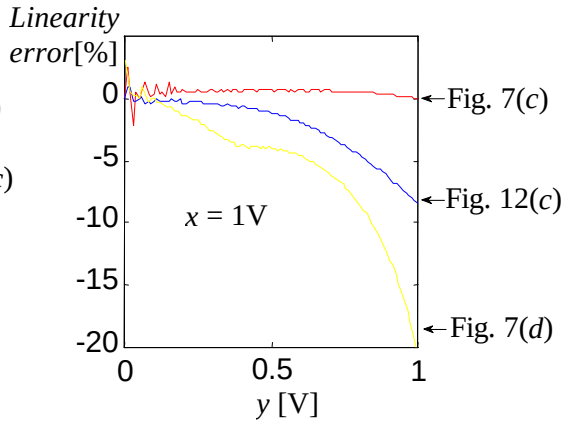


Effect of source follower's W/L ratio on THD

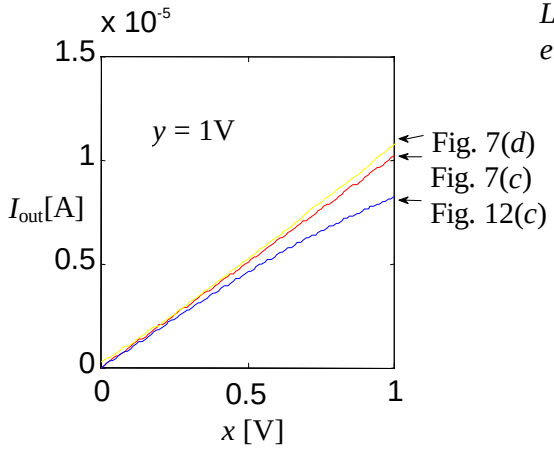
Linearity Comparison



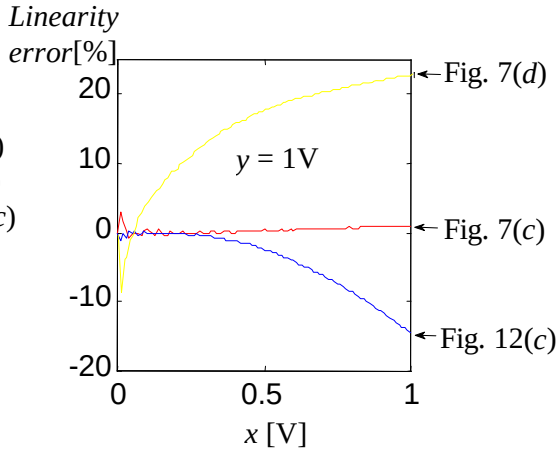
(a) Output current for fixed x



(b) Linearity error for fixed x



(a) Output current for fixed y



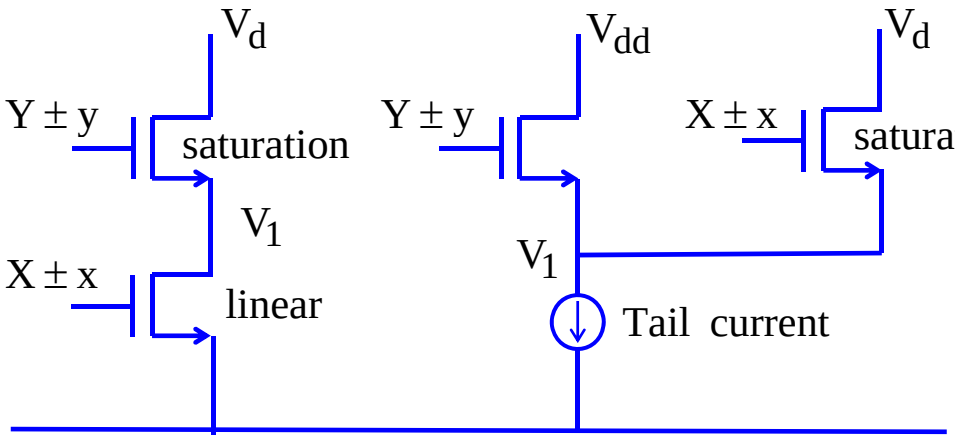
(b) Linearity error for fixed y

Measurement results for W/L_{m1} = 5µm/17µm and $W/L_{source\ follower}$ = 50µm/10µm.

$g_m = 10\mu A/V$, 360µW consumption, $x, y = \pm 2V$

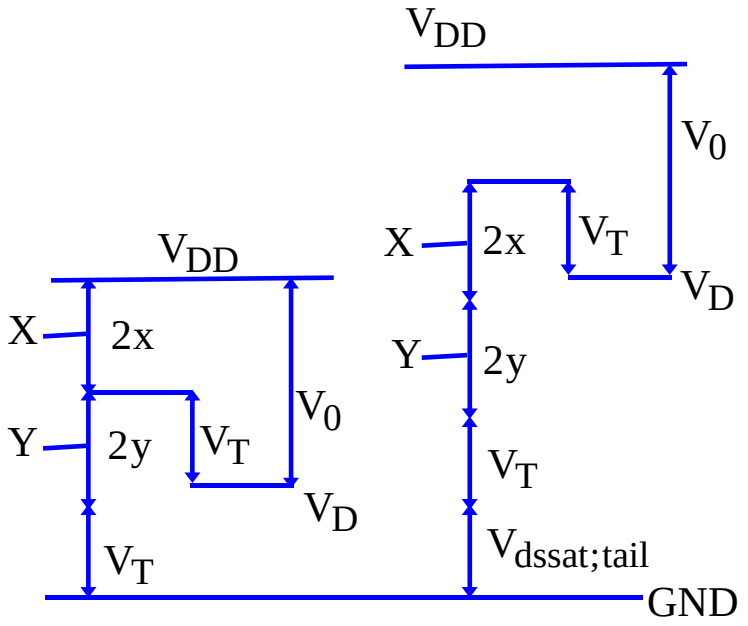
2µm CMOS technology.

Input Range and Minimum Power Supply



(a) Circuit Fig. 7(c) **(b) Circuit Fig. 12(c)**

Fig. 24 Bias conditions



(a) Circuit Fig. 7(c) **(b) Circuit Fig. 12(c)**

Fig. 25 Input range and power supply voltage

For Fig. 7(c):

$V_T < X \pm x$

$V_1 = Y \pm y - V_T < X \pm x - V_T$

$V_T < Y \pm y$

$Y \pm y - V_T < V_d$

For Fig. 12(c)

$V_{ds\ sat;\ tail} < V_1 = Y \pm y - V_T$

$V_1 + V_T = Y \pm y < X \pm x$

$X \pm x - V_T < V_D$

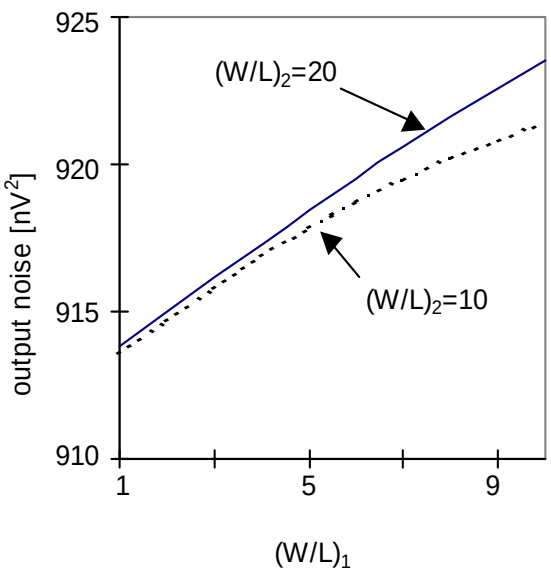
Table 3. Summary of a comparative multiplier study for equal size transistors.

Circuit	Max G_m [μA/V]	Power Consumption[mW]	Mismatch Sensitivity	Linearity x	Linearity y
Fig. 7(c)	20	238	Good	Good	Bad
Fig. 7(d)	4.6	270	Bad	Good	Bad
Fig. 12(b)	5	200	Worst	Bad	Bad
Fig. 12(c)	40	295	Best	Bad	Best
Fig. 12(d)	25	480	Good	Worst	Worst

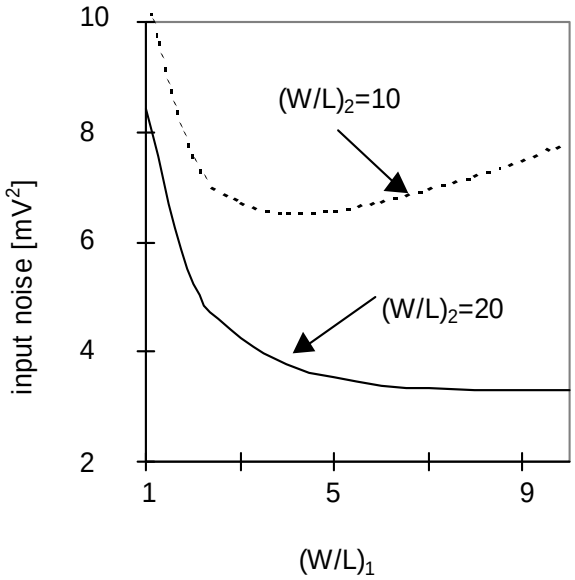
Table 4. Summary of comparison between circuit Fig. 7(c), Fig. 7(d), and Fig. 12(c)

Circuit	Linearity	Minimum Power Supply	Noise
Fig. 7(c)	Good	Good	Good
Fig. 7(d)	Bad	Bad	Bad
Fig. 12(c)	Good	Bad	Bad

Noise Consideration for Fig. 7(c).



(a)



(b)

Fig. 26 Noise dependency on $(W/L)_1$ for (X+Y)/2 = 4 volt and X-Y = 2 volt.

A Low Voltage Low Power CMOS Analog Multiplier

by Amir H. Miremadi*, Ahmad Ayatollah, Adib Abrishamifar (IUST)E-mail: amirh_miremadi@yahoo.com.a-miremadi@wtiau.ac.ir

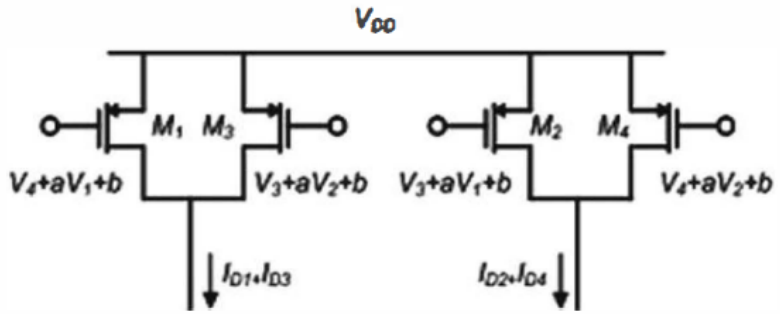


Fig. 1. Multiplier Core.

$$I_{OUT} = (I_{D1} + I_{D3}) - (I_{D2} + I_{D4}) = 2aK_1(V_1 - V_2)(V_3 - V_4) \quad (5)$$

From Fig. 1, The multiplier core requires the input signals V_4+aV_1+b, V_3+aV_1+b, V_3+aV_2+b and V_4+aV_2+b which are applied to the gate terminals where a and b are constants.

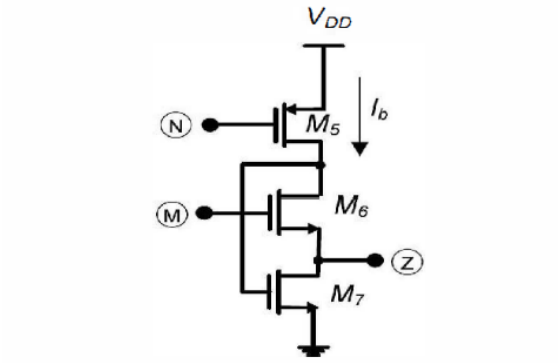


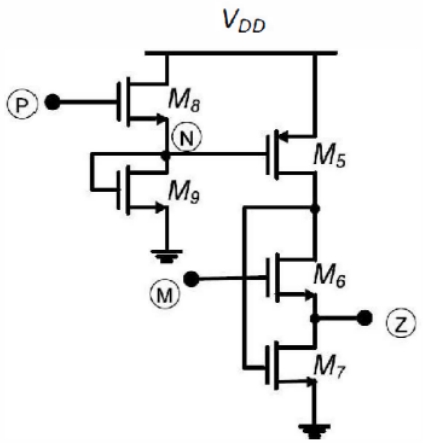
Fig. 2. Flipped Voltage follower cell.

$$V_Z = V_M + \sqrt{\frac{K_5}{4K_6}}V_P - V_B \quad (12)$$

The input signals V_1 and V_4 are applied to P and M nodes, respectively. Therefore, the output voltage V_{D1} can be rewritten as

$$V_Z = V_4 + aV_1 + b \quad (13)$$

Where $a = \sqrt{\frac{K_5}{4K_6}}$ & $b = -V_B$



The developed flipped voltage follower cell.

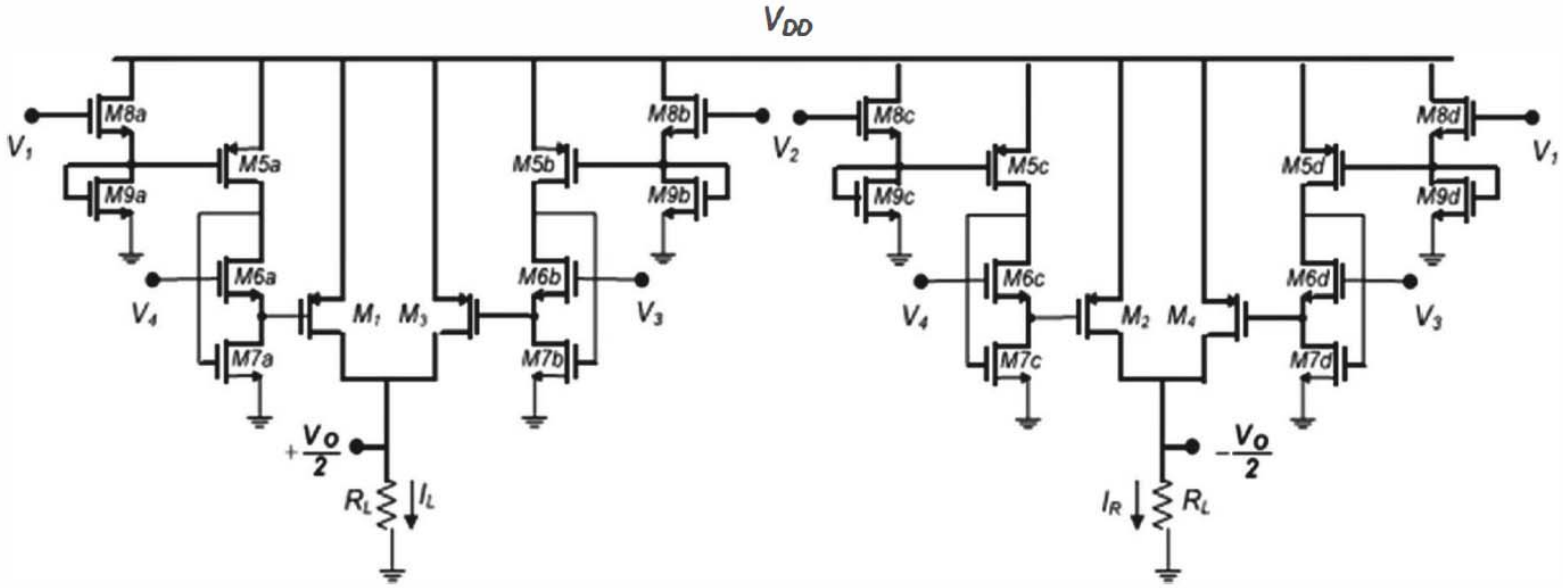
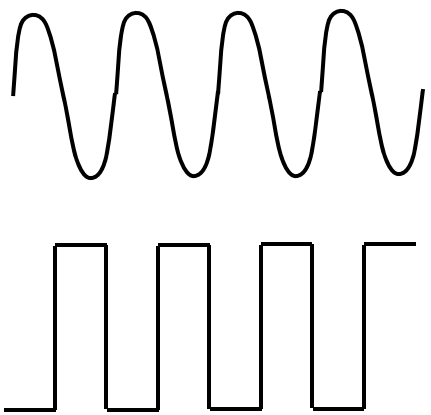


Fig. 4. The circuit diagram of the proposed analog multiplier.

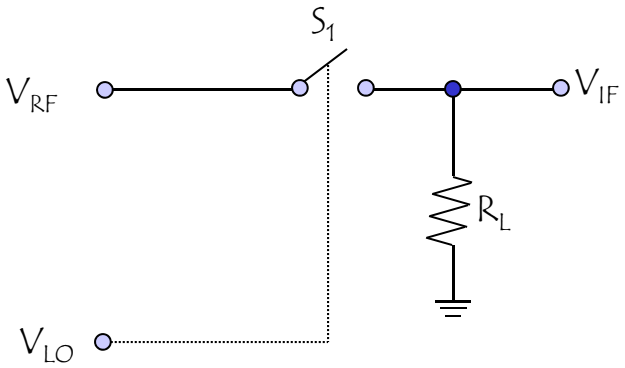
A low voltage low power CMOS analog multiplier has been presented. The proposed multiplier works with a single supply of 0.9V and low power consumption (58μW). It has linearity error less than 1.8% for linear range 400mVp-p.

THD is smaller than 0.88% under the maximum-scale input 400mVp-p at both inputs.

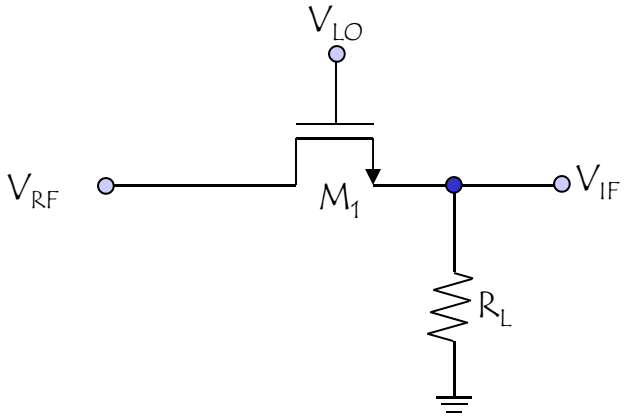
MIXERS



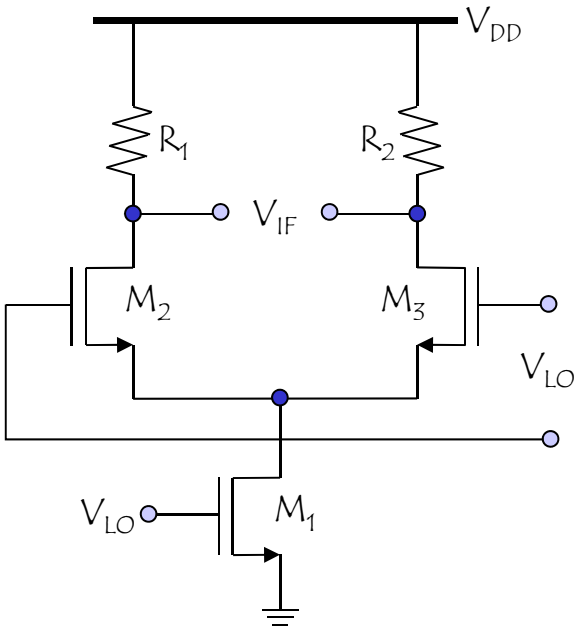
Simple switch
used as a mixer



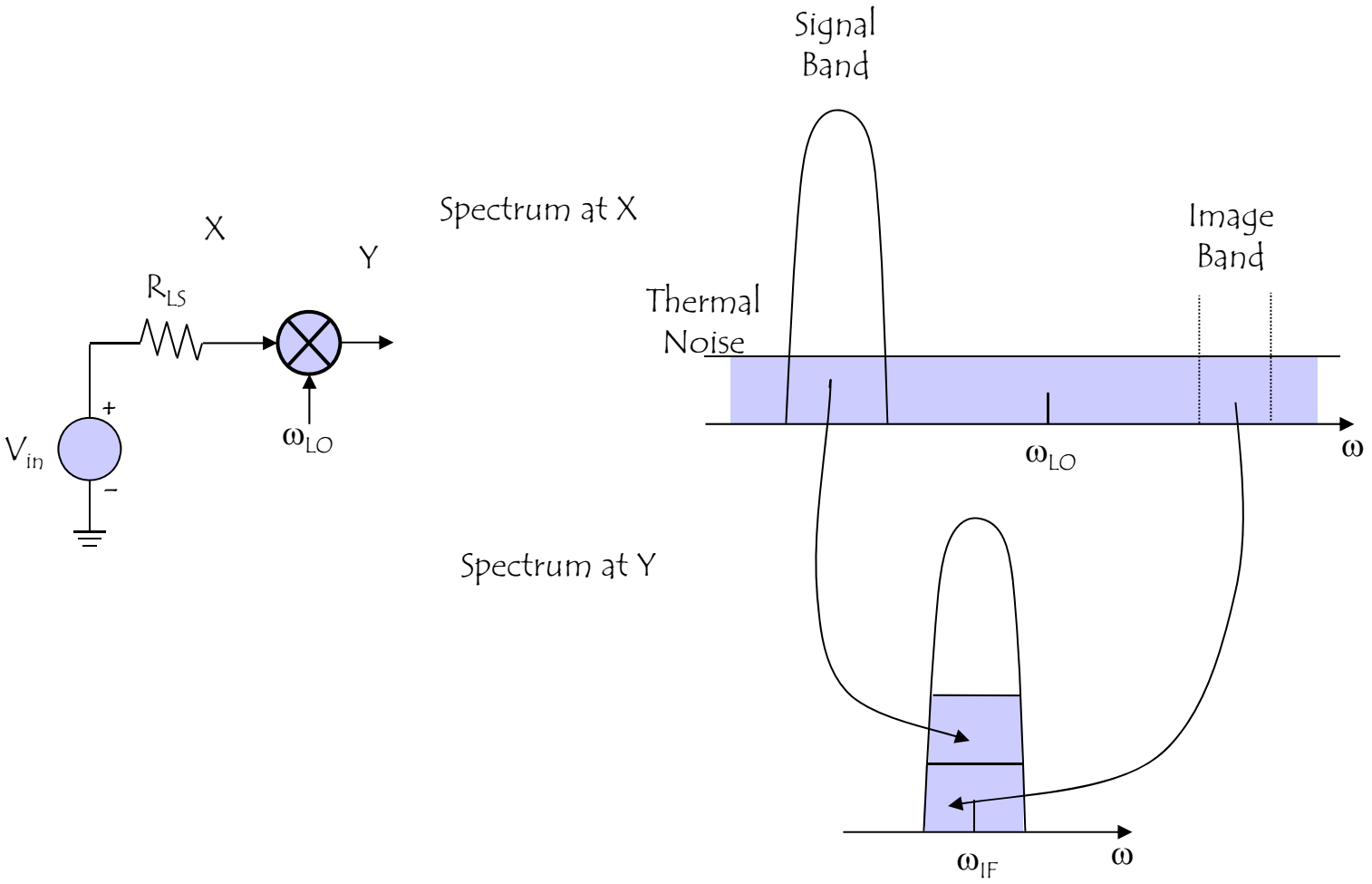
Implementation of switch
with an NMOS device



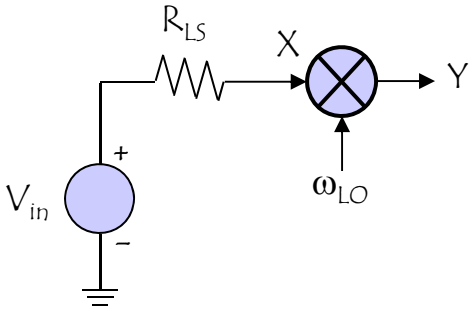
Active Mixer



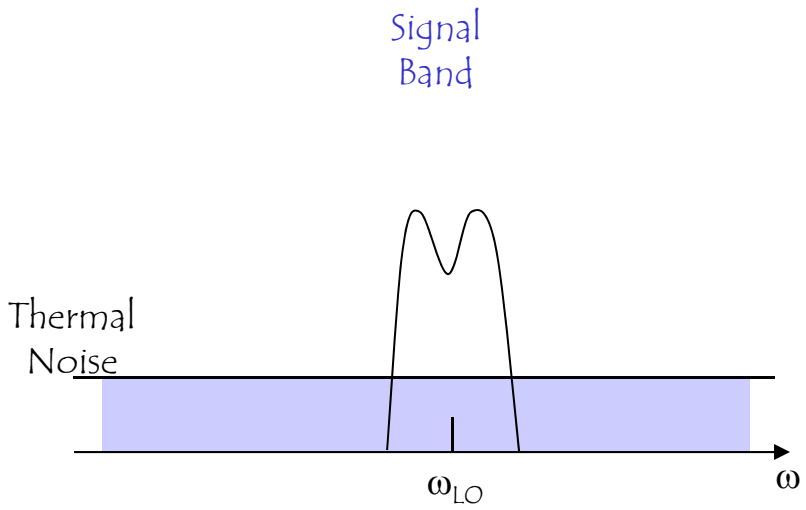
Folding RF and image noise into the IF band



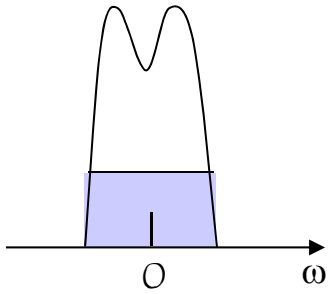
Downconversion of an AM Signal



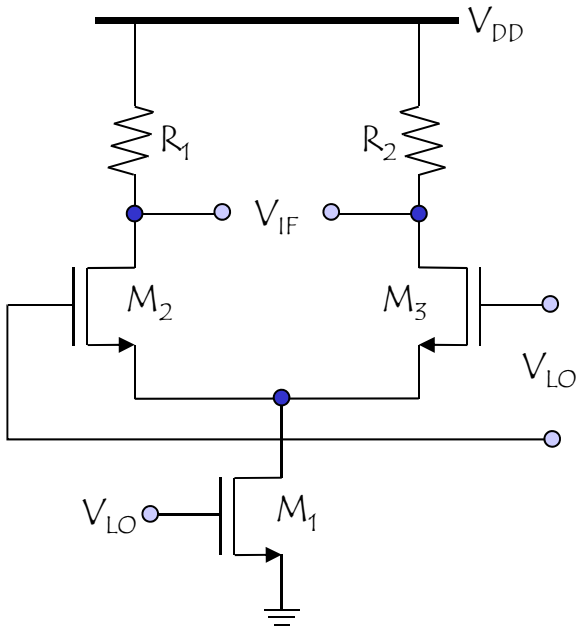
Spectrum at X



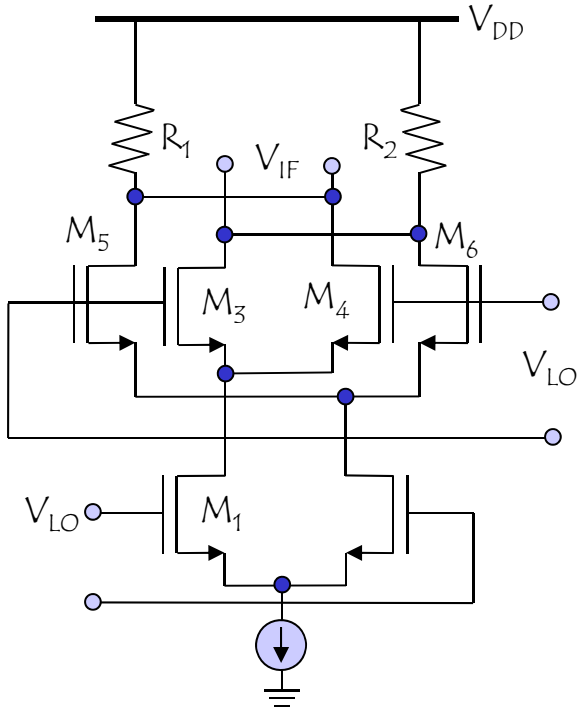
Spectrum at Y



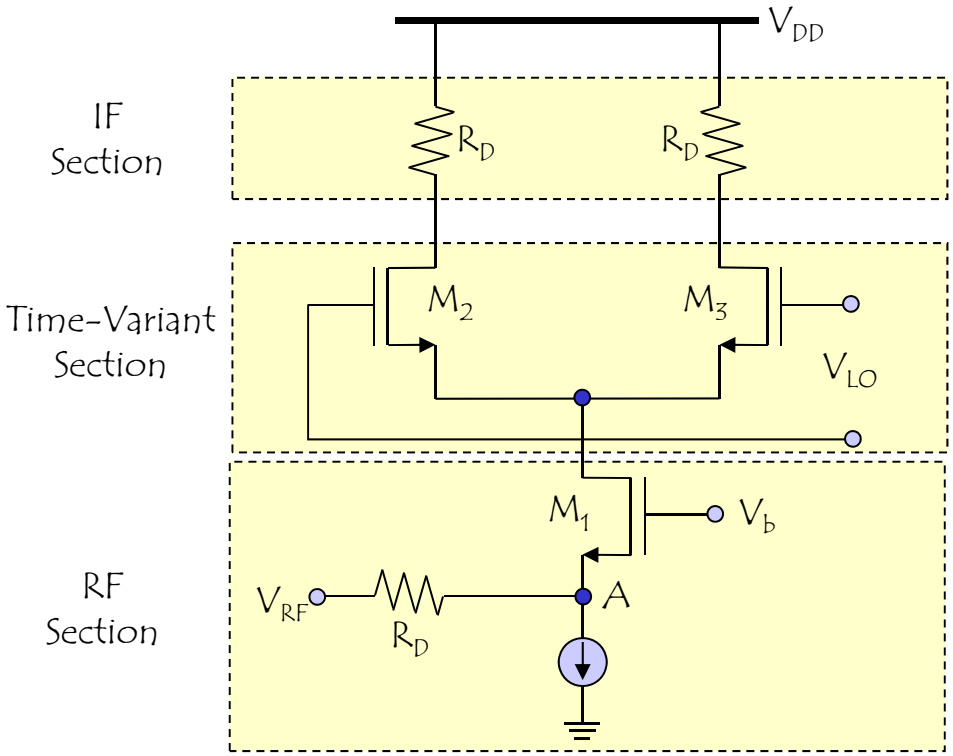
Single-balanced mixer



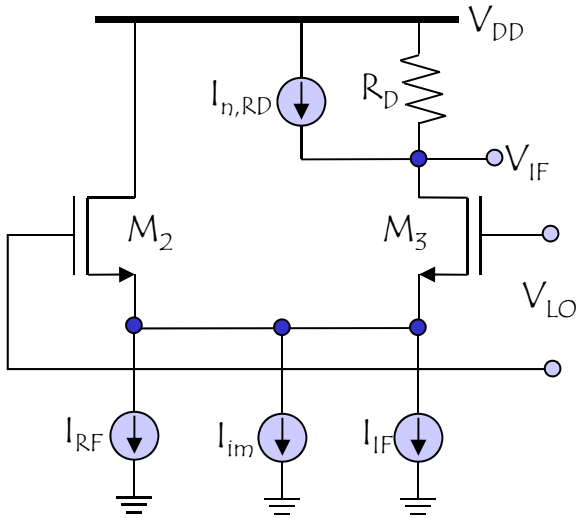
Double-balanced mixer



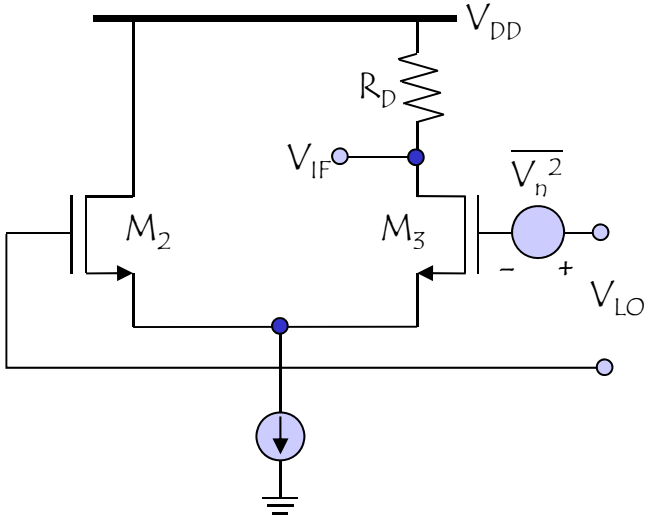
Sections of a mixer



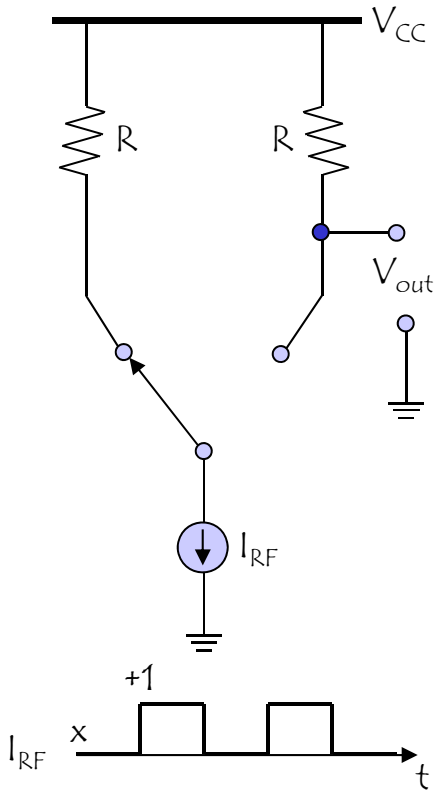
Modeling the noise in the RF section



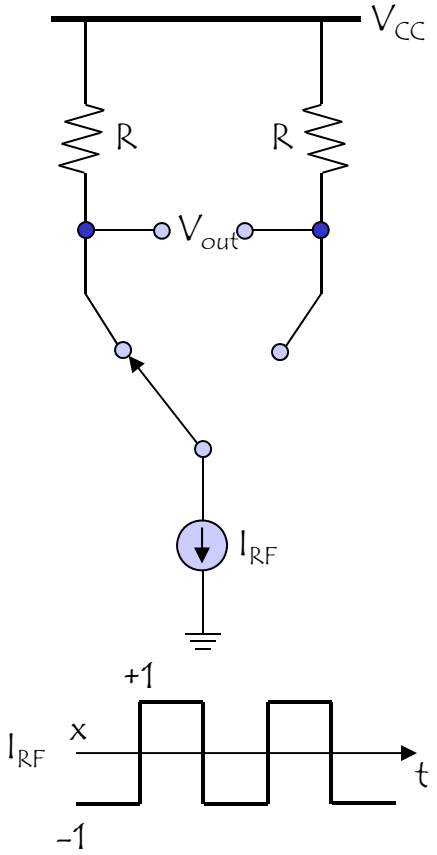
Modeling the noise in the time-variant section



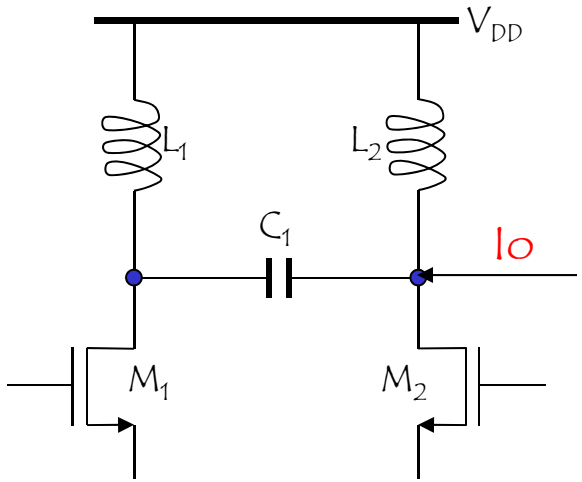
Simple mixer with single-ended output



Simple mixer with differential outputs



Conversion of differential currents to single-ended outputs



- Most mixers need to be single-ended because the IF SAW filters are single ended devices.

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