0.9-V Rail-to-Rail Operational Amplifiers with Adaptive Threshold Voltage Control

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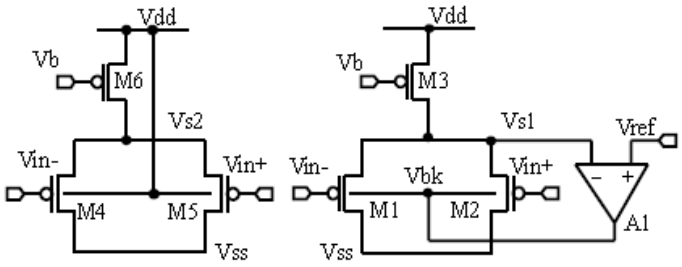
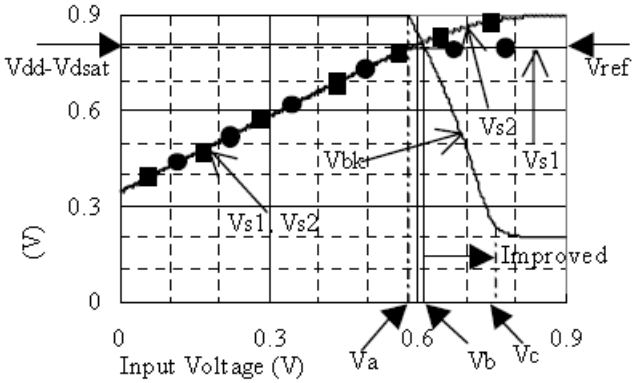


Fig. 1. (a) Typical input stage for op amps. (b) Input stage with adaptive threshold voltage control

$$V_{th} = V_{th0} + \gamma\left(\sqrt{|2\phi_f - V_{bs}|} - \sqrt{2\phi_f}\right) \quad (1)$$



g. 2. Vs1, Vs2 and Vbk vs input voltage in Fig. 1. (a), (b)

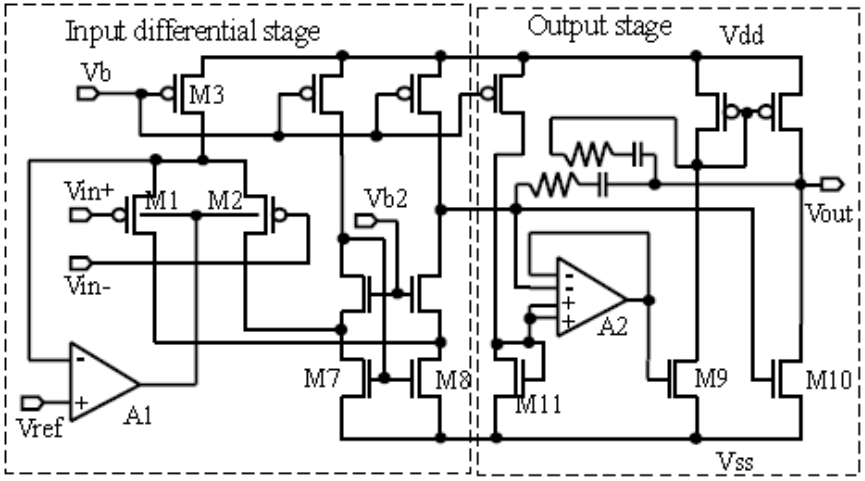


Fig. 3. Operational amplifier based on a single input pair

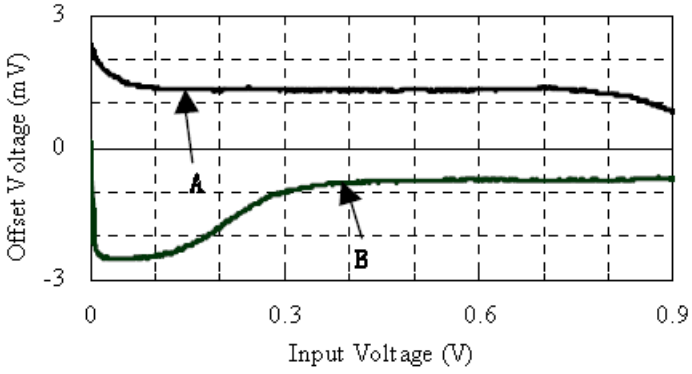


Fig. 4. Offset voltage vs input voltage for amplifier in Fig. 3 and amplifier based on complementary input pairs

TABLE I

Experimental Performance of amplifiers (Vsupply=0.9 V)

parameter	**Amplifier based on single input pair**	**Amplifier based on complemntary input pairs**
Active die area	0.044 mm^2	0.044 mm^2
Idd	92 µA	96 µA
DC Gain	94 dB	96 dB
GBW	2.3 MHz	2.2 MHz
THD **0.8 Vpp, 1 KHz**	81.4 dB	56.8 dB
Input offset 3σ	4.7 mV	4.5 mV
Output source current	**340** µA	**370** µA
Output sink current	**720** µA	**560** µA

Referrences

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