**ECEN 607 (ESS)**
**Spring 2008**

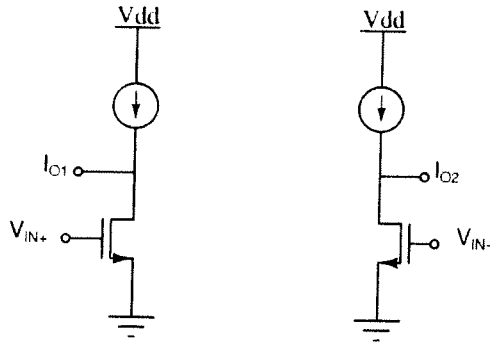
**Name** _____

# EXAM #1

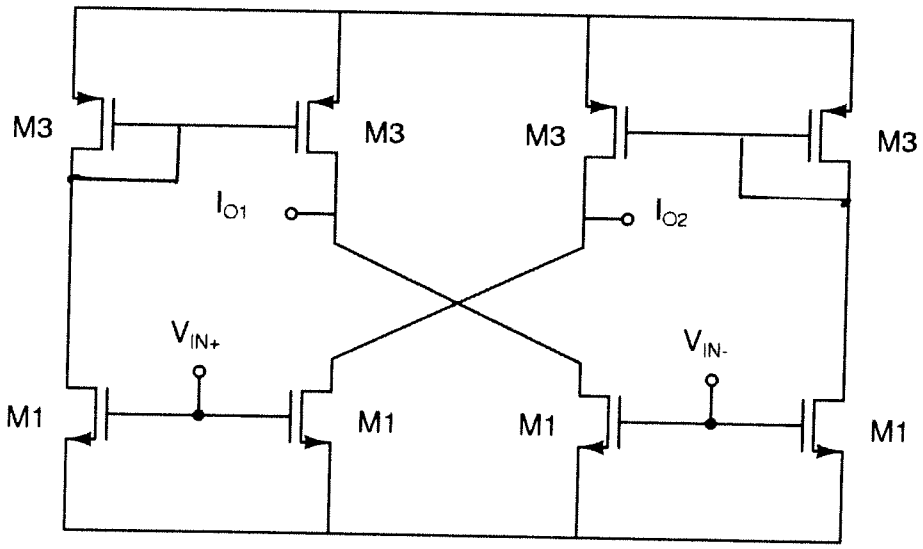
This is a closed book and notes exam. One information page is allowed for the exam. This exam is worth 17% of your total grade.

| Prob. | Maximum | Yours |
|---|---|---|
| 1 | 4 | |
| 2 | 4 | |
| 3 | 5 | |
| 4 | 4 | |
| Extra Credit | 1 | |
| Total | 18 | |

Prob. 1. Write the differential and common-mode transconductance gain for the pseudo-differential circuits shown below (ignore the effect of $g_{ds}$ and parasitic components). Discuss their differences i.e., effective transconductance, differential gains.




(a)

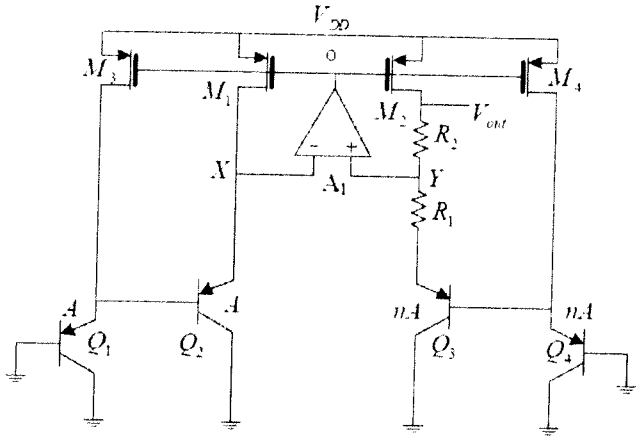



(b)

Prob.2

1) Assume Ideal Opamp. The current through M1 and M2 are equal. Obtain the expression for the bandgap reference output voltage $V_{out}$.

2) With a finite Opamp gain, in order to achieve the error voltage (Vx-Vy) smaller than Ve, what should be the minimum Opamp Gain $A_1$? (You can use square law equations)



Prob 3. In the circuit shown below, relative sizes and bias currents are given as follows.

Size(M1) = 100*W/L

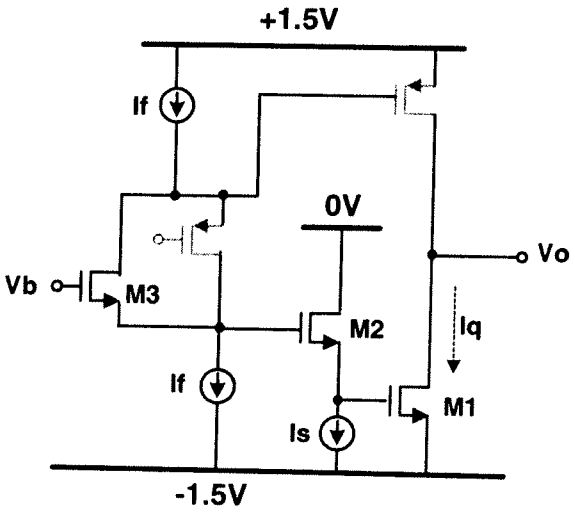
Size(M2) = W/(4L)

Size(M3) = W/(4L)

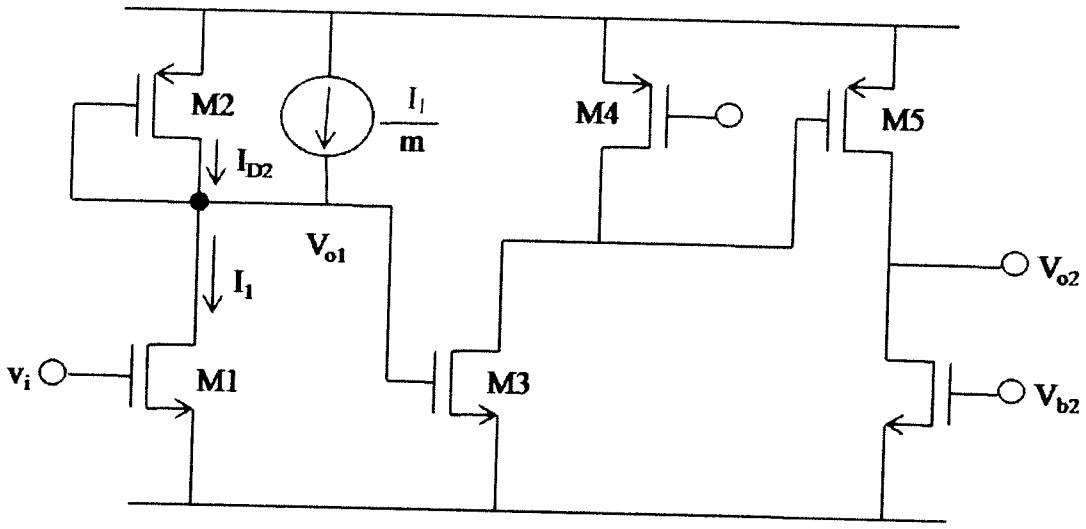
Iq = 8*Is = 4*If

a) Design a bias voltage generation circuit based on diode connected transistors that are scaled copies of M1, M2 and M3 to generate the bias voltage Vb. Assume small threshold voltage and ignore headroom constraints. Express the relative dimensions of the transistors in your design in terms of W/L or W/(4L). Specify the value of current source used in your bias generator.

b) It turns out that under quiescent condition, Vds(M3) = 2*Vgs(M3). Now, modify you bias generator to match the Vgs as well as the Vds of bias generation copy of M3 and M3.



Prob. 4. Obtain the low frequency small signal voltage gain expression (for $V_{01}$ and $V_{02}$) of the following circuit. Assume ideal current sources and transistors operating in saturation.



EXTRA CREDIT. Obtain $V_o$ as a function of $V_D$, $R_1$, $R_2$, kT, n and q.