ELEN 607 (ESS) **Due: January 31, 2017**
SPRING '17

HOMEWORK ASSIGMENT #1

Prob. 1. Use any size technology and generate the equivalent plot (see around page 21 Lect. #1) of various parameters versus the inversion level. i.e. f_T vs i_f, power consumption, (W/L) vs i_f. Also add a trace for Vdsat vs i_f in the same plot.

Prob. 2. Extract the parameters of transistors PMOS and NMOS for the ACM model, that is one equation all regions. See Ref. 6 on Lect. #1. Consider the 65nm and 130 nm CMOS technology and $i_f = 9$. Discuss how the parameters are extracted. Provide a table summarizing results of the extracted parameters. Discuss the results.

Prob. 3. a) Design, using conventional quadratic saturation transistor equation, a simple two stage transconductance amplifier for the following specs and using 0.13um technology

VDD = 1.2 V
VSS = 0 V
Gain > 50 dB
CMRR > 55 dB
GBW greater or equal to 4 MHz
PM > 60º
CL = 25 pF
Power < 500 µW
Feel free to use your design obtained in ECEN 704

b) Repeat the design but using one equation, all region transistor model, reduce the power consumption as much as possible while meeting the above specs. Summarize your results in a Table form. Indicate the " if " for each transistor in the amplifier.

Prob. 4 Design using one equation all region equation, an Ahuja current buffer amplifier that meets the specs in Prob. 3, except the SR but consumes at least 50% less than the one designed in 704 and can handle a 10X larger load capacitance.

Provide a table summarizing the results of Probs. 2 and 3, include in the comparison also active area, PSR at DC and 100 KHz, 1% settling time, CMRR (0), SR-, and SR+. Comment these results and trade-offs.

Reading Assignment.-

A.I.A. Cunha, Schneider, M.C.; Galup-Montoro C.; "An MOS transistor model for analog circuit design". *IEEE J. of Solid-State Circuits*, Vol. 33, Issue 10, pp. 1510-1518, Oct. 1998.

S. Yan and E. Sánchez-Sinencio, "Low Voltage Analog Circuit Design Techniques: A Tutorial", *IEICE Trans. Fundamentals*, Vol. E82-A, No 2, pp 179-196, February 2000

L.L.Lewyn et all, " Analog Circuit Design in Nano scale CMOS Technologies". *Proc. of the IEEE*, Vol. 97, No. 10, pp. 1687-1714, October 2009

http://www.designers-guide.org/Forum/Attachments/Gm_BY_ID_Methodology.pdf

"No thief, however skillful, can rob one of knowledge, and that is why knowledge is the best and safest treasure to acquire."
— L. Frank Baum, The Lost Princess of Oz

Download Steps:

1. Go to: http://www.eas.asu.edu/~ptm/
2. Select: Latest Models
3. Download the required model from 130nm down to 22nm
4. Save the Model card to: filename.m
5. Open the file and change:
   For NMOS: `.model nmos nmos level = 54` → `.model ptmn65 bsim4 type=n`
   For PMOS: `.model pmos pmos level = 54` → `.model ptmp65 bsim4 type=p`

In order to simulate using the predictive technology models in cadence the following steps should be done:

1. Copy the modified model files to the following directory: ("~/cadence/models/spectre").
2. Generate Library (In Cadence Library Manager) and don't attach any technology at this time.
3. Generate Cell with the schematic view.
4. Insert either an nmos4 and/or pmos4 transistors from ***analogLib*** library.
5. In the NMOS/PMOS object property menu set the ***Model Name*** parameter to ***ptmn65/ptmp65***
6. During the simulation phase if the simulator did not find the model files, you can attach the model files by:
   a. In Analog Design Environment→ Setup → Model Libraries..
   b. Attach the model files "don't forget to press the ADD button"

Important notes:

1. You can use these model files with cadence version v5.0.33 or higher. On EESUN machines: source /usr/local/bin/setup.ic5033
2. The models are written to be used with the ***simulator spectre*** not spectreS