ELEN 607 (ESS) **Due: February 16, 2017**
Spring '17

HOMEWORK # 3

Prob. 1 A resistive inverting amplifier with an Op Amp with a finite and SR=3.0 V/μs is connected to yield a voltage gain of -2 V/V.
Consider two cases for the input

i) A step of magnitude V_m
ii) A sinusoidal $v(t) = V_p \sin \omega t$

Determine:

a) Assuming a maximum value of Vm = 174mV yielding a bandwidth limited amplifier. Obtain the corresponding GB.
b) The corresponding peak magnitude Vp so the output is bandwidth limited when the maximum frequency for a sinusoidal input is fmax = 1.19MHz
c) The 3dB cutoff frequency of the inverting amplifier for a GB=4.2MHz

Prob. 2. Use your Op Amp design of HW 1 prob3b), but use a voltage follower and the compensation capacitor to eliminate the zero in the RHP. Added this result with the comparison Table of Previous (HW. 1) prob. 3. Determine for this design and Ahuja amplifier, THD, the third-order interception point, SFDR, 1-dB compression plot and IIP3 plot.

Provide, in addition, complete table(s) summarizing your result and previous in Prob. 3 (HW. 1), Show the step responses. Besides the specifications given above include CMR range, maximum output voltages for 1% THD, min and maximum inversion levels (i_F) for each design. ***Discuss your results from Tables and simulation graphs***. Tell me what you learned.

Prob. 3 a) Using current mirrors (CMs) design a negative capacitor multiplier of 15.625X, pick the value of C to be multiplied. Explore using one CM or several odd number of CMs. What are the trade-offs.? Summarize your results for the valid region for -C
b) Using current mirrors or Op Amp design a positive capacitor multiplier of 16X. Provide the frequency range of validity for the multiplier.

"An investment in Knowledge always pay the best interest"
- **Benjamin Franklin**