HW4

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ECEN 607

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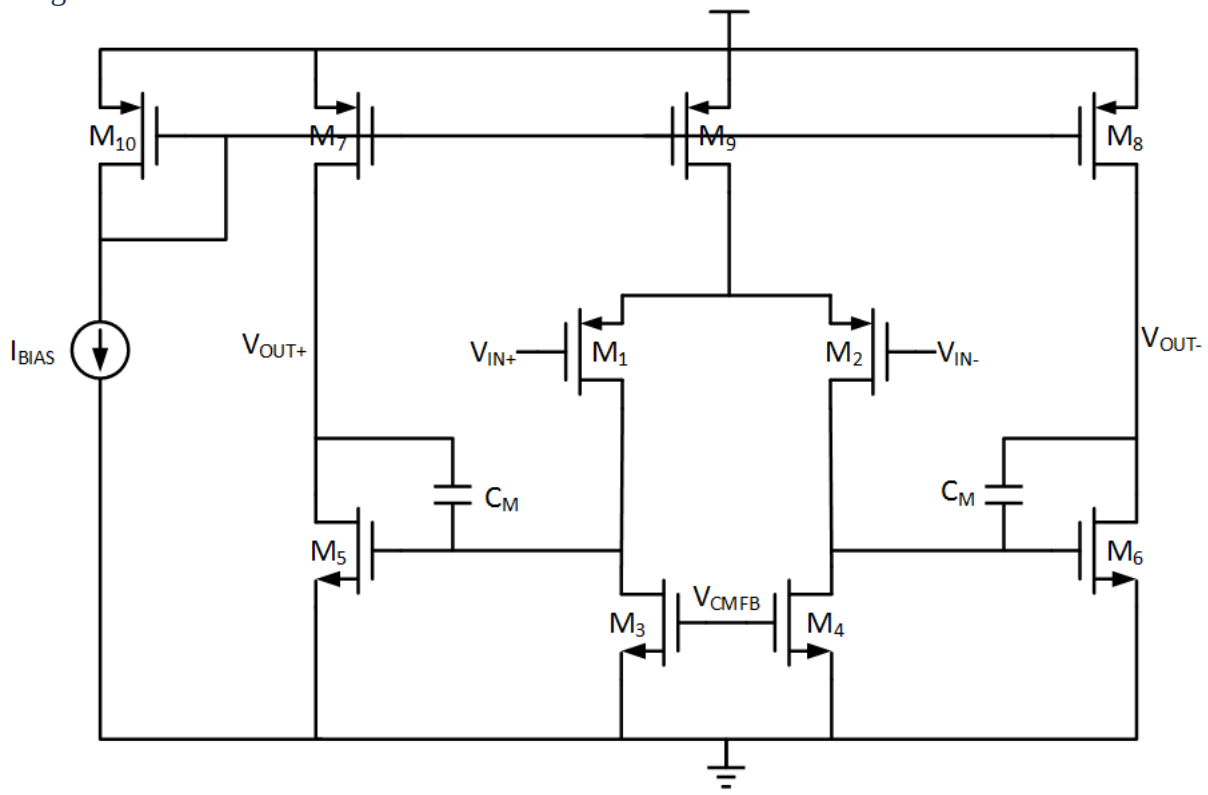
Problem 1

Part A

Design



The schematic above shows the fully differential section of the amplifier. This section will be designed first. First, the length of all transistors is set to 650nm to meet the gain specification. Next, we set the value of C_M to 12.5pF which is half of the load capacitance. From the GBW spec, we can find the required transconductance for $M_{1,2}$:

$$g_{m1,2} = 5MHz \cdot 2\pi \cdot 12.5pF = 400\mu A/V$$

We set an inversion level of i_f=10 for both of these transistors to ensure power consumption is kept as low as possible. We can therefore calculate the desired W/L and current:

$$I_{1,2} = \frac{1+\sqrt{1+10}}{2} \cdot 0.026V \cdot \frac{400\mu A}{V} \cdot 1.164 = 25\mu A$$

$$\frac{W}{L}_{1,2} = \frac{\frac{400\mu A}{V}}{\frac{85\mu A}{V^2} \cdot 0.026V} \cdot \frac{1}{\sqrt{1+10}-1} = 78.12 \rightarrow \left(\frac{W}{L}\right)_{1,2} = \frac{50\mu m}{650nm}$$

Next, we find the require value for $g_{m6,7}$ to produce the required phase margin. The phase margin should not be too high to ensure the settling time specification is met.

$$65° = 90° - \tan^{-1}\left(\frac{25pF}{12.5pF} \cdot \frac{g_{m1,2}}{g_{m6,7}}\right) - \tan^{-1}\left(\frac{g_{m1,2}}{g_{m6,7}}\right) \rightarrow \frac{g_{m1,2}}{g_{m6,7}} = 0.149 \rightarrow g_{m6,7} = 2.7mA/V$$

Again, we can find the required current and aspect ratio for an inversion level of i_f=1:

$$I_{5,6} = \frac{1+\sqrt{1+1}}{2} \cdot 0.026V \cdot \frac{2.7mA}{V} \cdot 1.194 = 100\mu A$$

$$\frac{W}{L}_{5,6} = \frac{\frac{2.7mA}{V}}{\frac{777\mu A}{V^2} \cdot 0.026V} \cdot \frac{1}{\sqrt{1+1}-1} = 322.66 \rightarrow \left(\frac{W}{L}\right)_{5,6} = \frac{210\mu m}{650nm}$$

We set I_{BIAS} to 5uA and the size of M_{10} to:

$$\left(\frac{W}{L}\right)_{10} = \frac{5\mu m}{1\mu m}$$

Therefore, the size of $M_{7,8}$ is:

$$\left(\frac{W}{L}\right)_{7,8} = 20 \cdot \frac{5\mu m}{1\mu m} = \frac{100\mu m}{1\mu m}$$

And the size of M_9 is:

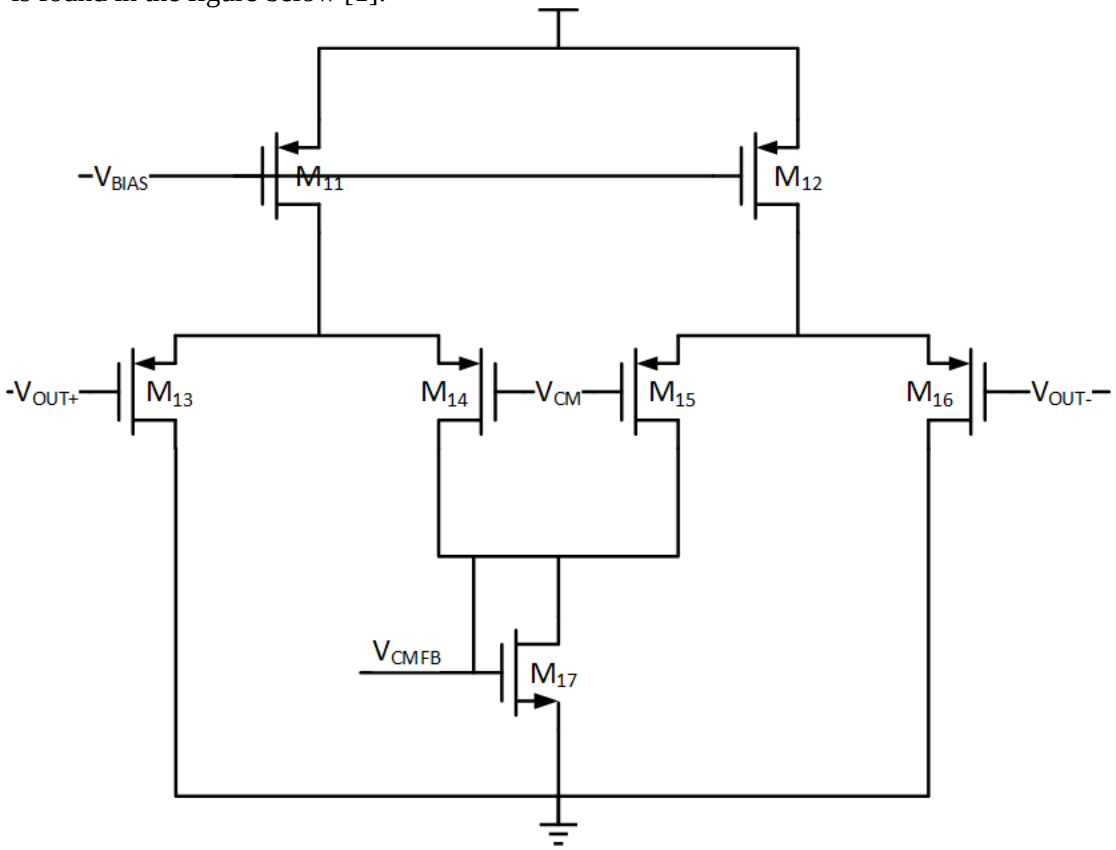
$$\left(\frac{W}{L}\right)_{9} = 10 \cdot \frac{5\mu m}{1\mu m} = \frac{50\mu m}{1\mu m}$$

We set the size of $M_{3,4}$ to:

$$\left(\frac{W}{L}\right)_{3,4} = 4 \cdot \frac{5\mu m}{1\mu m} = \frac{20\mu m}{1\mu m}$$

The size of these transistors is not critical since the gate voltage will be adjusted by the CMFB, but this size should provide reasonable V_{DSAT} and will be matched in the CM detector.

Next, we design two separate CM feedback loops using two different topologies. The first topology is found in the figure below [1]:



We set the bias current through $M_{11,12}$ to 30uA. This means that M_{17} will be made the same size as $M_{3,4}$ to provide the correct V_{CMFB}. Therefore, we find the following sizes:

$$\left(\frac{W}{L}\right)_{11,12} = 6 \cdot \frac{5\mu m}{1\mu m} = \frac{30\mu m}{1\mu m}$$

Next, we set the size of M_{17} equal to the size of $M_{3,4}$:

$$\left(\frac{W}{L}\right)_{17} = \frac{20\mu m}{1\mu m}$$

Lastly, we must size $M_{13\text{-}16}$ to make the GBW of the CMFB equal to the GBW of the differential section. This GBW is approximately 5MHz. We can find that the gain of CMFB loop is:

$$A_{V,CM} = \frac{g_{m9}}{2} \cdot r_{o1,CM} \cdot g_{m6} r_{o2} \cdot \frac{g_{m13}}{\frac{g_{m17}}{2}} = \frac{g_{m9} r_{o1,CM} g_{m6} r_{o2} g_{m13}}{g_{m17}}$$

Ideally, $g_{m9}=g_{m13}$, so the gain becomes:

$$A_{V,CM} = g_{m13} r_{o1,CM} g_{m6} r_{o2}$$

The CMFB loop has a dominant pole also at the output of the second stage. This dominant pole occurs at:

$$\omega_p = \frac{1}{r_{o1,CM} C_M \cdot g_{m6} r_{os}}$$

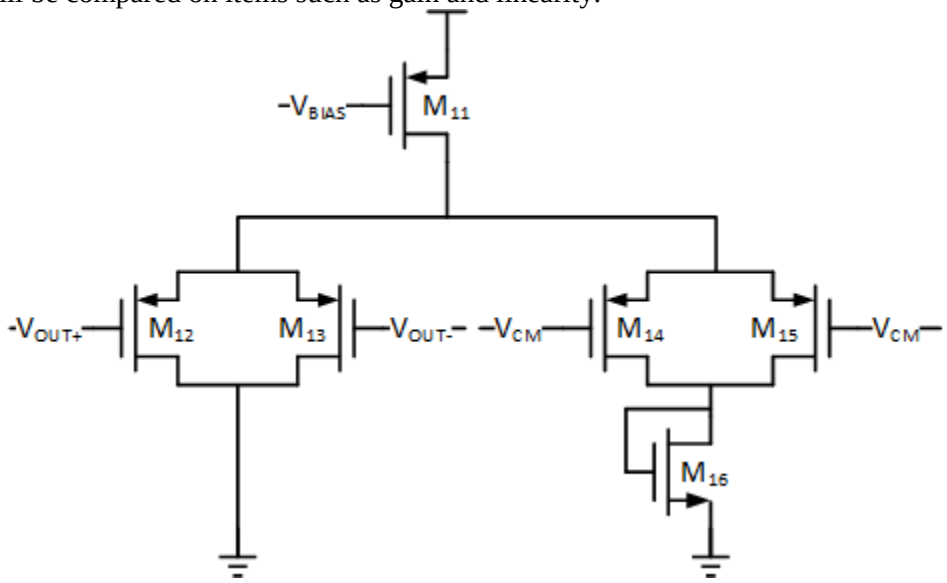
Therefore, the GBW of the CMFB loop is:

$$GBW_{CM} = g_{m13} r_{o1,CM} g_{m6} r_{o2} \cdot \frac{1}{r_{o1,CM} C_M \cdot g_{m6} r_{os}} = \frac{g_{m13}}{C_M}$$

Therefore, in order to make the GBW of the CMFB equal to the GBW of the differential part of the amplifier, g_{m13} should be made equal to g_{m1}. Therefore, the size of g_{m13} is made the same as the size of g_{m1}:

$$\left(\frac{W}{L}\right)_{13-16} = \frac{50\mu m}{650nm}$$

Another CMFB topology was designed and can be found in the figure below [1]. The two CMFB topologies will be compared on items such as gain and linearity.



Since M_{11} is providing current for both branches of the CMFB amplifier, we set its size to provide 60uA of current:

$$\left(\frac{W}{L}\right)_{11} = 12 \cdot \frac{5\mu m}{1\mu m} = \frac{60\mu m}{1\mu m}$$

We size M_{16} to the same size as $M_{3,4}$ to provide the proper CMFB voltage signal:

$$\left(\frac{W}{L}\right)_{16} = \frac{20\mu m}{1\mu m}$$

Using the same procedure as above, the GBW of the CMFB loop can be found and the expression for this CMFB amplifier is the same as the expression found previously:

$$GBW_{CM} = \frac{g_{m12}}{C_M}$$

Therefore, we once again size M_{12} to provide the same transconductance as M_1:

$$\left(\frac{W}{L}\right)_{12-15} = \frac{50\mu m}{650nm}$$

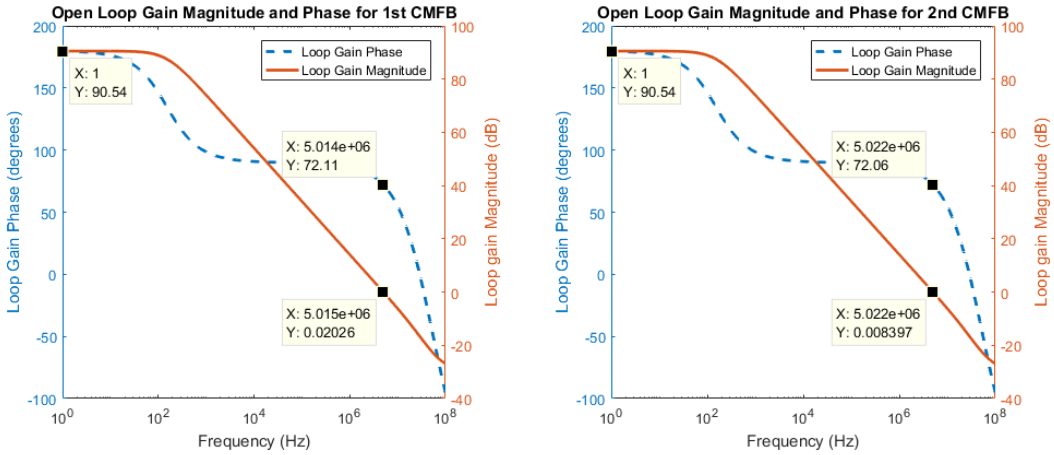
Simulation

It was found that the above transistor lengths did not provide the required gain with a load resistance of 47kΩ. As a result, some modifications had to be made to the transistor sizes. For the most part, the modifications involved increasing the length of various transistors to attempt to boost the gain. The aspect ratio of these transistors was kept approximately the same to provide the same transconductance with a higher output resistance. Any resized transistors were in the differential core of the amplifier. The final transistor sizes can be found in the table below:

Transistor	Calculated Size	Final Size
M_1	$\frac{50\mu m}{650nm}$	$\frac{200\mu m}{2\mu m}$
M_2	$\frac{50\mu m}{650nm}$	$\frac{200\mu m}{2\mu m}$
M_3	$\frac{20\mu m}{1\mu m}$	$\frac{10\mu m}{1\mu m}$
M_4	$\frac{20\mu m}{1\mu m}$	$\frac{10\mu m}{1\mu m}$
M_5	$\frac{210\mu m}{650nm}$	$\frac{370\mu m}{1\mu m}$
M_6	$\frac{210\mu m}{650nm}$	$\frac{370\mu m}{1\mu m}$
M_7	$\frac{100\mu m}{1\mu m}$	$\frac{600\mu m}{2\mu m}$
M_8	$\frac{100\mu m}{1\mu m}$	$\frac{600\mu m}{2\mu m}$
M_9	$\frac{50\mu m}{1\mu m}$	$\frac{100\mu m}{1\mu m}$
M_{10}	$\frac{5\mu m}{1\mu m}$	$\frac{10\mu m}{1\mu m}$

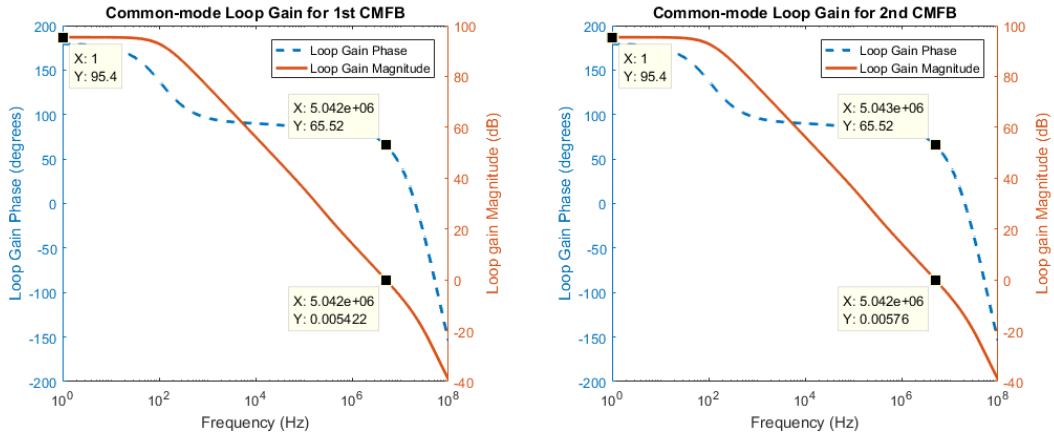
The aspect ratio of $M_{1,2}$ was increased slightly to increase the transconductance of the first stage. In addition to this, the length of these transistors was increased. Since the second stage has a resistive load, it is imperative that the first stage provide a large gain. Therefore, $M_{3,4}$ was split into two self-cascoded transistors to help increase the gain without affecting the output swing of the first stage. Lastly, the length of all current sources was increased to increase the gain of the second stage. Additionally, the amount of current through the second stage was increased to increase the transconductance of this stage and to provide better gain with the resistive load. After these modifications, all specs were met but the power dissipation had to increase.

First, the differential AC performance of the amplifier was measured for both CMFBs:



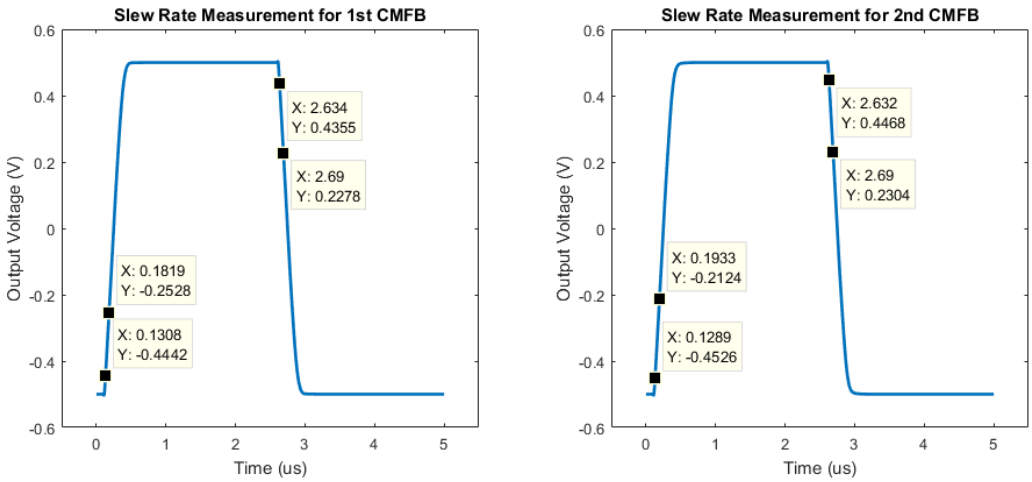
Both CMFBs have a DC gain of 90.54dB. The first CMFB has a phase margin of 72.11 degrees with a GBW of 5.015MHz while the second has a phase margin of 72.06dB and a GBW of 5.022MHz. Therefore, the differential performance of both amplifiers is much the same and the DC gain, GBW, and PM all meet the required specifications.

Next, the common-mode AC performance of both amplifiers was measured:



The DC gain of both CMFB loops is 95.4 dB. In addition to this, the GBW of both loops was 5.042MHz which is very close to the GBW of the differential section. This was an important goal during the design to ensure the bandwidth of the common-mode and differential-mode sections was not over-designed. The phase margin of both loops is 65.52 degrees which indicates that the common-mode loop of the amplifier is very stable.

Next, a large differential input step was used to measure the slew rate performance of both amplifiers:



The slew rates can be calculated for the 1st CMFB as follows:

$$SR_+ = \frac{-0.2528V + 0.4442V}{0.1819\mu s - 0.1308\mu s} = 3.75V/\mu s$$

$$SR_- = \frac{0.4355V - 0.2278V}{2.69\mu s - 2.634\mu s} = 3.71V/\mu s$$

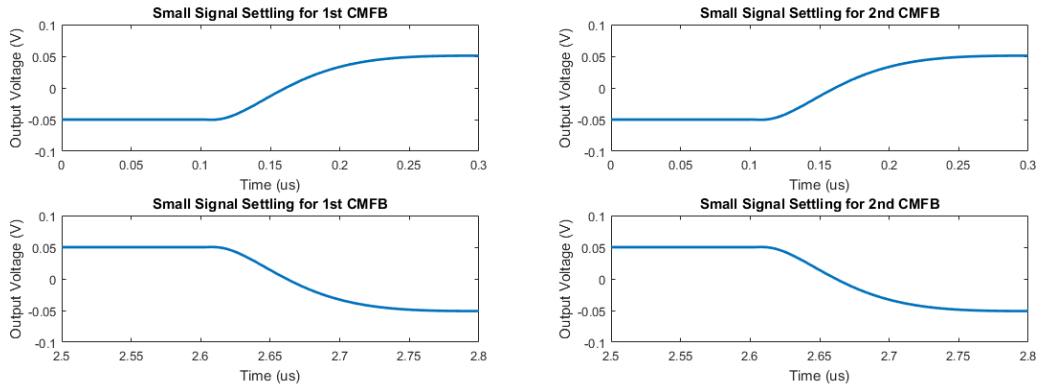
The slew rates for the 2nd CMFB can be calculated as follows:

$$SR_+ = \frac{-0.2124V + 0.4526V}{0.1933\mu s - 0.1289\mu s} = 3.73V/\mu s$$

$$SR_- = \frac{0.4468V - 0.2304V}{2.69\mu s - 2.632\mu s} = 3.73V/\mu s$$

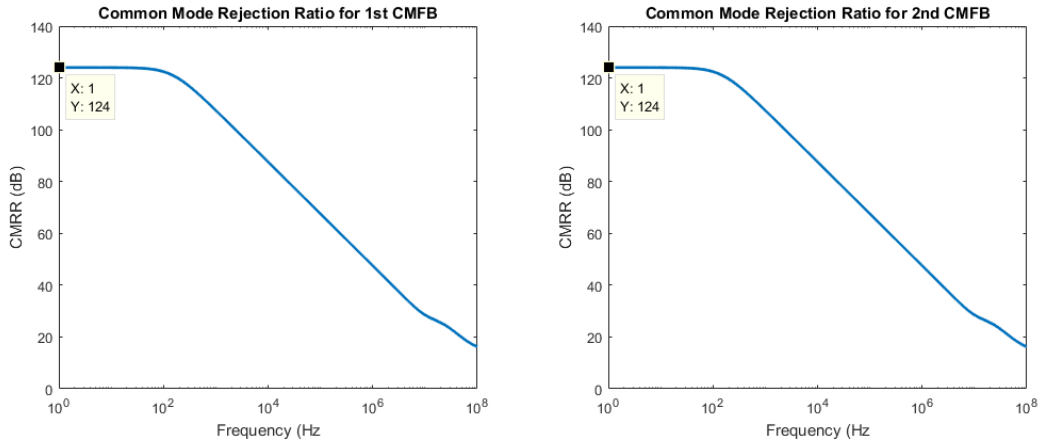
The slew rates for both amplifiers meet the specification of 2V/us.

Next, the differential-mode settling performance of the amplifiers was measured:



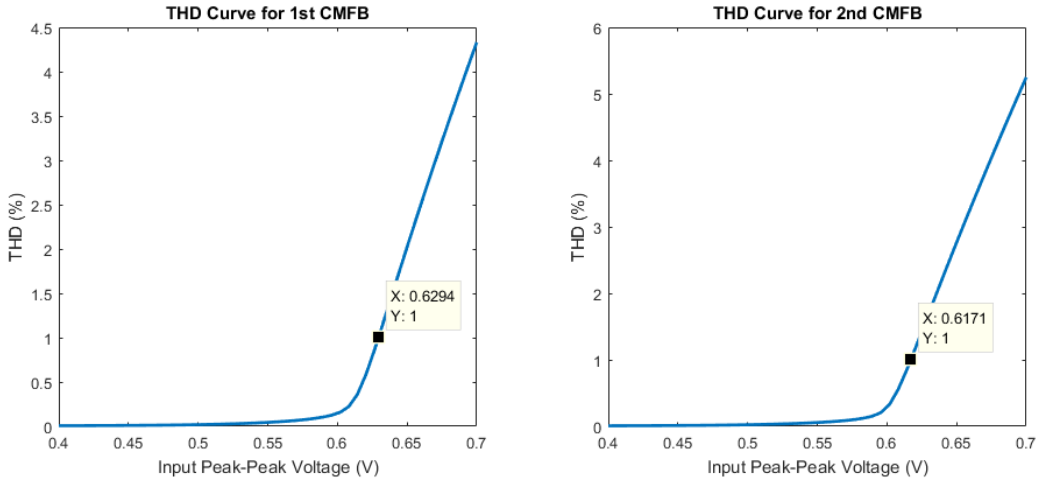
The first CMFB has a positive settling time of 152.2ns and a negative settling time of 152.3ns. The second CMFB has a positive settling time of 152.9ns and a negative settling time of 153ns. These times are for 1% settling. Therefore, the rising and falling settling times for both amplifiers met the specification of 160ns.

The CMRR of both amplifier was also measured:



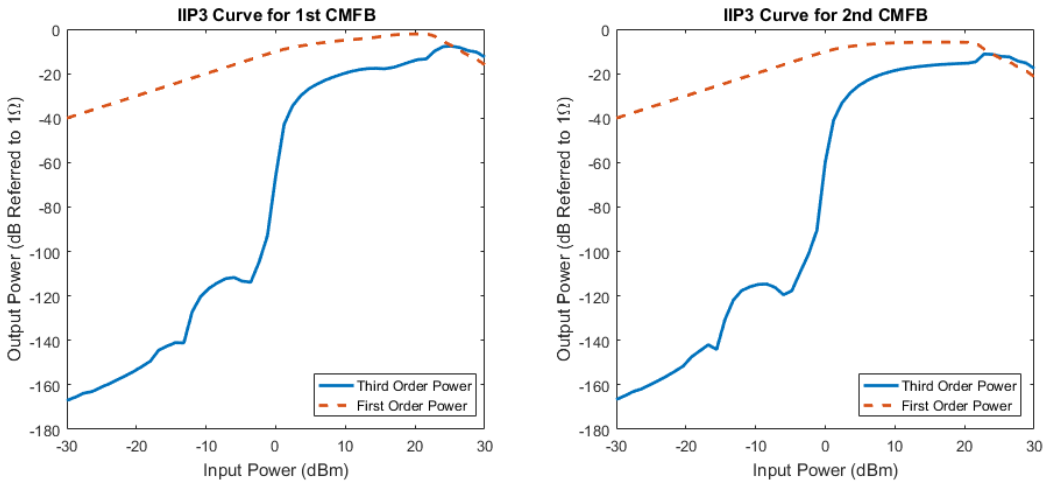
The CMRR of both amplifiers is the same at 124dB. This CMRR is well above the specification of 85dB.

The results above indicate that the two CMFB amplifiers provide very similar performance in CMRR. One major performance difference between them, however, is their effect on the linearity of the amplifier. From [1], we expect the amplifier with the 1st CMFB to be more linear than the second one. We can confirm this by measuring the THD over a range of input values:



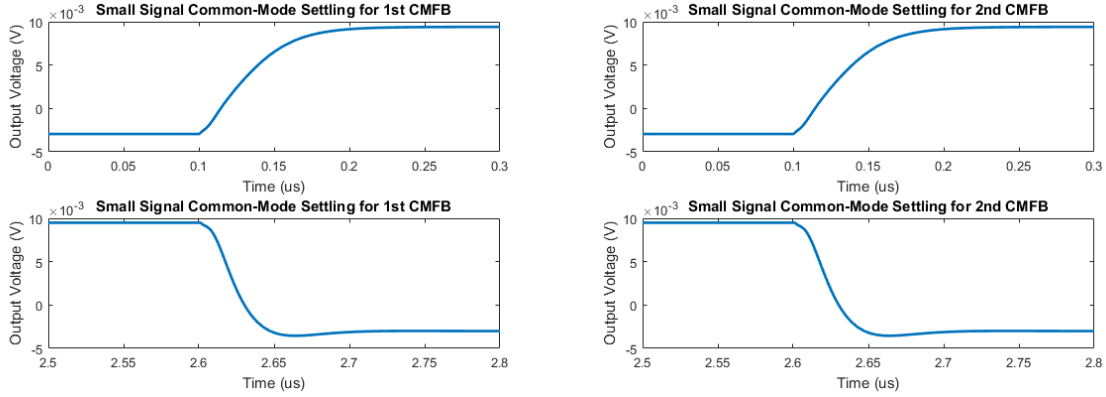
From the plots above, we can see that the maximum input peak-peak voltage for a 1% THD at 10kHz for the first CMFB is 0.6294V while for the second it is 0.6171V. Therefore, the first CMFB is slightly more linear than the second one. This agrees with the results discussed in [1].

We can also see the difference in linearity by measuring the IIP3 of the amplifier. Two tones with frequencies of 10kHz and 11kHz were used in the PSS analysis. The following IIP3 plots were generated:

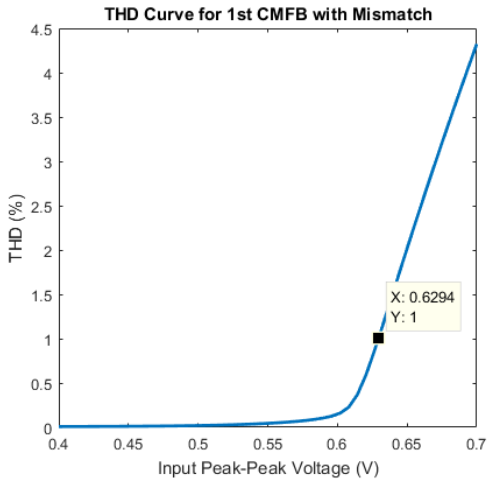


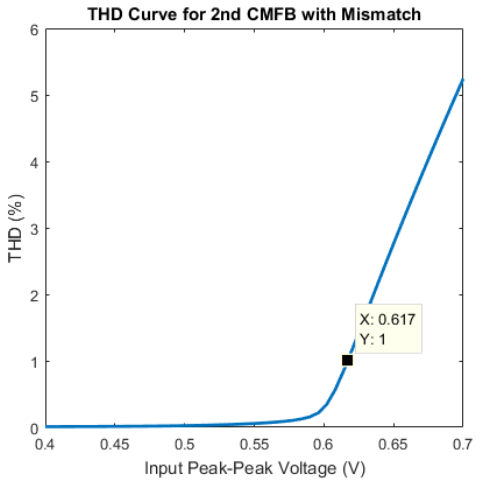
For the first CMFB, the IIP3 is 27.8921dBm while for the second CMFB it is 24.887dBm. Once again, we see that the linearity of the first CMFB is better and care must be taken during the design of the CMFB amplifier to ensure it does not greatly affect the linearity of the overall amplifier.

Next, a common-mode step of 0.5V was used at the input of the amplifier. The common-mode settling times for both amplifiers was the same. The rising settling time was 136.4ns while the falling settling time was 106.6ns for 1% settling:



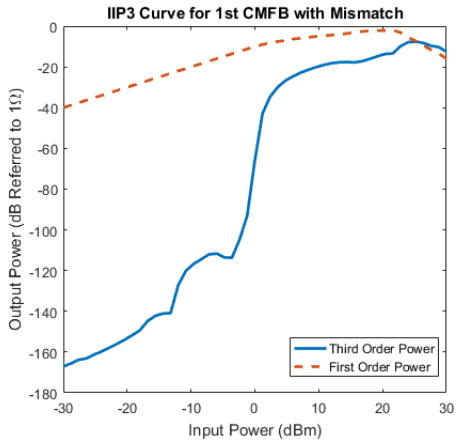
Lastly, the differential input transistors M_1 and M_2 were adjusted so they had a 2% size mismatch. To achieve this, the width of M_1 was increased to 204um. The effects of this mismatch on the linearity of the amplifier were observed by making the same measurements as before. First, the input peak-peak voltage is swept to find the maximum voltage for a 1% THD:

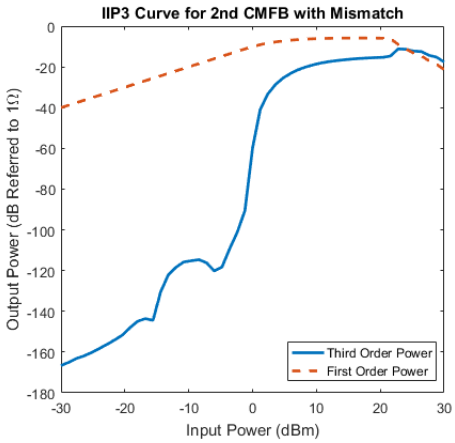




From these plots, it appears that the maximum voltage for a 1% THD does not change from the previous case without mismatch.

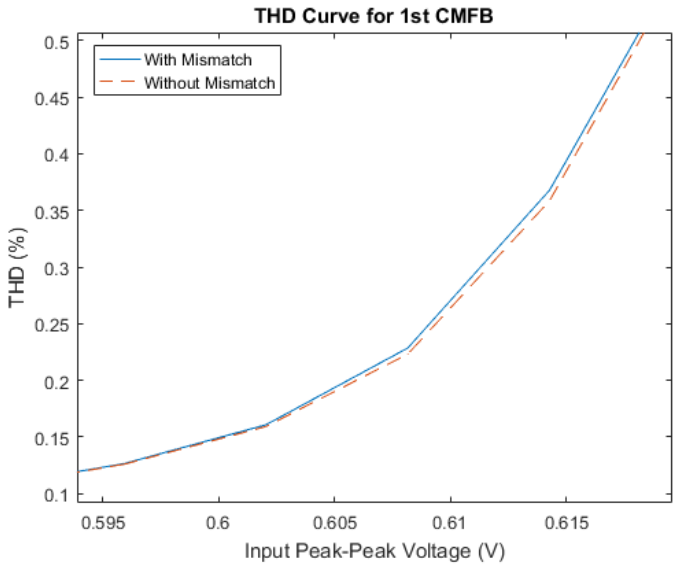
We can also measure the IIP3 of the amplifier with mismatch:





The measured IIP3 for the first CMFB with mismatch is 27.908dBm while for the second it is 24.8974dBm. These values are very close to the values simulated for the amplifiers without mismatch.

While it may seem from the above results that the linearity of the amplifier does not suffer with this mismatch present, that is not the case. The figure below shows the THD curve for the first CMFB with and without mismatch. Clearly, the THD with the mismatch is slightly higher.



In addition, the IIP3 measurement does not capture the effect that the mismatch would have on the linearity. This is because the mismatch will lead to an increase in even-order distortion since the even-order harmonics of the output will no longer be cancelled out perfectly. This leads to the increase in the THD but does not affect the IIP3 since that is mainly a measure of third-order distortion. The increase in second-order distortion can be seen clearly by examining the magnitude of the harmonics at the output of the amplifier:

Harmonic	Power without Mismatch (dBm)	Power with Mismatch (dBm)
0	-139.390	-40.091
1	5.556	5.556
2	-136.308	-71.392
3	-54.375	-54.404
4	-137.427	-76.365
5	-56.143	-56.156
6	-137.447	-77.429
7	-59.420	-59.413
8	-141.917	-78.803
9	-63.876	-63.829
10	-137.210	-80.390

Clearly, the even-order distortion with the mismatch is much higher than without. The third order distortion decreases a very small amount which accounts for the increase in the IIP3 for both amplifiers with mismatch. The very small increase in THD is most likely due to the fact that the mismatched transistors are operating in moderate inversion. If these transistors were operating in strong inversion, small mismatches in the size would cause large changes in the THD. A larger mismatch in the input transistors would be required to see a large effect on the linearity when they are operating in moderate inversion.

A summary of the results for this problem can be found below:

Parameter	Requirement	Amplifier with 1st CMFB	Amplifier with 2nd CMFB
DM Gain	>90 dB	90.54 dB	90.54 dB
DM GBW	>4 MHz	5.015 MHz	5.022 MHz
CM Loop Gain	N/A	95.4 dB	95.4 dB
CM Loop GBW	N/A	5.042 MHz	5.042 MHz
DC CMRR	>85 dB	124 dB	124 dB
SR	>2 V/us	3.71 V/us	3.73 V/us
1% Settling Time	<160 ns	152.3 ns	153 ns
Power Dissipation	N/A	907.08 uW	907.08 uW
Peak-Peak Voltage for 1% THD	N/A	629.4 mV	617.1 mV
IIP3	N/A	27.8921 dBm	24.887 dBm

It is interesting to note that although the second CMFB topology provides very similar settling and CM loop GBW performance with the same power, it provides slightly worse linearity.

Problem 2

Design

We start this problem by determining the requirements for the op amp used in the amplifier. The transfer function for the closed loop amplifier is:

$$H_{CL}(s) = -\frac{2R}{R+2R} \cdot \frac{\frac{GBW}{s}}{1+\frac{R}{R+2R} \cdot \frac{GBW}{s}} = -2 \cdot \frac{1}{\frac{s}{GBW \cdot \frac{1}{3}} + 1}$$

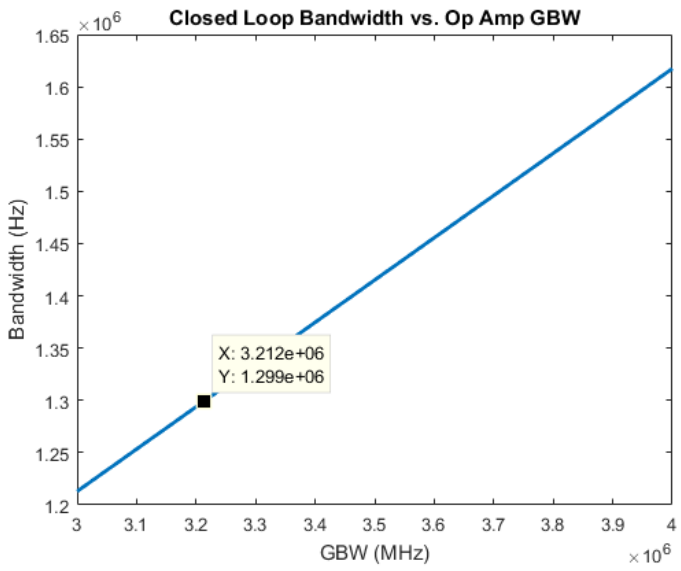
Therefore, the pole of the amplifier occurs at $\omega_p = \frac{1}{3} GBW$, which indicates that the GBW of the amplifier will need to be at least:

$$GBW = 3 \cdot 1.3MHz = 3.9MHz$$

This GBW is a very rough estimate of the GBW required to produce a bandwidth of 1.3MHz. MATLAB simulations with a more complex op amp model were performed to get a better estimate of the required GBW. The op amp is assumed to have the following transfer function:

$$A(s) = A_0 \cdot \frac{1 - \frac{s}{\omega_Z}}{\left(1 + \frac{s}{\omega_{p1}}\right)\left(1 + \frac{s}{\omega_{p2}}\right)}$$

This model is a good approximation of the two-stage amplifier with Miller compensation and takes into account the RHP zero created by the compensation capacitor. In order to achieve a good phase margin, the zero frequency is set to 10 times the GBW of the amplifier ($A_o \cdot \omega_{p1}$) while the second pole frequency is set to 2.5 times the GBW of the amplifier. This provides a phase margin of around 65 degrees in open loop. The GBW of the amplifier is then swept from 3MHz to 4MHz and the bandwidth of the closed-loop system is observed:



This curve indicates that to achieve a closed-loop bandwidth of 1.3MHz, the GBW of the op-amp must be approximately 3.25MHz.

Next, we determine the gain required to produce less than a 1.1% gain error. The DC gain of the closed-loop is:

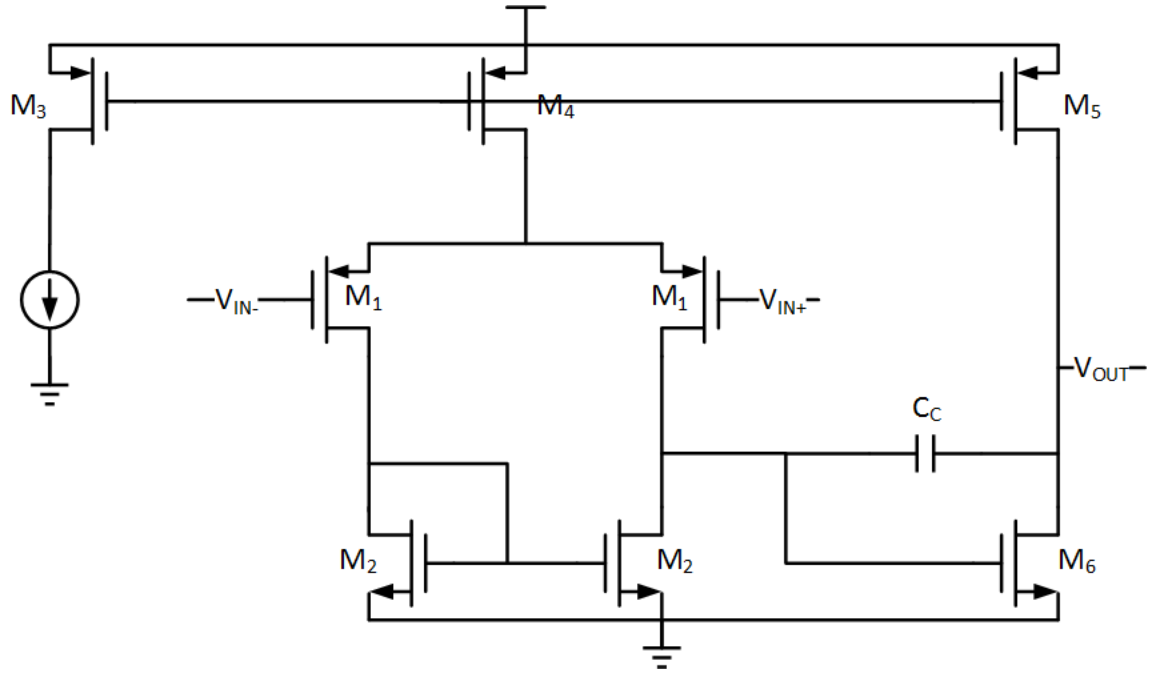
$$A_{CL} = -\frac{2}{3} \cdot \frac{A_{OL}}{1 + \frac{1}{3}A_{OL}}$$

We can solve for A_{OL} with a gain error of 1.1%:

$$-2 \cdot (1 - 0.011) = -\frac{2}{3} \cdot \frac{A_{OL}}{\left(1 + \frac{1}{3}A_{OL}\right)} \rightarrow A_{OL} > 270V/V$$

Therefore, the gain must be greater than 49dB when loaded with the feedback resistors. Since the op amp will ideally make both of the voltages the same, the negative terminal of the op amp will be a virtual ground. Therefore, the resistive load on the op amp will be 2R. We set 2R equal to 50kΩ to ensure the load does not decrease the gain too much.

Since the SR of the inverting amplifier must be greater than 1.5V/us, we ensure that the op amp used in the amplifier has this slew rate.



Next, we must design the op amp used in the amplifier with the above specifications as well as a SR of 1.5V/us. It is assumed that the load capacitance is 25pF. We will use the simple two-stage op amp schematic above. We start by setting C_C to 6.25pF since we earlier set the zero frequency to 10 times the GBW and the second pole frequency to 2.5 times the GBW. We can therefore find the required value for g_{m1}:

$$g_{m1} = 3.25MHz \cdot 2\pi \cdot 6.25pF = 130\mu A/V$$

We set the inversion level of the first stage to 10 to ensure power dissipation is kept somewhat low. Another consideration with the choice of this inversion level is the input capacitance of the amplifier. This input capacitance will create another pole in the feedback loop due to the feedback resistors. As a result, this input capacitance should be kept as low as possible. From the inversion level and transconductance, we can find the required current and aspect ratio. We set the length of all transistors to 520nm to ensure we meet the gain requirement:

$$I_1 = \frac{\left(1+\sqrt{1+10}\right)}{2} \cdot 0.026V \cdot \frac{130\mu A}{V} \cdot 1.164 = 8.5\mu A$$

$$\frac{W}{L}_1 = \frac{\frac{130\mu A}{V}}{\frac{85\mu A}{V^2} \cdot 0.026V} \cdot \frac{1}{\sqrt{1+10}-1} = 25.4 \rightarrow \left(\frac{W}{L}\right)_1 = \frac{15\mu m}{520nm}$$

Next, we know that g_{m6} must be 10 times g_{m1}. Therefore, we can find the required current and size for this transistors with an inversion level of 1:

$$I_6 = \frac{1+\sqrt{1+1}}{2} \cdot 0.026V \cdot \frac{1.3mA}{V} \cdot 1.194 = 51\mu A$$

$$\frac{W}{L}_6 = \frac{\frac{1.3mA}{V}}{\frac{777\mu A}{V} \cdot 0.026V} \cdot \frac{1}{\sqrt{1+1}-1} = 155.4 \rightarrow \left(\frac{W}{L}\right)_6 = \frac{80\mu m}{520nm}$$

Next, we size M_2 to provide minimal input-referred offset:

$$\left(\frac{W}{L}\right)_2 = \frac{8.5\mu A}{51\mu A} \cdot \frac{80\mu m}{520nm} = \frac{13.3\mu m}{520nm}$$

We set the bias current source to 4.25uA and the size of M_3 to:

$$\left(\frac{W}{L}\right)_3 = \frac{10\mu m}{1\mu m}$$

Next, we size M_4 to provide 17uA of bias current in the first stage:

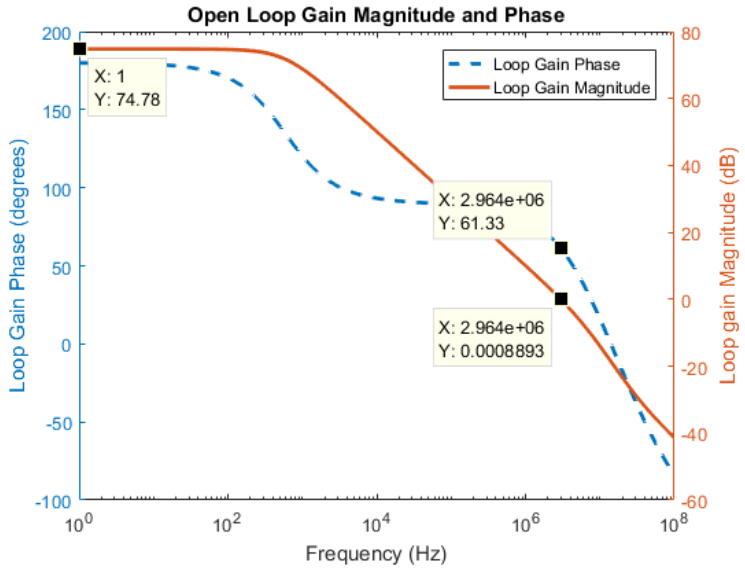
$$\left(\frac{W}{L}\right)_4 = \frac{40\mu m}{1\mu m}$$

Lastly, we size M_5 to provide 51uA of bias current in the final stage:

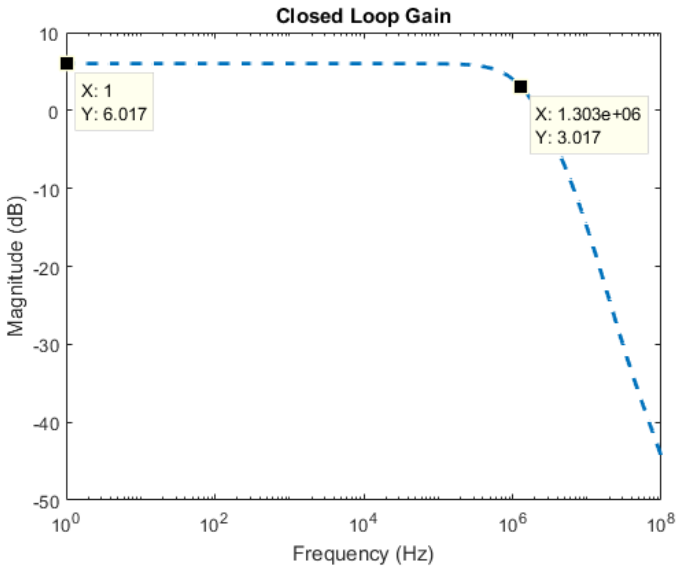
$$\left(\frac{W}{L}\right)_5 = \frac{120\mu m}{1\mu m}$$

Simulation

First, the AC response of the amplifier was simulated with a load of 20pF in parallel with 50kΩ. This can be found in the figure below. The amplifier has a gain of 74.78dB which is well above the 49dB required to have a gain accuracy of 1.1% in closed loop. In addition to this, the GBW of the amplifier is 3.207MHz which is very close to the value required to obtain a closed-loop bandwidth of 1.3MHz. Lastly, the phase margin for a unity-gain configuration is 61.33 degrees which should provide very good stability in closed loop.



Next, the loop was closed around the amplifier with an input resistance of 25kΩ and a feedback resistance of 50kΩ. The resulting closed-loop gain can be found below:

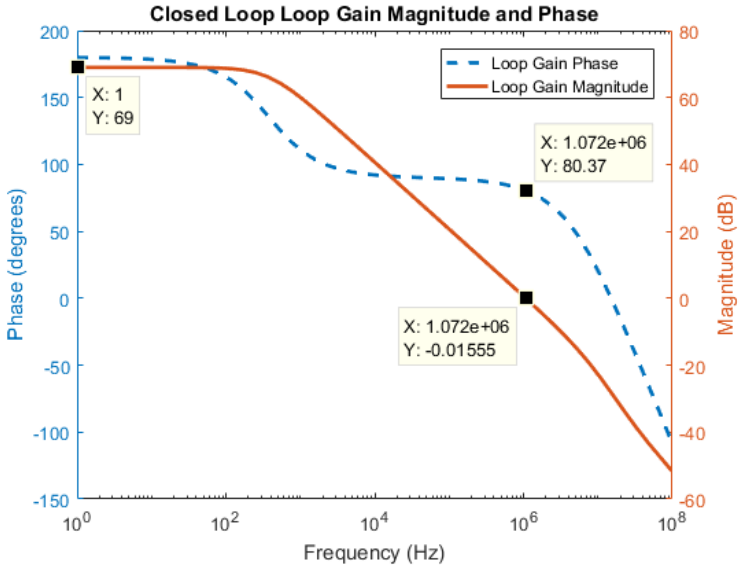


The bandwidth of the amplifier is 1.303MHz which is very close to the desired value of 1.3MHz. In addition to this, the gain error can be calculated as:

$$\%error = \frac{\left|10^{\frac{6.017dB}{20}} - 2\right|}{2} \cdot 100 = 0.041\%$$

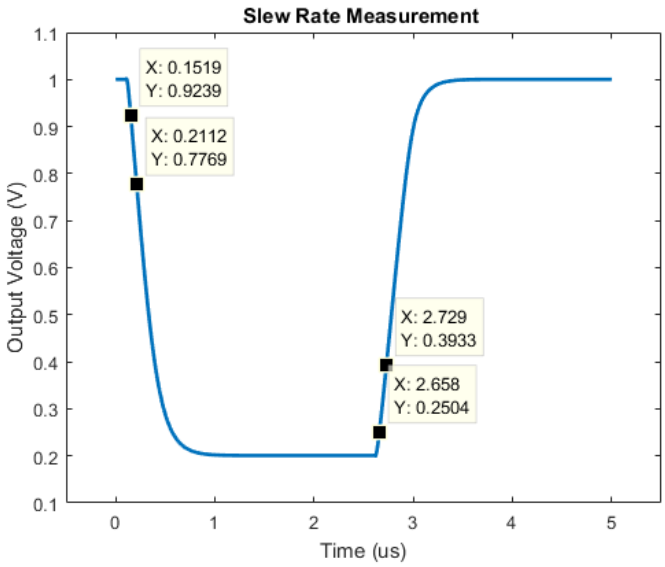
Therefore, this gain error is well within the given specification.

Next, the stability of the amplifier in closed loop was checked to ensure the phase margin is above 60 degrees:



From this graph, we can clearly see that the phase margin is 80.37 degrees which should provide a very stable amplifier for this load capacitance of 20pF.

Lastly, the slew-rate of the amplifier was checked by using a large signal input:



The slew rates can be calculated as follows:

$$SR_{-} = \frac{0.9239V - 0.7769V}{0.2112\mu s - 0.1519\mu s} = 2.48V/\mu s$$

$$SR_{+} = \frac{0.3933V - 0.2504V}{2.729\mu s - 2.658\mu s} = 2.01V/\mu s$$

Both slew rates are above the required specification of 1.5V/us.

These results, along with the required specifications, can be found in the table below:

Parameter	Specification	Simulated Value
Closed Loop Gain	6.0206 dB	6.017 dB
Closed Loop Bandwidth	1.3 MHz	1.303 MHz
Slew Rate	>1.5 V/us	2.01 V/us

Analysis

If we use the op amp transfer function found in the first part of this problem, we can estimate the locations of the poles and zeros in the closed loop response. The closed loop response will be:

$$H_{CL}(s) = -\frac{2}{3}\frac{A(s)}{1 + \frac{1}{3}\cdot A(s)} = -2\cdot\frac{A(s)}{3 + A(s)}$$

We can now substitute A(s):

$$H_{CL}(s) = -2 \cdot A_0 \cdot \frac{\frac{1-\frac{s}{\omega_Z}}{\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{s}{\omega_{p2}}\right)}}{3 + A_0 \cdot \frac{1-\frac{s}{\omega_Z}}{\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{s}{\omega_{p2}}\right)}} = -2 \cdot A_o \cdot \frac{\left(1-\frac{s}{\omega_Z}\right)}{3\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{s}{\omega_{p2}}\right) + A_o\left(1-\frac{s}{\omega_Z}\right)}$$

We can expand the terms in the denominator to find the standard second-order response parameters:

$$H_{CL}(s) = -2 \cdot A_o \cdot \frac{\left(1-\frac{s}{\omega_Z}\right)}{3 + \frac{3s}{\omega_{p1}} + \frac{3s}{\omega_{p2}} + \frac{3s^2}{\omega_{p1}\omega_{p2}} + A_o - \frac{A_o s}{\omega_Z}}$$

We can normalize the denominator so the s^2 term has a coefficient of 1:

$$D(s) = \omega_{p1}\omega_{p2} + s\omega_{p2} + s\omega_{p1} + s^2 + \frac{A_o\omega_{p1}\omega_{p2}}{3} - s\frac{A_o\omega_{p1}\omega_{p2}}{3\omega_Z}$$

Reordering the terms, we get:

$$D(s) = s^2 + \left(\omega_{p1} + \omega_{p2} - \frac{A_o\omega_{p1}\omega_{p2}}{3\omega_Z}\right) + \left(\omega_{p1}\omega_{p2} + \frac{A_o\omega_{p1}\omega_{p2}}{3}\right) = s^2 + 2\zeta\omega_n s + \omega_n^2$$

Therefore:

$$\omega_n = \sqrt{\frac{\omega_{p1}\omega_{p2}(A_o+3)}{3}}$$

$$\zeta = \frac{\omega_{p1} + \omega_{p2} - \frac{A_o\omega_{p1}\omega_{p2}}{3\omega_Z}}{2\omega_n}$$

For our op amp, we can calculate ω_n and ζ:

$$\omega_n = \sqrt{\frac{3670.64rad}{s} \cdot \frac{55.083Mrad}{s} \cdot \frac{(5483+3)}{3}} = \frac{19.23Mrad}{s} = 3.06MHz$$

$$\zeta = \frac{\frac{3670.64rad}{s} + \frac{55.083Mrad}{s} - \frac{5483 \cdot \frac{3670rad}{s} \cdot \frac{55.083Mrad}{s}}{3 \cdot \frac{199.58Mrad}{s}}}{2 \cdot \frac{19.23Mrad}{s}} = 1.384$$

From these parameters, we can find the values of the closed-loop poles:

$$\omega_{p1,CL} = 3.06MHz \cdot \left(-1.384 + \sqrt{1.384^2 - 1}\right) = -1.307MHz$$

$$\omega_{p2,CL} = 3.06MHz \cdot \left(-1.384 - \sqrt{1.384^2 - 1}\right) = -7.16MHz$$

Lastly, we see from the closed loop transfer function that the zero in the open loop transfer function remains at the same location:

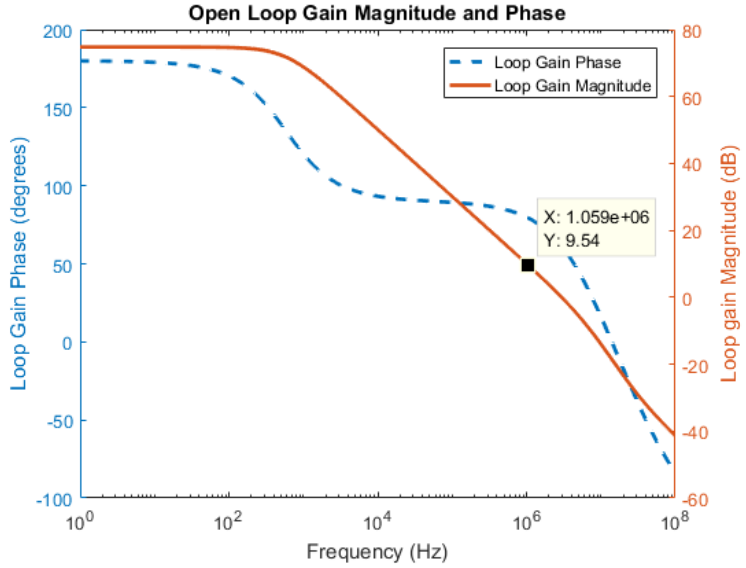
$$\omega_z = \frac{199.58Mrad}{s} = 31.764MHz$$

These pole locations were confirmed in simulations using the PZ analysis. The results can be found in the table below:

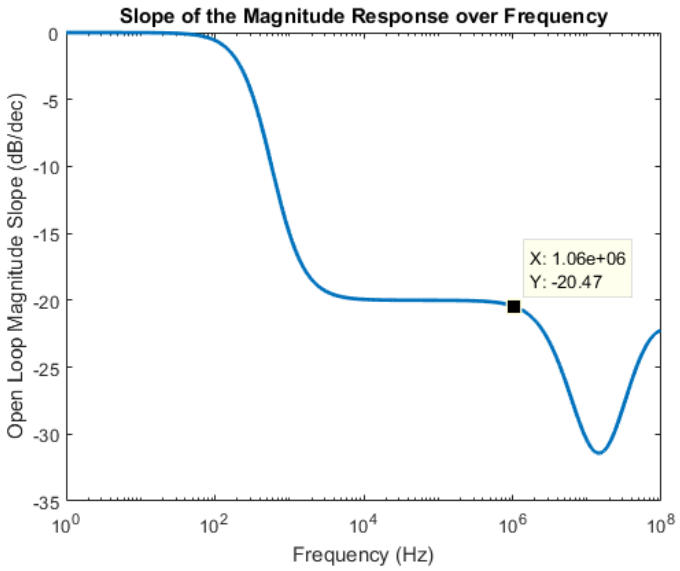
Parameter	Calculated	Simulated
First Pole	1.307 MHz	1.359 MHz
Second Pole	7.16 MHz	7.914 MHz
Zero	31.764 MHz	29.12 MHz

Therefore, we can see that the closed-loop poles calculated from the simple two-stage op amp transfer function match somewhat closely with the poles simulated in Spectre.

While the phase margin of the closed loop system was found in the simulation section, we can also cross-check this phase margin with the rate of convergence. Since we are placing the amplifier in a feedback circuit with a beta value of 1/3, the inverse beta value is 3 or 9.54dB. We can find the frequency at which the open-loop transfer function of the op amp crosses this gain value:



Next, we plot the slope of the transfer function in dB/dec:



The slope of the open loop transfer function is -20.47dB/dec. Since the feedback network ideally has no frequency dependence, the ROC is:

$$ROC = \left| -\frac{20.47dB}{dec} - 0 \right| = 20.47dB/dec$$

From this, we can estimate the phase margin:

$$PM \approx 180° - 4.5 \cdot ROC = 180° - 4.5 \cdot 20.47 = 87.885°$$

This is close to the phase margin found from the closed loop LG shown in the simulation section. This measured phase margin, which is more accurate, was 80.37 degrees.

Appendix A: Matlab Code

```
close all;

%Create an array of the GBW we would like to check
GBW_array=linspace(3e6, 4e6, 100);

s=tf('s');

%Iterate through each GBW
for i=1:100
    GBW=GBW_array(i);
    Gain=270;
    P2_1=2.5;
    PZ_1=10;
    %Construct the open-loop transfer function
    H=Gain*(1-s/(GBW*PZ_1))/(1+s/(GBW/Gain))/(1+s/(GBW*P2_1));
    %Make sure our phase margin is okay
    [Gm, Pm, Wgm, Wpm]=margin(H);
```

```
    %Construc the cloesd loop transfer function
    sys=2/3*feedback(H, 1/3, -1);

    %Find the bandwidth of the closed loop function
    fb(i)=bandwidth(sys);


end
%Plot the GBW and bandwidth
plot(GBW_array, fb, 'LineWidth', 2);
xlabel('GBW (MHz)');
ylabel('Bandwidth (Hz)');
title('Closed Loop Bandwidth vs. Op Amp GBW');
```

References

[1] J. F. Duque-Carrillo, "Control of the Common-Mode Component in CMOS Continuous-Time Fully Differential Signal Processing," *Analog Integrated Circuits and Signal Processing,* vol. 4, pp. 131-140, 1993.