ELEN 607 (ESS) **Due: March 21, 2017**
Spring 2017

Homework Assignment #6

Problem 1 a) Design a FD amplifier with two stages for the following specs using

0.13μm technology

$V_{DD} = 0.6V$ or $V_{DD} = -V_{SS} = 0.3V$

$SR > 2V/\mu sec$

$A_{o,DC} \geq 90dB$

DC $CMRR \geq 85dB$

$GBW > 4MHz$

$PM > 60^o$

$C_L // R_L = 25pF // 47K\Omega$

Power to be minimum

$1\%\ T_s < 160nS$

Use LV techniques such as FG, self-cascode, and/or bulk bias or bulk driven Describe your design procedure for the differential and common-mode gains and bandwidths. Use two different CM detectors and compare results. Provide a summary table including IIP3, 1% THD and indicate the bandwidths and gains of A_{DM} and A_{CM}.

b) Provide the output step response for a common-mode step of 0.25V. What is the Ts?

Problem 2. Design an amplifier topology capable to handle a large capacitance load and be stable under the whole capacitive range that meets the following specs.

Load 0-1,000pF
GBW > 1.5MHz
DC Gain> 100dB
Phase Margin >50
SR>0.8V/us
1% Ts (us) < 0.6
Power < 70uW at 1.2V
CMOS 0.13um
Vdd=1.2V

Ref.- W. Qu, S. Singh, Y. Lee, Y. S. Son and G. H. Cho, "Design-Oriented Analysis for Miller Compensation and Its Application to Multistage Amplifier Design," *in IEEE Journal of Solid-State Circuits*, vol. 52, no. 2, pp. 517-527, Feb. 2017

Education is the passport to the future, for tomorrow belongs to those who prepare for it today.
Malcolm X