# OUTPUT AMPLIFIERS

Material partially provided by Vijayakumar Dhanasekaran

- The main goal of an output amplifier, also called driver amplifier, is to efficiently drive signals into an output load.

- The output load typically consists of small resistor ( 50-100Ω ) and a large capacitor ( 5-1000pf)

- The primary objective of the CMOS output amplifier is to function as a current transformer.

- Conventional requirements of an output amplifier are:

1. Be efficient; 2. Provide sufficient output power in the form of current or voltage; 3 Avoid signal distortion; 4. Provide protection from abnormal conditions (over temperature, short circuit, etc.)

# Outline

1. Introduction to Drivers
    - 1.1 What is a driver
    - 1.2 Application examples
    - 1.3 Crest factor and its implication to power efficiency

2. Class-AB amplifier design
    - 2.1 Class-AB interpretation and properties
    - 2.2 Floating current mirror biasing
    - 2.3 Design example (100ohms driver)
    - 2.4 Low-voltage biasing scheme

3. Compensation of Class-AB amplifiers
    - 3.1 Piece-wise modeling of class-AB stage
    - 3.2 NMC driver design example

4. Practical issues
    - 4.1 Mismatch effects, Load variation, Effect of parasitic resistance, Process and temperature variation

# What is a Driver ?

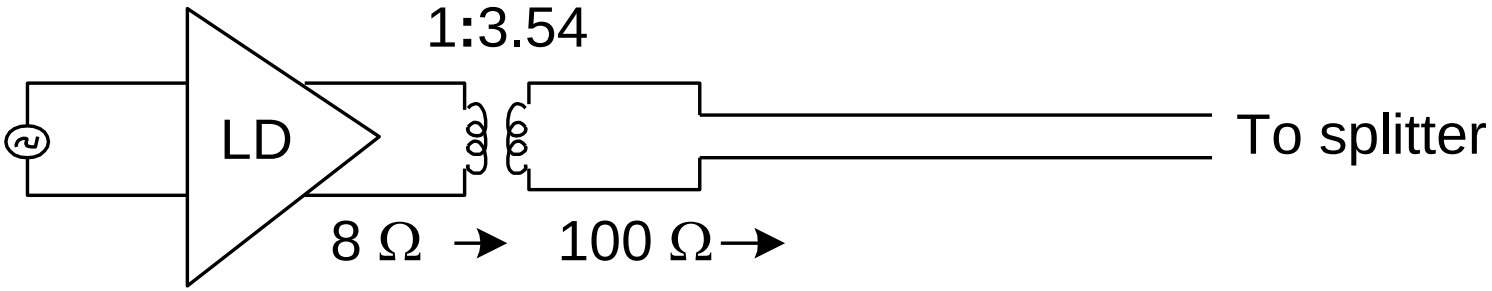
Drivers are amplifiers that interface with external world

| | **Typical Amplifier** | **Driver Amplifier** |
|---|---|---|
| Location of load | On-chip | Off-chip |
| Typical load | Small-medium C and large R | Small R sometimes along with Large C |
| Power delivery | Small | Large |
| Stability | Designed for fixed load condition | Designed for wide range of loads |
| Power efficiency | Mostly non-critical | Very important |
| Application examples | Fixed gain, PGA, active filter | DSL/Ethernet line driver, speaker driver |

# Application Examples

## 1. DSL Line driver

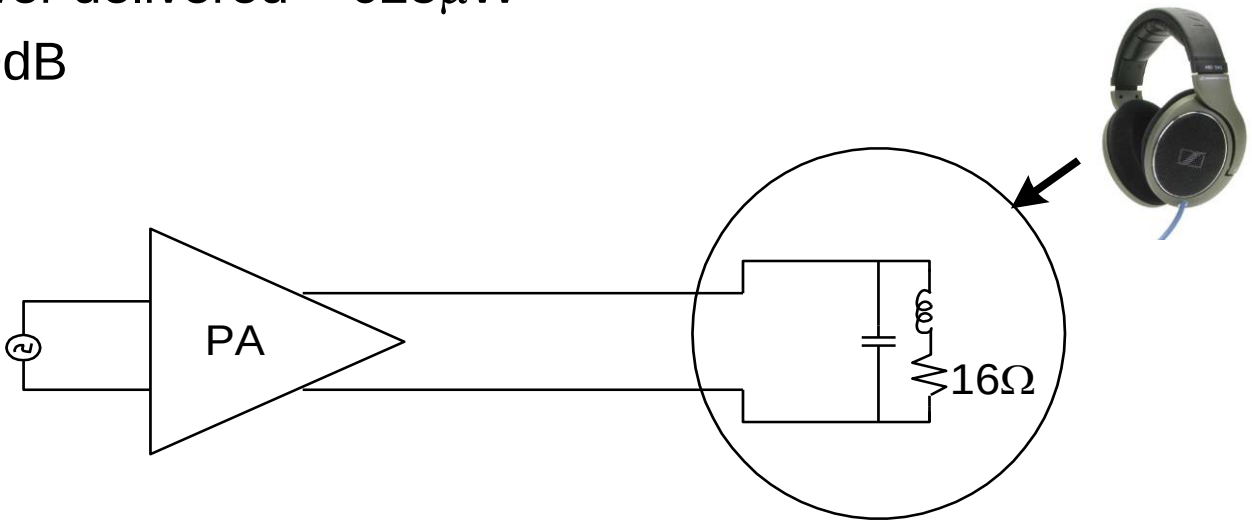
- Drives phone line through a transformer
- 8Ω load (drives 100ohms phone line through 1:3.54 transformer)
- Max swing = 4.4Vpp differential
- Crest Factor = 6.3
- RMS Power delivered = -12dBm
- Signal Bandwidth 1.104MHz THD > 80dB



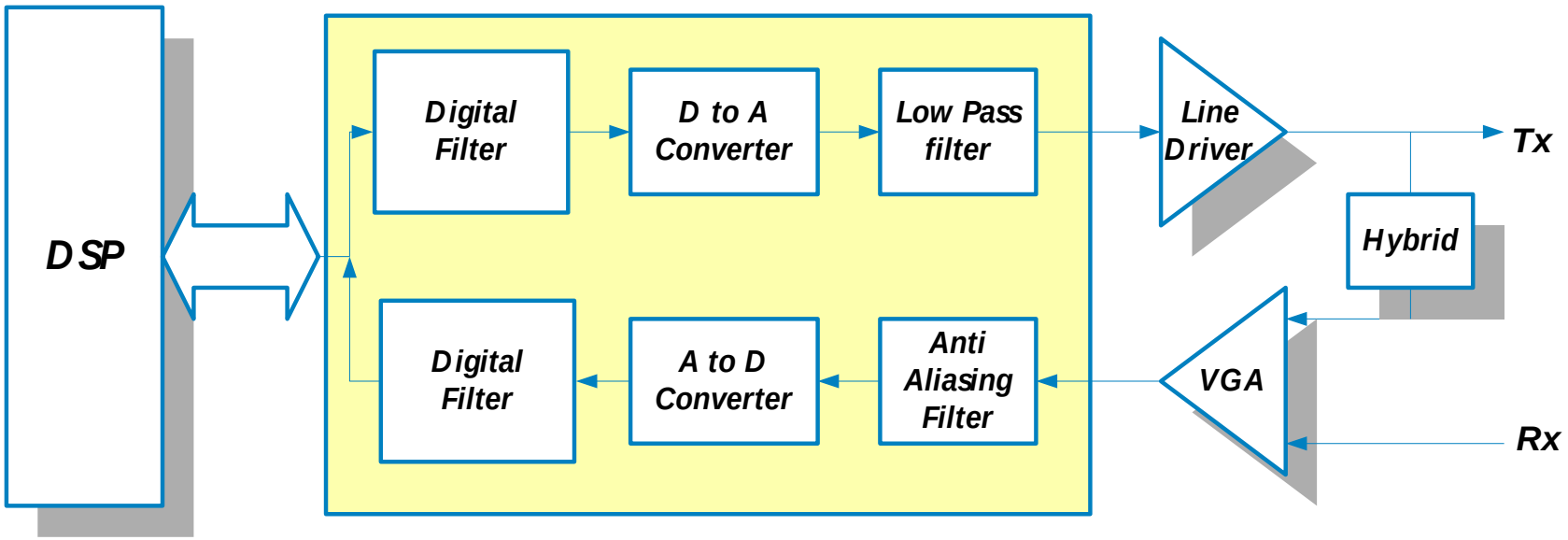
# Application Examples continued…

## 2. Speaker driver

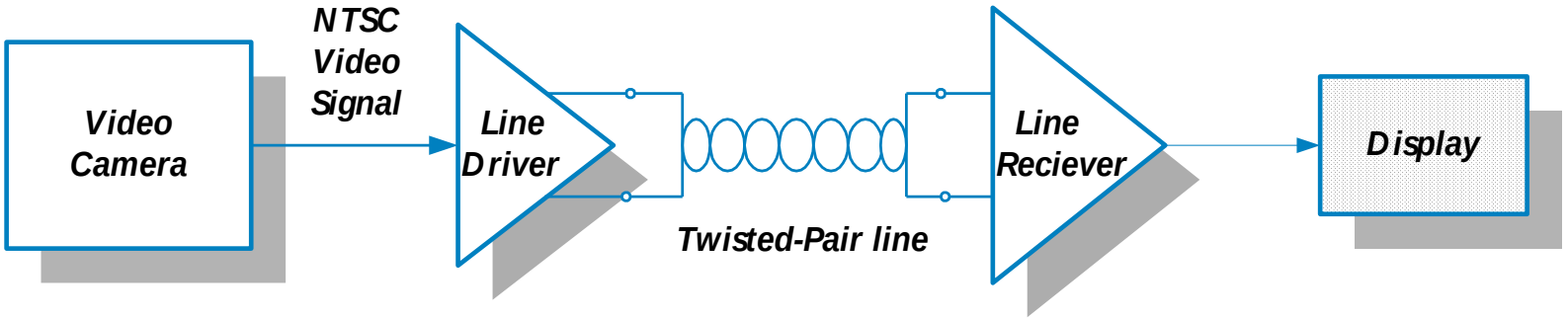
- Drives speaker/headset loads
- 16ohms resistive load
- 100pF to 1nF capacitive load
- Max swing = 2V
- Crest Factor = 10
- RMS Power delivered = 625μW
- THD > 90dB



# 3 Analog Video Line Driver Amplifier



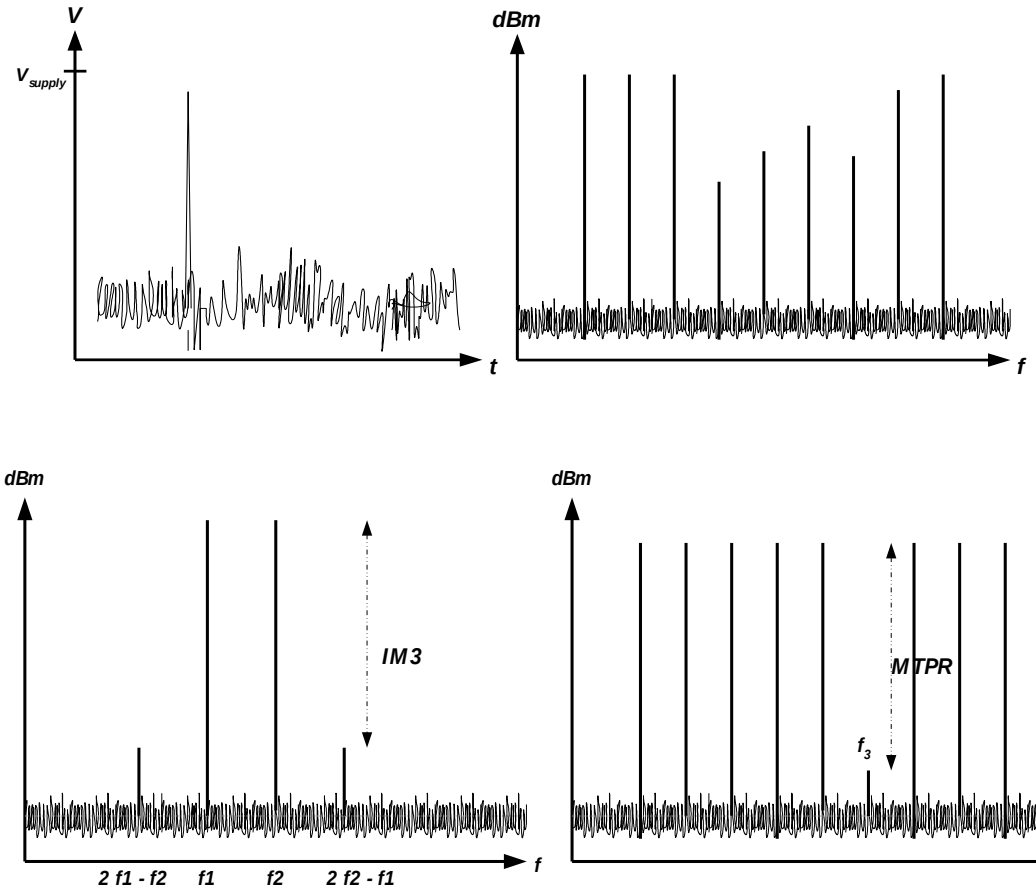

- ISDN
- ADSL, VDSL
- HDSL
- Cable modem




- Set top box
- Security surveillance
- Personal Video recorders

# Requirements

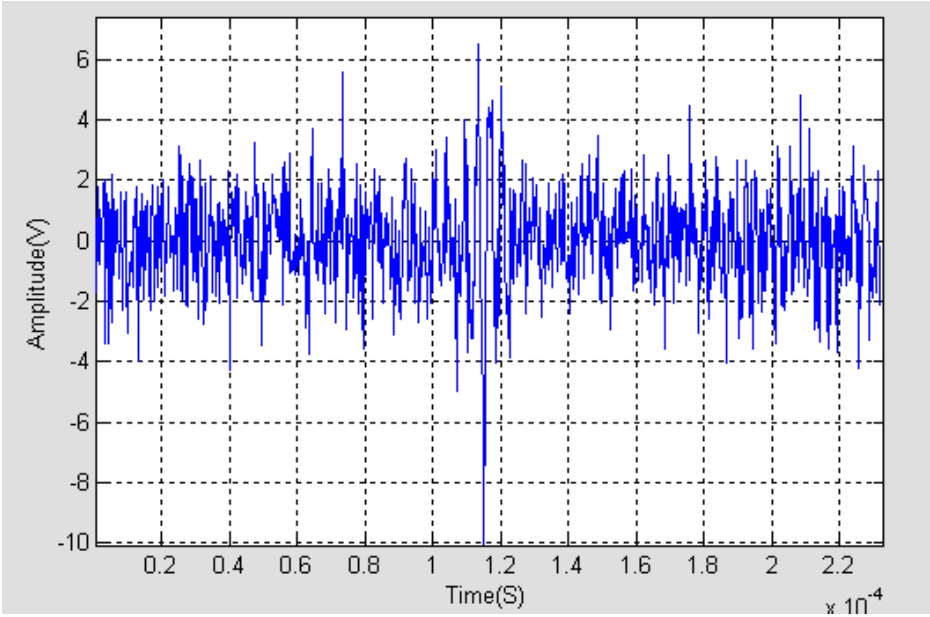
- ***High output swing***
  - Line attenuation $\alpha$ $e^{rl}$
  - Crest factor
- ***Linearity***
  - BER requirements
  - Multi-tone transmission
- ***Bandwidth***
  - Application specific
- ***Power Efficiency***
  - Battery back-up & cooling
- ***Matching***
  - Avoid signal reflections



# Crest factor and power efficiency of amplifiers

- "Real world" signals have amplitude distribution that is very different from that of a sine-wave (typical test signal)
- Peak signal voltage and current is much greater than RMS
- Consequences of large Crest factor (CF) for amplifiers
  - Large supply voltage for given power delivered
  - Large bias current
  - Huge "stand-by" power

Crest Factor is defined as the peak to RMS ratio of the signal



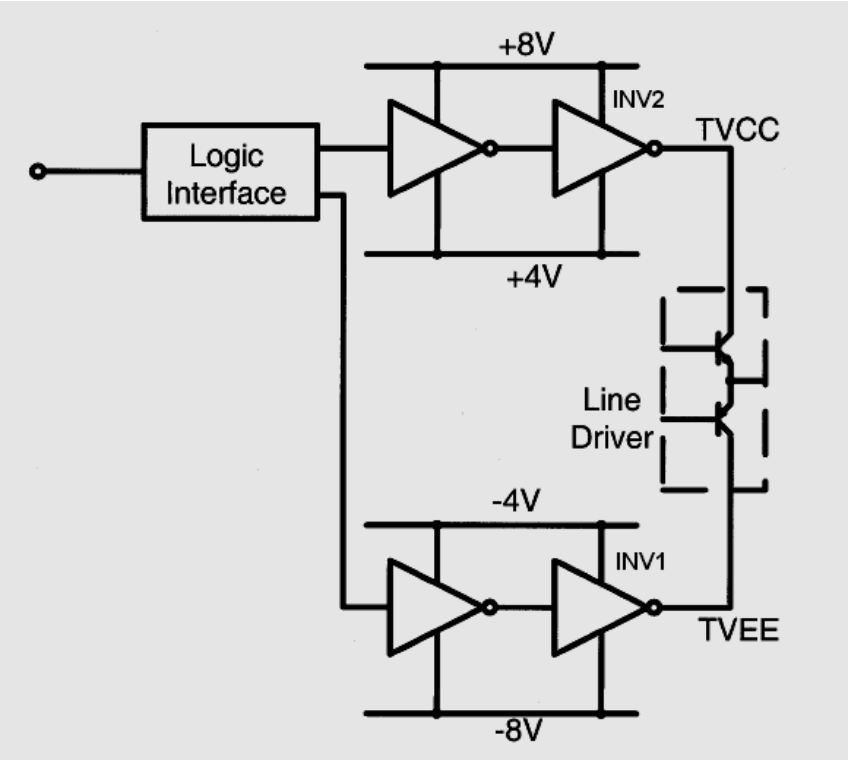

Muli-tone DSL signal in time domain with crest factor of 6

**Solution:**

**Dynamically change the supply voltage and/or bias current of the amplifier**

# Crest factor and power efficiency Contd…

- Class-G amplifiers save power by switching between multiple supplies depending on signal level †
- Drawbacks
  - Need multiple power supplies, which is not attractive for portable devices
  - Need peak prediction logic in digital. A memory array and possibly a digital filter
  - Switching could lead to interference problems




Block diagram of Class-G switching scheme presented in †

**† K.Maclean et al., "A 610-mW zero-overhead class-G full-rate ADSL CO line driver,"** ***IEEE J. Solid-State Circuits*****, Vol. 38, no. 12, pp. 2191-2200, Dec 2003**

# Crest factor and power efficiency Contd…

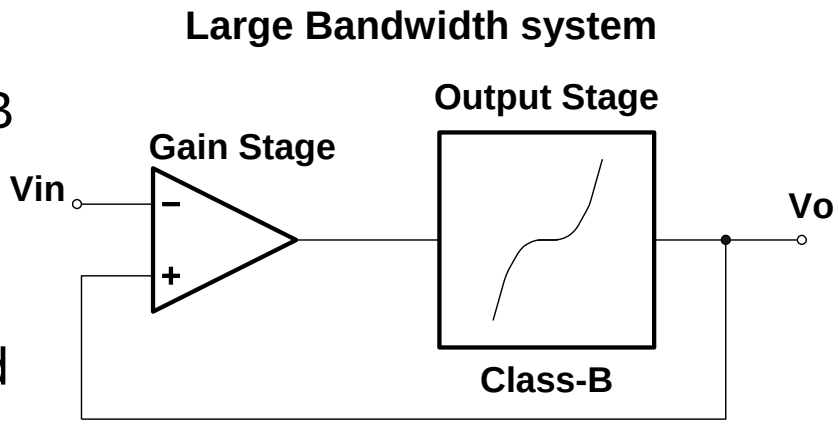
- Class-AB biasing is most commonly used to improve power efficiency
- Current drawn from supply is mostly signal dependant
- A simple analysis
  - Power delivered = $\frac{Vp^2}{CF^2 R}$
  - Power efficiency = Power delivered / Average Power dissipation

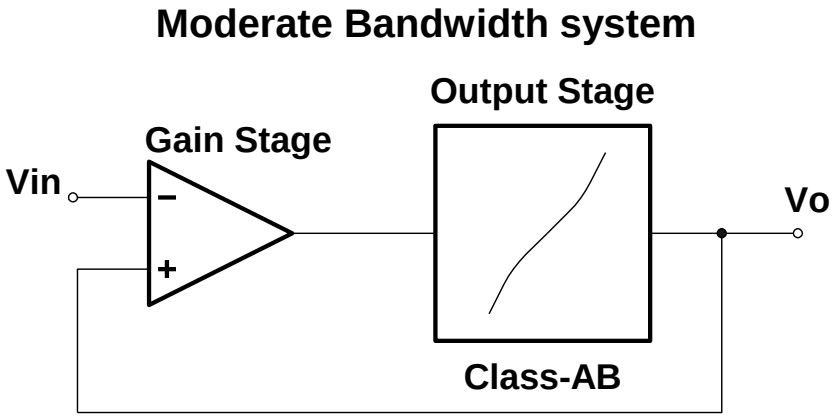
| | Class-A | Class-B | Class-AB |
|---|---|---|---|
| Avg. Power dissipation | $\frac{2Vp^2}{R}$ | $\frac{Vp^2}{CF*R}$ | $\approx \frac{Vp^2}{CF*R} + 2VpI_Q$ |
| Power efficiency | $\frac{1}{2CF^2}$ | $\frac{1}{CF}$ | $\approx \frac{1}{CF\left(1+2CF\frac{I_Q}{Ip}\right)}$ |

where Vp is peak output voltage, R is load resistance, CF is crest factor, Ip is peak current to load and $I_Q$ is bias current under quiescent condition

# Class B Vs Class AB

- Although a Class-B output stage seems to be more efficient, Class-AB is preferred in practice
- Large GBW is required to linearize the “cross over distortion” associated with Class-B output stage
- For Class-AB, minimizing $I_Q/I_P$ improves output stage efficiency but GBW requirement and associated power must be kept in mind
- Spending some power in linearizing the output stage can potentially result in an overall efficient solution



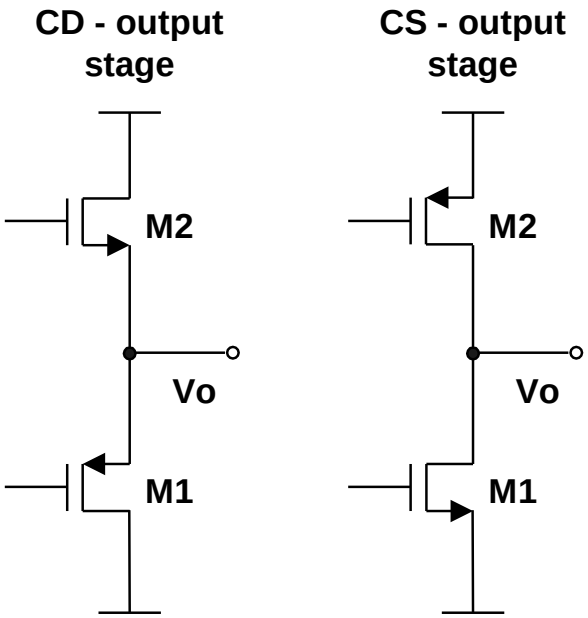



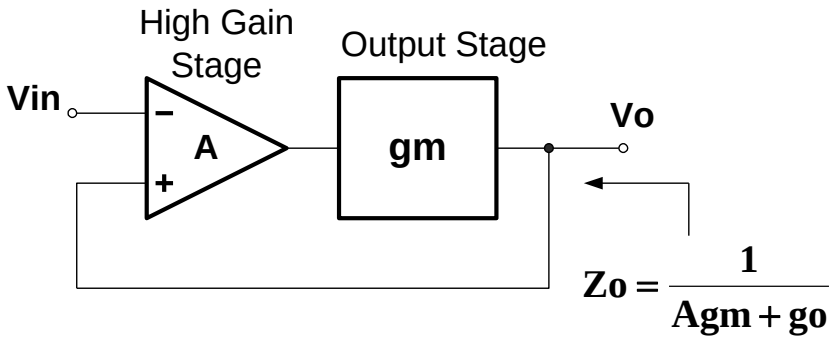
# An apparent paradox with push-pull stage

- The output resistance of a common-drain transistor is 1/gm while that of common-source transistor is 1/gds
- Why is the common-source output stage used for drivers even if the swing requirement is relaxed ?

- The output impedance is mainly determined by 1/(Agm)

  where A is gain of the high-gain stage and gm is transconductance of the output stage
- Common-drain stage performs better as a buffer by itself but is not preferred in closed loop amplifiers
- Common-source output stage is assumed for rest of this presentation



# CLASS-AB OUTPUT STAGE DESIGN

$$Efficiency = \frac{P_{RL}}{P_{SUPPLY}} = \frac{\pi}{2}\frac{v_{OUT}}{V_{DD} - V_{SS}}$$

Class-AB

$$Efficiency = \frac{P_{RL}}{P_{SUPPLY}} = \frac{v_{OUT}{}^2(peak)}{(V_{DD} - V_{SS})^2}$$

Class-B

- Class-AB interpretation and properties
- Floating current mirror biasing
- Design example (100ohms driver)
- Low-voltage biasing scheme

# Class AB output stage interpretation

• Start with a class-B amplifier with input Vin biased such that

**Vgs = Vin + $V_T$**

$$Io \propto sign(Vin) * (Vin)^2$$

• If Vgs gets smaller due to process variation and mismatch, there could be “dead zone” in which Io ~= 0

• This problem is alleviated by shifting the current curves using fixed bias current ($I_Q$)

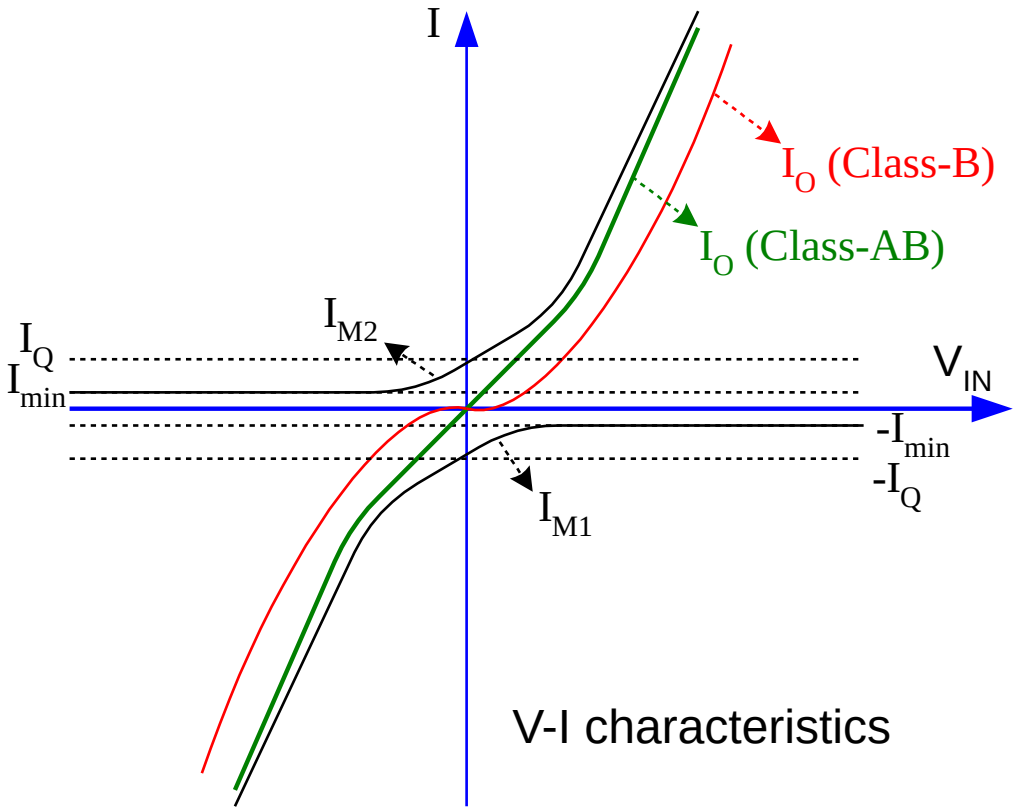
• In the region |Vin| < Vx,

$$Io \propto (Vin + Vx)^2 - (Vin - Vx)^2$$

$$Io \propto VinVx$$

• For |Vin| > Vx

$$Io \propto sign(Vin) * (|Vin| + Vx)^2$$




Shift the +ve part of red curve to left by Vx and the –ve part of red curve to right by Vx and add them together to get the green curve

• Fixing a minimum current (Imin) helps alleviate dynamic non-linearity due to completely off transistor

# Desired Properties of class-AB bias Circuit

1. Set the current of both NMOS and PMOS (to $I_Q$) under quiescent condition

2. Limit the minimum current of the weakly conducting device (to $I_{min}$)

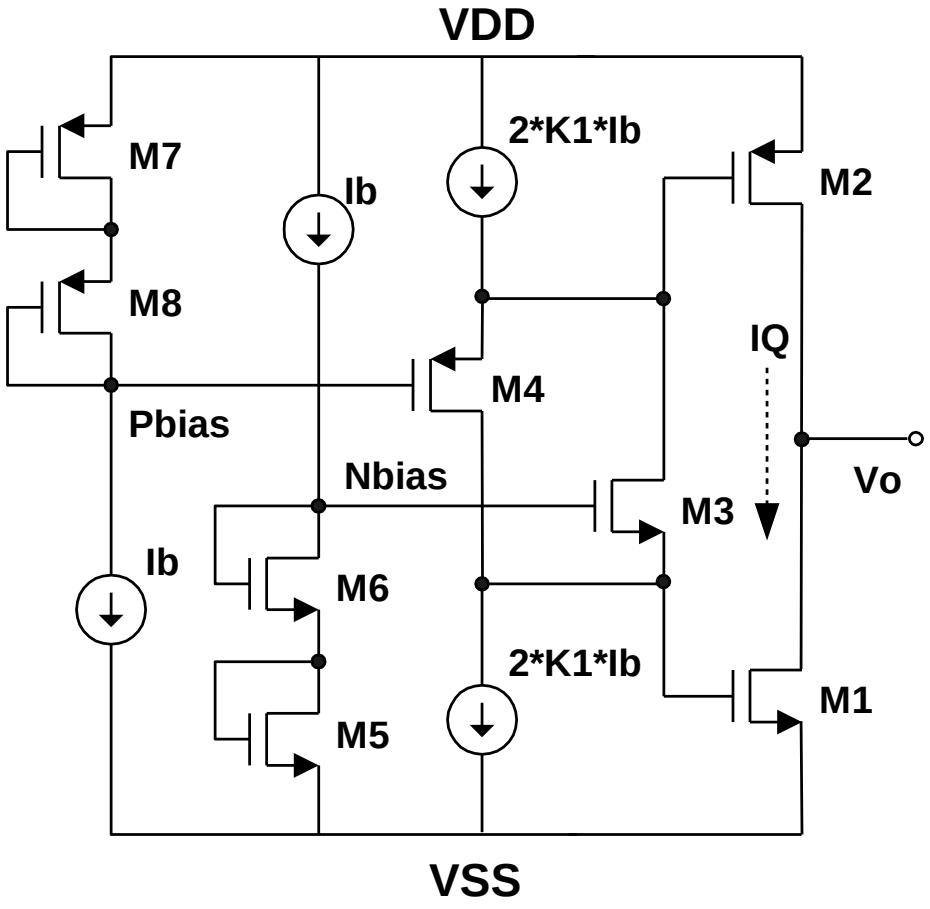
3. Allow maximum possible voltage swing at the gate of strongly conducting device

# Class-AB bias circuit

- Introduced by Monticelli †
- Transistor M3,4 acts as a "floating current mirror"
- Biasing is based on Quadratic translinear principle (QTL) ††
- Vgs5+Vgs6 = Vgs1+Vgs3
- If $\left(\frac{W}{L}\right)_3 = K1*\left(\frac{W}{L}\right)_6$ and

  $\left(\frac{W}{L}\right)_1 = K2*\left(\frac{W}{L}\right)_5$

then $I_Q = K2*Ib$




Monticelli's Class-AB biasing scheme

† D. M.Monticelli, "A quad CMOS single-supply opamp with rail-to-rail output swing," *IEEE J. Solid-State Circuits*, vol. SSC-21, pp. 1026-1034, Dec. 1986

†† W. Gai, H. Chen, E.Seevinck, "Quadratic-translinear CMOS multiplier-divider circuit," *Electron. Lett.*, vol. 33, Issue 10, pp. 860-861, 8 May 1997

# Bias circuit operation

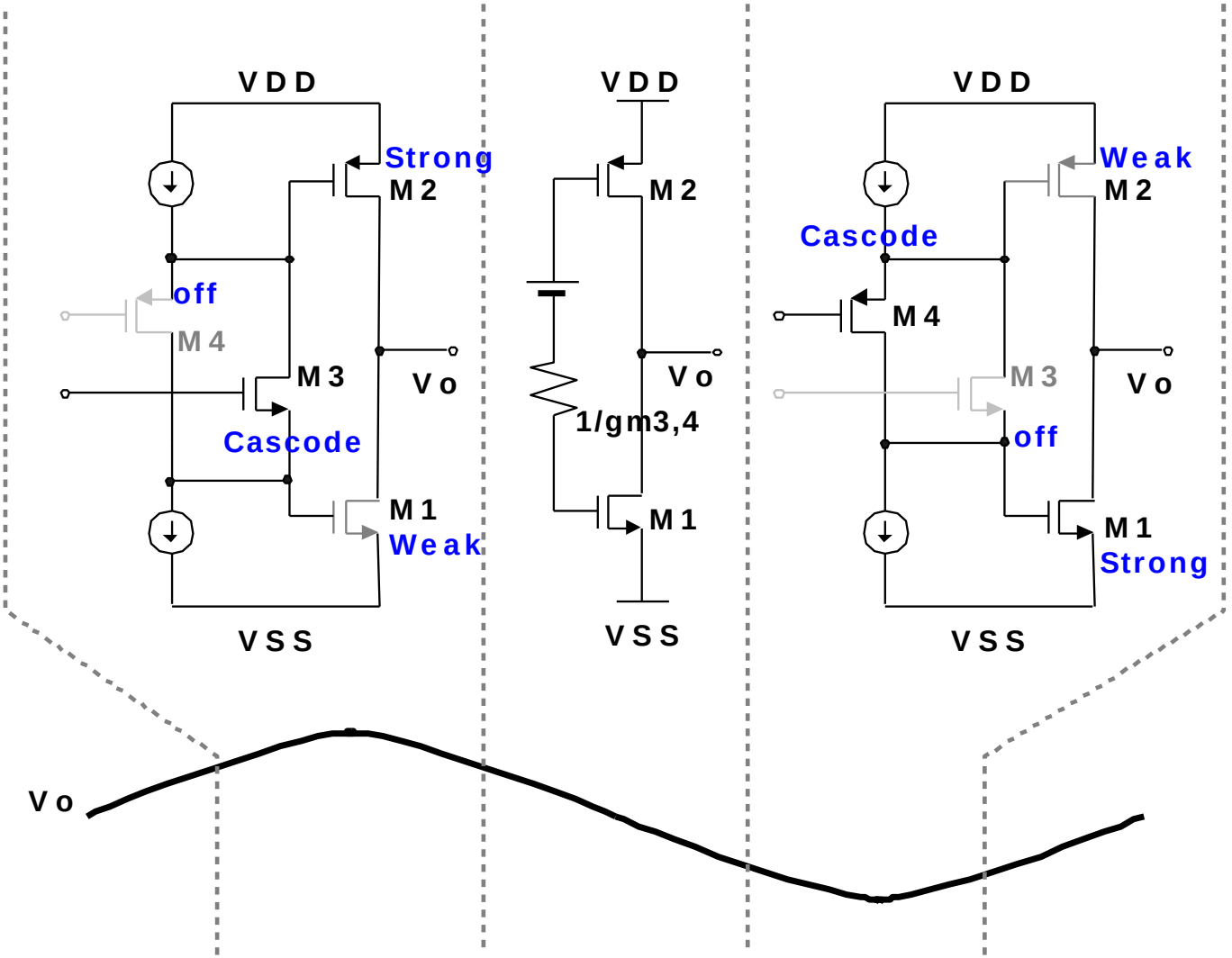
- Nonlinear circuit that has good class-AB properties
- Signal current is accepted at the source node of M3 and/or M4
- Under Q condition, M3 and M4 are designed such that gm3=gm4
- With gm3 = gm4, the floating current mirror acts like a level shifting voltage source with series resistance 1/gm3,4
- For large overdrive of M1(2), M3(4) turns off and M4(3) acts as a cascode transistor
- The cascode transistor serves to pin down the minimum current flowing through the weakly conducting transistor to $I_{min}$
- When M1 is weakly conducting,

  $Vg3 - Vss = Vgs3max + Vgs1min$

- When M1 is strongly conducting,

  $Vgs1max = Vdd - Vss - Vdsat_{IB}$

# Behavior of floating current mirror across output voltage levels



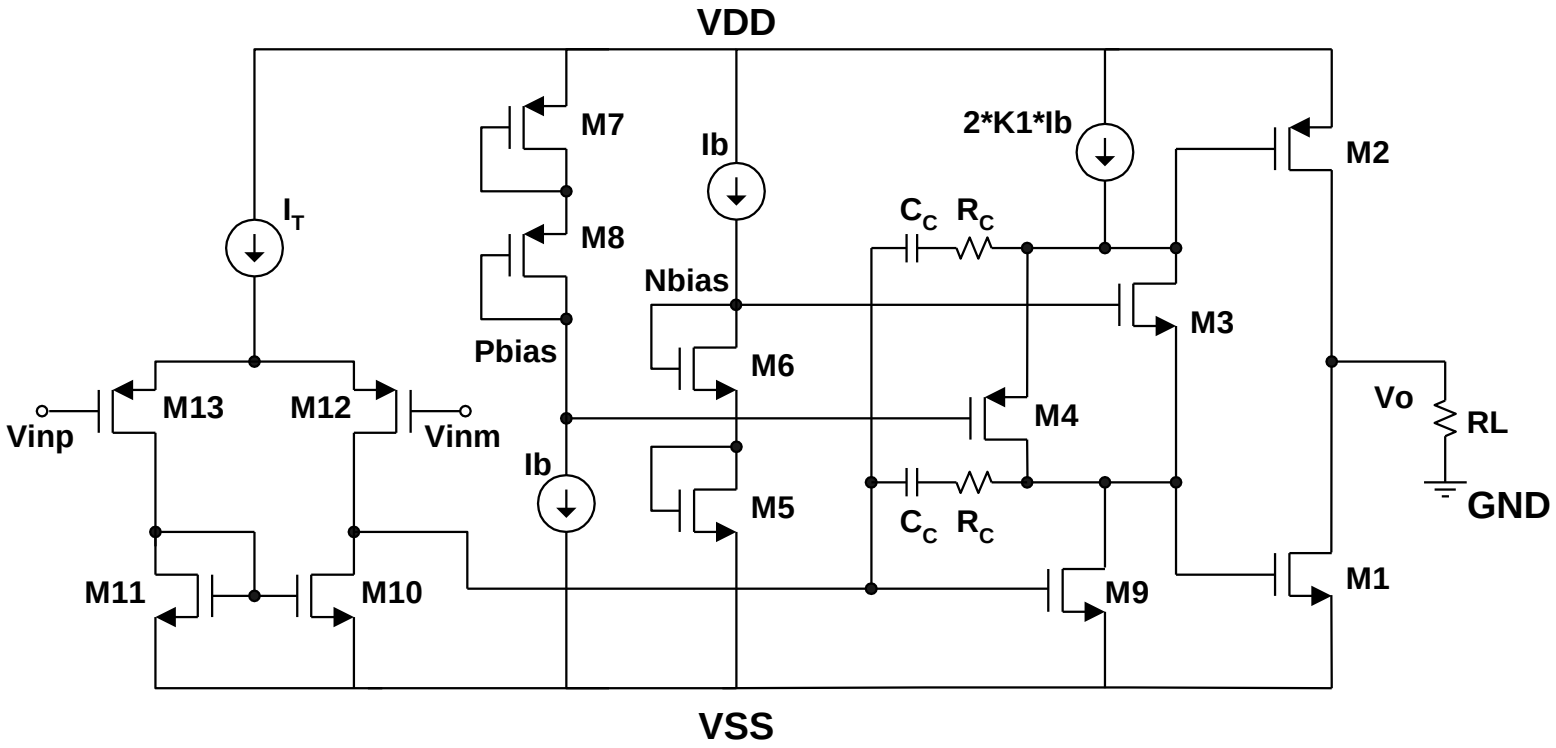
# Design Example – 100Ω driver

- Specifications
  - Output swing = +/- 2V
  - Supply voltage = +/- 2.5V
  - GBW = 180MHz
  - THD with 1MHz, 2Vpp sine-wave > 30dB
  - Full power bandwidth 10MHz
  - Technology = 0.5μm
- Extreme swing condition
  - Vdsat = 0.5V
  - $$\mathbf{I_O = \frac{Vp}{R_L} + I_{min} = 21mA}$$
  - rds not relevant
  - L = 1.0um
  - Calculate W
  - check using simulator if W/L is sufficient to provide Ipeak
- Calculate Vgs of M1 under Q and peak swing condition
- Quiescent state

  Vg3 – Vss = Vgs3Q + Vgs1Q
- Weakly conducting state

  Vg3 – Vss = Vgs3max + Vgs1min
  - Use this to set the minimum current drawn by M1

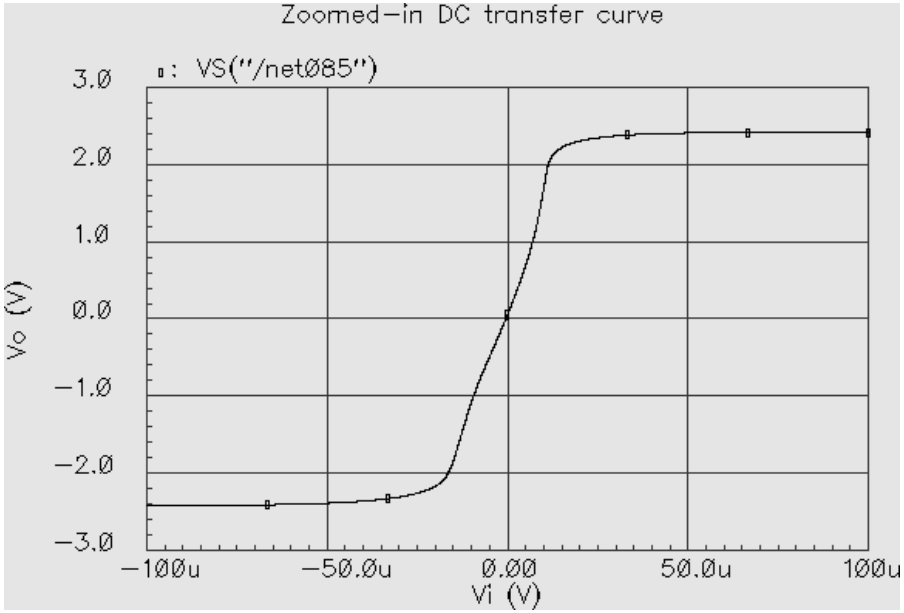
# 100Ω driver – Circuit Diagram

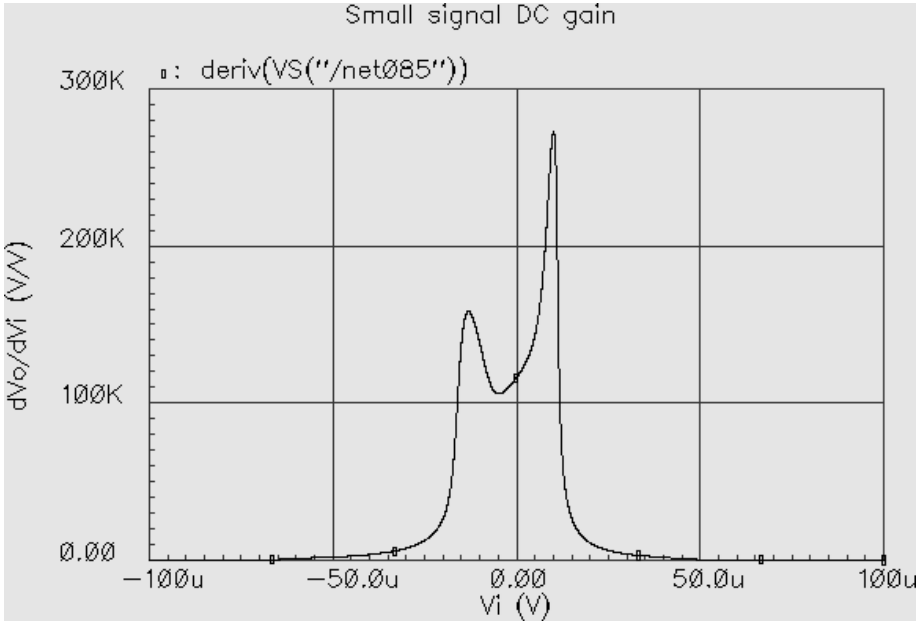



| | |
|---|---|
| M1 | 125 x (10.3/1) |
| M2 | 125 x (31.6/1) |
| M3 | 25 x (2.4/1) |
| M4 | 25 x (5.7/1) |
| M5 | 2 x (10.3/1) |
| M6 | 8 x (2.8/1) |
| M7 | 2 x (31.6/1) |

| | |
|---|---|
| M8 | 8 x (5.7/1) |
| M9 | 1 x (119/2.2) |
| M10,11 | 1 x (6/1) |
| M12,13 | 12 x (28.5/1) |
| Rc | 12KΩ |
| Cc | 1.5pF |
| RL | 100Ω |

# Open Loop Simulation Results

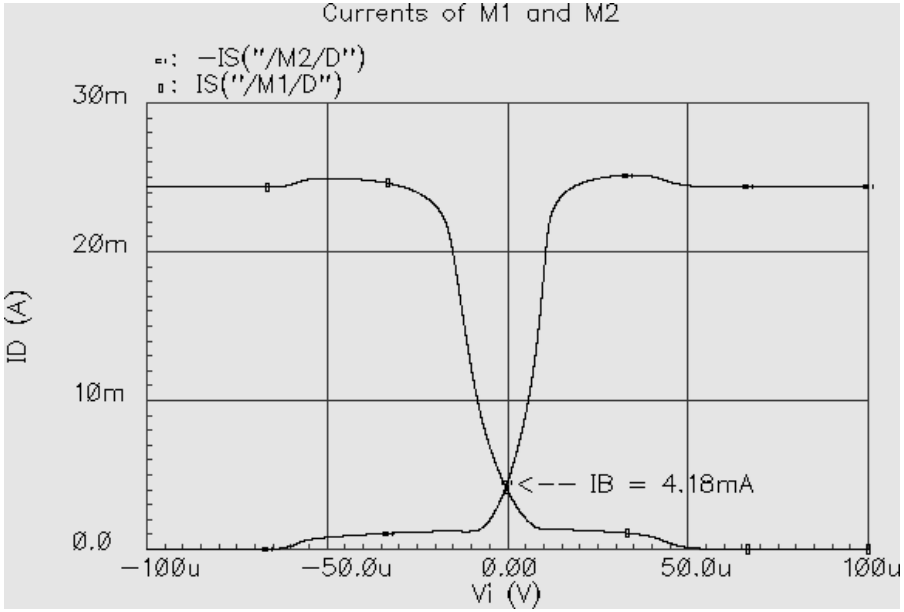


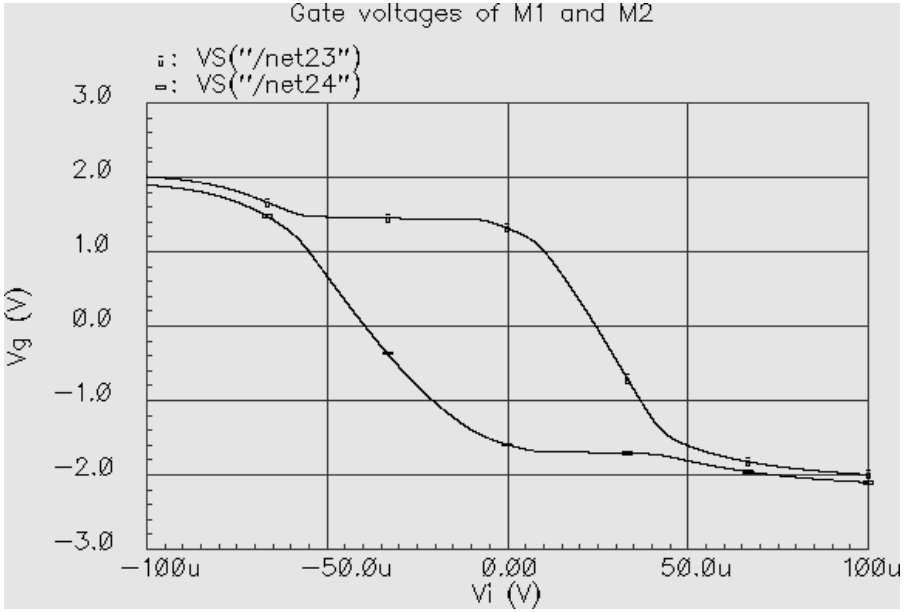

**Vo versus Vi transfer curve** **dVo/dVi versus Vi curve**

- The characteristic shape of the gain curve (dVo/dVi versus Vi) is a reflection of different regions of operation of output transistors
- Around Vi = 0, the output transistors are in weak inversion/sub-threshold and saturation region.
- Gain increases with Vi due to higher current drawn with increasing swing
- Increase in Vi beyond certain point pushes the output transistors in triode region, which result in sharp fall in the gain

# Open Loop Simulation Results … Contd



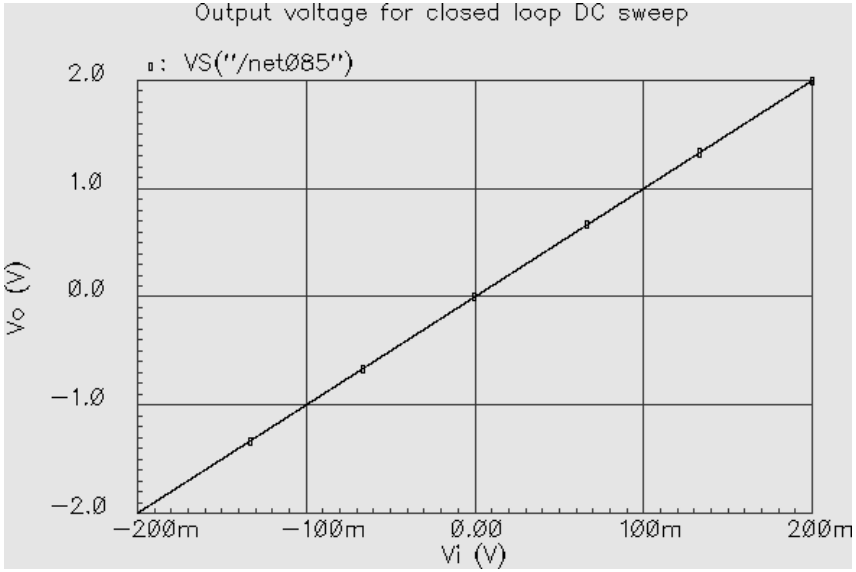

**M1,2 currents versus Vi**

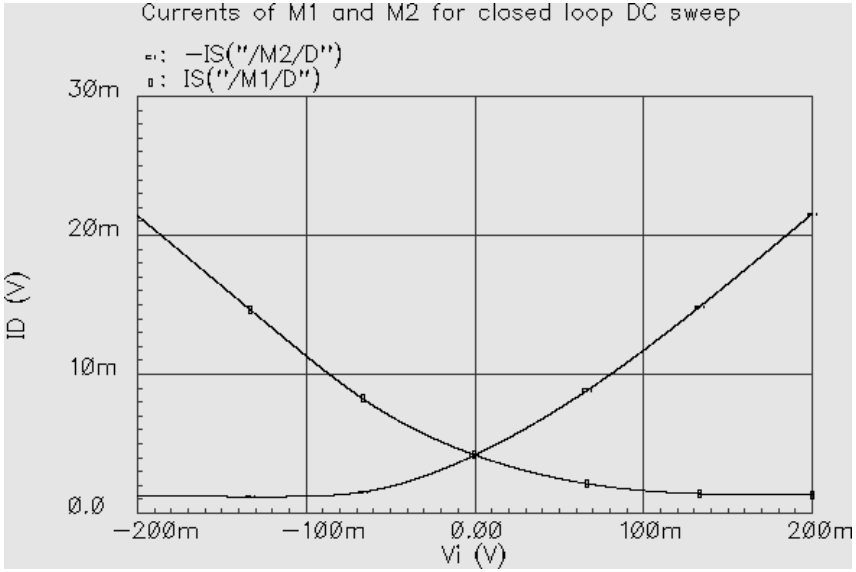



**Vgs1,2 versus Vi**

- The current curves shows an $I_Q$ ~ 4mA. A modest $I_Q/I_P$ (~1/5) is used. $I_{min}$ is set to about 1mA.
- Note that $I_{min}$ is not maintained when the amplifier is driven in saturation (Vi > +/- 40μV)
- Gate voltage plot reflects the non-linear control due to bias circuit

# Closed loop simulation with Gain=-10



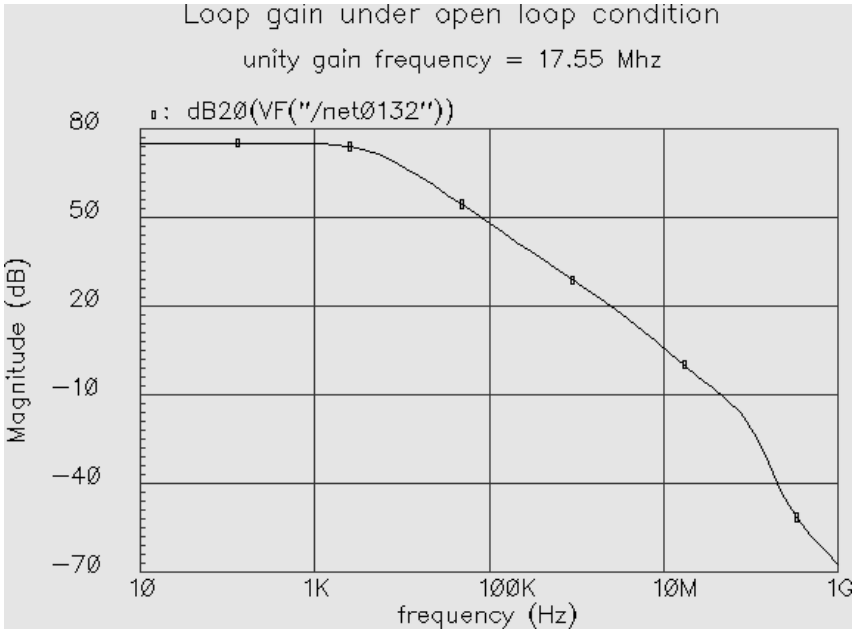



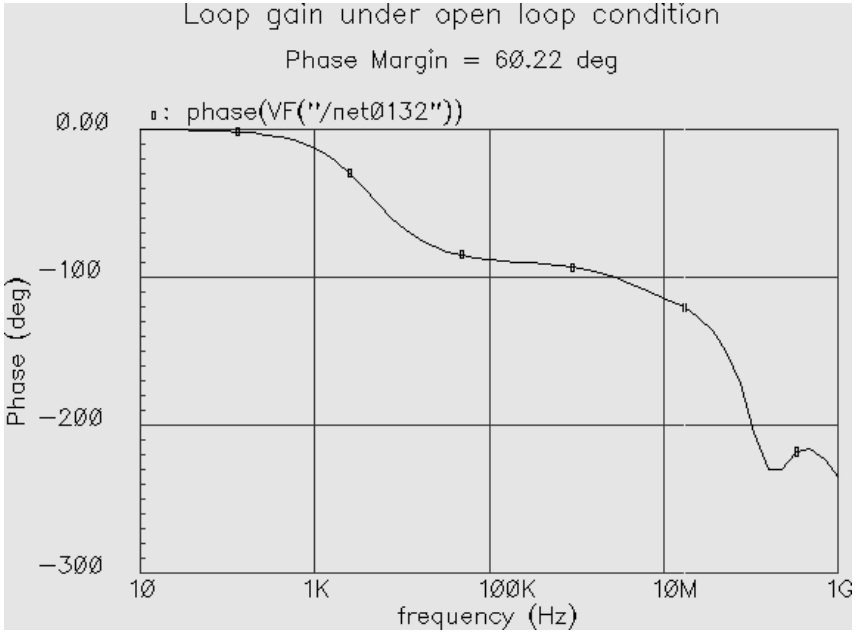

**Vo versus Vi**

**M1,2 current versus Vi**

- The current curves are linear with respect to Vi at high swing levels
- For small swings, the sum of currents of M1 and M2 is linear versus Vi

# Loop Gain AC response for Gain = -10

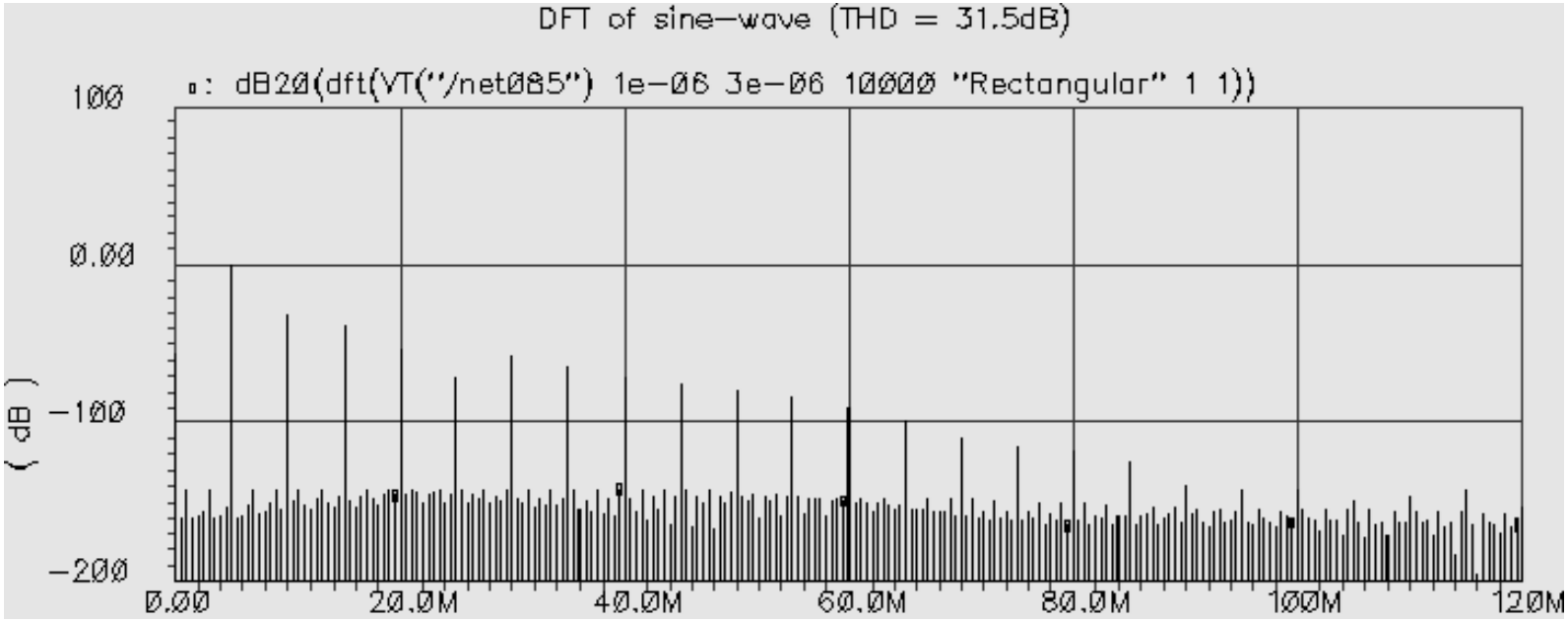



**AC response (inverting gain = 10)**

- Unity gain bandwidth ~ 17.6MHz (due to feedback factor of 1/10)
- Stability must be verified for entire output swing range
- Miller compensation around 2nd stage is employed (pole at the output of 3rd stage is neglected)
- In this example, the amplifier is treated as a 2 stage amplifier. However, more advanced compensation scheme is required for 3 stage designs

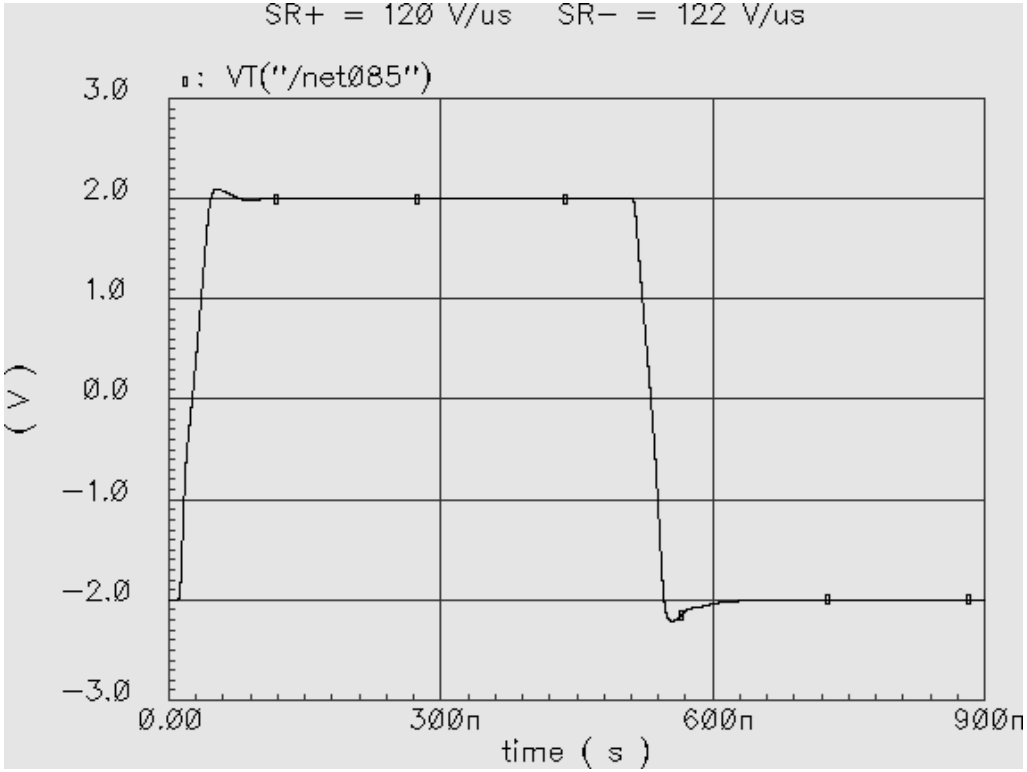
# Transient simulation result for Gain=-10 case




**Output spectrum for 1MHz +/-1V output**

- Second harmonic would be suppressed in a differential version of this amplifier
- Better linearity can also be achieved with higher GBW but requires more advanced compensation schemes (discussed later)

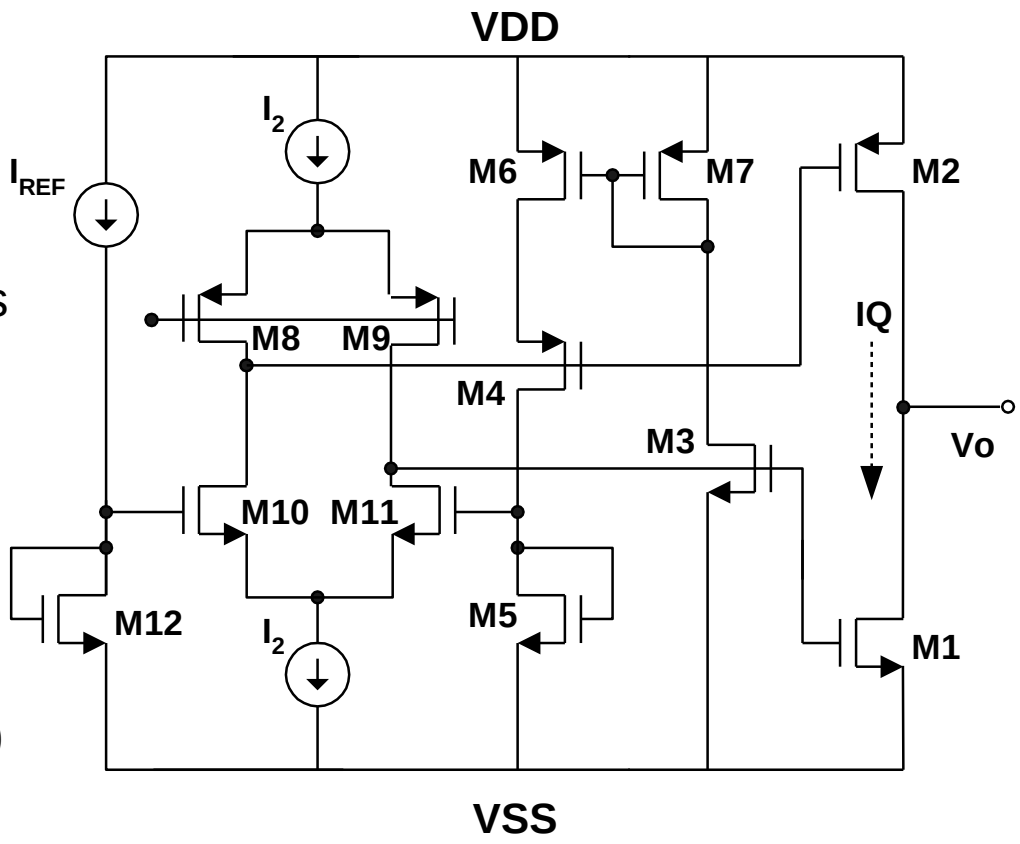
# Step Response




- “Split compensation network” is used in this amplifier. Rc and Cc is connected between gate of M9 and gates of M1 and M2
- This is to ensure symmetric slewing in either direction of swings
- Splitting the compensation network is also critical to maintain stability across entire swing range

# Low voltage Class-AB biasing

- Monticelli's biasing needs min supply of $2Vgs_{M7,8} + Vdsat_{Ib}$
  - Not favorable for low voltage designs in digital CMOS process
- "Folded mesh biasing"† can be used to alleviate this problem
- Min supply: $Vdsat_{M8,9} + Vdsat_{M10,11} + 2*Vdsat_{I2}$
- QTL: Vgs5+Vgs11 = Vgs12+Vgs10
- M3-M7 implements minimum selector circuit




Class-AB biasing scheme using folded mesh

† K. J. de Langen, J. H. Huijsing, "Compact low-voltage power-efficient operational amplifier cells for VLSI," *IEEE J. Solid-State Circuits*, vol. 33, no. 10, pp. 1482–1496, Oct. 1998.

# Operation of Folded Mesh Biasing

- Assume $(W/L)_5 = (W/L)_{12}$ and $(W/L)_6 = (W/L)_7$
- Amplifier consisting of M8-M11 serves to force $I_5 = I_{REF}$
- Quiescent state
  - M6 is in triode region. M4 and M6 together acts like a "composite transistor" with twice the length
  - IQ can be set using the following relation

$$I_5 = I_Q\left(\frac{1}{2}\frac{(W/L)_3}{(W/L)_1} + \frac{1}{2}\frac{(W/L)_4}{(W/L)_2}\right) = I_{REF}$$

- M1 is strongly conducting
  - M6 is in deep triode region, acting like a closed switch
  - M4 serves to mirror the current through M2

$$I_5 = I_{2\min}\left(\frac{(W/L)_4}{(W/L)_2}\right) = I_{REF}$$

- M2 is strongly conducting
  - M4 acts like a cascode device
  - M3,6,7 serves to mirror the current through M1

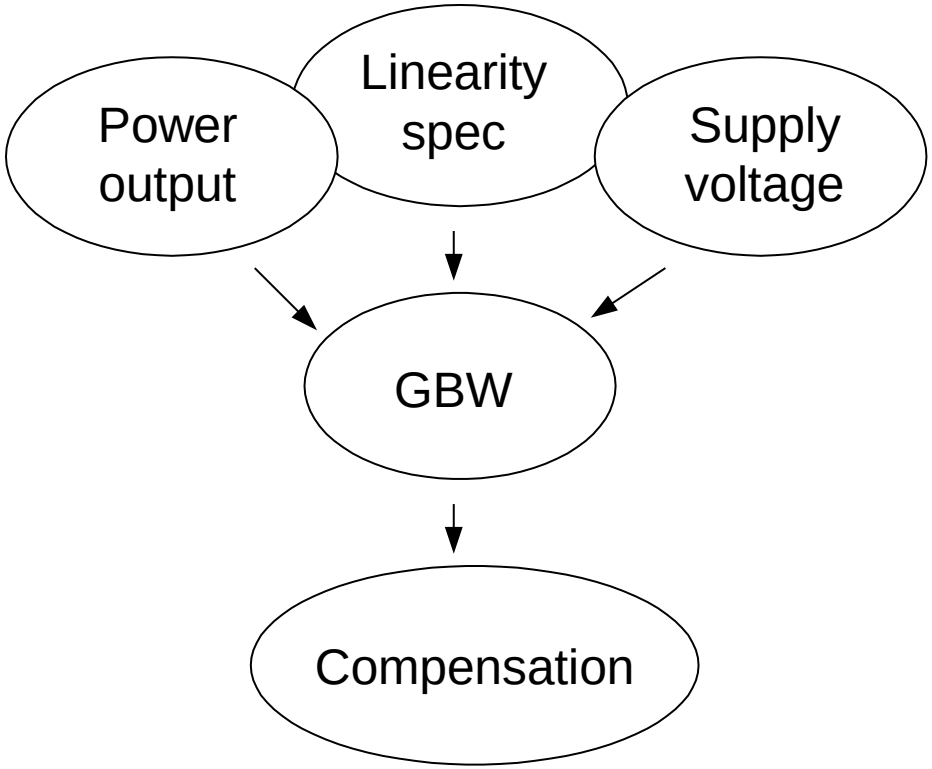
$$I_5 = I_{1\min}\left(\frac{(W/L)_3}{(W/L)_1}\right) = I_{REF}$$

# COMPENSATION OF CLASS-AB DRIVERS

- Piece-wise modeling of class-AB stage
- NMC driver design example

# Compensation of Class-AB drivers

- As mentioned earlier, GBW and the linearity of the output stage determines the overall closed loop linearity of the driver
- Since GBW is a major factor in determining stability, we need to analyze the linearity of class-AB stage more closely
- Due to large power delivery and swing requirements, it is desirable to have the class-AB stage swing near rail-rail
- Rail–rail output swing is a major cause of distortion and will be investigated in next few slides



# Piece-wise model for class-AB V-I curve

- Three distinct operating regions
  - Region1 - Linear versus Vin
  - Region2 - Square law versus Vin
  - Region3 - Parabolic versus Vin
- Region 1 and 2 were discussed already
- When the strongly conducting device enter triode region, the third regime of operation (parabolic vs Vin) comes into play

- Region1 $\mathbf{I_O = 4KVinVx}$
- Region2 $\mathbf{I_O = K * sign(Vin) * \left(|Vin| + Vx\right)^2}$
- Region3 $I_O$ is the solution of the following quadratic equation

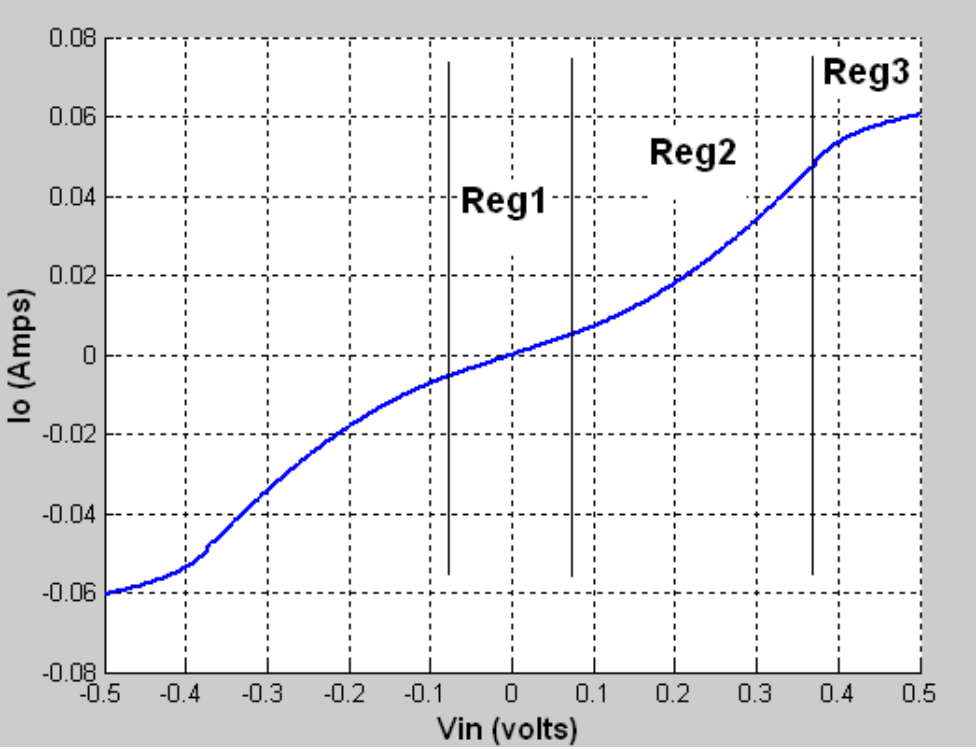
$$\mathbf{I_O^2 R_L^2 K + I_O\left(1 + 2K\left(|Vin| + Vx\right)R_L - 2KV_{SUP}R_L\right) + KV_{SUP}^2/4 - K\left(|Vin| + Vx\right)V_{SUP} = 0}$$

where $V_{SUP} = V_{DD}-V_{SS}$, $K=1/2*Kp*W/L$, $R_L$ is load resistance, Vin and Vx are as already defined

*Exercise :– Derive the above V-I relation for Region 3 and specify the range of Vin for which it is valid*

# Inferences from the piece-wise model

- Large gate voltages might be required to supply current when the output stage is in region3
- The distortion due to region3 is typically the limiting factor
- On the other hand, restriction of operation to region1 and 2 might imply extremely wide output transistors, which could in turn pose compensation problems
- GBW is determined based on gain required to “linearize” the distortion components due to this
- Often times, IQ required for compensation (given this GBW) is sufficient to check cross-over distortion

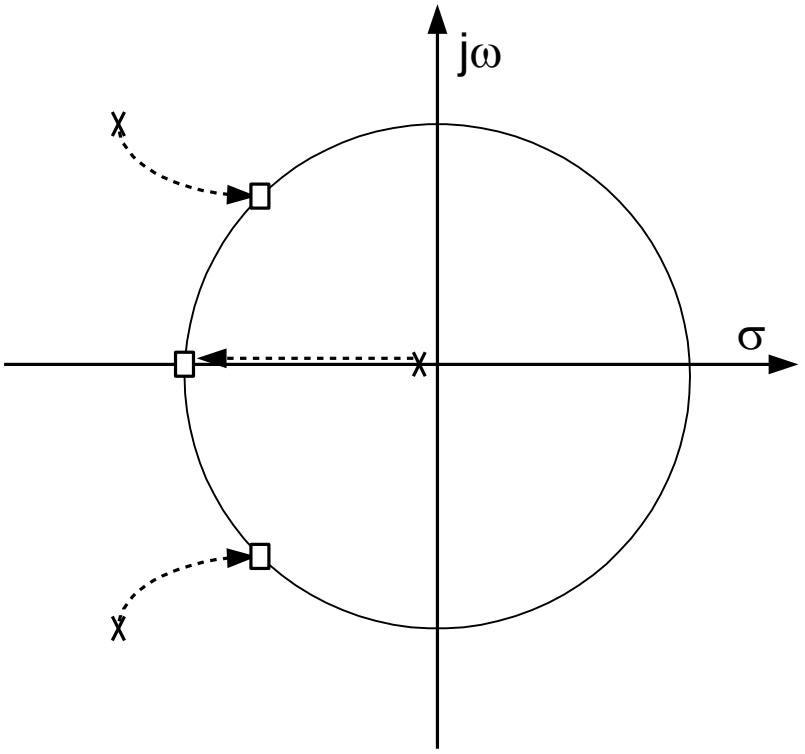



Matlab plot of an example piece-wise model

• MATLAB ‘Polyfit’ function indicates that co-eff of up to 9$^{th}$ order term is significant

# 3-stage driver and NMC compensation

- Nested Miller Compensation (NMC)† is widely used for 3-stage amplifiers owing to its simplicity
- The basic idea is to consider a two-stage Miller compensated amplifier as a composite transistor and use it within another two-stage Miller amplifier
- Design equations given in † are designed to yield a Butterworth (maximally flat) transfer function when the amplifier is used in closed loop condition



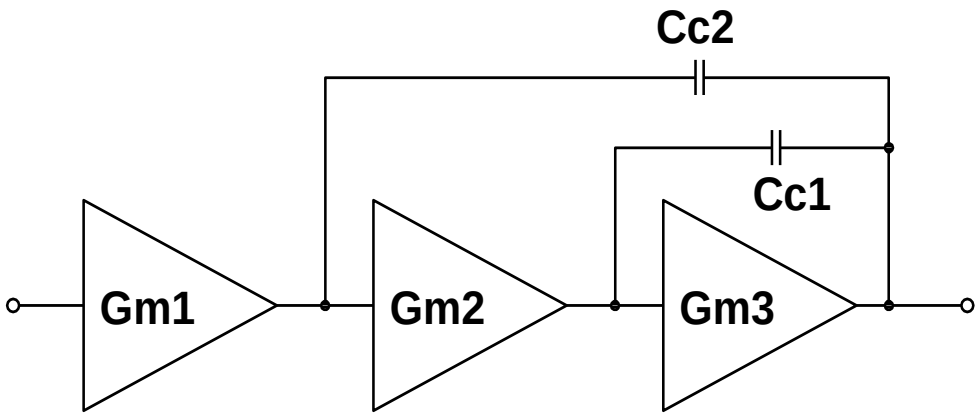

x - Open loop poles

□ - Closed loop poles

† R.G.H Eschauzier, J.H.Huijsing, “Frequency compensation techniques for low-power operational amplifiers,” Kluwer, Netherlands, 1997

# Design Example – 16Ω headset driver

- Specifications
  - Output swing = +/- 1V (2Vpp)
  - Supply voltage = 2.5V
  - THD (1KHz, 2Vpp) > 90dB
  - SNR > 90dB
  - Power < 2.5mW
  - Technology = 0.25μm
  - Load 16Ω || 100pF



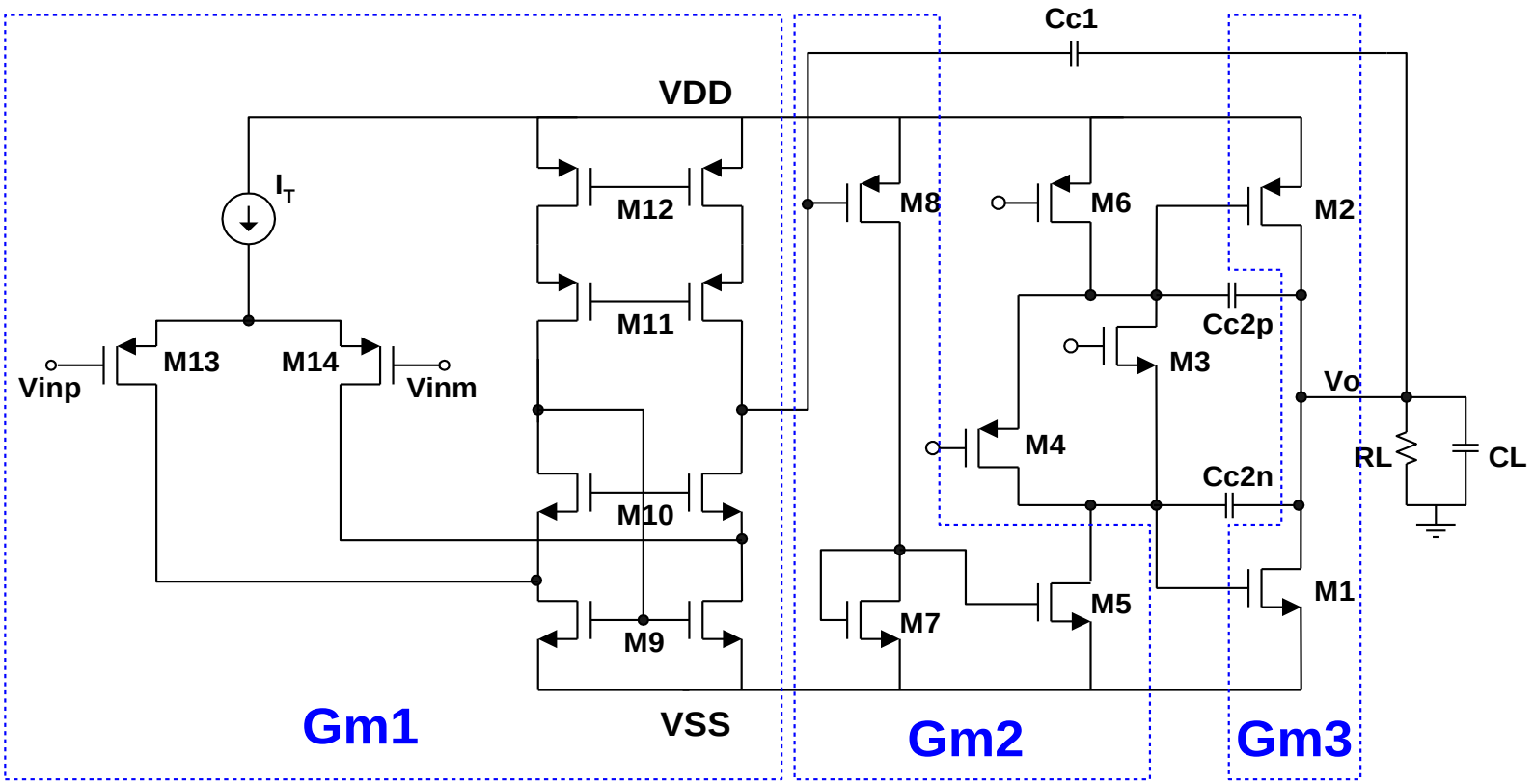

- Design Procedure
  1. Start with designing the class-AB output stage
  2. Size the output transistor so that +/-1V swing is achieved (while 16Ω load is present) without excessive gate swing (~$V_{DD}$/2)
  3. Use ideal gain stage and simulate the output stage in closed loop
  4. Find the required GBW to meet THD spec (using above simulation)

# Design Procedure

continued…

5. For the chosen $I_Q$, check if Gm3/CL is about 4*GBW
6. If not, readjust $I_Q$ and repeat above steps
7. Choose Cc1 (and Gm1) based on SNR spec and GBW determined is previous steps
8. Verify if $I_T$/Cc1 is greater than the slew rate required by Full-power bandwidth (20KHz in this case)
9. Make sure the 1st stage has enough DC gain (most of the gain comes from this stage)
10. Split Cc2 into two pieces to be placed around NMOS (Cc2n) and PMOS (Cc2p) output transistors
11. Choose Cc2p(n) to be about 5-10 times the gate capacitance of the PMOS(NMOS) output device
12. Fix Gm2 such that Gm2/(Cc2n+Cc2p) ~ 2*GBW
13. If required, increase the length (and width to keep W/L) of transistors to check flicker noise and mismatch variations

# Headset Driver – Circuit Diagram

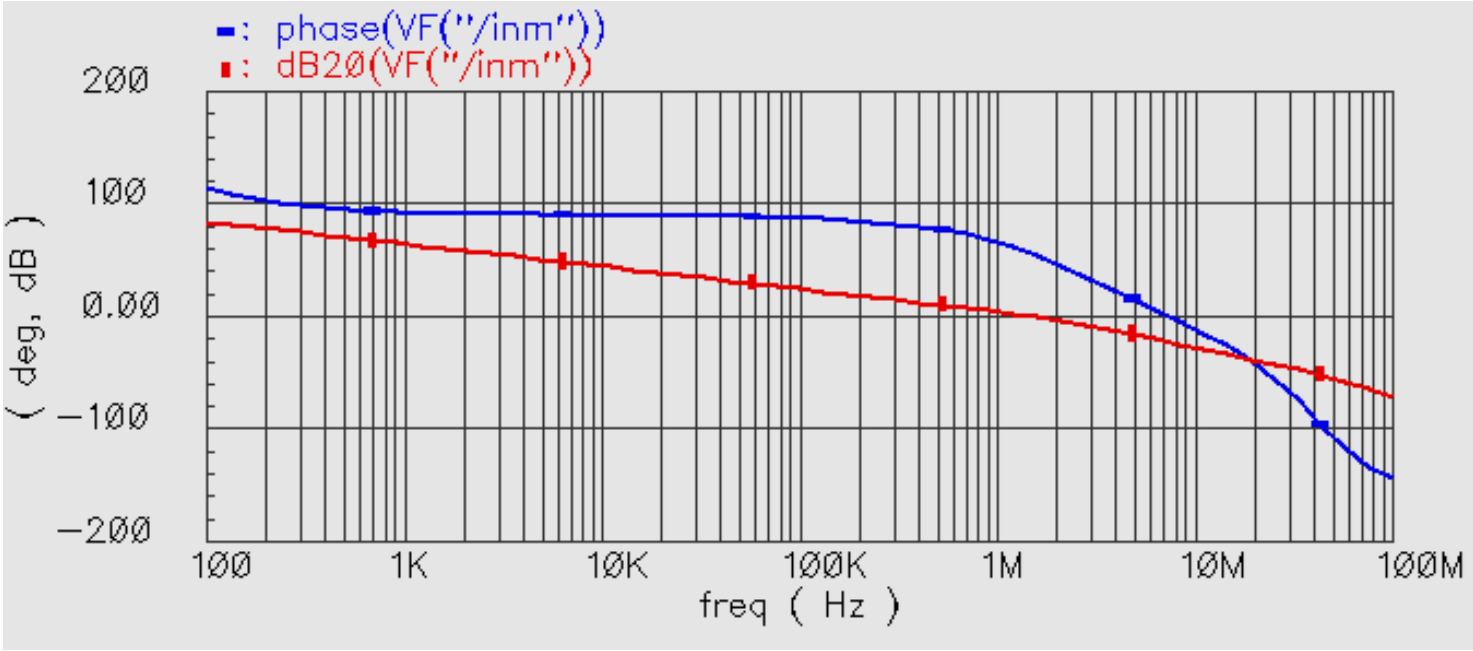



| M1 | 32 x (20/0.24) |
|---|---|
| M2 | 96 x (18/0.24) |
| M3 | 12 x (2.5/0.8) |
| M4 | 12 x (7.5/0.8) |
| M5 | 20 x (2.0/0.5) |
| M6 | 20 x (6/0.4) |

| M7 | 6 x (2.0/0.5) |
|---|---|
| M8 | 6 x (6/0.4) |
| M9 | 6 x (24/6.0) |
| M10 | 3 x (7/1.2) |
| M11 | 6 x (10.5/1.2) |
| M12 | 6 x (22.5/3.0) |

| M13,14 | 6 x (20/1.2) |
|---|---|
| RL | 16Ω |
| CL | 100pF |
| Cc1 | 16pF |
| Cc2p | 13.5pF |
| Cc2n | 5pF |

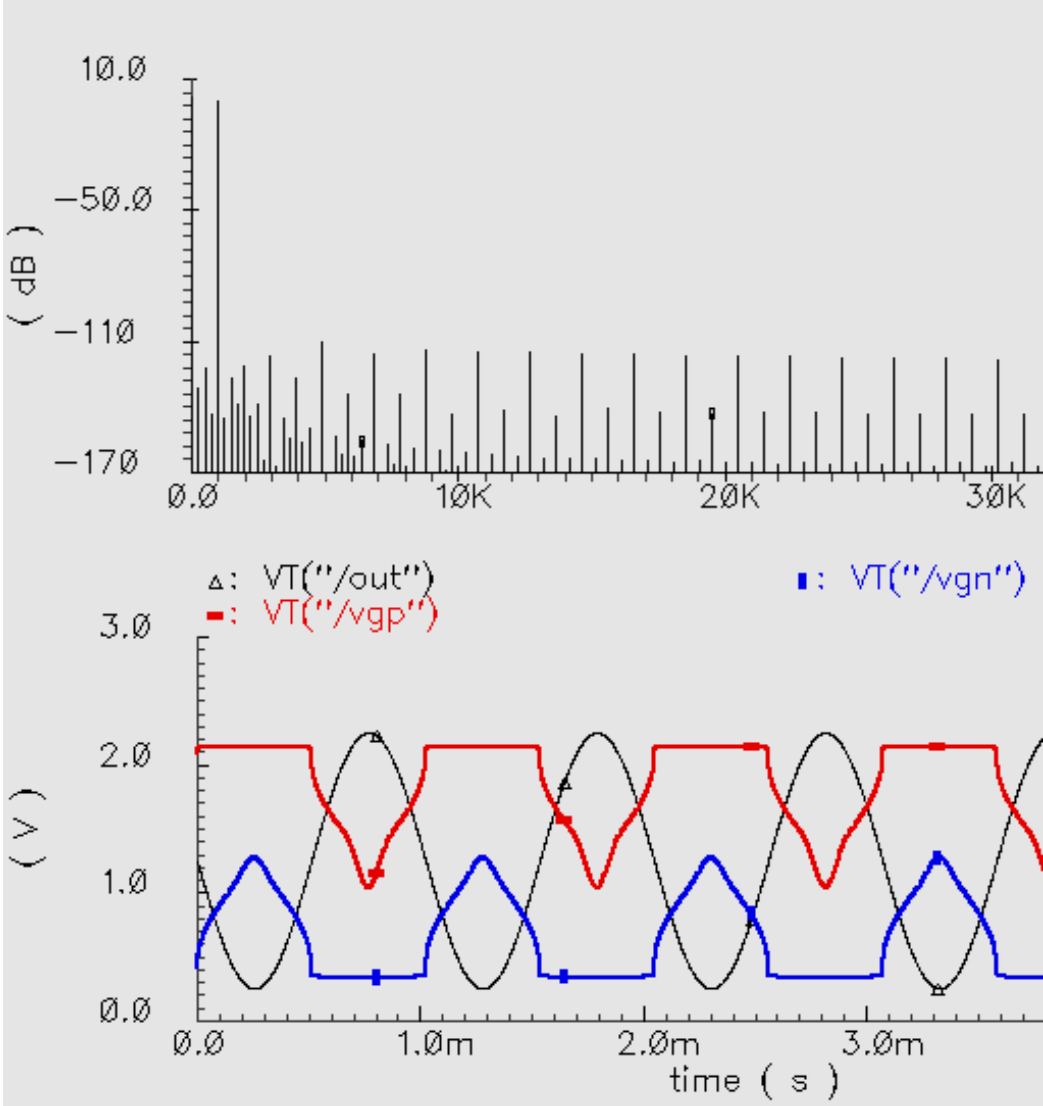
# Simulation Results




- AC Response displays a phase margin on 56° for GBW = 1.4MHz
- Large DC gain ~85dB is achieved (even with 16Ω load)
- A total supply current of 850uA is used
- Compensation capacitances and supply current can be further reduced by moving to more advanced compensation schemes

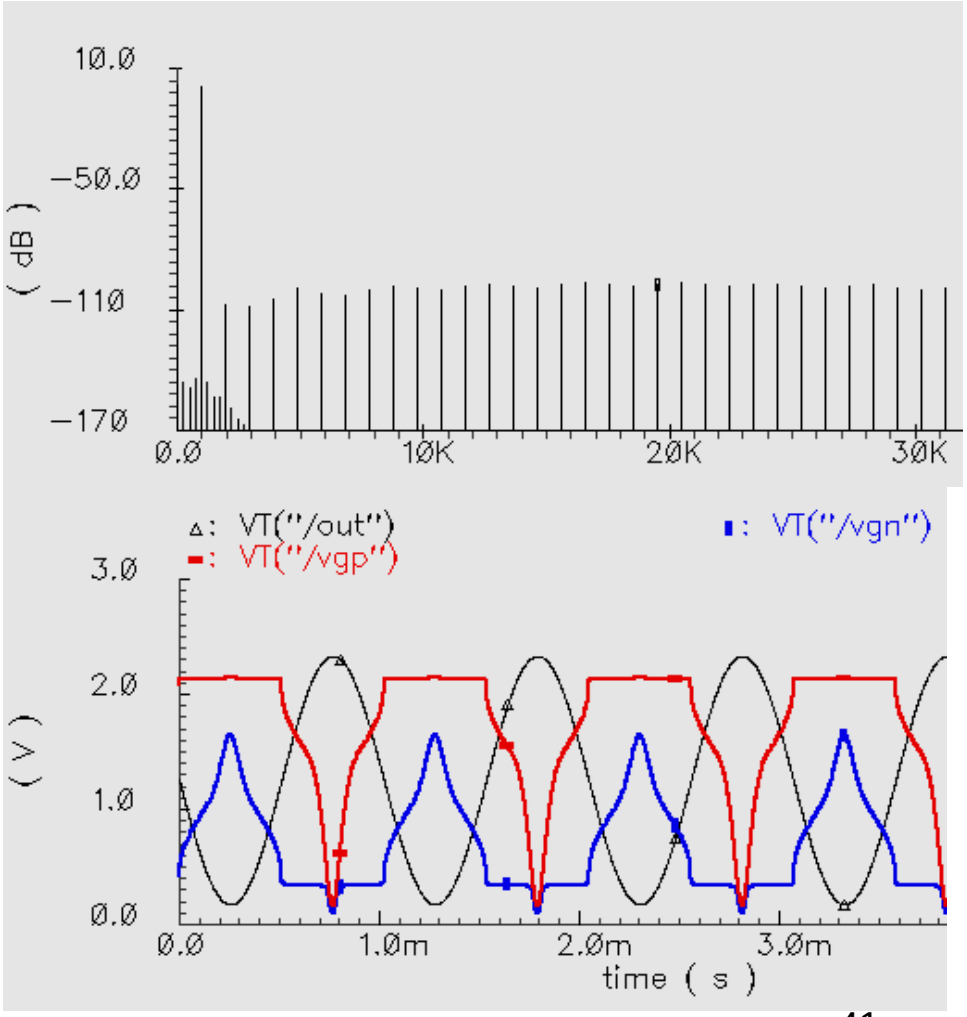
# Transient Simulation

- 1KHz 2Vpp sine-wave is used as the test signal
- The FFT shows a THD of 105dB
- Strong presence of higher order harmonics is a reflection of region3 operation
- Output waveform along with gate voltage swings at PMOS gate (red curve) and NMOS gate (blue curve) of Class-AB stage are shown
- It can be seen that the feedback is driving the gate hard to get the output swing to peak

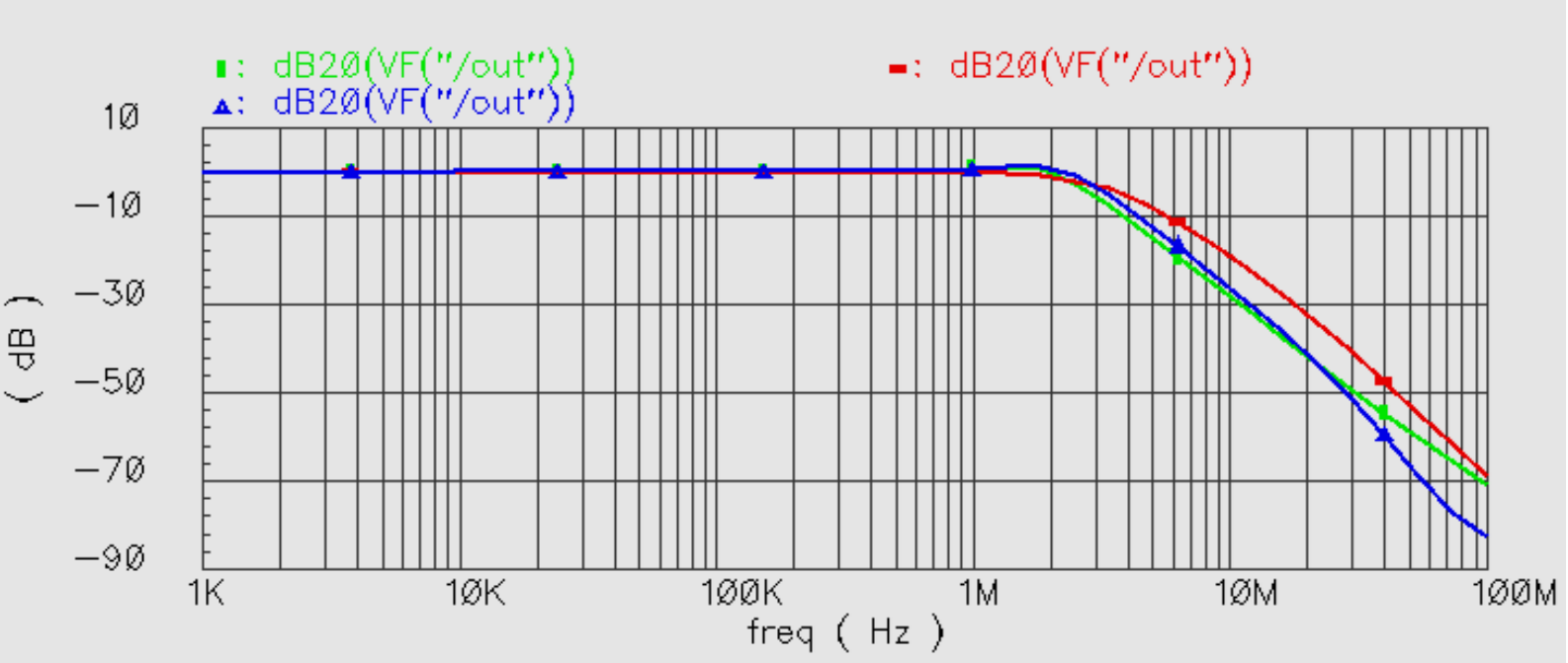


# What happens if the output voltage swing is increased to 2.2Vpp ?

- Distortion level increases significantly (THD = 86dB) due to operation in deep triode region
- Gate swings display some asymmetry in sizing (little smaller PMOS) but maybe a reasonable trade-off for parasitic capacitance
- Typically, systems let this happen at the highest level of volume setting



# Closed loop AC response of the amplifier




- Since Gms are designed for quiescent condition, the closed loop curve under this condition (green curve) is closed to Butterworth response
- When output swings, Gm3 varies from quiescent value, which results in deviation from green curve
- The red (blue) curve display variation in Q and frequency of the non-dominant pole pair when output swings close to VDD (VSS)

# Noise simulation

| Device | Param | Noise Contribution | % Of Total |
|---|---|---|---|
| /NM6 | fn | 9.65217e-06 | 22.77 |
| /NM7 | fn | 9.65119e-06 | 22.77 |
| /PM8 | fn | 8.47373e-06 | 17.55 |
| /PM9 | fn | 8.47373e-06 | 17.55 |
| /PM7 | fn | 3.69314e-06 | 3.33 |
| /PM6 | fn | 3.68917e-06 | 3.33 |
| /R26 | rn | 2.75181e-06 | 1.85 |
| /R25 | rn | 2.75181e-06 | 1.85 |
| /R27 | rn | 2.7518e-06 | 1.85 |
| /R28 | rn | 2.7518e-06 | 1.85 |
| /NM7 | id | 2.21069e-06 | 1.19 |
| /NM6 | id | 2.21008e-06 | 1.19 |

Integrated Noise Summary (in V) Sorted By Noise Contributors
Total Output Noise = 2.02263e-05
Total Input Referred Noise = 1.01134e-05
The above noise summary info is for noise data

Flicker noise is a dominant contributor which can be reduced further by using longer transistors. However, the additional parasites pose compensation issues

# PRACTICAL ISSUES

- Mismatch effects, Load variation, Effect of parasitic resistance, Process and temperature variation

# Mismatch Effects

- Mismatch due to “small” bias arms
  - Consider transistor M1 and M5 in Monticelli’s bias circuit (slide 15)
  - From QTL, we get $Vgs_{M1} = Vgs_{M5}$ and from ratios of W/L we further infer that current densities (I/(W/L)) of M1 and M5 are same
  - It is not uncommon to scale down the bias arms to $1/100^{th}$ - $1/20^{th}$ of the signal arms
  - Although using small bias currents may save supply current under nominal condition, this could result in large current variation when mismatch is taken into account

$$\frac{\mathbf{I}_5}{\left(\frac{\mathbf{W}}{\mathbf{L}}\right)_5} = \beta\left(\mathbf{Vgs}_{\mathbf{M5}} - \mathbf{V}_{\mathbf{T}}\right)^2 \qquad \frac{\mathbf{I}_1}{\left(\frac{\mathbf{W}}{\mathbf{L}}\right)_1} = \beta\left(\mathbf{Vgs}_{\mathbf{M5}} - \mathbf{V}_{\mathbf{T}} + \Delta\mathbf{V}_{\mathbf{T}}\right)^2$$

  - If $Vgs_{M5}$ is 100mV and $\Delta V_T$ is 10mV, where $\Delta V_T$ is the difference in threshold voltage between M5 and M1, the current density of M1 can be higher than that of M5 by 21%

# Mismatch Effects …continued

- The mismatch in current density is more pronounced when M1/M5 is biased in sub-threshold region (due to exponential V-I characteristics)
- To alleviate this problem, focus on the small devices (don't make the small devices too small)
- Spending some additional current in bias circuits will make the amplifier more robust to mismatches (you will have more working chips in the end of the day)

- DIBL induced mismatch effect
  - M3 and M6 in the same circuit (slide 15) has different drain voltages
  - Due to DIBL (Drain Induced Barrier Lowering) M3 and M6 usually have different (M3 has less) $V_T$, which QTL fails to capture
  - The circuit in slide 35 uses transistors more than 3x longer than minimum length for M3 and M4 (and their corresponding floating mirror transistors) to alleviate this effect

# Load Variation

- Gm of output stage (GmL) strongly depends on output current
- With swing, GmL varies by a factor $\sqrt{(I_p/I_Q)}$ - about 3 to 10 for many applications
- Hence the Q (or Damping factor) of non-dominant poles varies with swing
- This phenomenon already changes the closed loop amplifier response. Having load variation makes matters worse
- Since drivers handle external loads, users could change the load conditions and stability must be ensured for wide load ranges
- What if the capacitive load is reduced from 100pF to 10pF in previous example?
- Fortunately, an NMC compensated amplifier designed for 100pF can handle smaller capacitive loads without much trouble but this is not true for all schemes

***Exercise :– Assume that an NMC amplifier is designed to have Butterworth response under closed loop condition. Find out the new response (pole locations) and phase margin if the load capacitance is dropped to 1/10th the original value***

# Effect of Parasitic Resistance

- Since many drivers are integrated in Baseband ICs, there may be a significant routing resistance (100-500mΩ) from the supply pins to the actual layout of the driver in the chip
- This is also the case with output pins
- These parasitic resistances “eat away” the headroom of driver transistors and make them enter region3 sooner than we think
- This leads to unexpectedly large distortion after the layout
- In case of output pins, this resistance leads to gain error
- Solution:
  - Use wide metal lines (as much as area constraint allows) and augment multiple metal layers to minimize resistance
  - Over-design the transistor sizes or alternately design them with an estimate of these resistances included in the schematics
  - Start the feedback routing from as close to bond pad as possible and simulate with this additional resistance in the loop

# Process and temperature variation

- As with any amplifier, always perform digital corner simulations (Strong/weak/hot/cold) right from the first cut design
- Pay more attention to the Class-AB stage since it is more vulnerable to these variations
- Hot temperature typically reduces $V_T$ while strong corner improves mobility
- Watch out for strong-hot combination that kills the headroom available for the stage that drives the output stage (M5 and M6 in circuit in slide 35)
- Weak-hot combination results in poor transconductance that could lead to poor distortion performance and phase margin
- Check for headroom problems in weak-cold corner (especially if Monticelli's biasing is used