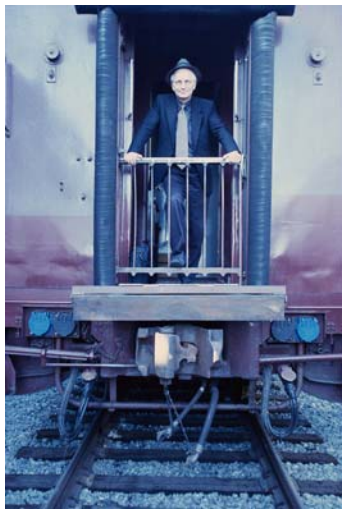
RAIL-to-RAIL OP AMPS



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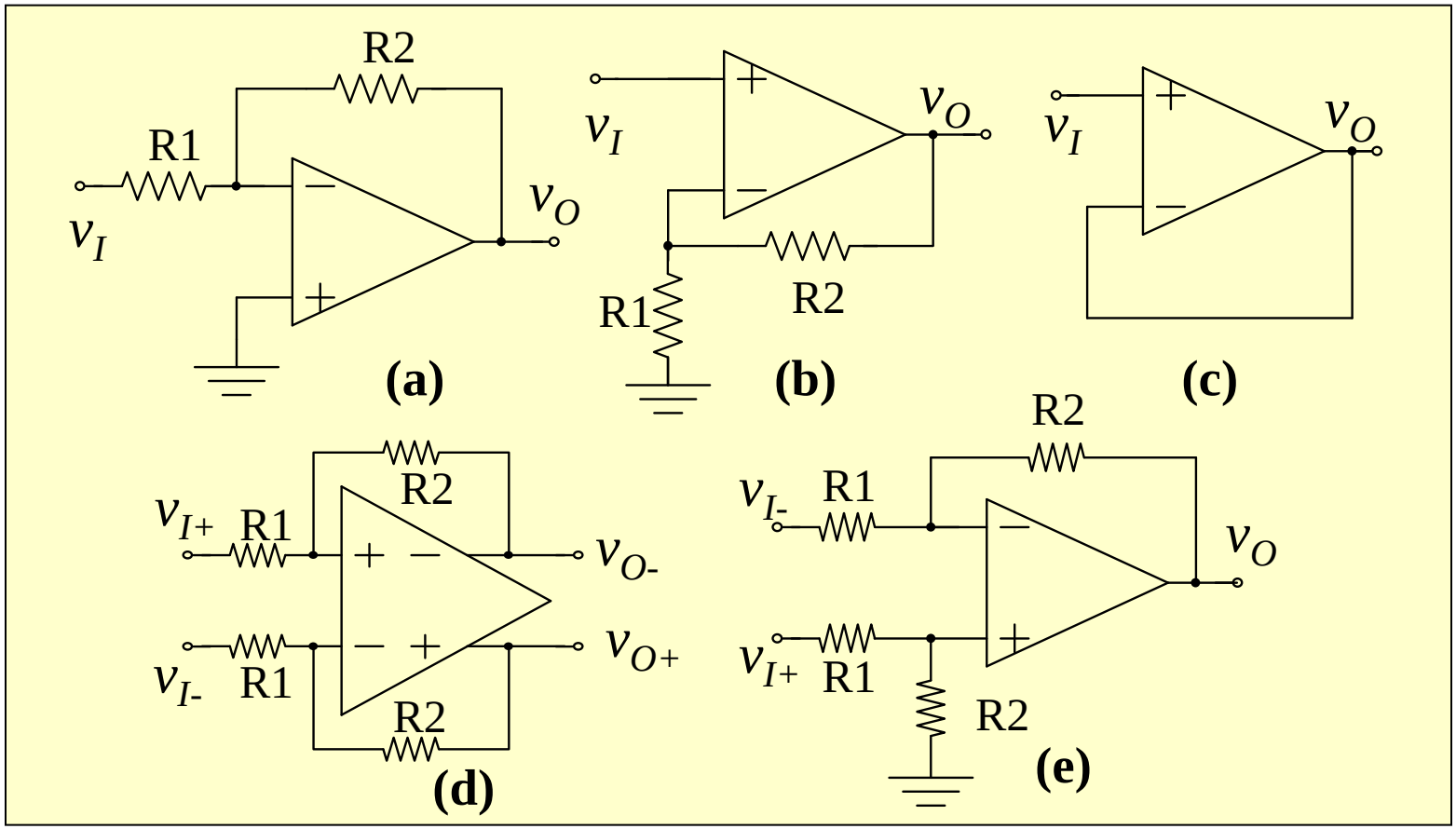
Thanks to Dr. Shouli Yan for his valuable input in helping in generating part of this material

Op Amp Configurations

(a) Inverting configuration, (b) Non-inverting configuration, (c) Voltage follower (or voltage buffer, a special case of (b)), (d) Fully-differential configuration, (e) Fully-differential to single-ended conversion



Why Rail-to-Rail Differential Input Stage?

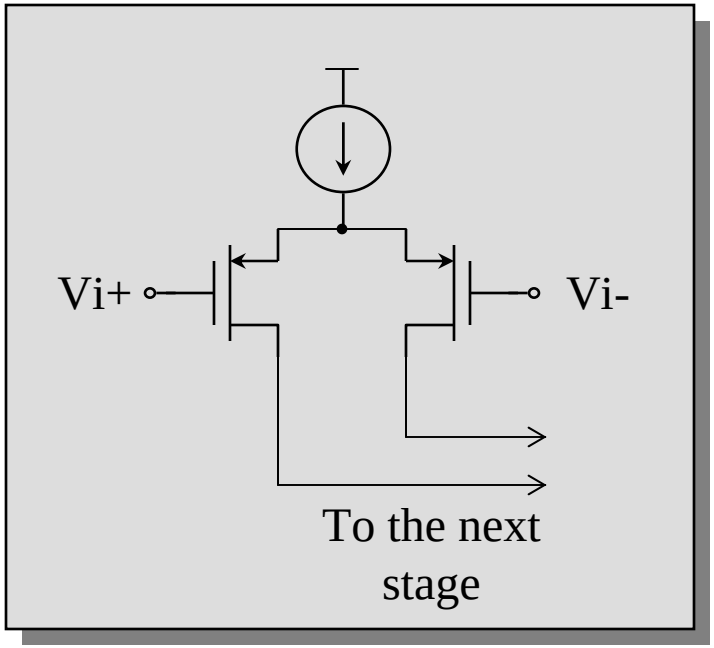
- The input and output swing requirements

Configuration	Figure	Input common mode voltage swing	Output voltage swing
Inverting	(a)	≈0	Rail-to-rail
Non-inverting	(b)	$R1/(R1+R2) * V_{SUP}$	
Voltage follower	(c)	Rail-to-rail	
Fully Differential	(d)	$R2/(R1+R2)*V_{I,CM}$	
FD to SE	(e)	$R2/(R1+R2)* V_{I+}$	

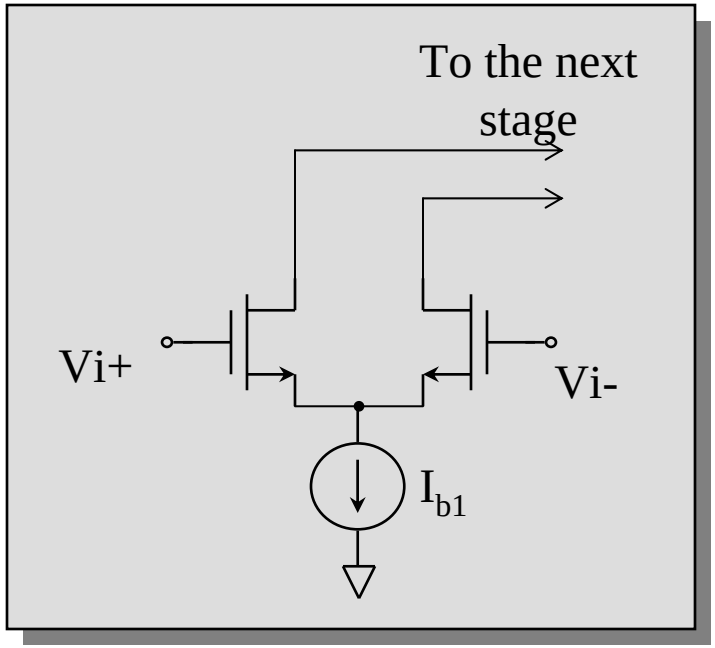
- From the above table, we see that for the inverting configuration, rail-to-rail input common mode range is not needed. But for all other configurations, there is a common mode voltage swing required. In particular for a voltage follower which usually works as an output buffer, **rail-to-rail** input common mode voltage range is required! To make an Op Amp work under any feedback condition, a differential input with **rail-to-rail** common mode range is very much needed.

How to Obtain a Rail-to-Rail Input Common Mode Range?

- The input stage of an op amp typically consists of a differential pair. There are two variations of differential pairs.



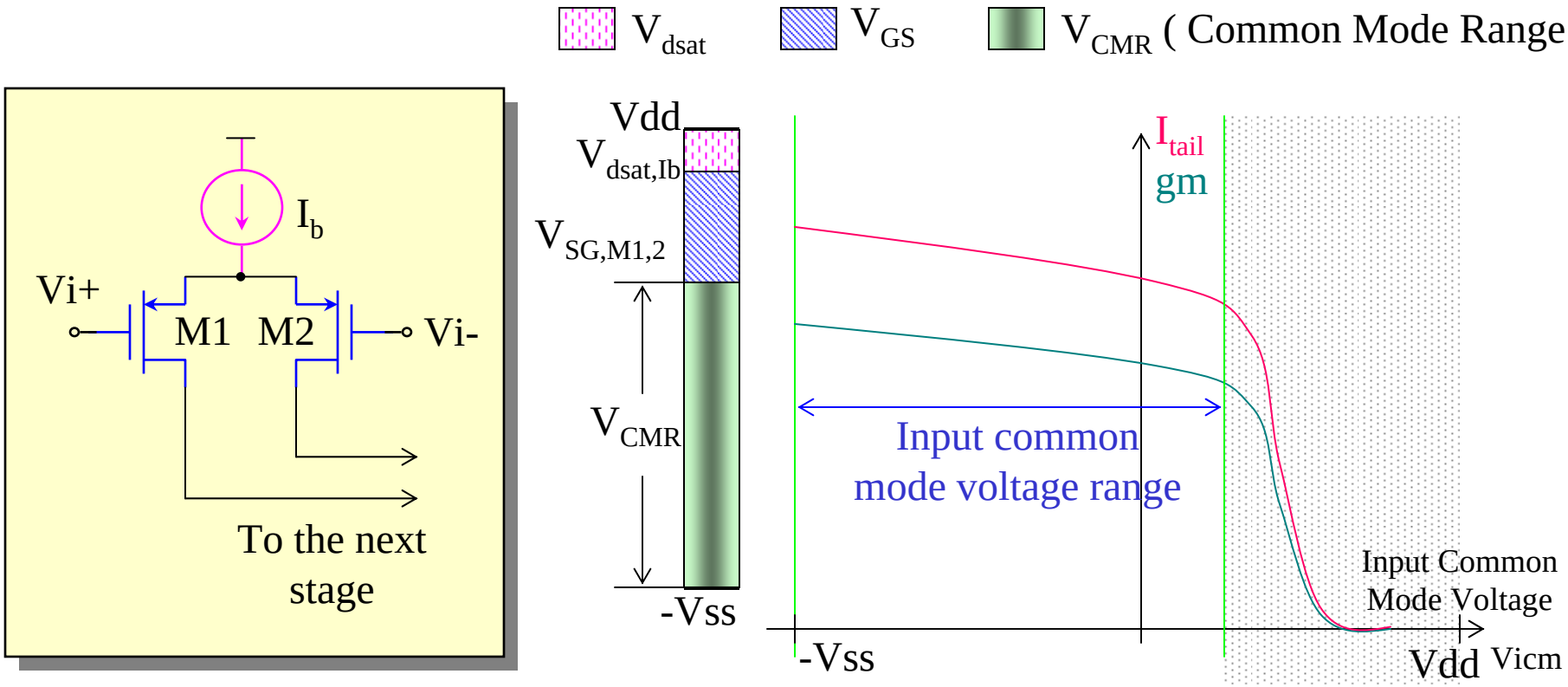
(a) P-type differential input stage



(b) N-type differential input stage

How to Obtain a Rail-to-Rail Input Common Mode Range? (cont'd)

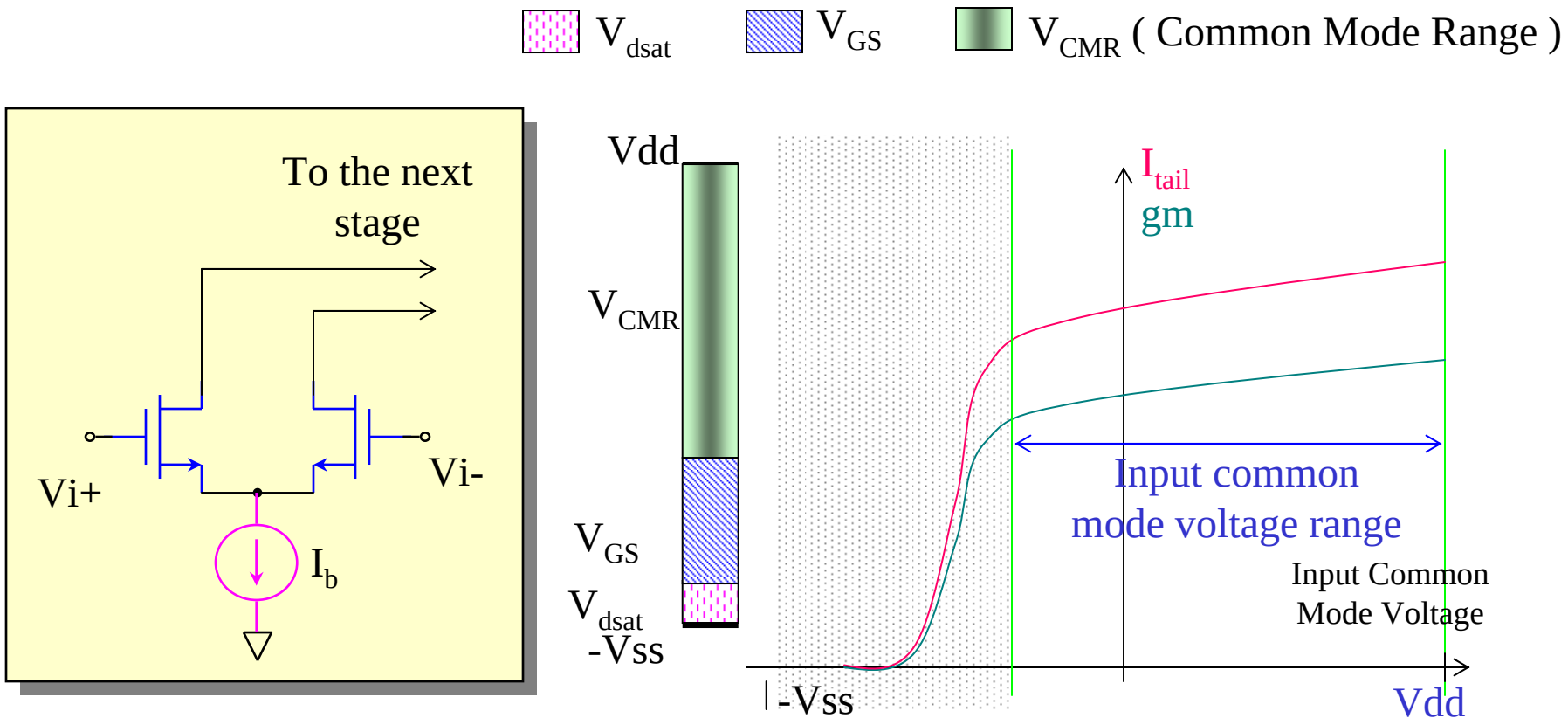
- First, let us observe how a PMOS differential pair works with different input common mode voltage
  - P-type input differential pair



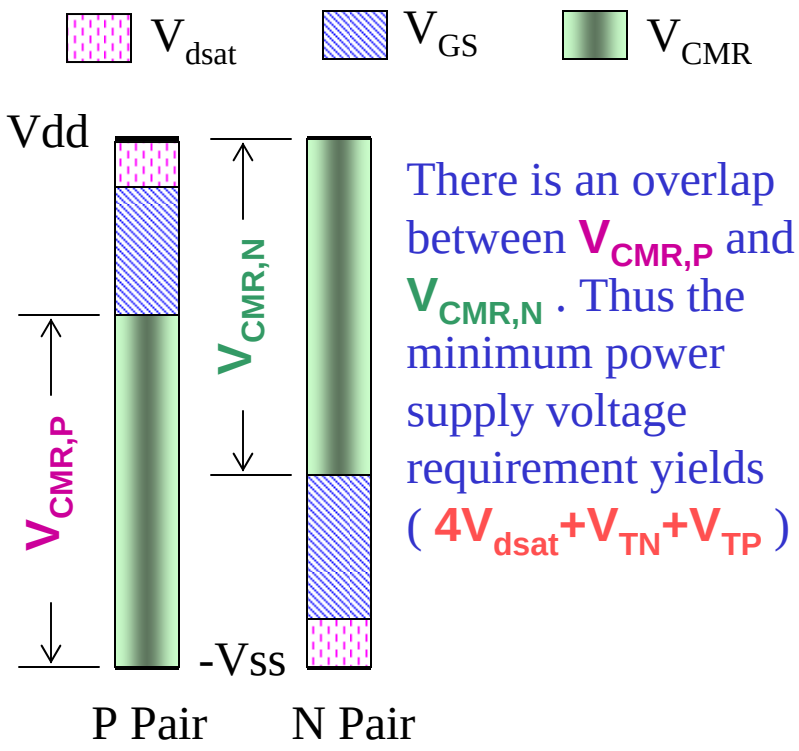
Where $V_{SG}=V_{dsat}+V_T$

How to Obtain a Rail-to-Rail Input Common Mode Range?

– N-type differential input stage

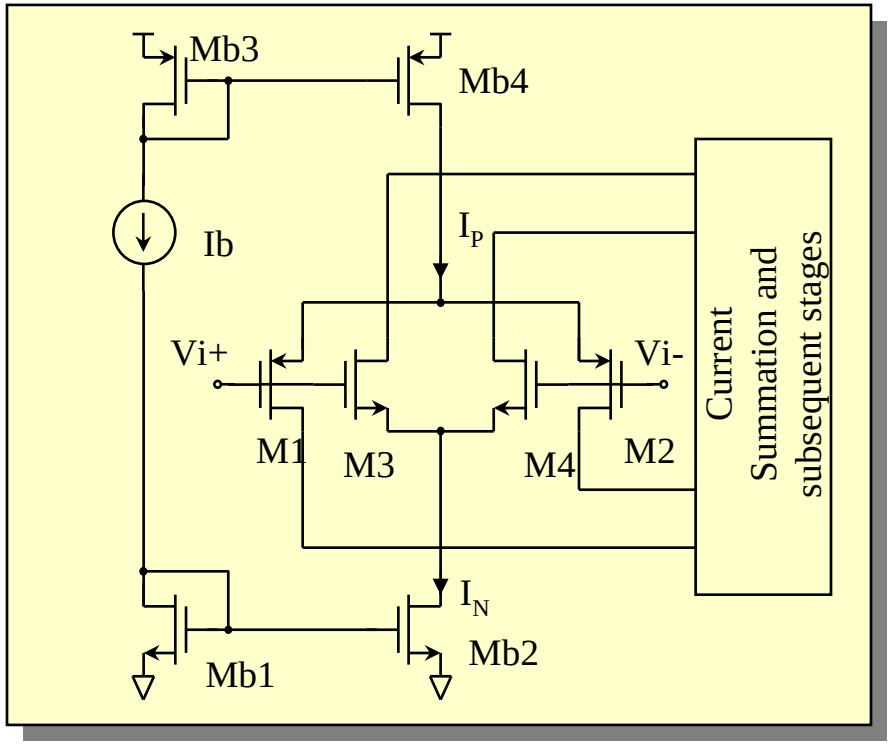


By combining a PMOS and a NMOS Differential pairs a Rail-to-Rail Input Common Mode Range can be implemented



There is an overlap between $V_{CMR,P}$ and $V_{CMR,N}$. Thus the minimum power supply voltage requirement yields ($4V_{dsat}+V_{TN}+V_{TP}$)

$V_{SUP} \geq 4V_{dsat}+V_{TN}+V_{TP}$

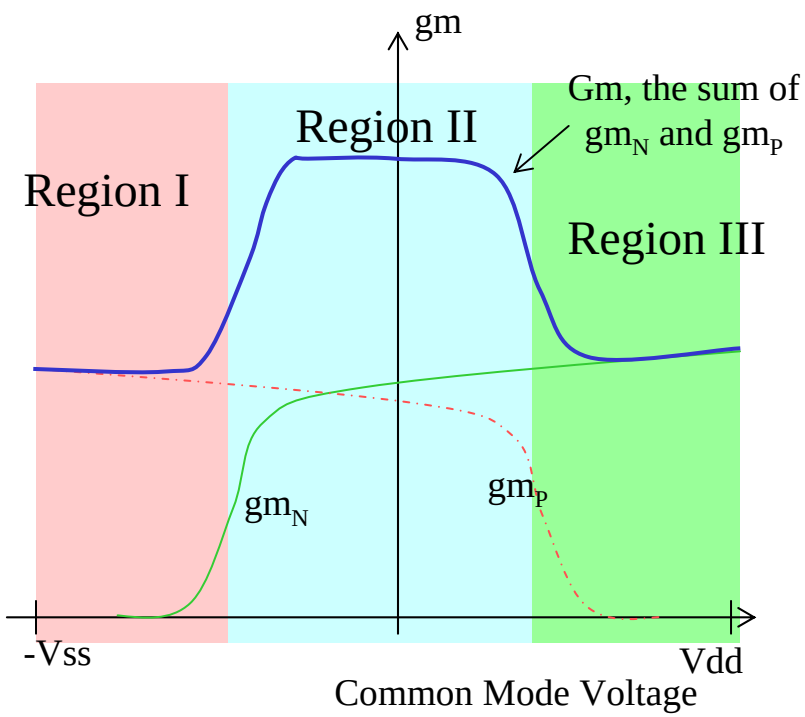


Simple N-P complementary input stage

Almost all of the rail-to-rail input stages are doing in this way by some variations! But how well does it work?

How to Obtain a Rail-to-Rail Input Common Mode Range? (cont'd)

- Transconductance vs. Vicm



The total transconductance of the input stage varies from gm to 2gm, the variation is **100%** !

- If $K = \frac{1}{2} KP_N (\frac{W}{L})_N = \frac{1}{2} KP_P (\frac{W}{L})_P$ and

  $I_N = I_P = I_{TAIL}$

  then $gm_N = gm_P = gm = \sqrt{2KI_{TAIL}}$.

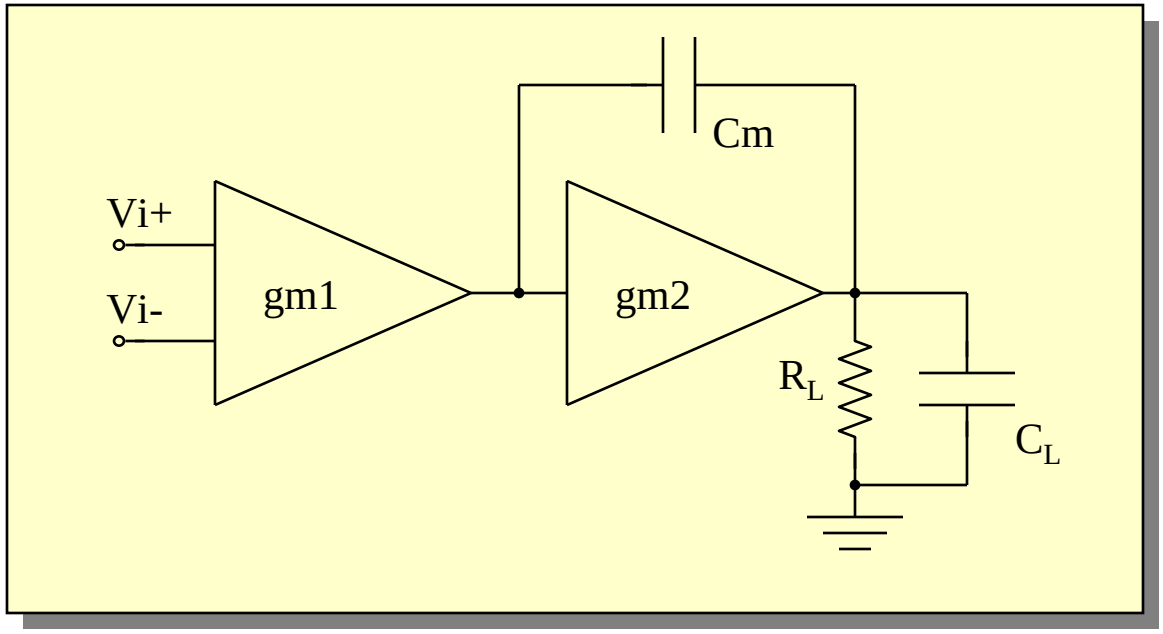
Region I. When Vicm is close to the negative rail, only P-channel pair operates.The N channel pair is off because its V_{GS} is less than V_T. The total transconductance of the differential pair is given by $gm_T = gm_P = gm$.

Region II. When Vicm is in the middle range, both of the P and N pairs operate. The total transconductance is given by $gm_T = gm_N + gm_P = 2gm$.

Region III. When Vicm is close to the positive rail, only N-channel pair operates. The total transconductance is given by $gm_T = gm_N = gm$.

Why is a Constant Gm needed ?

- The total transconductance, g_{mT}, of the input stage shown in the previous slide varies as much as twice for the common mode range!
- For an operational amplifier, constant transconductance of the input stage is very important for the functionality of the amplifier.
- As an example, we will analyze a simple two-stage CMOS operational amplifier. The conceptual model of the amplifier is shown below.



Why is a Constant Gm needed ? (cont'd)

- The transfer function of the amplifier is given by

$$A(s) \approx \frac{g_{m1}g_{m2}(1 - s\frac{C_m}{g_{m2}})}{s^2 C_L C_m + sC_m g_{m2} + g_{o1}g_L} = A_0 \frac{1 - s\frac{1}{z}}{s^2 \frac{1}{p_1 p_2} + s\frac{1}{p_1} + 1}$$

where $A_0 = \frac{g_{m1}g_{m2}}{g_{o1}g_L}$, which is the DC gain of the amplifier.

$p_1 = \frac{GBW}{A_0} = \frac{g_{m1}/C_m}{A_0}$, $p_2 = \frac{g_{m2}}{C_L}$, and $z = \frac{g_{m2}}{C_m}$,

p_1 and p_2 are the dominant pole and non-dominant pole of the amplifier respectively, and $p_1 << p_2$.

z is the zero generated by the direct high frequency path through C_m.

Why Should We Have a Constant Gm (cont'd)

GBW is the Gain Bandwidth product, or the unity gain frequency of the amplifier, which is given by

$$GBW = \frac{g_{m1}}{C_m}.$$

We may notice that *GBW* changes with g_{m1}! If g_{m1} changes 2 times, the *GBW* also does so!

- To ensure the stability of the amplifier, we should maintain a sufficient phase margin. Usually, we let p_2 to be 2.5 times of GBW. Let's assume $C_m=C_L/2$, then $z=2p_2=5\times GBW$.

- If the total transconductance of the input stage, g_{m1}, varies 2 times as we have encountered in previous discussion, from *gm* to *2gm*, let us check how the stability is affected.

Why is a Constant Gm needed ? (cont'd)

- We can change *gm* by varying some parameters of the input stage. Let us assume that we design an amplifier with sufficient phase margin when g_{m1} is low (which is now *gm*). That is

$$p_2 = \frac{g_{m2}}{C_L} = 2.5GBW_{LOW} = 2.5\frac{g_{m1,LOW}}{C_m} = 2.5\frac{gm}{C_m},$$

  - When g_{m1}=*gm*, we can get that the phase margin as **57**°, which is sufficient to ensure the stability of the amplifier.
  - When the g_{m1} is at its maximum value, *2gm*, the *GBW* doubles, at this point, the phase margin changes to **29**° ! It is not enough and the amplifier may be unstable and may oscillate !!

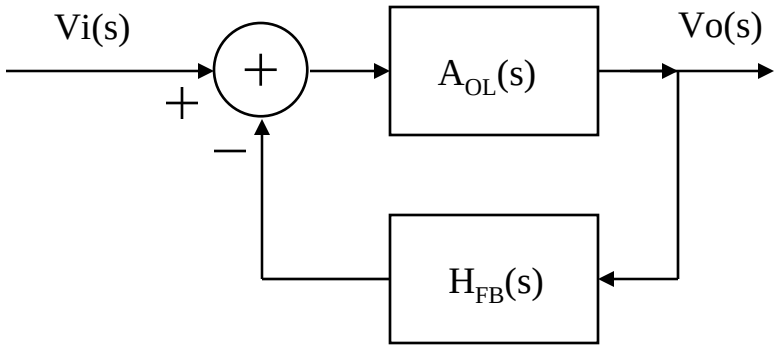
- We could design such that, when g_{m1} is *2gm*, we set the amplifier with sufficient phase margin, which means,

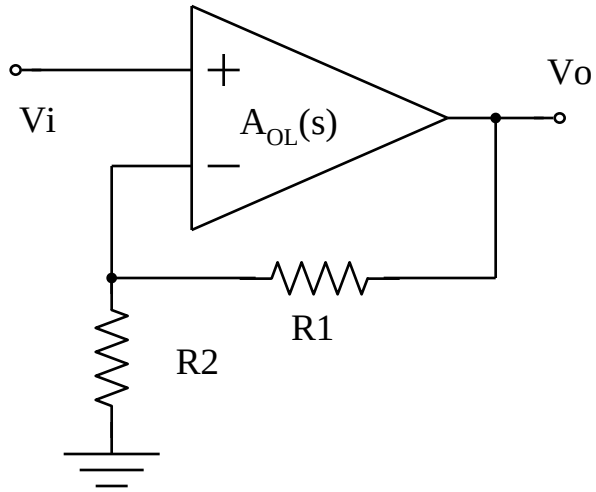
$$p_2 = \frac{g_{m2}}{C_L} = 2.5GBW_{HIGH} = 2.5\frac{g_{m1,HIGH}}{C_m} = 5\frac{gm}{C_m},$$

(cont'd)

We have to push g_{m2} to 2 times of its original value in previous case! It means **more power**, and might be near the limitation of the process, that is we can only design an amplifier with **50% of the GBW** that a specific process permits. Of course, we do not want either of these two situations.

- Transconductance variation of the input stage is not desirable, it prevents the optimal frequency compensation of the amplifier. There are other negative effects of the changing transconductance. For instance, gm variation may introduce extra harmonic distortion because of the changing voltage gain.
  - Let us consider a feedback voltage amplifier with input gm variation. As shown in the next slide.
  - Assume the open loop gain of the Op Amp is $A_{OL}(s)$, and the transfer function of feedback branch is $H_{FB}(s)$. The close loop gain of the amplifier is defined by





$$A_{CL}(s) = \frac{1}{H_{FB}(s) + \frac{1}{A_{OL}(s)}}$$

- For the practical case, close loop gain of the amplifier in the right figure is given by

$$A_{CL}(s) = \frac{1}{H_{FB} + \frac{1}{A_{OL}(s)}}$$, where $H_{FB} = \frac{R_2}{R_1 + R_2}$,

- $A_{CL}(s)$ changes if $A_{OL}(s)$ varies with the input voltage, although to a less extent, which will introduce some nonlinear distortion at the output, especially at higher frequencies when $A_{OL}(s)$ is low.

- In summary, we need a **constant** transconductance for the input stage!

- What are the structures capable to yield constant-gm N-P complementary input stage ?

- What are the tradeoffs and sensitivity to process variations ?

Techniques for N-P Complementary Rail-to-Rail Input Stage

There is a host of constant gm rail-to-rail input stage structures in literature, we will do a review from their implementation basic ideas

1. For input stages with input transistors working in weak-inversion region, using current complementary circuit to keep the sum of I_N and I_P constant [1][2][6];

2. Using square root circuit to keep $(\sqrt{I_p}+\sqrt{I_n})$ constant [3][13][16];

3. and 4. Using current switches to change the tail current of input differential pairs [3][4][5][6];

5. Using hex-pair structure to control the tail currents of backup pairs [7];

Techniques for N-P Complementary Rail-to-Rail Input Stage (cont'd)

6. Using maximum/minimum selection circuit to conduct the output current of the differential pair with larger current, as well as larger gm, to the next stage [8][9];

7. Using electronic zener diode to keep $V_{GSn} + |V_{GSp}|$ constant [10];

8. Using DC level shift circuit to change the input DC level [11].

   We will analyze them one by one in the following sections.

   There are still other techniques [12][14][15][17][18], interested readers may check these references.

Note: Unless explicitly stated in this notes, we assume that the square law characteristic of MOS transistors in strong inversion and saturation region. Please notice that for short channel transistors in sub-micron processes, square law is not exactly followed.

Rail-to-Rail Input Stage, Structure 2 [3][13*][16]

- Using square root circuit to keep $(\sqrt{I_p}+\sqrt{I_n})$ constant
- Basic idea
  - For an input differential pair, using a 1st order approximation,

$$gm=\sqrt{2K_P(W/L)I_D}=\sqrt{K_P(W/L)I_{TAIL}}$$

Where the I_{TAIL} is the tail current of the differential pair. We can change gm by altering the tail current of the differential pair!

  - The total transconductance of the input stage is given by

$$gm_T=gm_N+gm_P=\sqrt{KP_N(W/L)_N I_N}+\sqrt{KP_P(W/L)_P I_P}$$

If $KP_N(W/L)_N = KP_P(W/L)_P=2K$

We can get

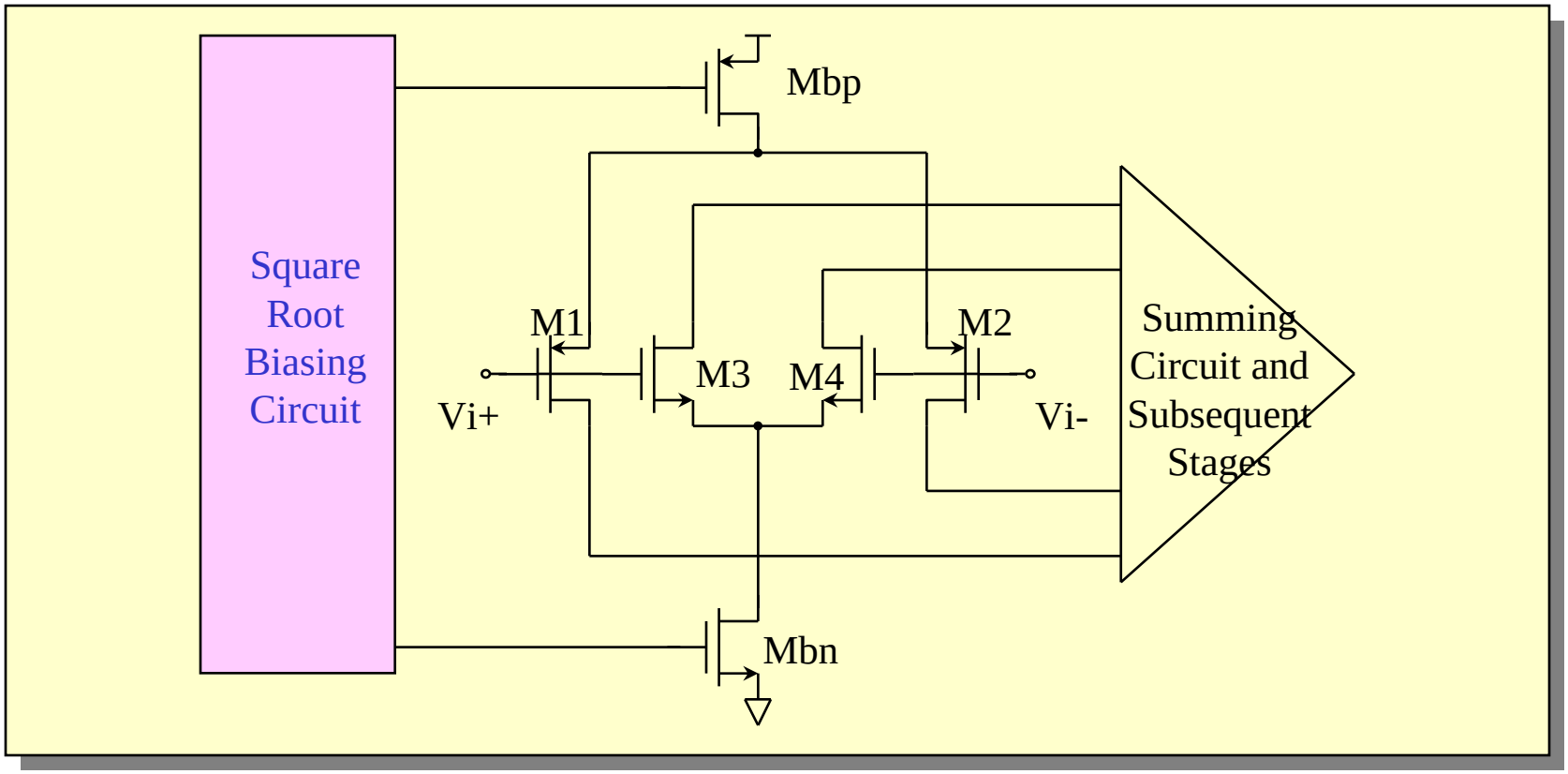
$$gm_T=gm_N+gm_P=\sqrt{2K}(\sqrt{I_N}+\sqrt{I_P})$$

  - To keep gm_T constant, we just need to keep $(\sqrt{I_N}+\sqrt{I_P})$ constant!

*:[13] is an improved version of this scheme, in [13] $KP_N(W/L)_N=KP_P(W/L)_P$ is not required. The authors presented techniques to compensate KP variations.

Rail-to-Rail Input Stage, Structure 2 (cont'd)

- Block diagram



- We can utilize the square law characteristic of MOS transistors to implement the square root biasing circuit.

Rail-to-Rail Input Stage, Structure 2 (cont'd)

- Working Principle
  - The input transistors work in strong inversion region.
  - The square-root circuit M121-M125 keeps the sum of the square-roots of the tail currents of the input pairs and then the gm constant.
  - The current switch, M111, compares the common-mode input voltage with Vb3 and decides which part of the current Ib7 should be diverted to the square-root circuit.
  - In the common-mode input voltage range from Vdd to -Vss+1.8V only the N channel pair operates. The current switch M111 is off and thus the tail current of the N channel input pair I_N equals Ib7=4Iref=20uA.
  - The sum of the gate-source voltages of M123 and M125 is equal to reference voltage which is realized by M121 and M124. Since the current through M125 equals I_N and the current through M123 equals the tail current of the P channel input pair I_P.

Rail-to-Rail Input Stage, Structure 2 (cont'd)

- The summing circuit M21-M24 adds the output signals of the complementary input stage, and forms the output voltage at node #20.

- Discussion
  - The circuit is somewhat complex and the functionality relies on the square law of MOS transistors. For current sub-micron processes, the square law is not closely followed, which may introduce large error for the total transconductance.

Rail-to-Rail Input Stage, Structure 3 [3][4][6]

- Using current switches to change the tail current of input differential pairs

- Basic idea
  - We know that, by first order approximation, for a MOS transistor working in strong inversion and saturation region, square law applies, that is

    $I_D = K(V_{GS} - V_T)^2$, and $gm = 2\sqrt{KI_D}$,

    where $K = \frac{1}{2} KP(\frac{W}{L})$
  - Suppose for the N and P input pairs, $KP_N(\frac{W}{L})_N = KP_P(\frac{W}{L})_P = 2K$

    and the tail currents of N and P pairs are equal, with the value of I_{tail}.

Rail-to-Rail Input Stage, Structure 3 (cont'd)

– When the input common mode voltage is in the mid-range, both of N and P pairs are conducting, so the total transconductance is

$$gm_T = gm_N + gm_P = 2\sqrt{2KI_{TAIL}}$$

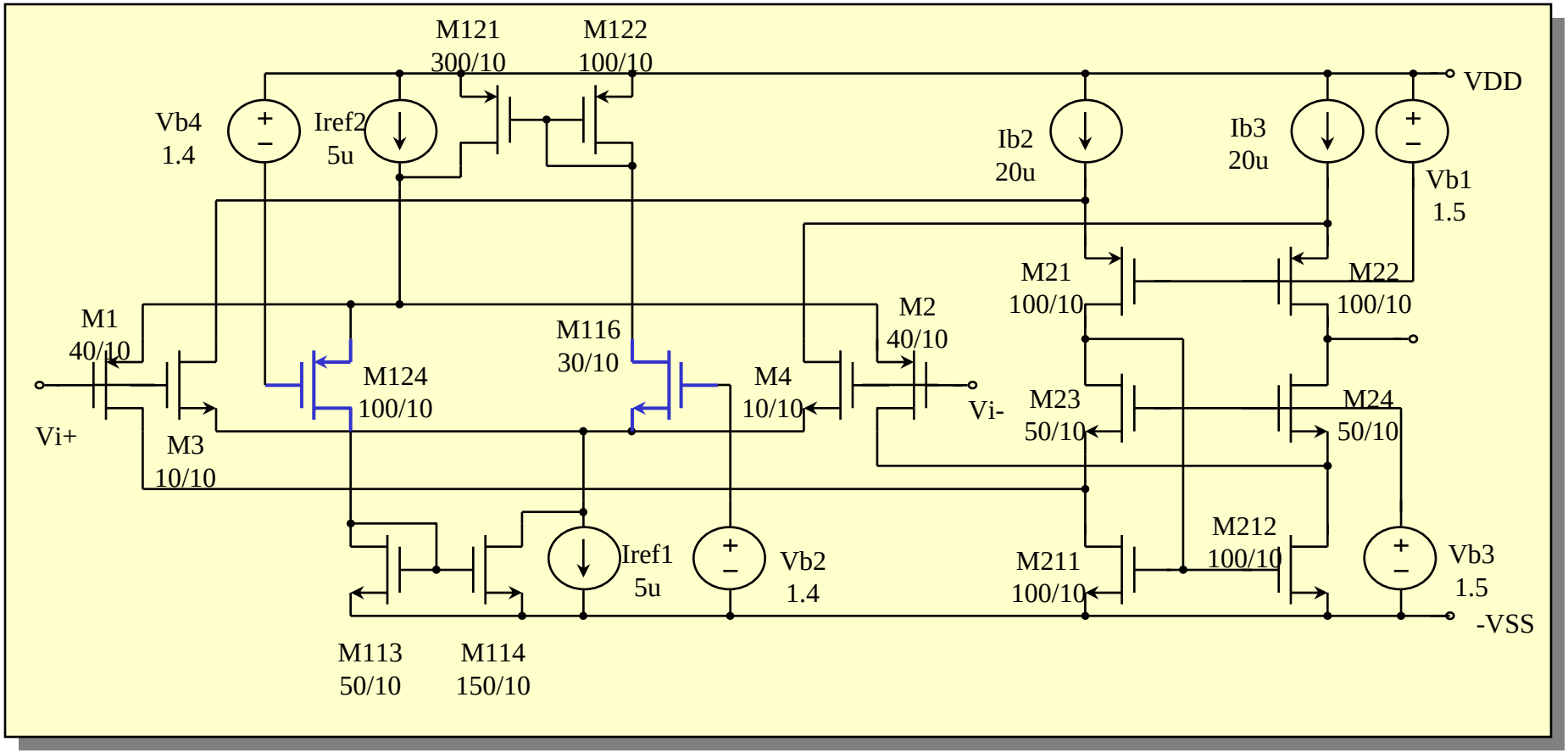
– When the input common mode voltage is close to Vdd, the N pair operates. And when it is close to the -Vss, the P pair operates. In both cases, the total transconductance is only **half** of that when both of N and P pairs operate.

$$gm_T = gm_N = gm_P = \sqrt{2KI_{TAIL}}$$

We can increase the tail current to **4** times of its original value to have the same transconductance as that when both of N and P pairs operate.

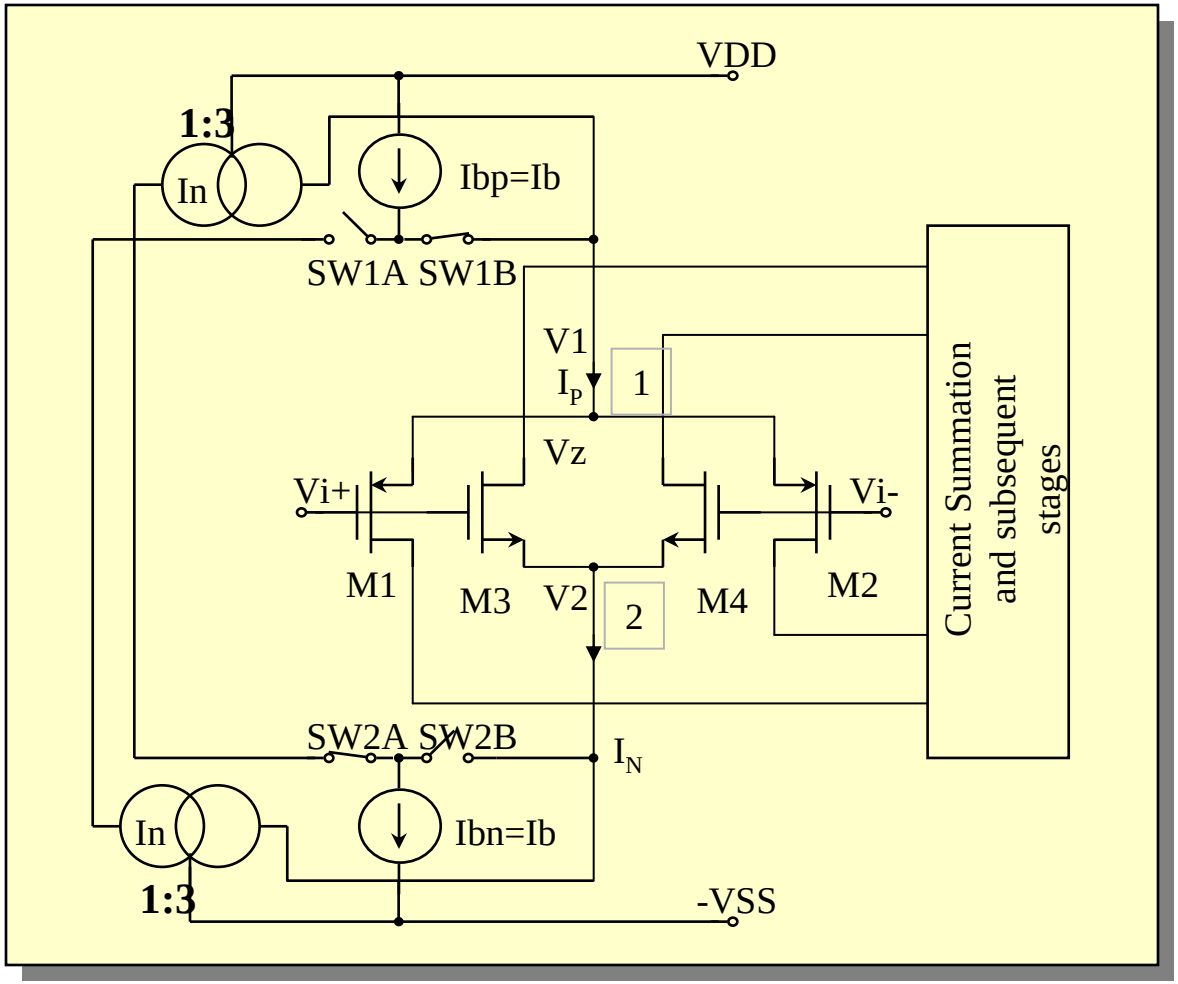
Rail-to-Rail Input Stage, Structure 3 (cont'd)

- The circuit



Rail-to-Rail Input Stage, Structure 3 (cont'd)

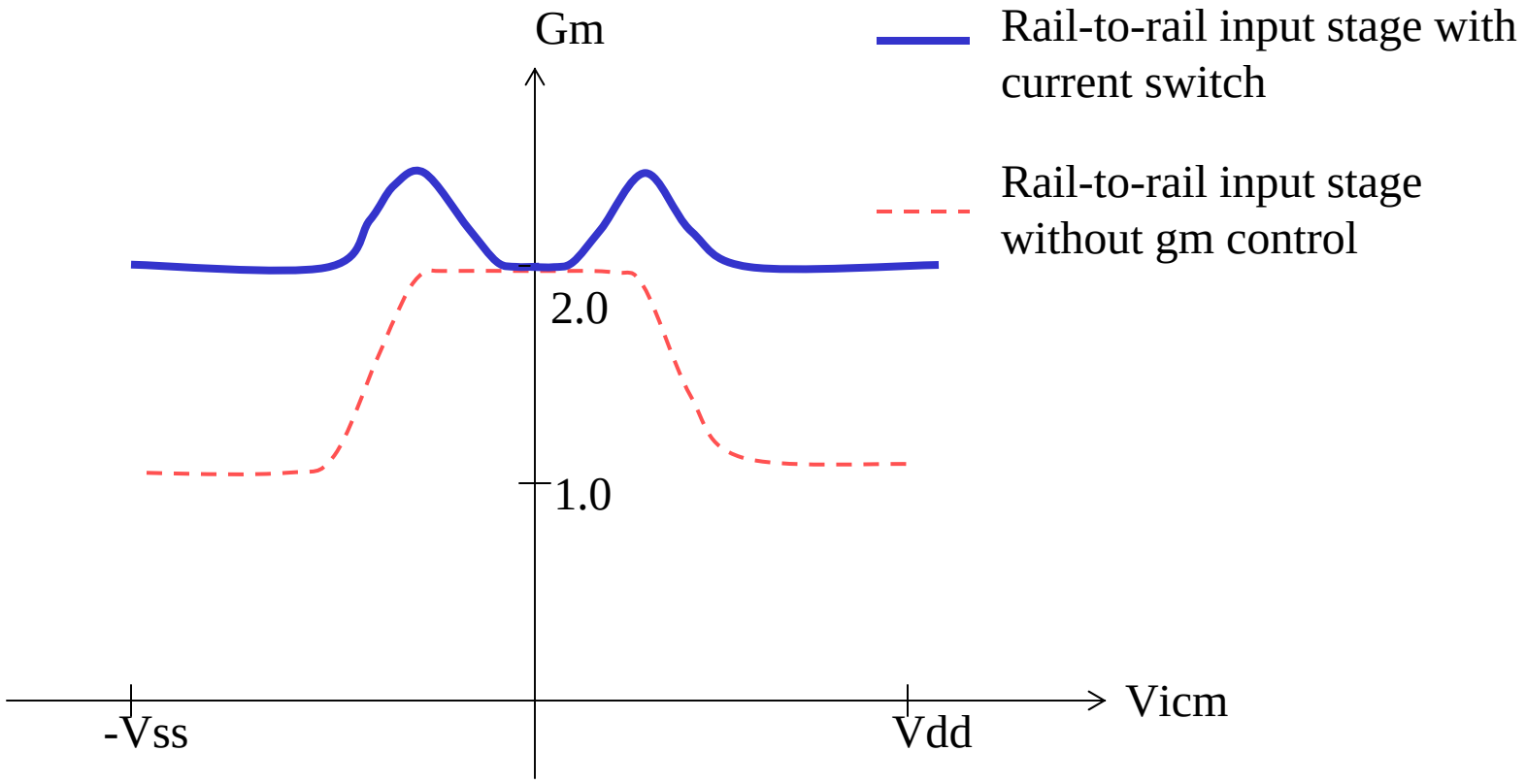
- Conceptual circuit



- When common mode input voltage, Vicm, is close to $-V_{ss}$, SW1B and SW2A are on, and SW1A and SW2B off.
- When Vicm is close to Vdd, SW1A and SW2B are on, and SW1B and SW2A off.
- In between, SW1B and SW2B are on, SW1A and SW2A off.
- In practice, SW1B and SW2B are never required, just short circuits. Say, if SW1A is on, Ibp will be diverted to the 1:3 current mirror; if SW1A is off, Ibp will provide tail current for M1 and M2.

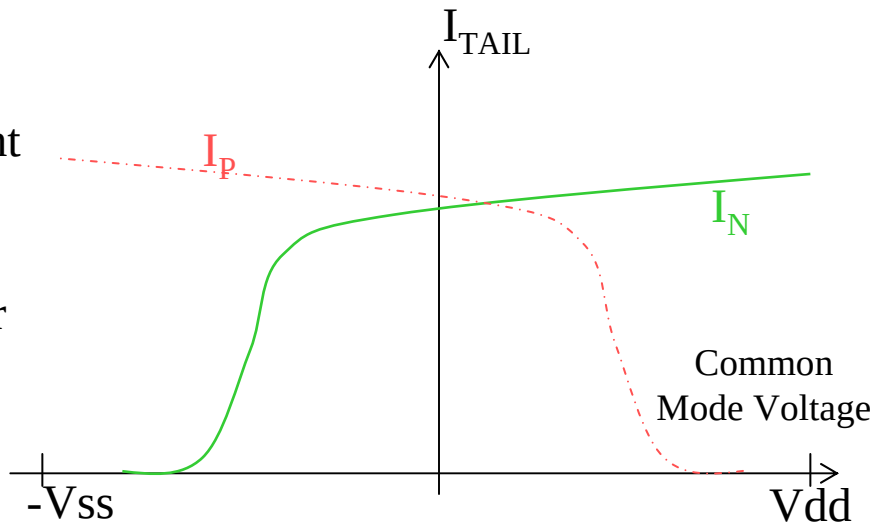
Rail-to-Rail Input Stage, Structure 3 (cont'd)

- Transconductance vs. input common mode voltage



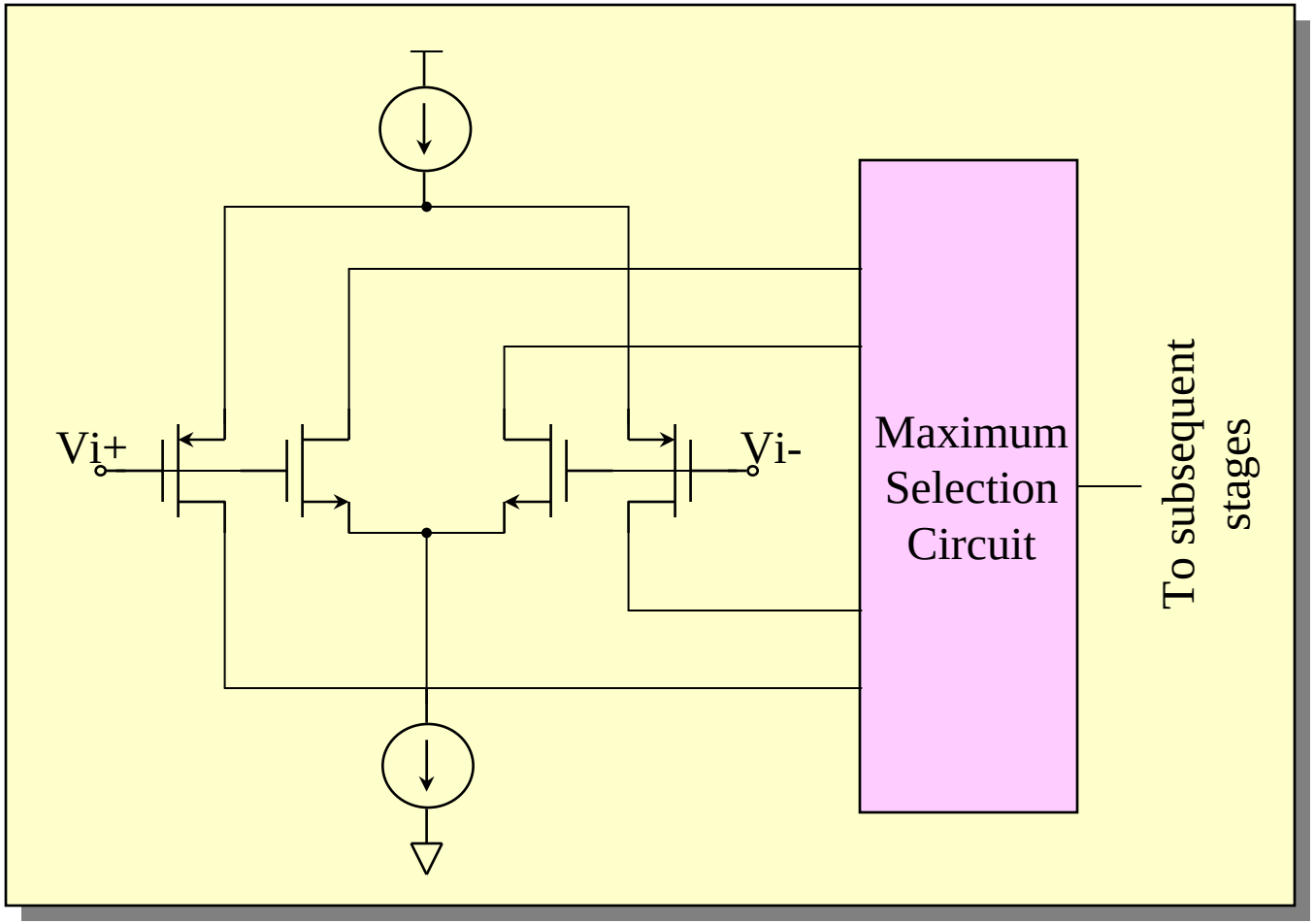
Rail-to-Rail Input Stage, Structure 6 [8][9]

- Using Maximum/Minimum selection circuit
- The basic idea
  - From previous analysis, we know that, when the common mode voltage drives the tail current transistor out of saturation region, the tail current of a differential pair decreases dramatically with the common mode voltage. As shown in the following figure.
  - The differential pair, whichever it is N pair or P pair, with the larger current should be working properly. We just try to choose the pair with larger working current, and discard the output of another pair.



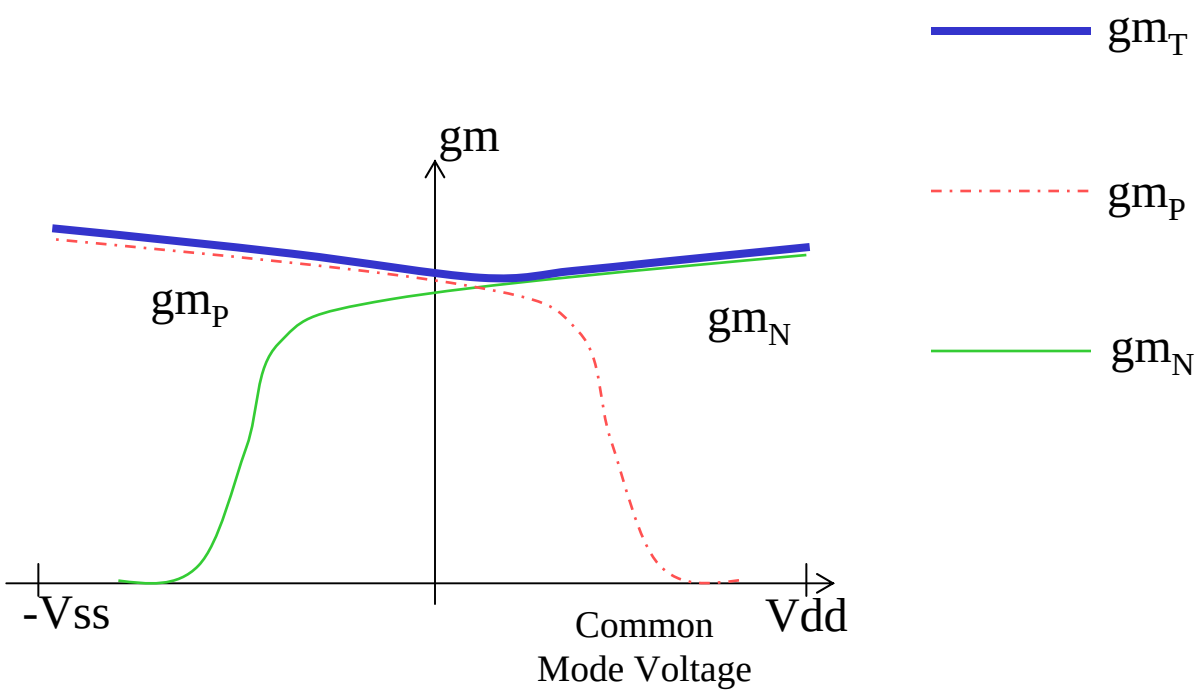
Rail-to-Rail Input Stage, Structure 6 (cont'd)

- The block diagram



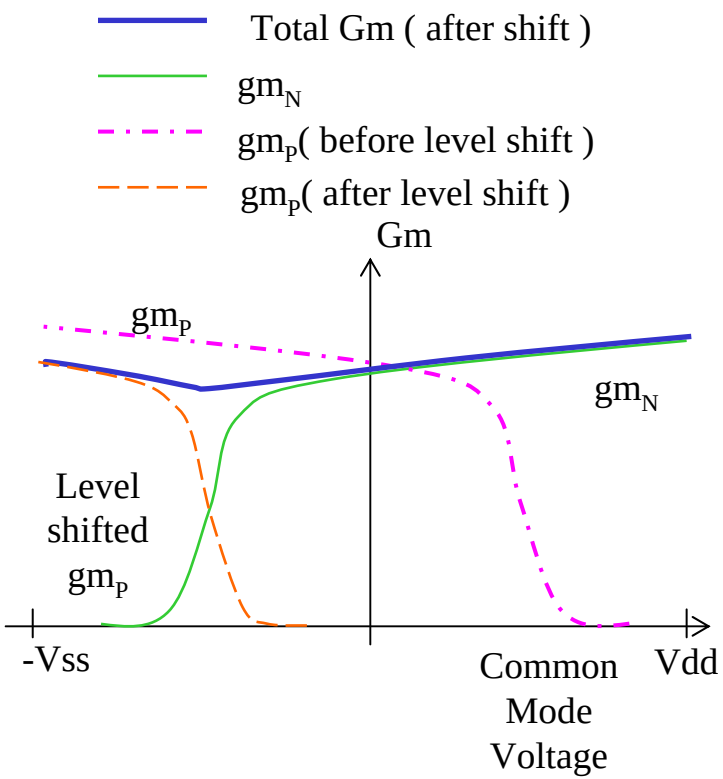
Rail-to-Rail Input Stage, Structure 6a (cont'd)

- Transconductance vs. input common mode voltage

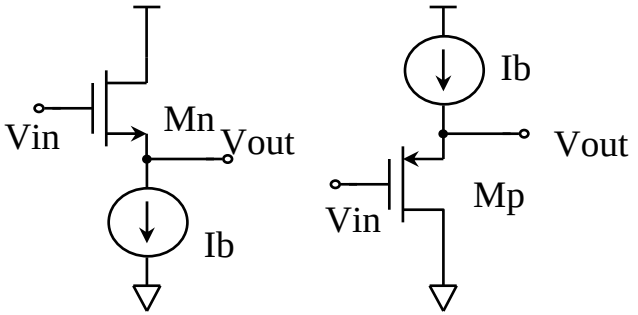


Rail-to-Rail Input Stage, Structure 8 [11]

- Using DC shifting circuit to change the input DC level
- Basic idea

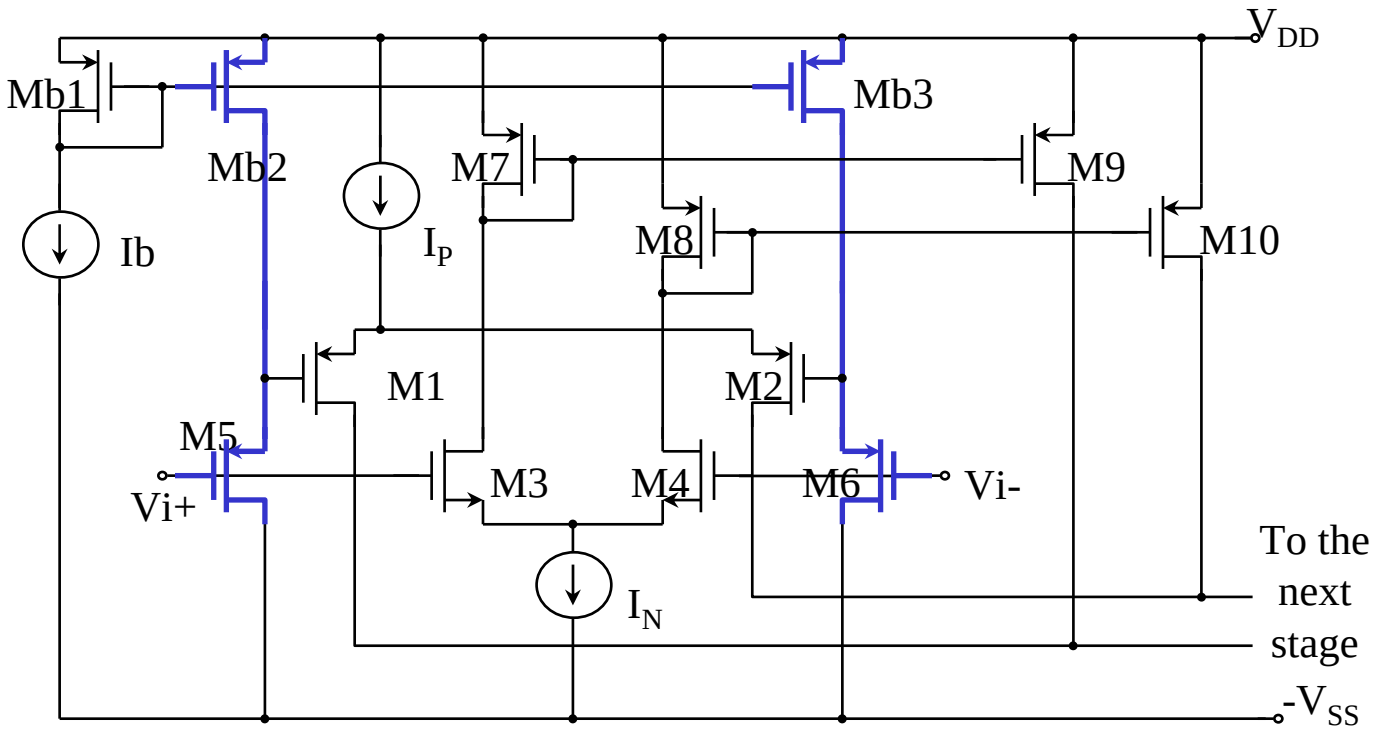


- We may notice that there is an overlap between gm_N and gm_P, so in the middle of the common mode voltage, the transconductance is doubled.
- How about shift one of the gm_N and gm_P curve? And let the transition regions of gm_N and gm_P come together, so that the total transconductance will be nearly constant among the common mode input range.
- Level shift can be implemented by common source voltage follower. We can change the shift level by altering the bias current Ib.



Rail-to-Rail Input Stage, Structure 8 (cont'd)

- The circuit [11]

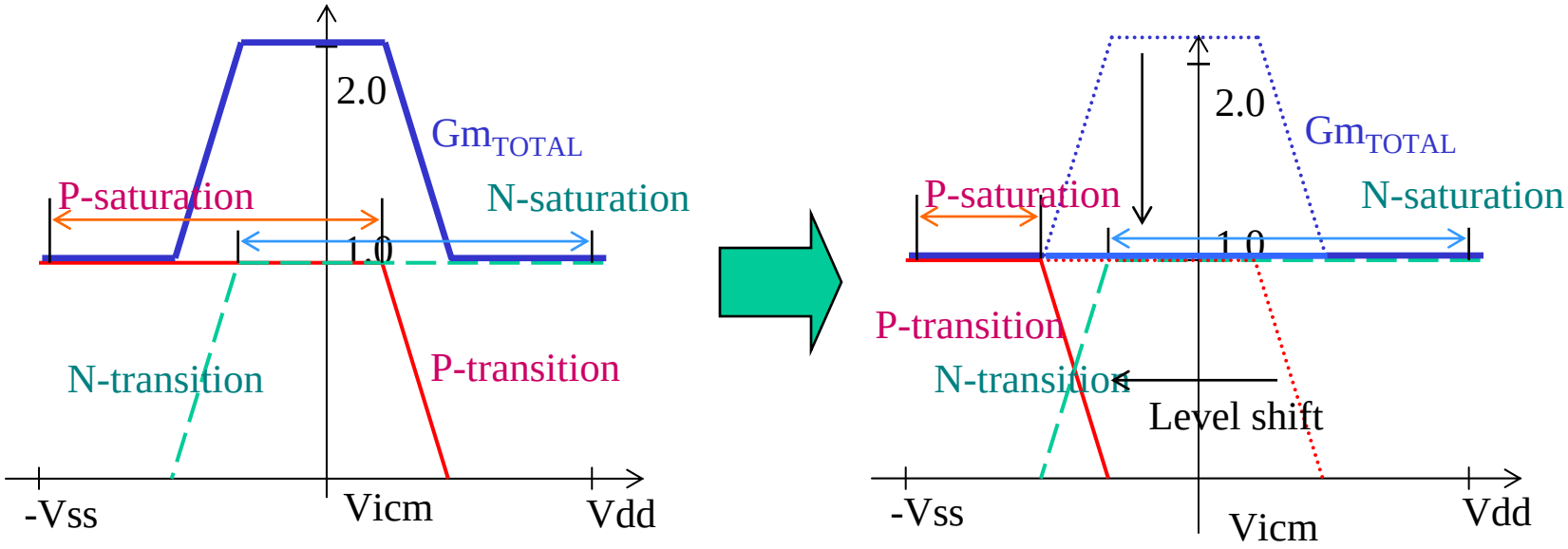


Note: 1) M5 and M6 are level-shifting transistors

2) The voltage shifted by M5 and M6 can be altered by changing Ib

Rail-to-Rail Input Stage, Structure 8 (cont'd)

- Working principle
  - The input voltages are shifted by M5, M6 by $|V_{GS,M5,M6}|$ towards the positive power supply rail, so the transition region for gm_P is shifted by the same value towards the negative power supply rail.
  - The transistions region of gm_N and gm_P overlap and we can get an constant gm over the common mode range.



Rail-to-Rail Input Stage, Structure 8 (cont'd)

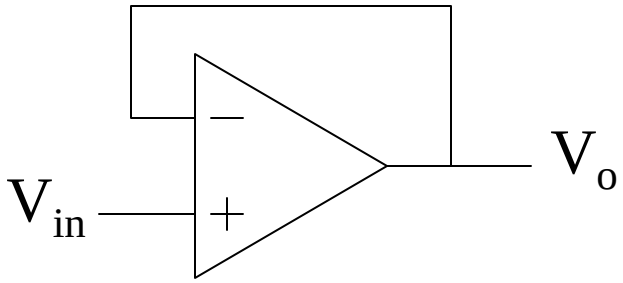
- Characteristics
  - We can obtain very small gm variation (±5%) if the DC shift level is tuned well [11].
  - This circuit structure is sensitive to the power supply changes and V_T variations, but we can add some auto-bias circuit to overcome this problem.

Summary and Comparison

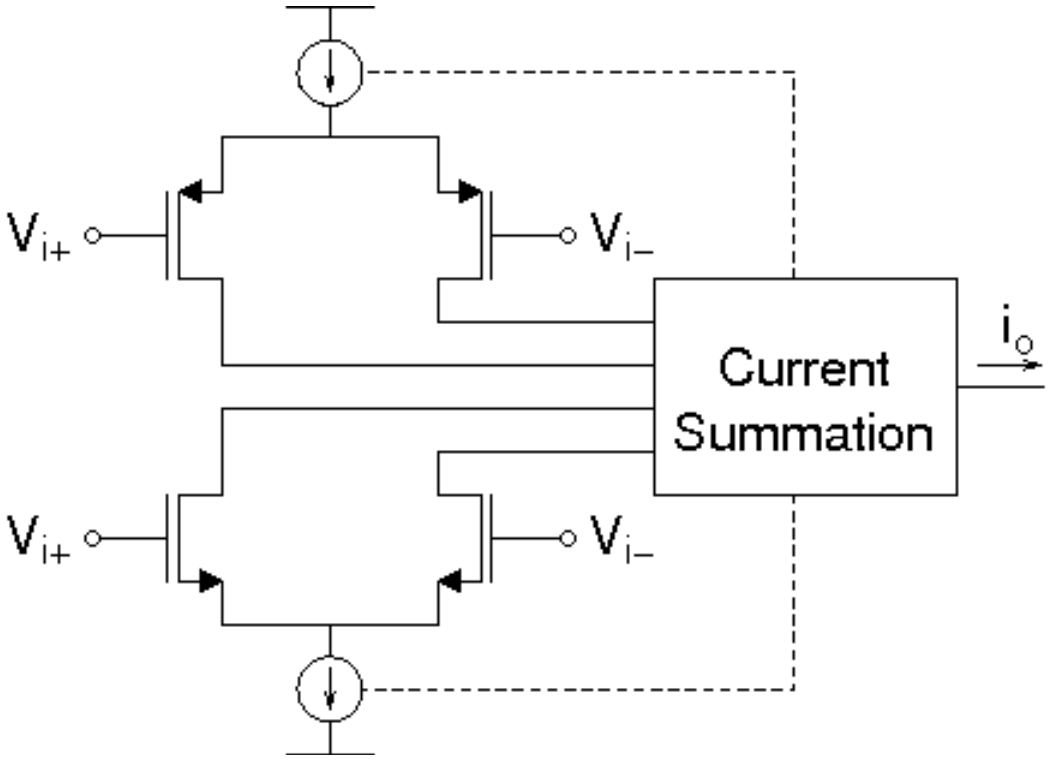
Case	Principle	Δgm	Slew Rate	CMRR	Advantage	Limitations
1	$I_N + I_P = const$ [1][2][6]	N/A for weak inversion 40% if in strong inversion	Constant	56dB@10Hz, 52dB@100KHz, measured in [2]	Small gm variation (6%) in weak inversion operation	Only work well in weak inversion, can not used in high speed application
2	$\sqrt{I_N} + \sqrt{I_P} = const$ [3] [16]	-12% +6% (simulated in this presentation)	$\sqrt{2}$ times variation	80 dB / 53 dB (measured in [3])		Depends on quadratic characteristics of MOSFETs, which is not exactly followed for short channel transistors in sub-micron processes
3	4 times I_N or I_P when only one pair operates [3][4][6]	+15% systematic gm variation	2 times variation	70dB / 43 dB (measured in [4])	Somewhat simple	1) Same with case 2, but we can change 4 to other numbers to have smaller gm variation for short channel transistors 2) Systematic gm deviation of 15% even for ideal MOSFETs with quadratic characteristics
4	Current switch, backup pairs [5]	+20% systematic gm variation	Constant	N/A	Constant slew rate	Systematic gm deviation of 20% even for ideal MOSFETs with quadratic characteristics
5	6-pair structure, back pairs [7]	+20% systematic gm variation (analytical), ±10% (measured in [7])	Constant	N/A	Constant slew rate	Same with Case 4
6	Max/min selection [8][9]	7% (simulated [9]) 5% (strong inversion, measured [8]) 20% (weak inversion, measured [8])	Constant	N/A		Somewhat complex
7	Electronic zener [10]	8% (measured)		80 dB / 43 dB (measured in [10])		Same with Case 2
8	Level shift [11]	±4% after tuning 13% before tuning (measured)		≥80 dB (DC) (measured in [11])	Simple	Gm variation sensitive to V_T variation and power supply voltage change

A Rail-to-Rail Amplifier Input Stage with Less than ±0.5% Fluctuation in g_m

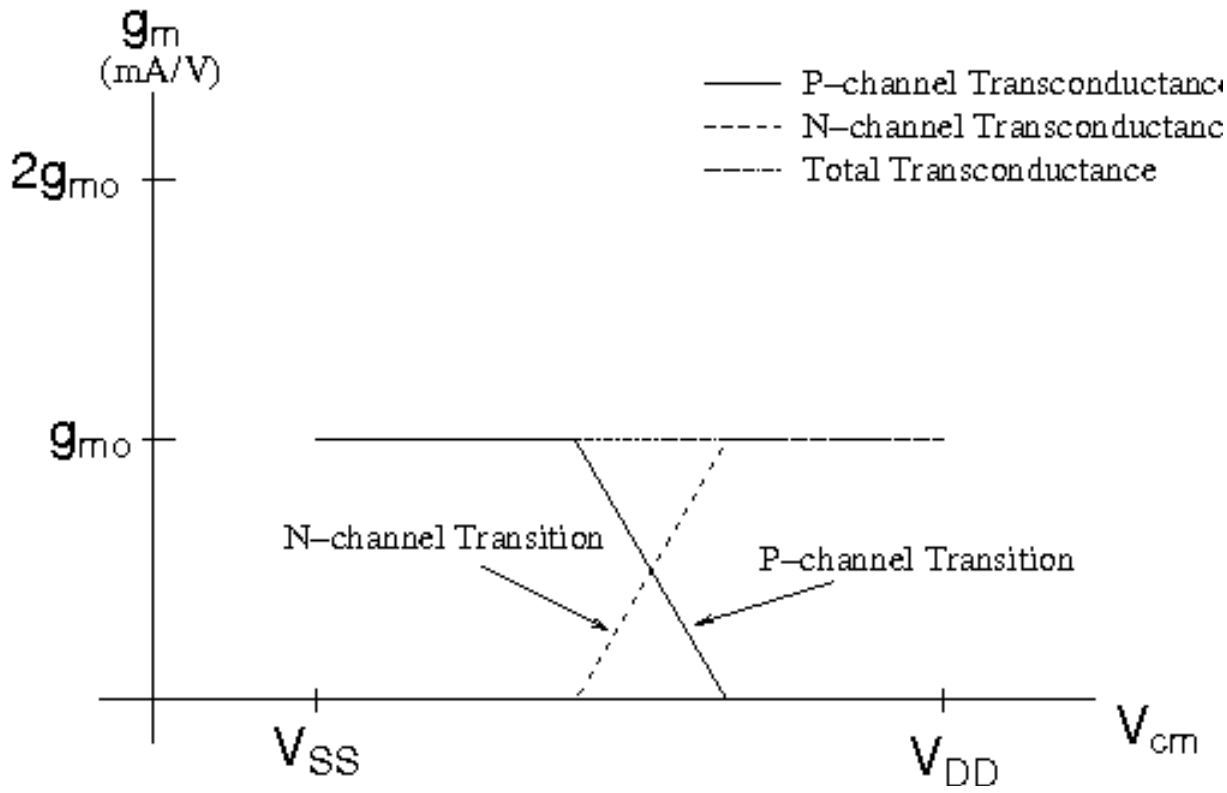
By courtesy of Timothy W. Fischer



Previous Work



Previous Work [2]

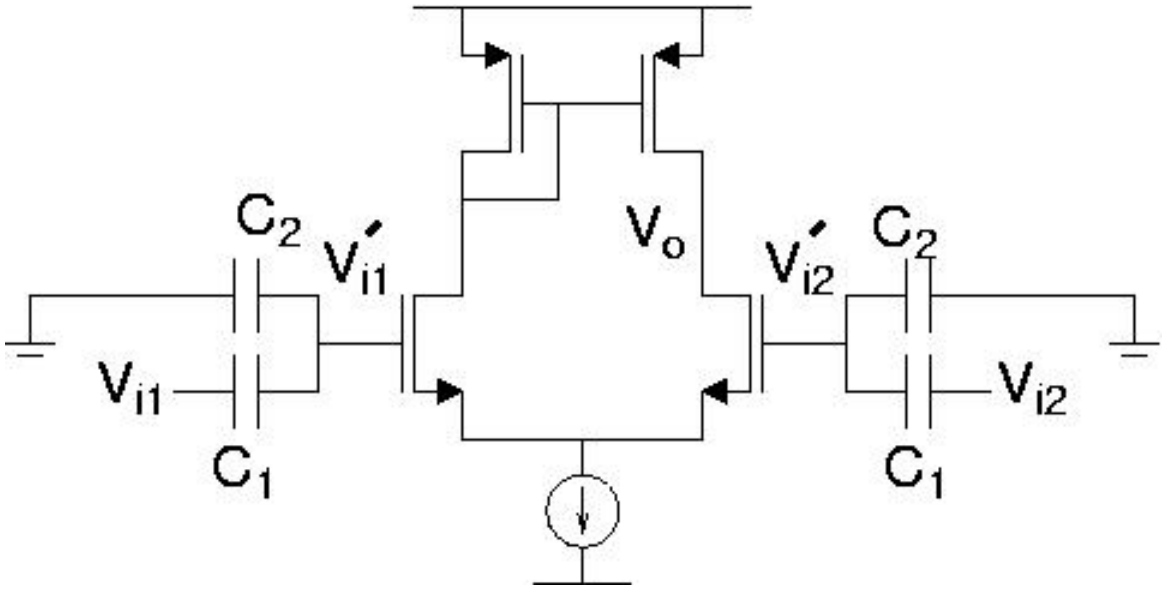


Problems with Previous Work

- Mismatch between N-channel and P-channel transconductors

- Transition Region
  - CMRR degradation (40-60 dB)
  - Nonlinearity

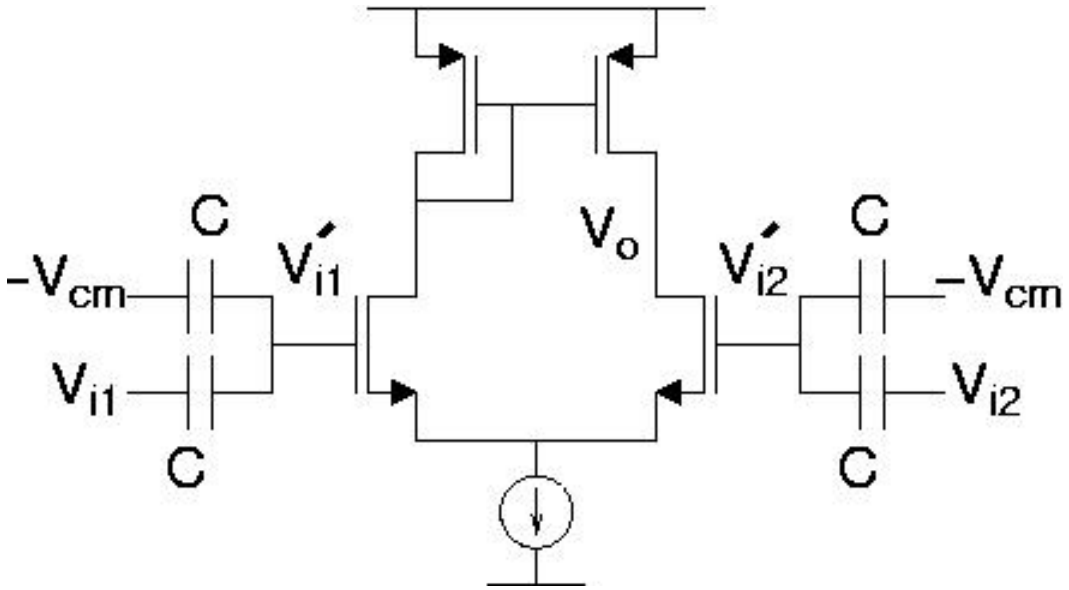
One Differential Pair Solution[4]



$$v_{in} = v_{cm} + v_{dm}$$

$$v_{in}' = \frac{C_1}{C_1 + C_2} v_{cm} + \frac{C_1}{C_1 + C_2} v_{dm}$$

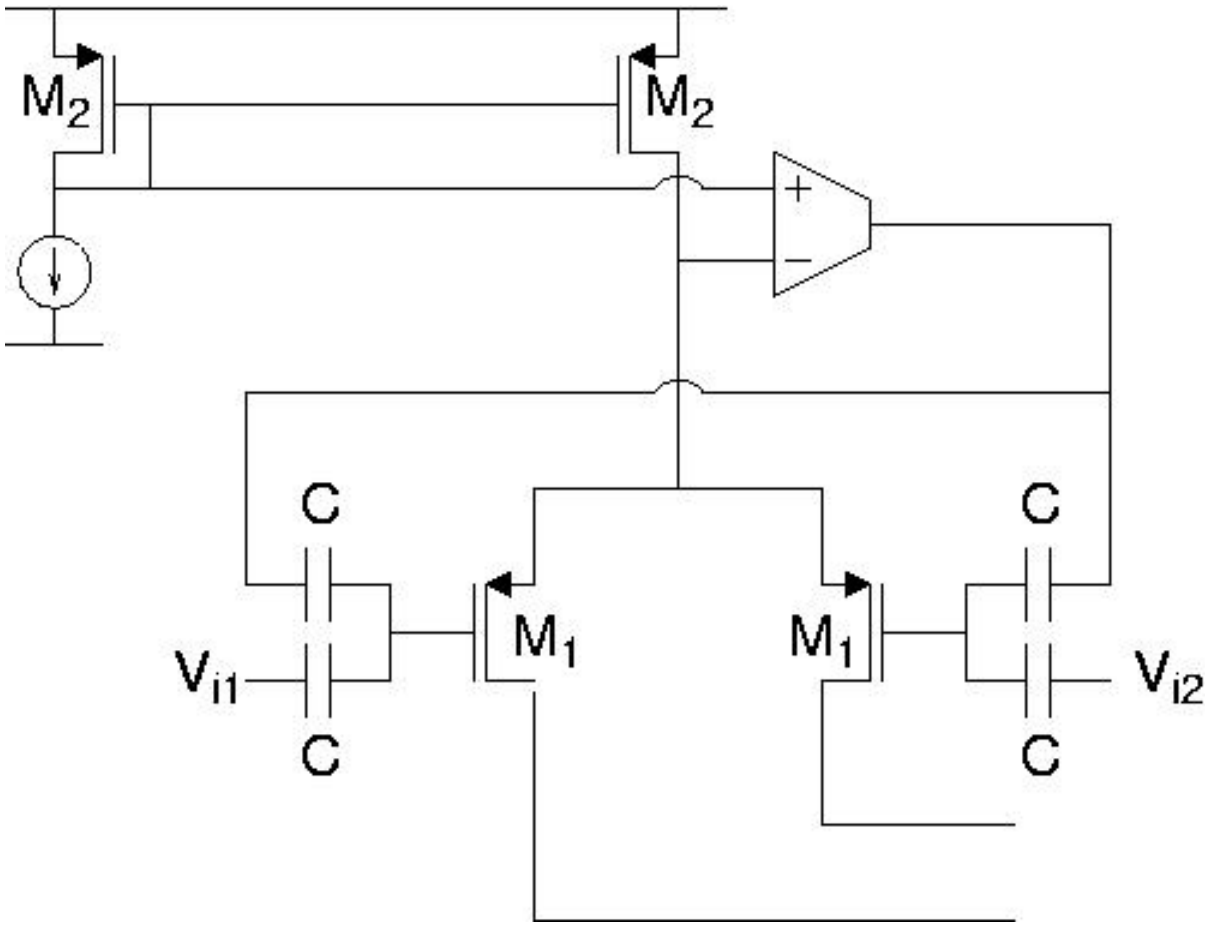
Proposed Solution



$$v_{in} = v_{cm} + v_{dm}$$

$$v_{in}' = \frac{v_{dm}}{2}$$

Proposed Solution



Design Considerations

- Typically Floating Gate Caps are 5x-10x size of Parasitics

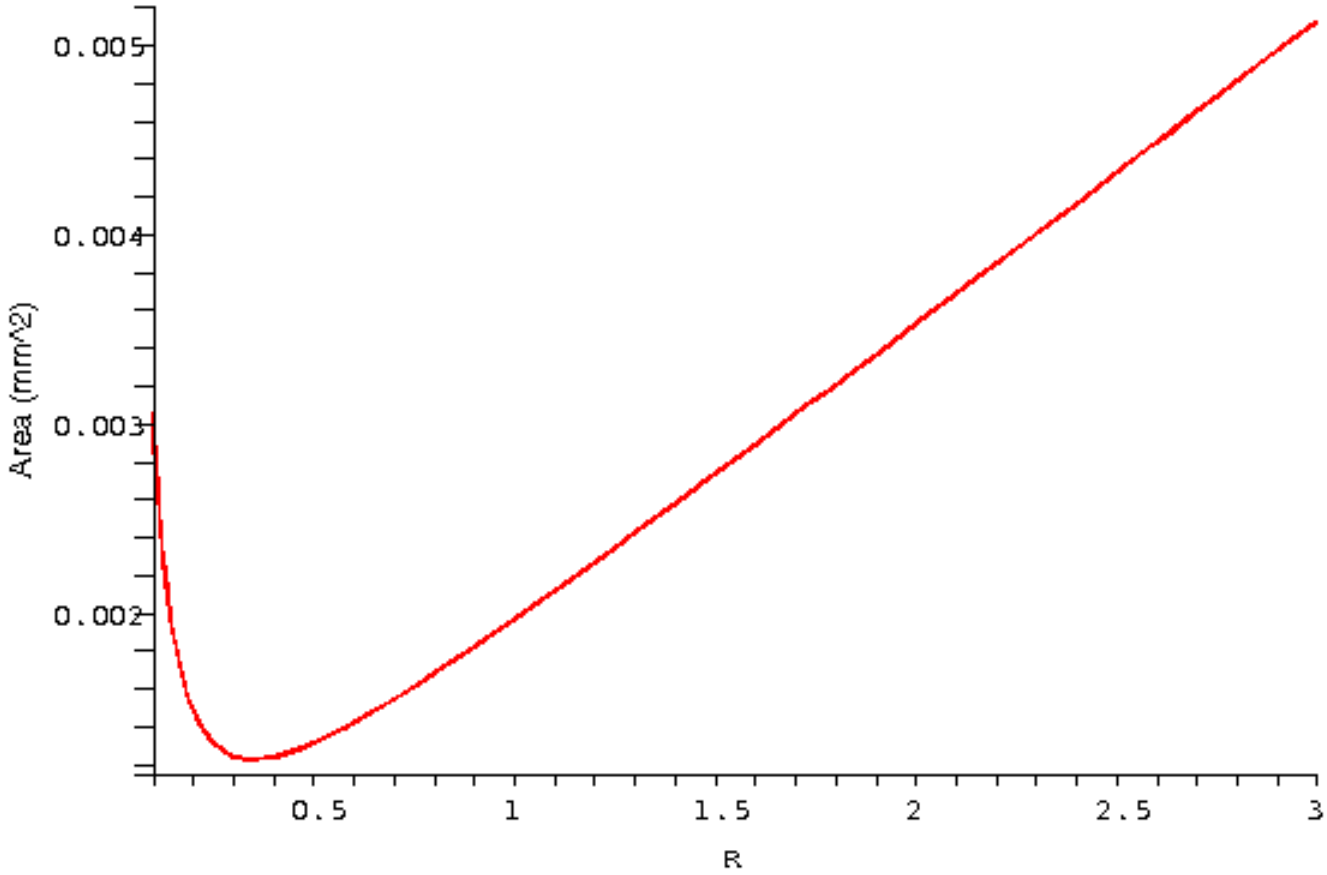
$$G_m = g_m \frac{C}{2C + C_{gs1} + C_{gd1} + C_{gb1}}$$

- What is effect of decreasing C?

Design Considerations

- Decrease C, Increase W_1/L_1 to compensate
- Increasing W_1/L_1 increases size of parasitics, area
- Minimize total area
- $Area_{C,drivers}=4C/C_{poly}+2W_1L_1$
- Define $C=RC_{gs1}$
- $Area_{C,drivers}=8RW_1L_1C_{ox}/3C_{poly}+2W_1L_1$
- Combine Area, G_m equations, find minimum R

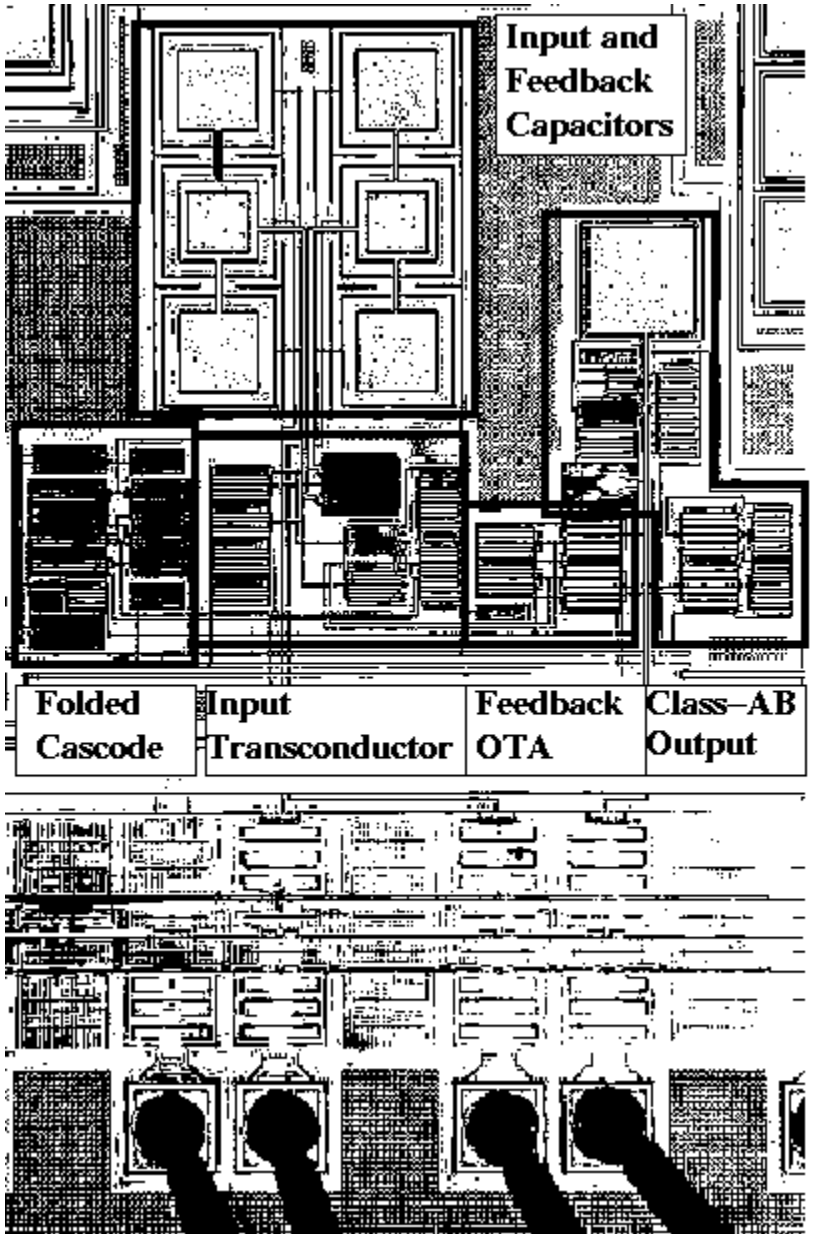
Minimized Area



Complete Amplifier Design

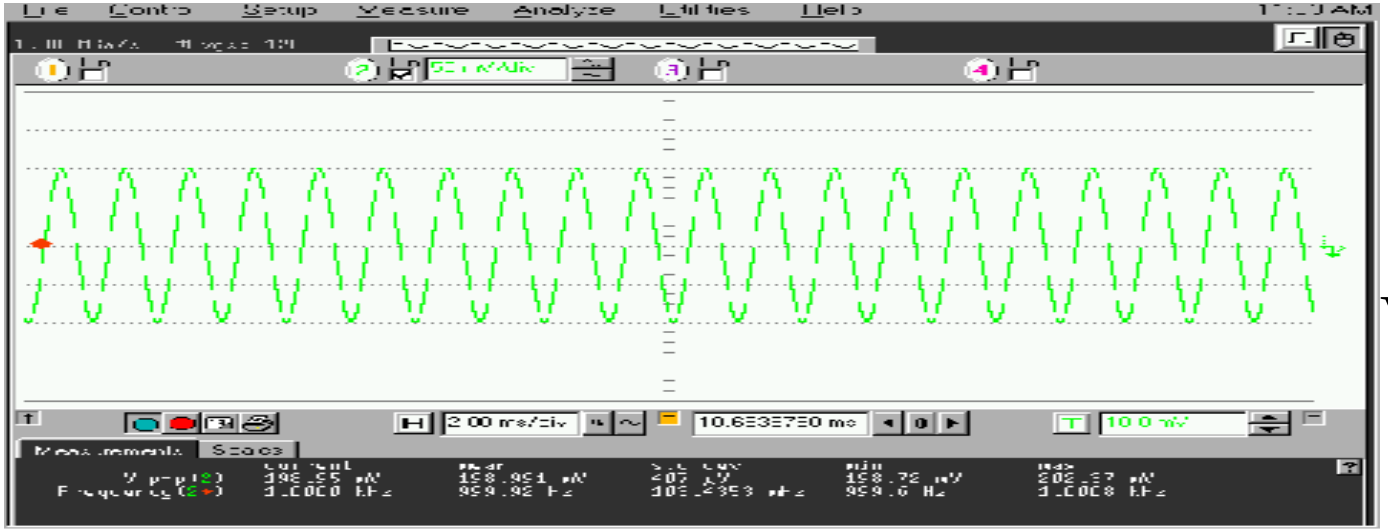
- Proposed Input Transconductor
- Folded Cascode for High Gain
- Class-AB Output Stage for Rail-to-Rail Output Swing

Die Micrograph



Experimental Results – Input Stage

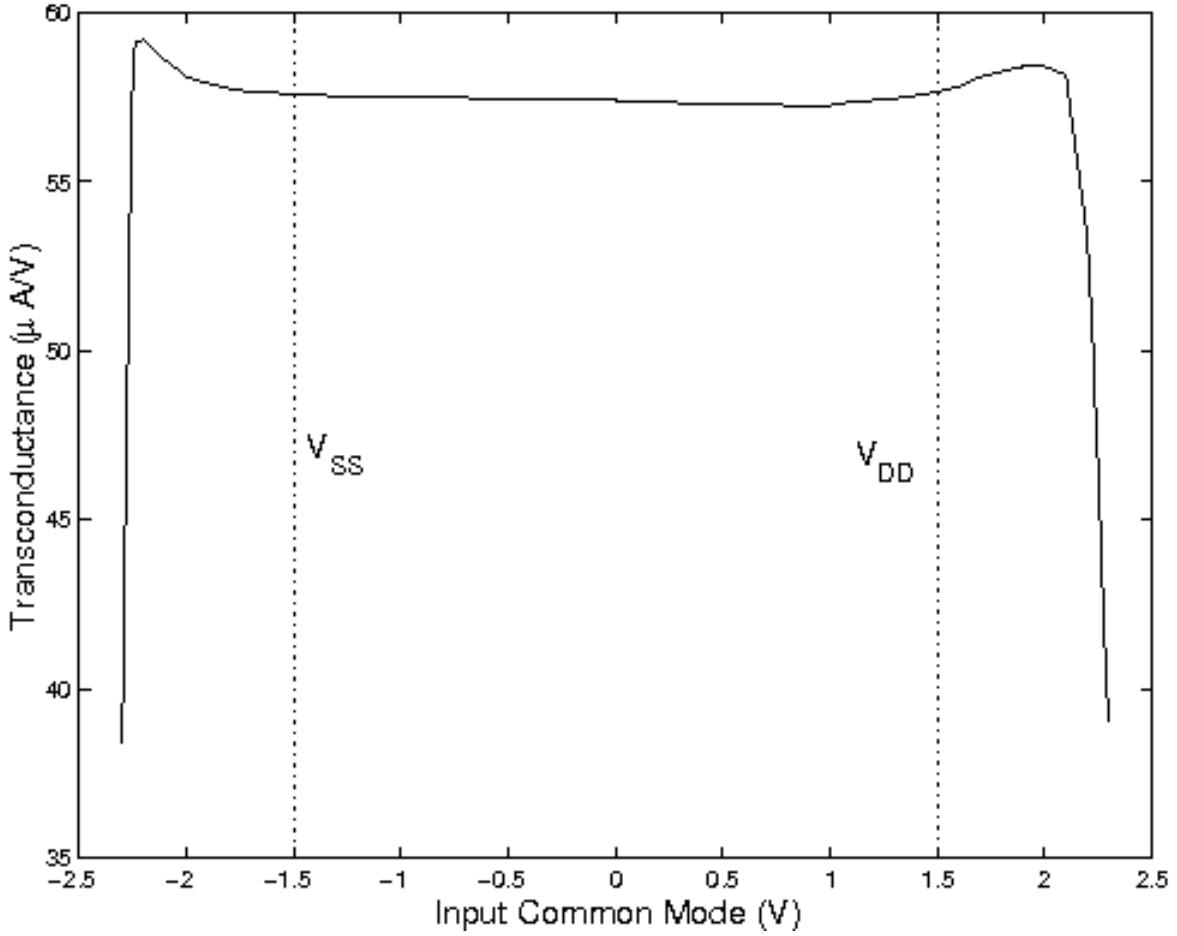
V_{icm}=4.4 V_{pp} 50 Hz Triangle Wave



V_{idm}=0.1sin(2kπt)

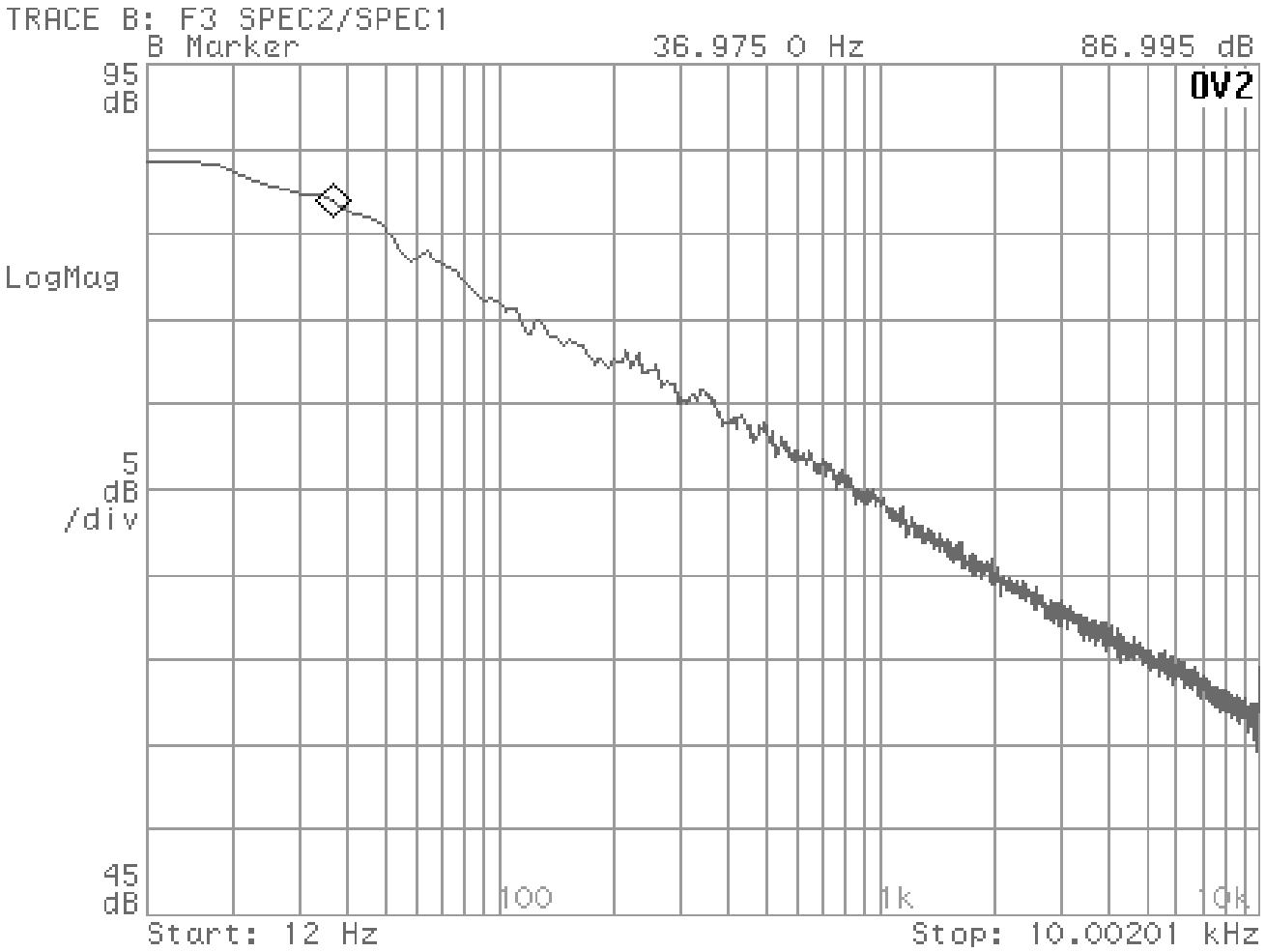
Experimental Results – Input Stage

Experimental Results – Input Stage



G_m varies ±0.35% from V_{SS} to V_{DD}
G_m varies ±1% from -2V to 2V

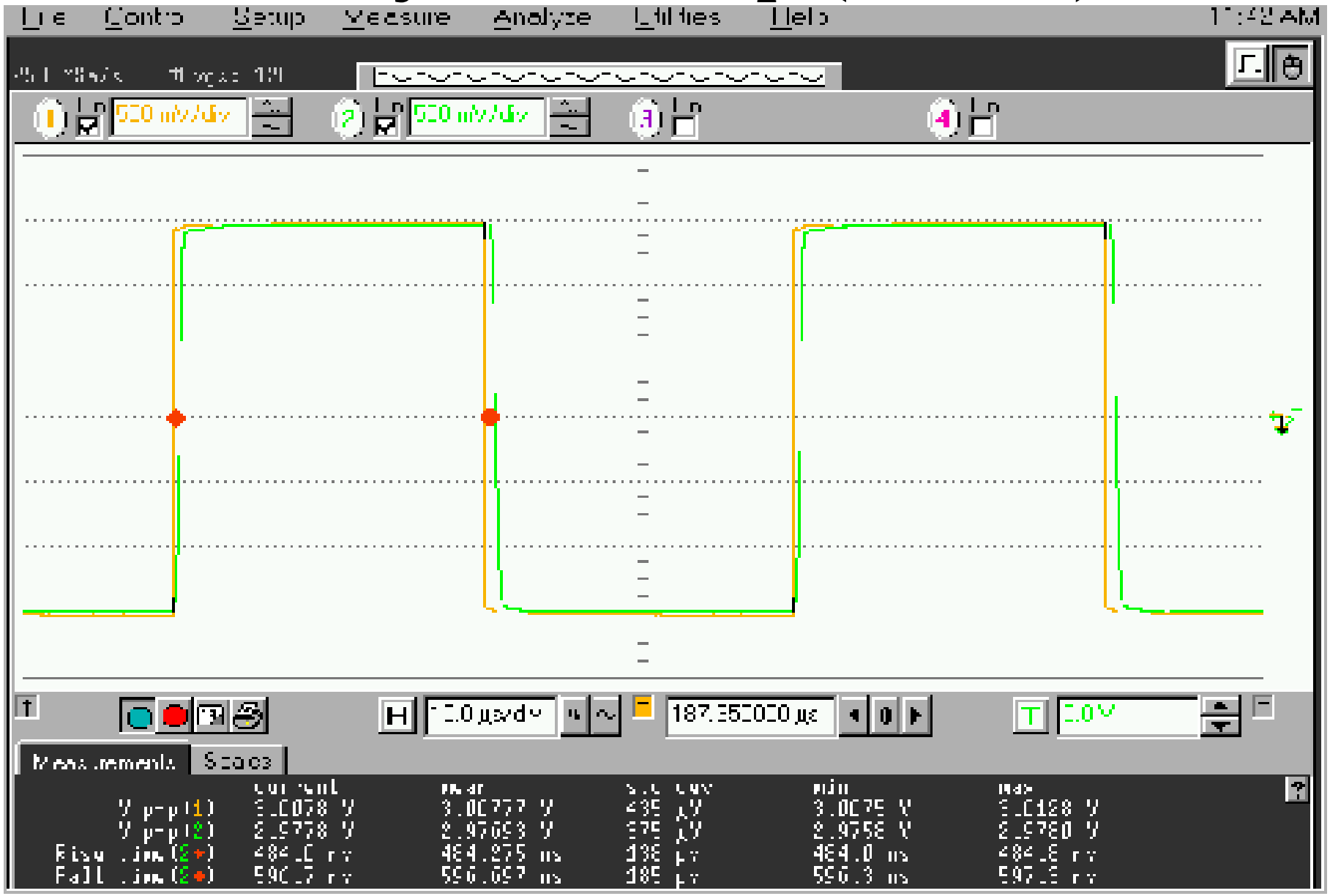
AC Gain – Complete Amplifier



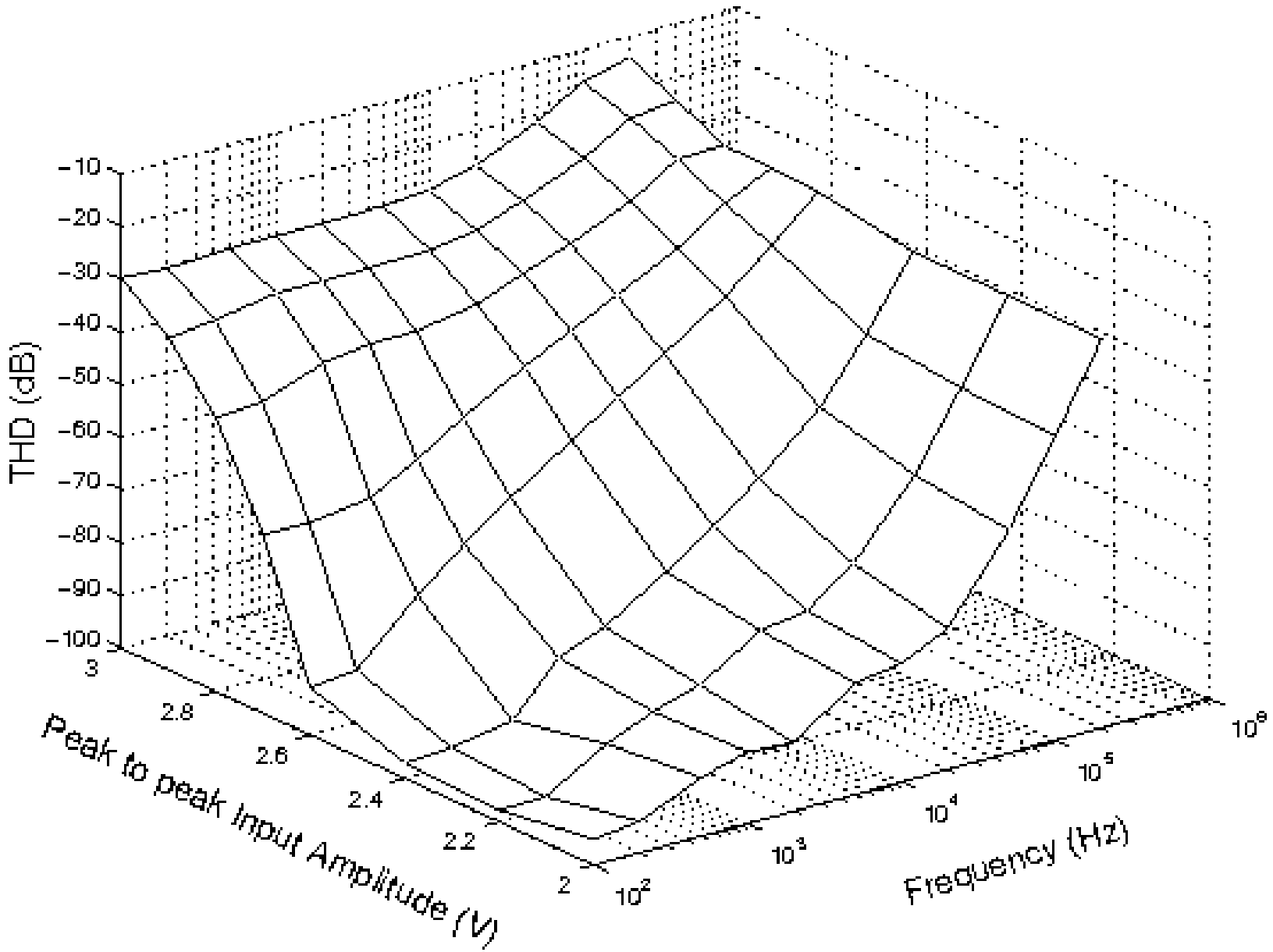
A_{v0}=89dB

GBW=1.2MHz

Unity Gain Step (Buffer)



Buffer Linearity



Comparison to Other Work

Parameter	**This Work**	**[1]**	**[2]**	**[3]**	**[4]**	**[5]**
ΔG_m	±0.35%	±1.5%	±4%	±3%	NA	±4.6%
A_{v0} (dB)	89	70	110	84	60	59
GBW (MHz)	1.2	1	3.2	1.3	5	5.9
CMRR	80	NA	88	56	47	NA
SR (V/μs)	5	NA	5.8	1	7	6.4
Power (mW)	.51	NA	.31	.46	.19	NA
Area (mm^2)	.36	NA	.12	1.2	.09	NA
Tech.	0.5 μm	0.8 μm	1.2 μm	0.7 μm	0.8 μm	0.8 μm

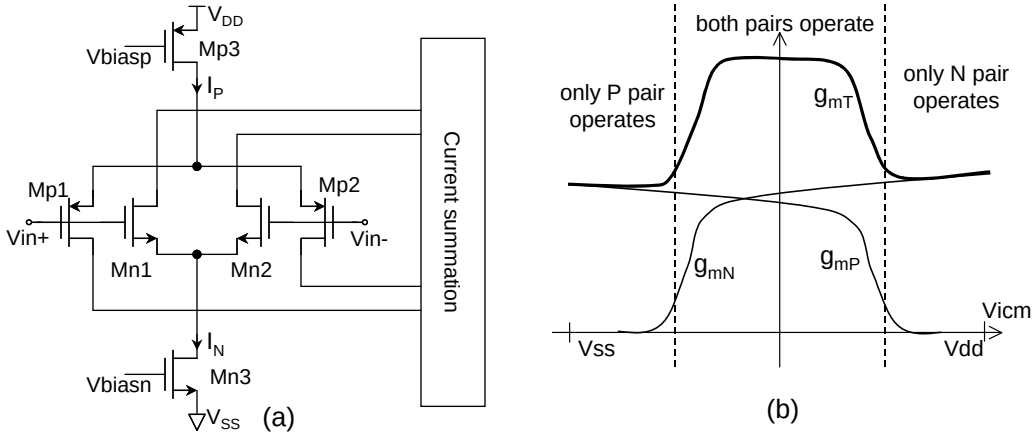
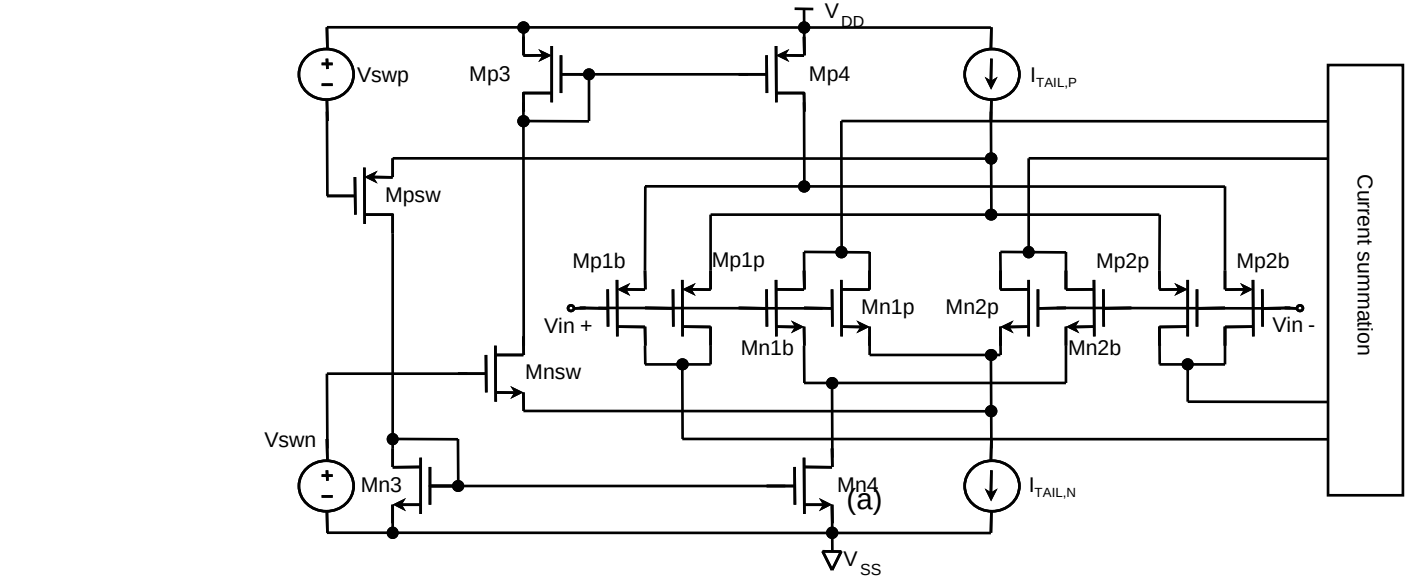


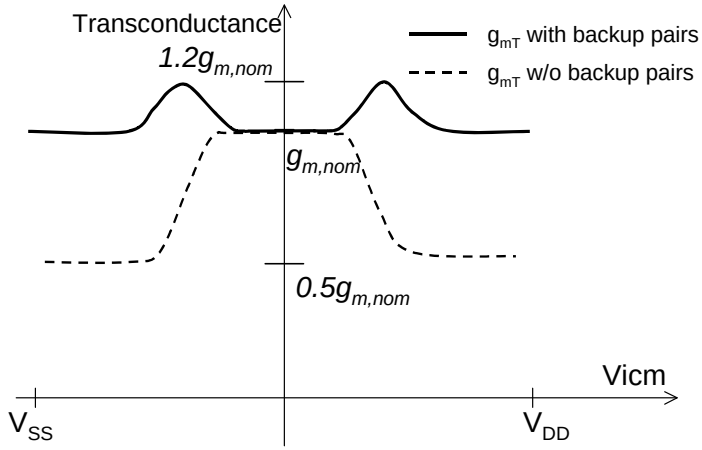
Fig. 1

IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS { I: FUNDAMENTAL THEORY AND APPLICATIONS 1

A Robust and Scalable Constant-*gm* Rail-to-Rail
CMOS Input Stage with Dynamic Feedback for
VLSI Cell Libraries

Tongyu Song, *Student Member, IEEE*, Jingyu Hu, Xiaohong Li,
Edgar Sanchez-Sinencio, *Fellow, IEEE*, and Shouli Yan, *Member, IEEE*





$$g_{mT} = \sqrt{\beta}(\sqrt{I_{TAIL}} + \sqrt{I_{TAIL} - I_x} + \sqrt{I_x}) \quad (4)$$

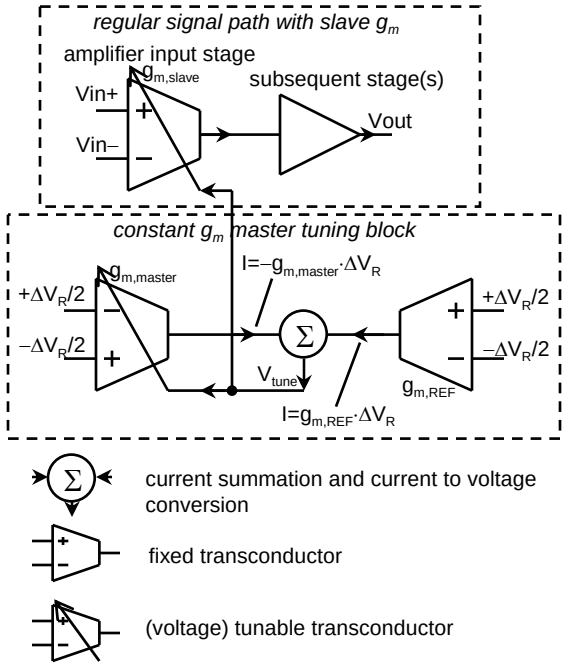
When $I_x = I_{TAIL}/2$, g_{mT} reaches its maximum value, given by:

$$g_{mT,max} = \sqrt{\beta I_{TAIL}}(1 + \sqrt{2}) = g_{mT,nom}\frac{1+\sqrt{2}}{2} \quad (5)$$

as illustrated in Fig. 2(b).

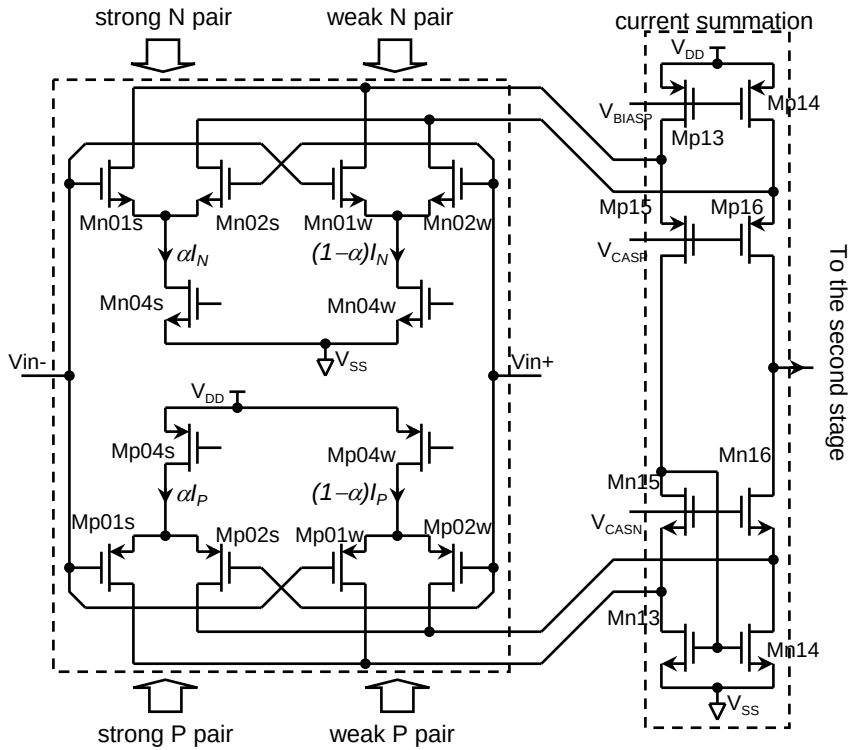
(b)

Fig. 2



$$k = \frac{I_X}{I'_X} = \frac{g_{m,X}}{g'_{m,X}} \qquad (6)$$

Fig. 3



$$m = \frac{(W/L)_{N,strong}}{(W/L)_{N,weak}} = \frac{(W/L)_{P,strong}}{(W/L)_{P,weak}} \qquad (7)$$

$$\begin{aligned} \beta_{strong} &= \mu_n C_{ox}(W/L)_{N,strong} \\ &= \mu_p C_{ox}(W/L)_{P,strong} \end{aligned} \qquad (8)$$

and similarly

$$\begin{aligned} \beta_{weak} &= \mu_n C_{ox}(W/L)_{N,weak} \\ &= \mu_p C_{ox}(W/L)_{P,weak} \\ &= \frac{1}{m}\beta_{strong} \end{aligned} \qquad (9)$$

Fig. 4 (old version)

The transconductance of the NMOS weak (narrow) pair is given by:

$$g_{mN,weak} = \sqrt{\frac{\beta_{strong}}{m}(1-\alpha)I_N} \tag{11}$$

The total transconductance of NMOS strong and weak composite pairs can be written as:

$$g_{mN} = (\sqrt{\alpha} + \sqrt{\frac{1-\alpha}{m}})\sqrt{\beta_{strong} I_N} = \sqrt{\beta_{eff} I_N} \tag{12}$$

where β_{eff} is defined as:

$$\beta_{eff} = (\sqrt{\alpha} + \sqrt{\frac{1-\alpha}{m}})^2 \beta_{strong} \tag{13}$$

Similarly, the total transconductance of PMOS strong and weak composite pairs is given by:

$$g_{mP} = (\sqrt{\alpha} + \sqrt{\frac{1-\alpha}{m}})\sqrt{\beta_{strong} I_P} \tag{14}$$

where I_P is the total bias current of PMOS composite input pairs.

Therefore, the total transconductance of the NMOS and PMOS composite pairs is given by:

$$g_{mT} = g_{mN} + g_{mP} = \sqrt{\beta_{eff}}(\sqrt{I_N} + \sqrt{I_P}) \tag{15}$$

If the sum of I_P and I_N is kept constant, as $I_P + I_N = I_{TAIL}$, $(\sqrt{I_N} + \sqrt{I_P})$ varies from $\sqrt{I_{TAIL}}$ to $\sqrt{2I_{TAIL}}$. This large g_m variation can be compensated for by changing the value of $\beta_{eff}/\beta_{strong}$ from 0.5 to 1, as shown in Fig. 6. For example,

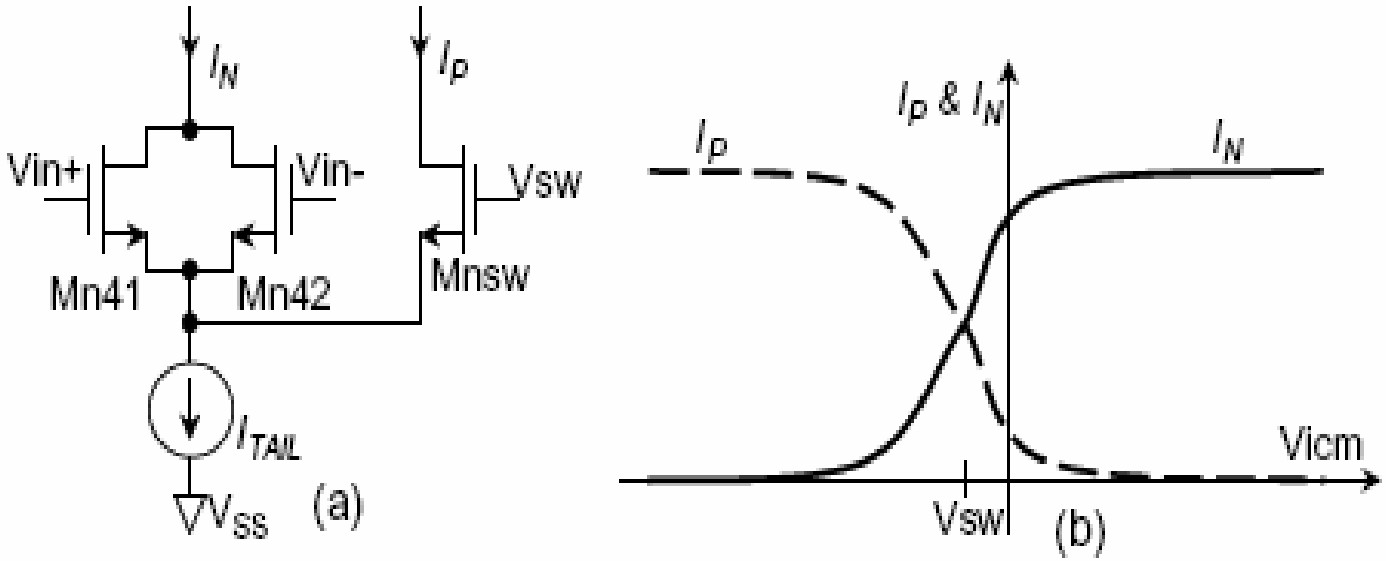


Fig. 5. Current switch circuit to keep $I_N + I_P$ constant; (a) schematic; (b) I_N and I_P vs. input common-mode voltage.

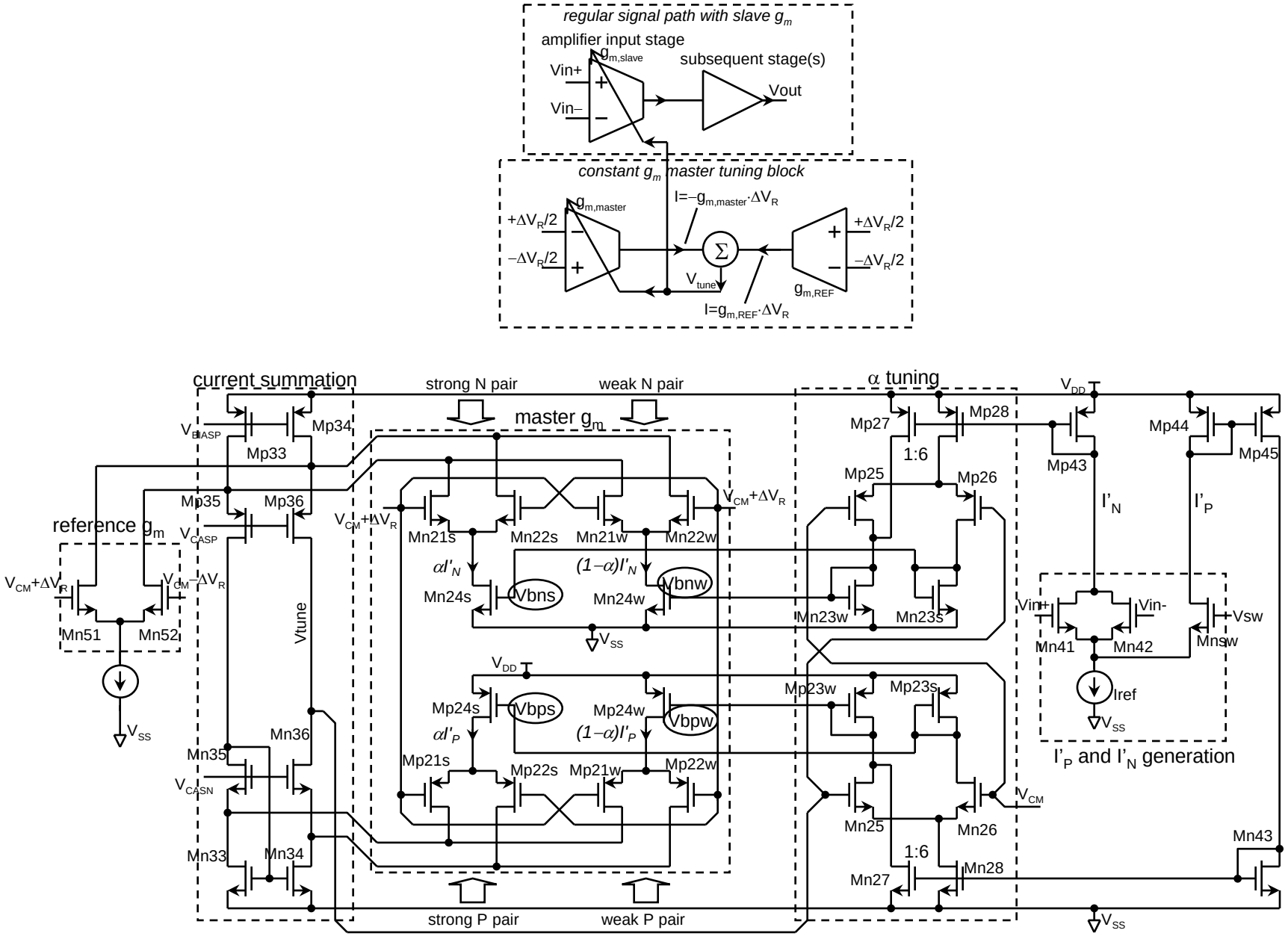

regular signal path with slave g_m
amplifier input stage
$g_{m,slave}$
Vin+
Vin–
subsequent stage(s)
Vout
constant g_m master tuning block
$g_{m,master}$
$I=-g_{m,master}\cdot\Delta V_R$
$+\Delta V_R/2$
$-\Delta V_R/2$
V_{tune}
$g_{m,REF}$
$I=g_{m,REF}\cdot\Delta V_R$
current summation
strong N pair
weak N pair
master g_m
α tuning
reference g_m
V_{BIASP}
V_{CASP}
V_{CASN}
$V_{CM}+\Delta V_R$
$V_{CM}-\Delta V_R$
Vtune
V_{DD}
V_{SS}
Mp33
Mp34
Mp35
Mp36
Mn21s
Mn22s
Mn21w
Mn22w
$\alpha I'_N$
$(1-\alpha)I'_N$
Mn24s
Vbns
Mn24w
Vbnw
Mp24s
Vbps
Mp24w
Vbpw
$\alpha I'_P$
$(1-\alpha)I'_P$
Mp21s
Mp22s
Mp21w
Mp22w
Mn51
Mn52
Mn35
Mn36
Mn33
Mn34
Mp27
Mp28
1:6
Mp25
Mp26
Mp43
Mp44
Mp45
I'_N
I'_P
Mn23w
Mn23s
Mp23w
Mp23s
Mn25
Mn26
Mn27
Mn28
Mn43
Vin+
Vin-
Vsw
Mn41
Mn42
Mnsw
Iref
I'_P and I'_N generation
strong P pair
weak P pair

Fig. 7

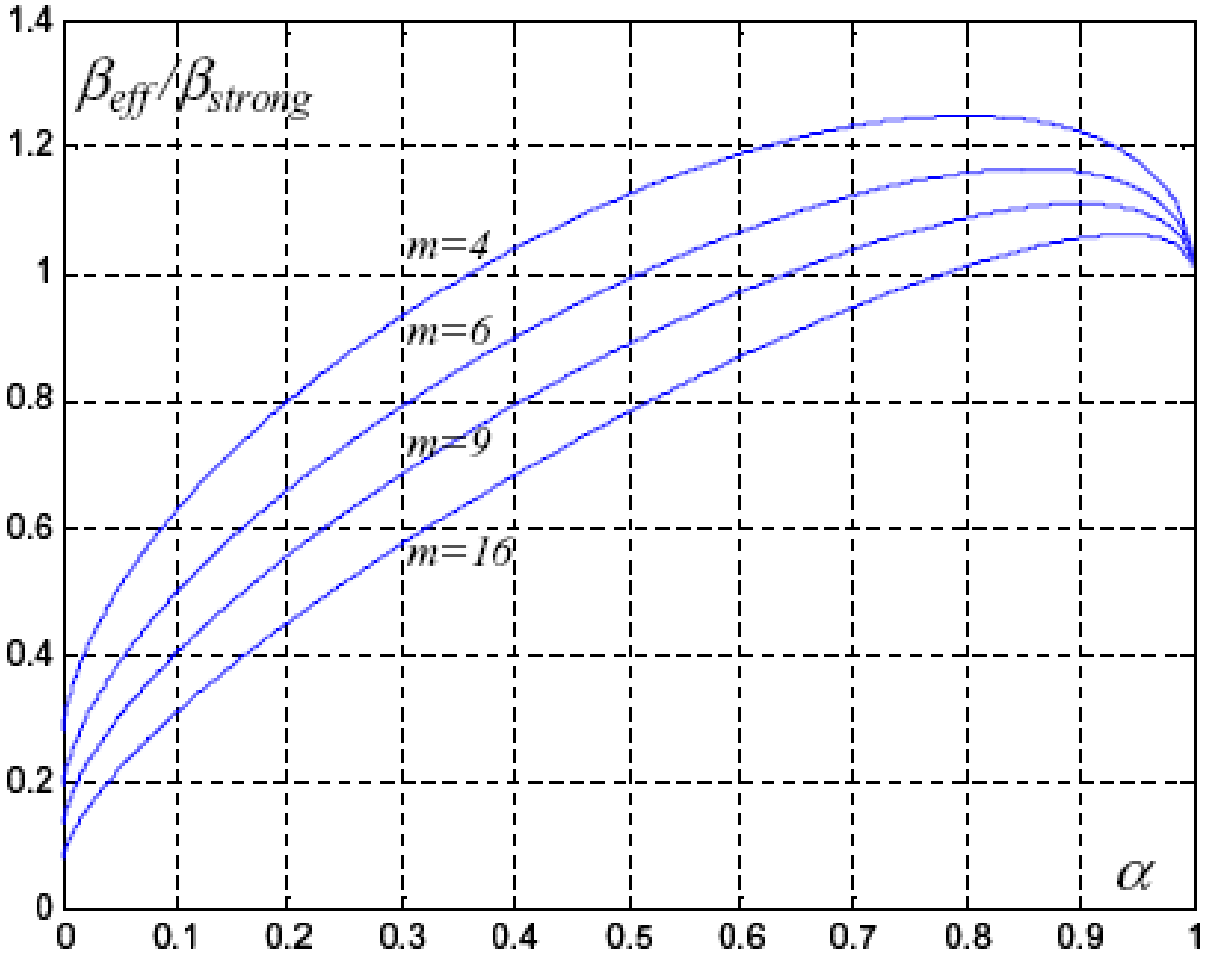


Fig. 6. $\beta_{eff}/\beta_{N,strong}$ vs. α for different values of m.

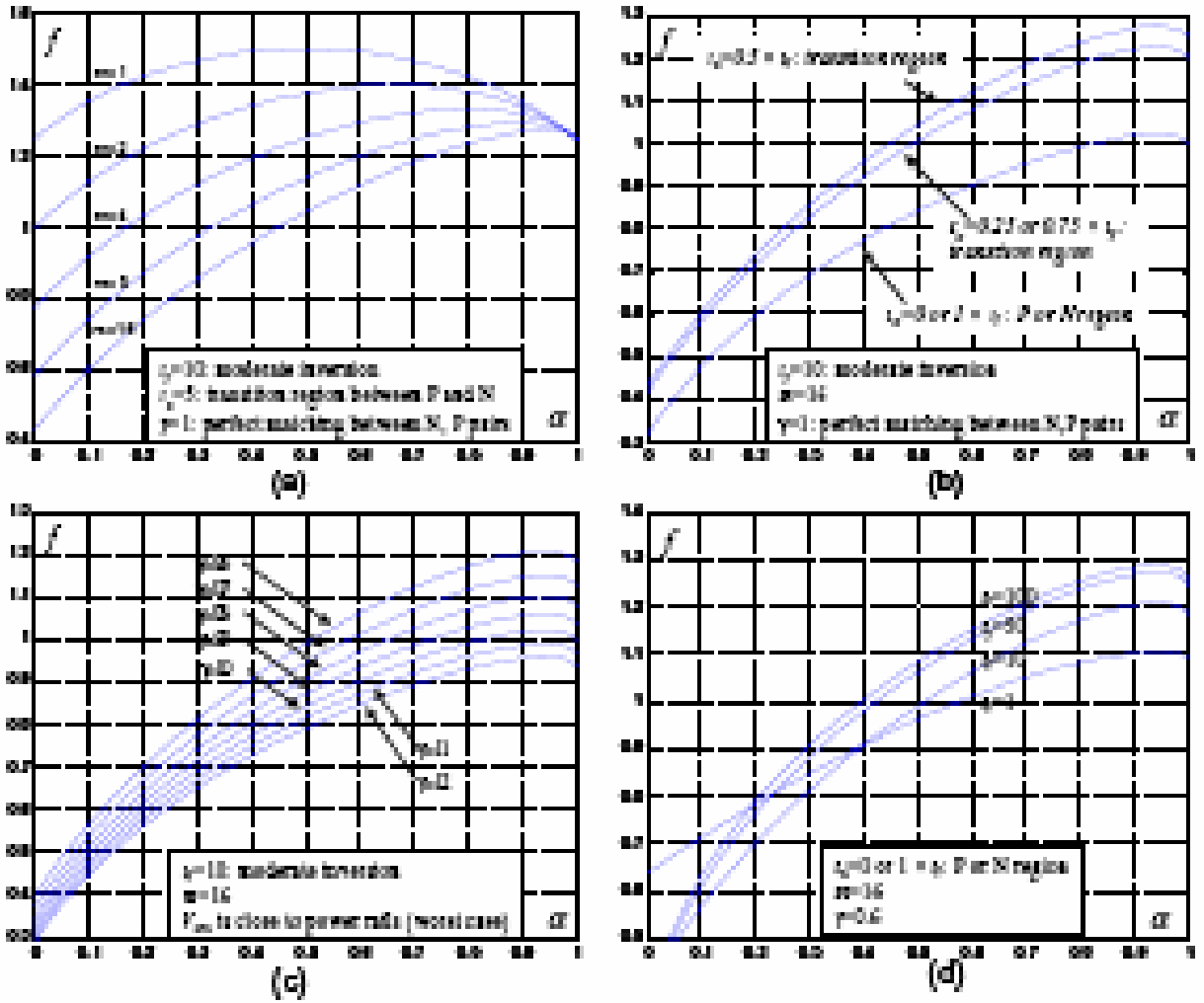


Fig. 8. Normalized total transconductance g_{mT} as a function of α; (a) f vs. α with different values of m; (b) f vs. α with different input common mode voltages; (c) f vs. α with process and temperature variations; (d) f vs. α with different operation region of input transistors.

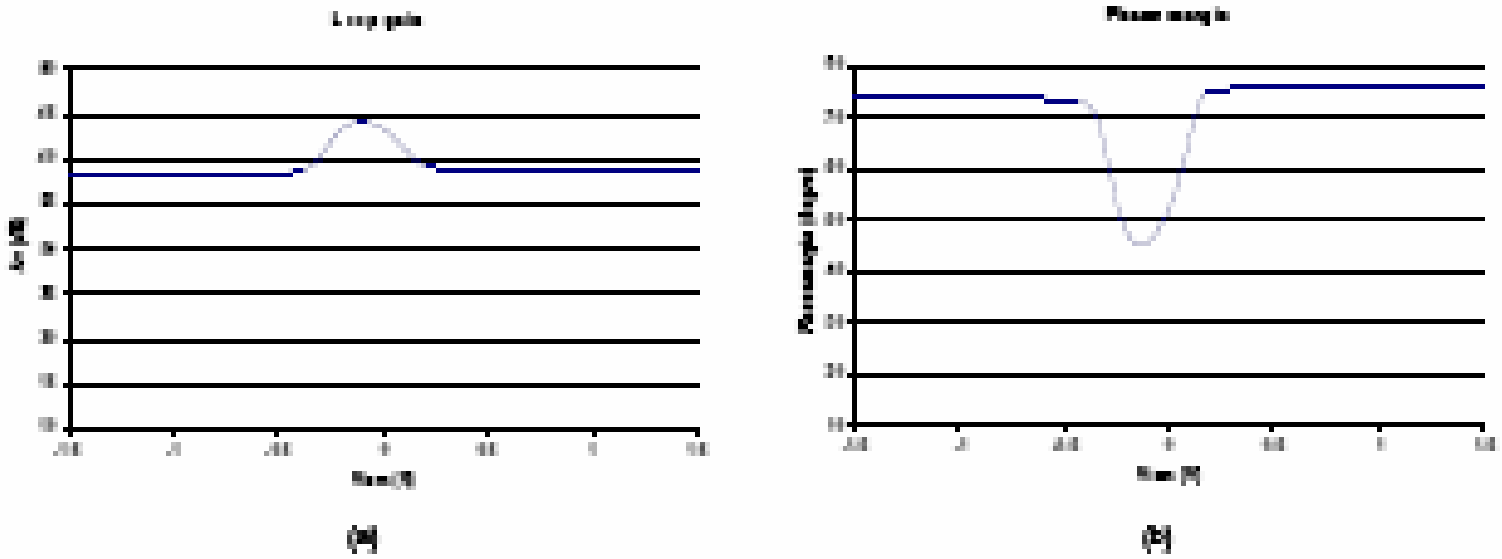


Fig. 10. Gain and phase of the dynamic feedback loop as a function of the input common mode voltage V_{cm}; (a) gain magnitude (in dB) vs. V_{cm}; (b) phase margin vs. V_{cm}.

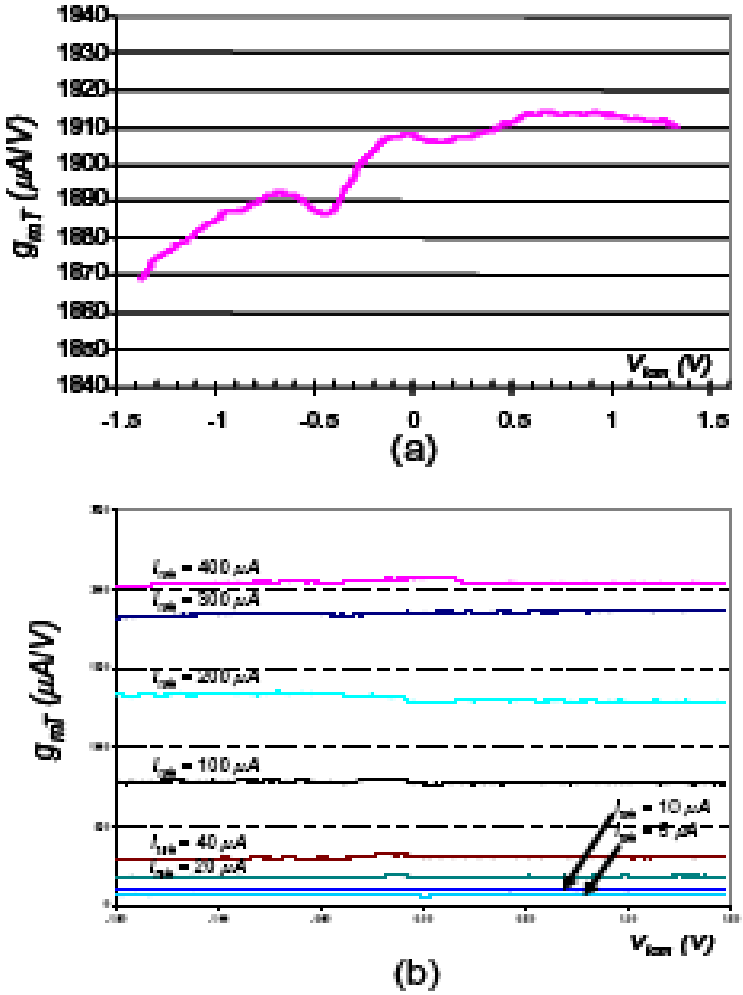


Fig. 12. Measured total transconductance g_{mT} vs. input common mode voltage V_{com}: (a) for a bias current I_{TAIL} = 300μA and (b) for a bias current I_{TAIL} varied from 400μA to 5μA.

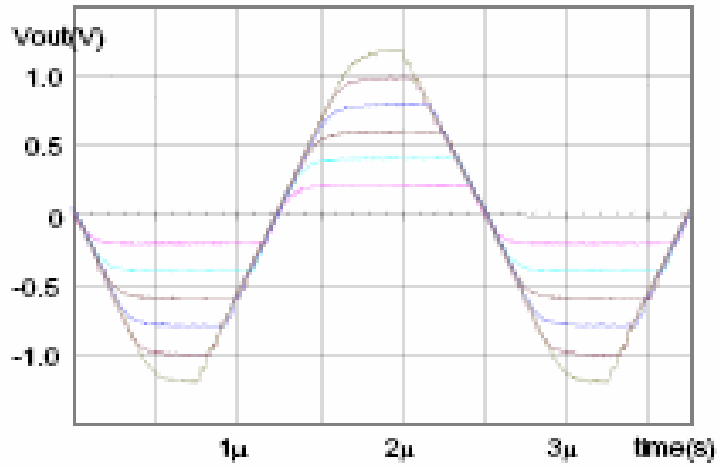


Fig. 13. Measured slew rate of the opamp in noninverting unity-gain configuration (CL=130 pF). The input is a 400 kHz square wave. Vertical axis: 0.5 V/div, horizontal axis: 0.5 µs/div.

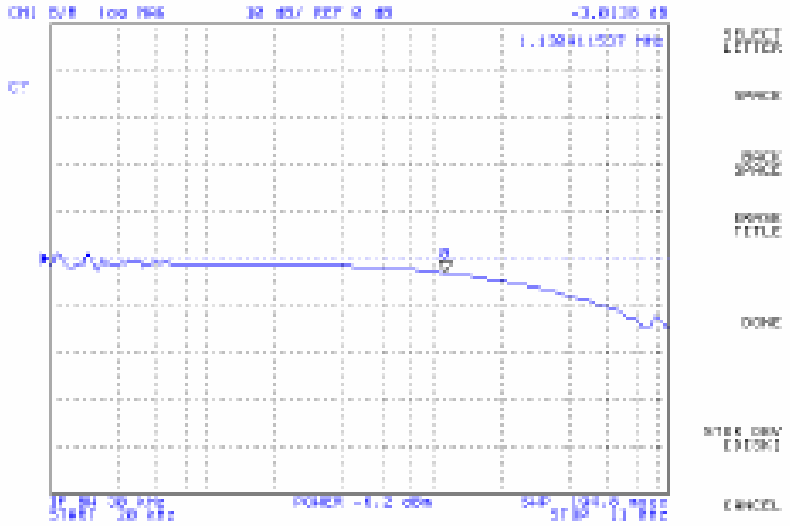


Fig. 14. Measured frequency response of the opamp in noninverting unity-gain configuration (load capacitance CL=150pF).

TABLE I

SUMMARY OF THE MEASURED PERFORMANCE

Transconductance g_{mT}	1.895±0.025 mA/V
Nominal bias current	300μA
DC open loop voltage gain	> 80 dB
Unity gain frequency	1.1 MHz (CL = 180 pF)
Phase margin	89°
Settling time of common-mode loop	2μs
Supply voltage	3 V
Power consumption	3.3 mW
CMRR	> 50 dB
PSRR	> 50 dB
Slew rate+ / Slew rate -	2.52/2.43 V/μs (CL = 130 pF)
Input referred noise @ 100KHz / 1MHz	48.4/21.0 $nV/\sqrt{Hz}$
Input referred offset	-6mV to 3mV; 1mV to 4mV variation from rail to rail
Active area	0.09 mm^2
Technology	4-metal 2-poly 0.35μm CMOS

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