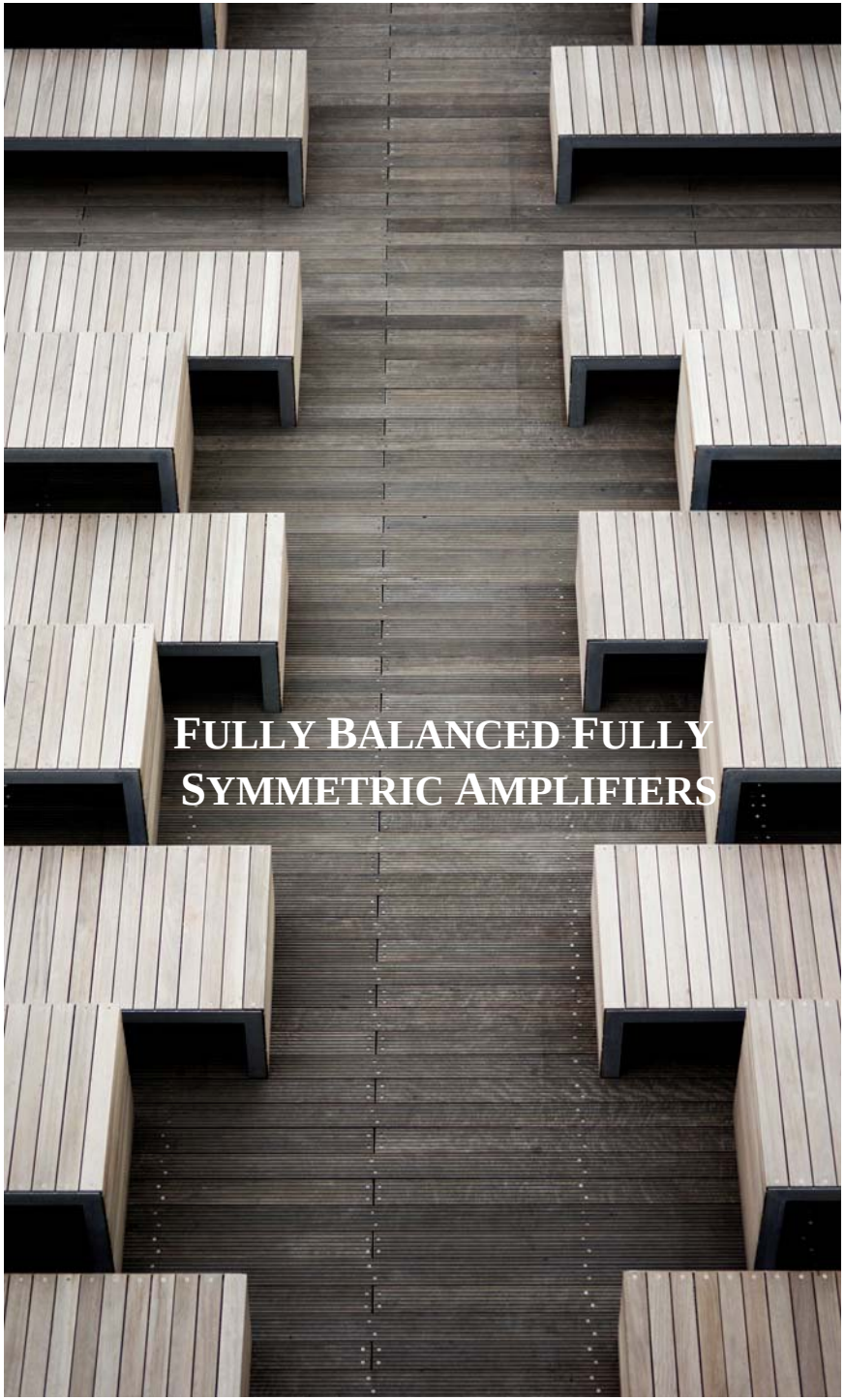
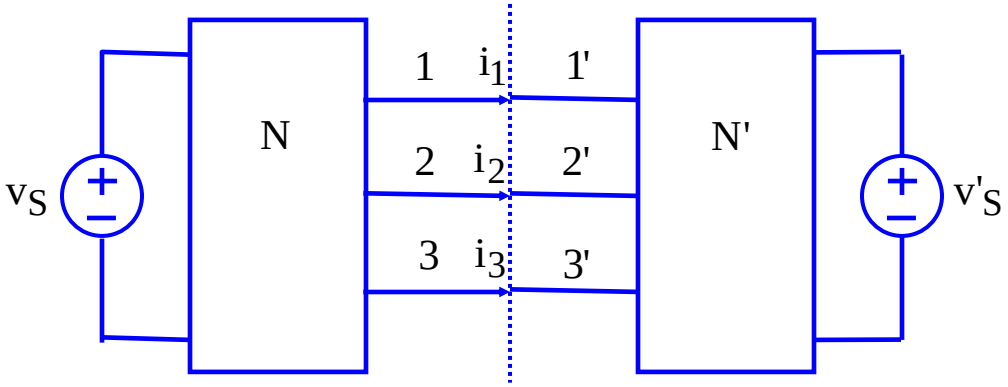
Analog and Mixed-Signal Center



FULLY BALANCED FULLY SYMMETRIC AMPLIFIERS

ECEN 607
Edgar Sánchez-Sinencio

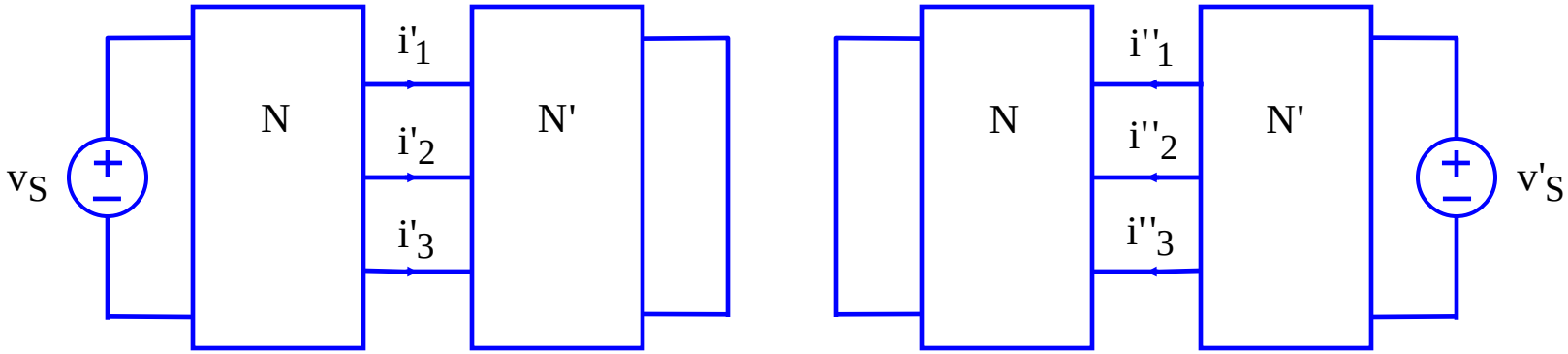
Symmetrical Circuits



N and N' are identical.
Vs and V's can be equal or opposite in sign

Symmetrical Circuit

Common-Mode Input Signals: $V_S = V'_S$



Application of Superposition

$$\left.\begin{aligned} i_1 &= i'_1 + i''_1 \\ i_2 &= i'_2 + i''_2 \\ i_3 &= i'_3 + i''_3 \end{aligned}\right\} \quad \text{Now since} \quad v_S = v'_S$$

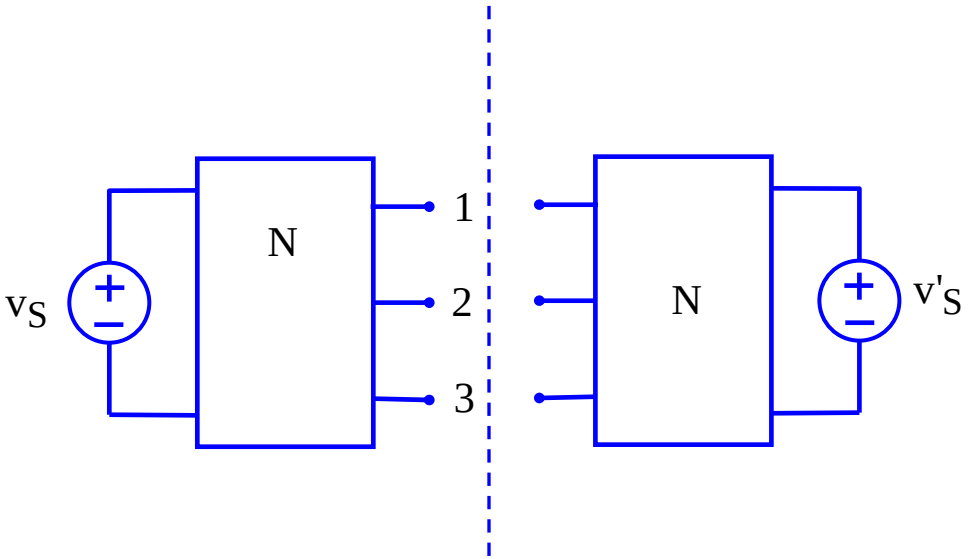
$$i'_j = -i''_j \quad , \quad j = 1,2,3$$

$$\text{so } i_j = 0 \quad , \quad j = 1,2,3$$

So we can simplify the analysis to half circuit for equal (common) inputs.

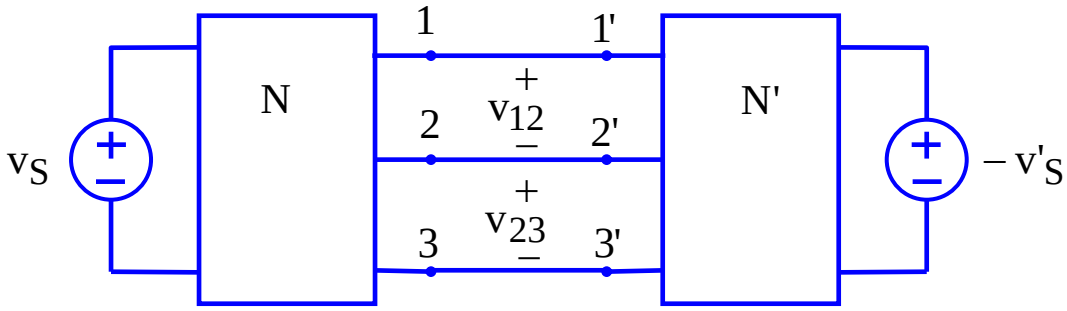
Common-Mode Equivalent Circuit $V_S = V'_s$

Since the current between blocks are zero, when equal signals are applied $V_S = V_S'$ the line of symmetry can be open. Thus we can just analyze half of the open circuit for common mode signals.



Symmetrical Input (common-mode)

Differential-Mode Input Signals



For anti -symmetrical inputs (differential)

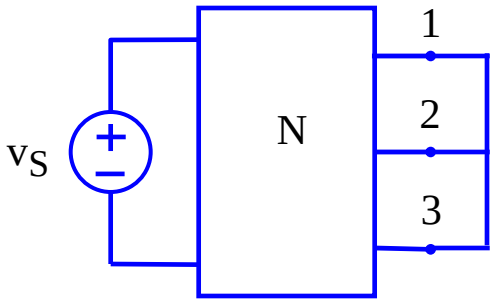
Superposition can be applied, thus, the voltages between any pair of terminals on the axis of symmetry is :

$$v_{ij} = v'_{ij} + v''_{ij}$$

However, symmetry conditions yield :

$$v'_{ij} = -v''_{ij}$$

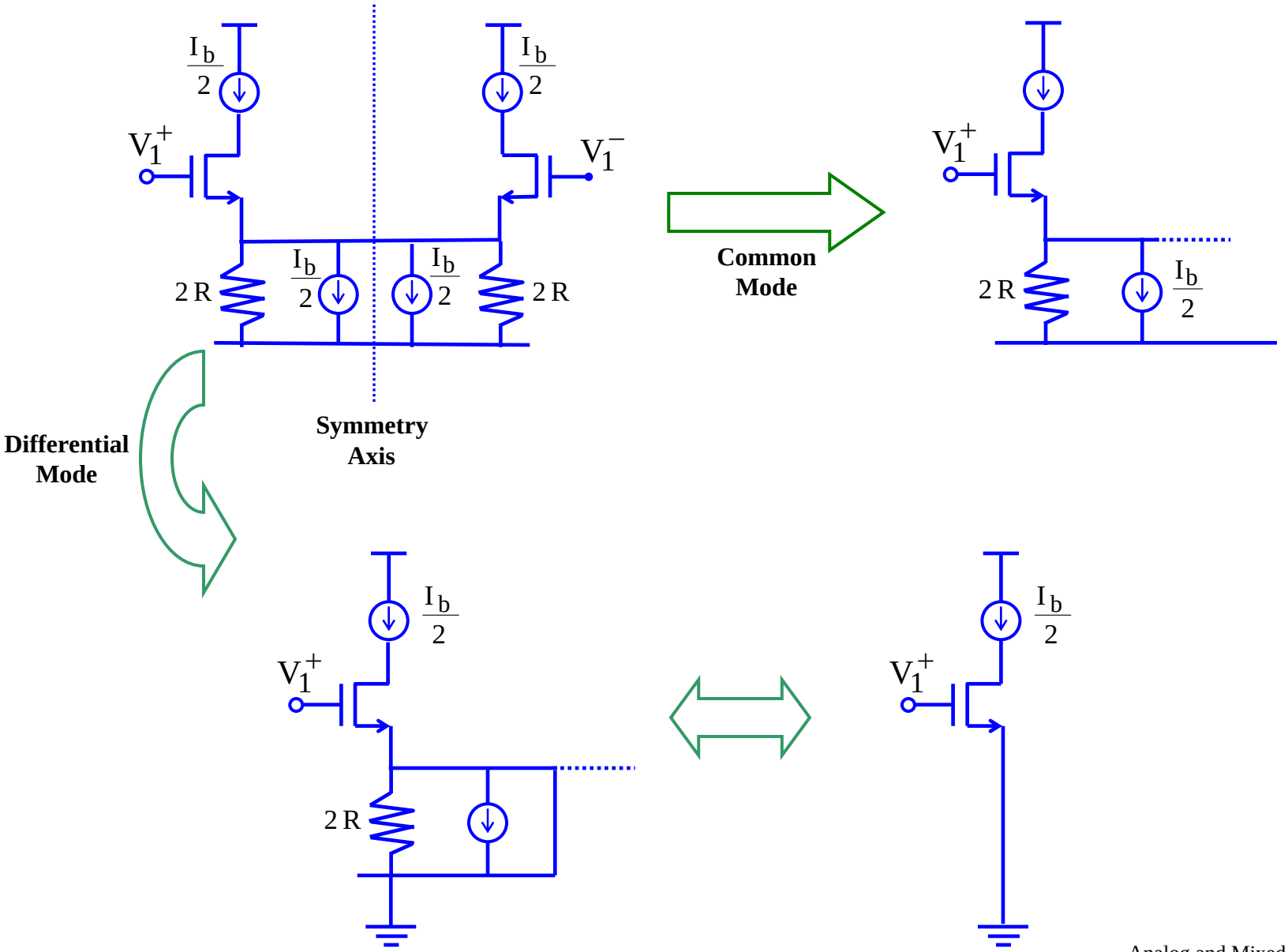
Therefore, the equivalent half circuit becomes



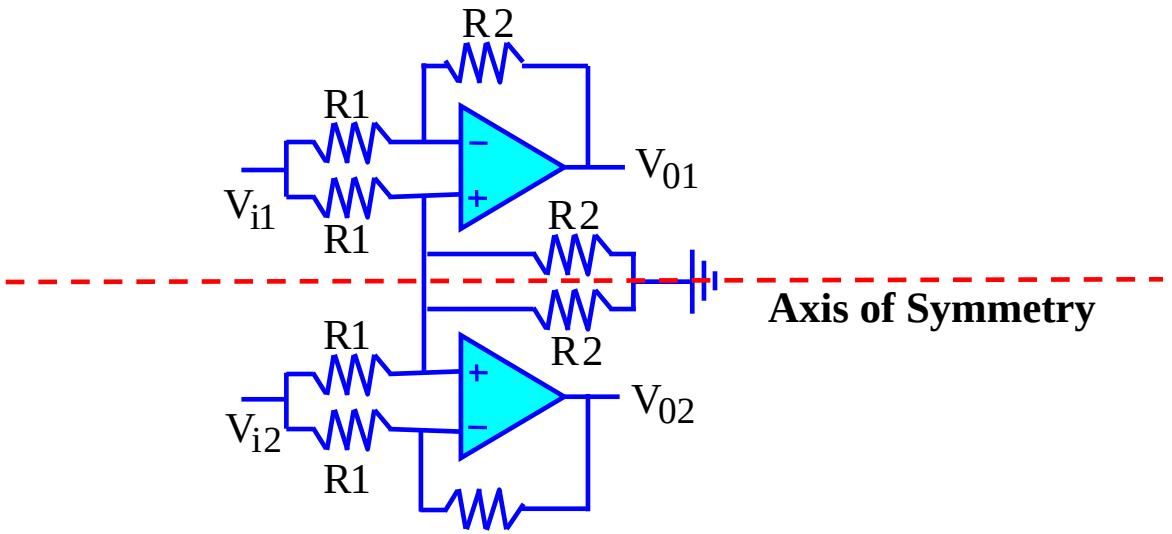
Line of symmetry is shorted

Antisymmetrical Input (Differential-mode)

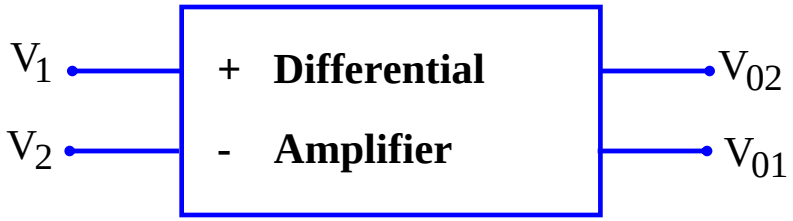
Example of a Symmetric Circuit



Another example of Symmetric Circuits



What are the differential gain, and the common mode gain ?



A fully differential amplifiers have both input and output differential.
Next let us assume a single-ended output V_0 , then

$$V_0 \cong (V_1 - V_2)A_d + \frac{V_1 + V_2}{2} A_C$$

$$V_0 = v_{id}A_d + v_{iC}A_C$$

Ideally $A_C \to 0$ then $V_0 = A_d v_{id}$

What is needed for a fully differential system to operate properly?

- **A control for the output amplifier (CM) component must be provided by an additional internal feedback network (CMF) which must satisfy:**

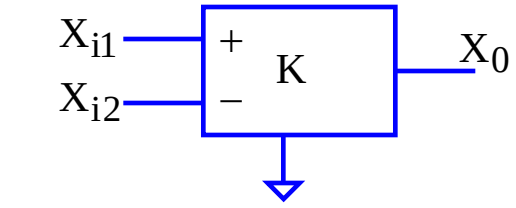
i) Capability to set the output CM to a V_{ref} , i.e. , optimal V_{ref} value occurs where the maximum DM gain is obtained.

ii) Speed and accuracy of CM and DM loops must be similar

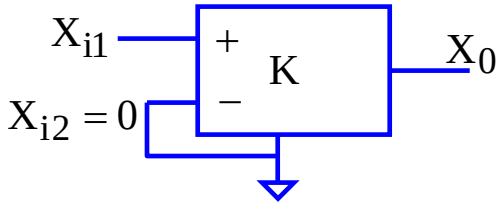
iii) Minimization of interaction between CM- and DM-output components.

FULLY BALANCED SYSTEMS

I) Single-Ended.
II) Differential-Ended.
III) Balanced-Ended also called Fully Balanced.



(a)



(b)

(a) Block diagram of a single-ended system, **(b)** practical application of single-ended system.

$$X_0 = K(X_{i1} - X_{i2}) \qquad (A \cdot 1)$$

$$X_{iCM} = \frac{X_{i1} + X_{i2}}{2}\ , \qquad (A \cdot 2)$$

and a differential - mode input signal given by :

$$X_{iDM} = \frac{X_{i1} - X_{i2}}{2}\ . \qquad (A \cdot 3)$$

$$X_{i1} = X_{iCM} + X_{iDM} \qquad (A \cdot 4)$$

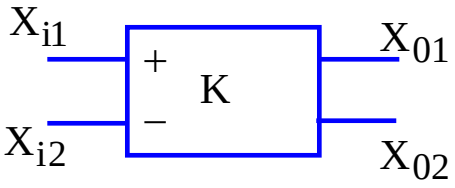
$$X_{i2} = X_{iCM} - X_{iDM} \qquad (A \cdot 5)$$

Inserting $X_{i2} = 0$ and $(A \cdot 4)$ into $(A \cdot 1)$ the practical single - ended system shown in Fig. $A \cdot 1(b)$ is described by :

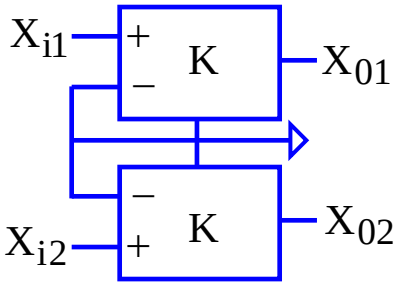
$$X_0 = K(X_{iCM} + X_{iDM}) \qquad (A \cdot 6)$$

Note that X_0 can not discriminate X_{iCM}. Both inputs CM and DM are equally treated.

Differential (Double-) Ended System



(a)



(b)

(a) Block diagram of a differential-ended system, **(b)** example of differential system which is not balanced

$$X_{01} - X_{02} = K(X_{i1} - X_{i2}) \qquad (A \cdot 7)$$

A common - mode output signal given by :

$$X_{0CM} = \frac{X_{01} + X_{02}}{2} \qquad (A \cdot 8)$$

and a differential - mode output signal given by :

$$X_{0DM} = \frac{X_{01} - X_{02}}{2} \qquad (A \cdot 9)$$

From $(A \cdot 8)$ and $(A \cdot 9)$ the differential system in Fig. 2(b) is described as follows

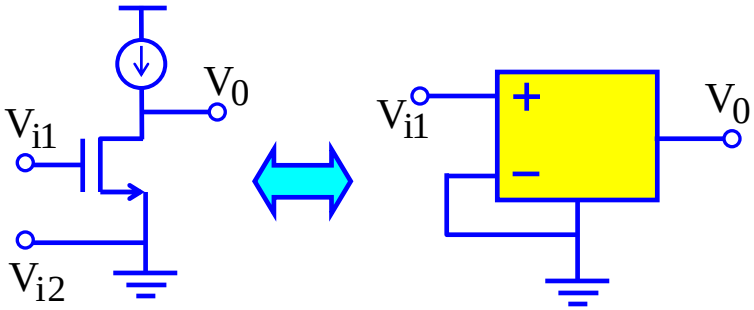
$$X_{0DM} = K\frac{X_{i1} - X_{i2}}{2} = KX_{iDM} \qquad (A \cdot 10)$$

$$X_{0CM} = K\frac{X_{i1} + X_{i2}}{2} = KX_{iCM} \qquad (A \cdot 11)$$

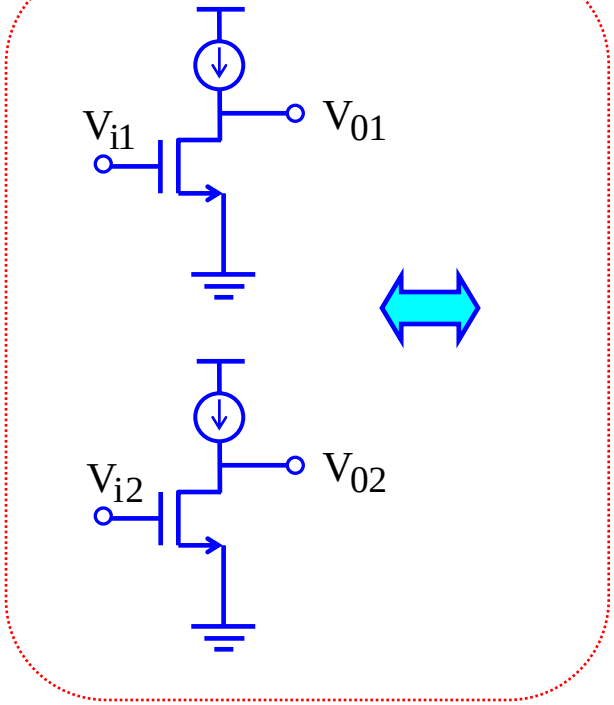
Although the differential output signal $(X_{01} - X_{02})/2$ of a system in Fig. $A \cdot 2$(b) does not depend on the common - mode signal $(X_{i1} + X_{i2})/2$ (as required for a performance improvement), an unwanted common - mode input signal X_{iCM} is still transmitted to the output.

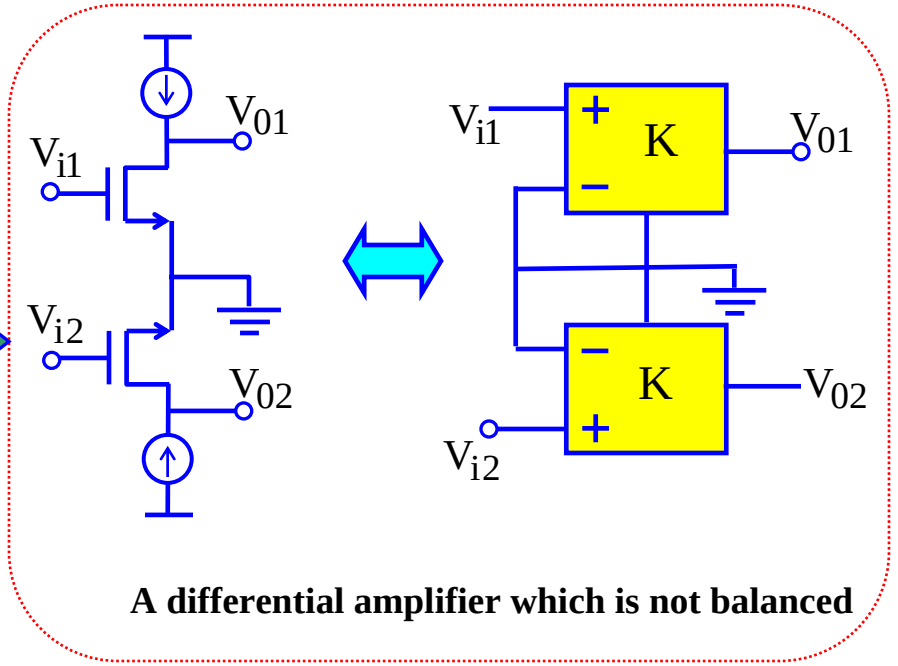
Not all differential systems are balanced, although all balanced systems are differential.

Example of single- and differential-ended



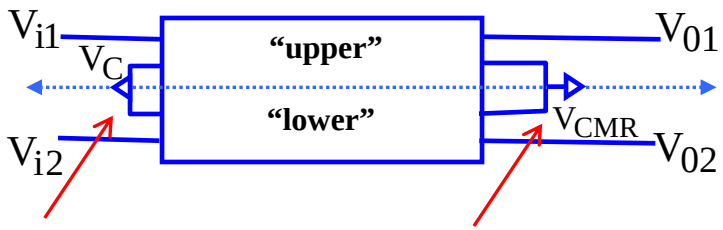
Single-ended amplifier





A differential amplifier which is not balanced

Fully Balanced Systems Using Single-Ended Op Amps.



V_C is a voltage at node,which is or can be employed to control a common-mode output voltage $(V_{01}+V_{02})/2$

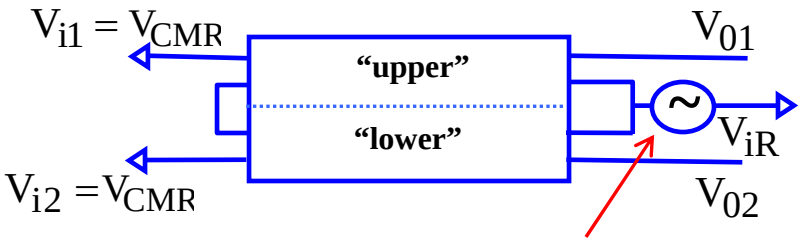
V_{CMR} is a constant reference voltage

Conditions for a FB system

$$V_{01}(s) - V_{02}(s) = K(s)\left[V_{i1}(s) - V_{i2}(s)\right], \qquad (1)$$

$$V_{01}(s) + V_{02}(s) = 2V_{CMR}\,(=0), \qquad (2)$$

Basic concept of an FB System



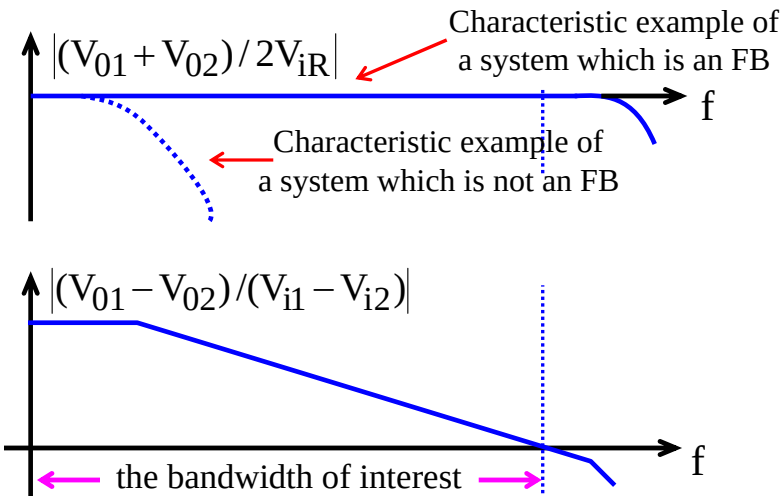
V_{iR} is an input voltage

If $V_{i1} = V_{i2} = 0$ and $V_{CMR} = V_{iR}(w)$, then (2) yields:

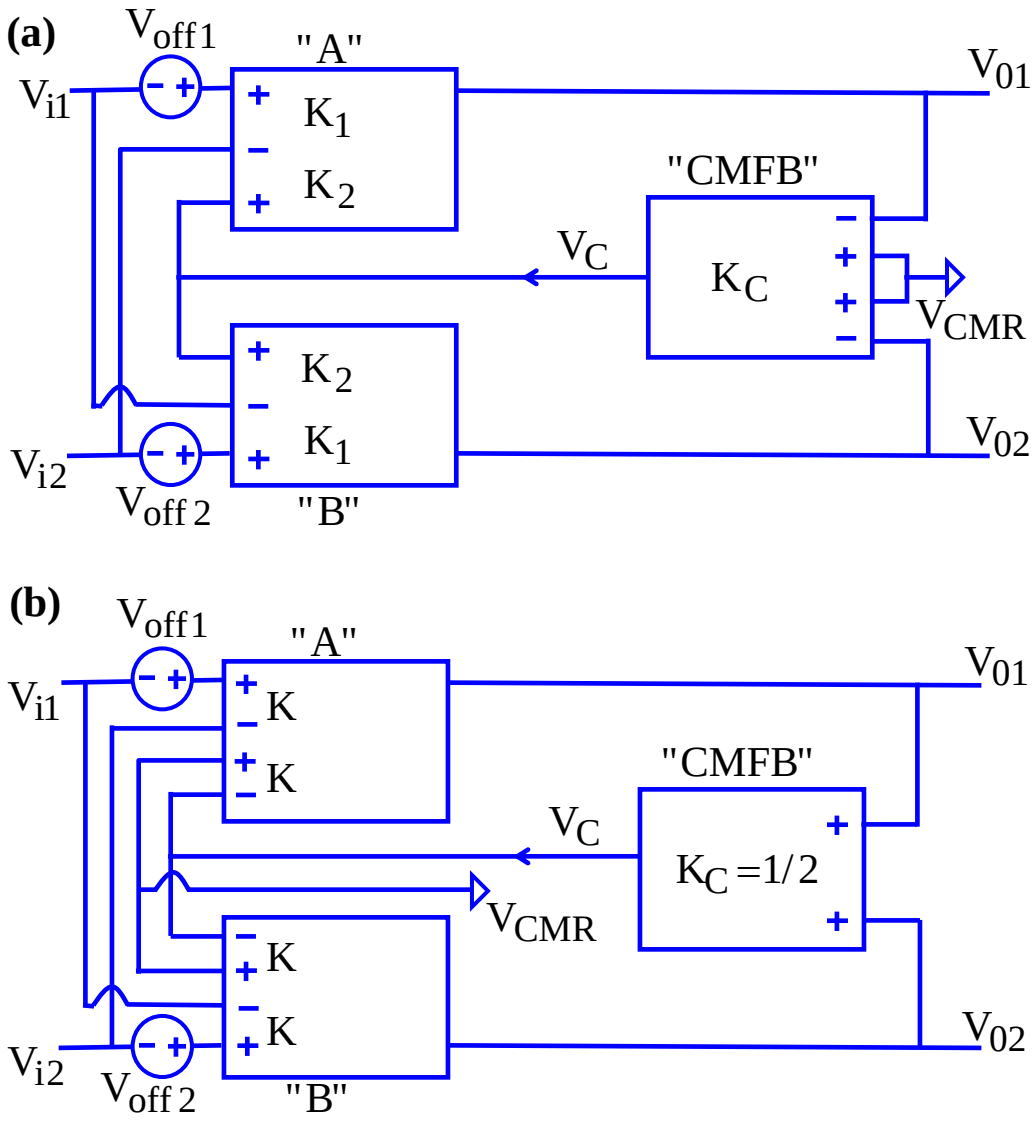
$$\frac{\left[V_{01}(s) + V_{02}(s)\right]/2}{V_{iR}(s)} = 1 \qquad (3)$$

A method of a quality evaluation of a fully balanced system.

Bandwidth of CMF vs DM



How to Design Fully Balanced system based on a single-ended system?



(a) Classical architecture of an FB system with CMFB,
(b) Modified architecture of an FB system with CMFB. (not difficult to implement).

CM output voltage $(V_{01}+V_{02})/2$, and an FB system can be implemented with a CM feedback (CMFB) path, as shown in Fig.

$$V_{01}(s) = K_1(s)\left[V_{i1}(s) - V_{i2}(s) + V_{off1}\right] + K_2(s)V_C, \quad (4)$$

$$V_{02}(s) = K_1(s)\left[V_{i2}(s) - V_{i1}(s) + V_{off2}\right] + K_2(s)V_C, \quad (5)$$

$$V_{01}(s) - V_{02}(s) = 2K_1(s)\left[V_{i1}(s) - V_{i2}(s)\right] + K_1(s)(V_{off1} - V_{off2}), \quad (6)$$

$$V_{01}(s) + V_{02}(s) = 2K_2(s)V_C(s) + K_1(s)(V_{off1} + V_{off2}), \quad (7)$$

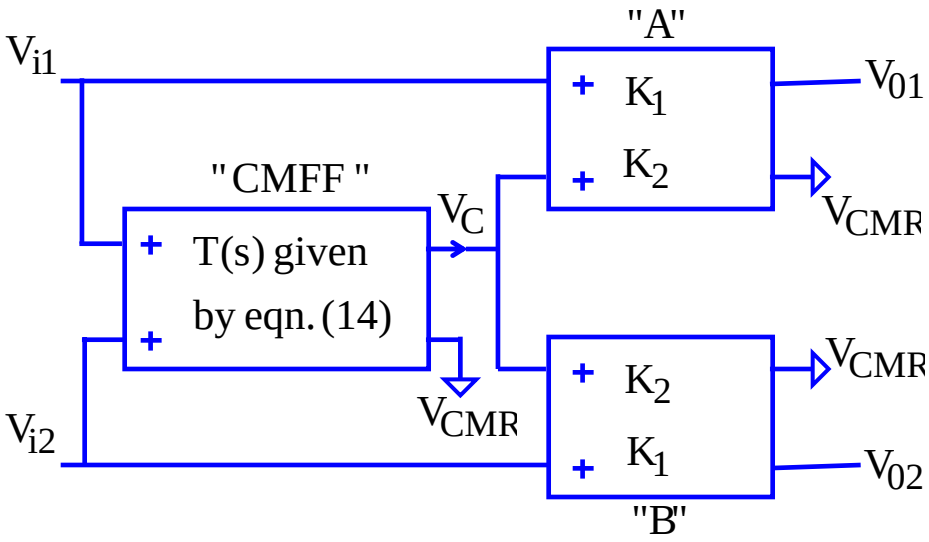
$$V_C(s) = -K_C(s)\left[V_{01}(s) + V_{02}(s)\right]. \quad (8)$$

Inserting (8) into (7) we obtain

$$V_{01}(s) + V_{02}(s) = \frac{K_1(s)\cdot(V_{off1} + V_{off2})}{1 + 2K_C(s)K_2(s)}. \quad (9)$$

Compare (9) to (2). Difficult to satisfy.

Fully Balanced based on CM feedforward



An architecture of an FB system with CMFF

$$V_{01}(s) = K_1(s)V_{i1}(s) + K_2(s)V_C(s), \qquad (10)$$

$$V_{02}(s) = K_1(s)V_{i2}(s) + K_2(s)V_C(s), \qquad (11)$$

The relations (10) and (11) can be rewritten as follows :

$$V_{01}(s) - V_{02}(s) = K_1(s)[V_{i1}(s) - V_{i2}(s)], \qquad (12)$$

$$V_{01}(s) + V_{02}(s) = K_1(s)[V_{i1}(s) + V_{i2}(s)] + 2K_2(s)V_C(s). \qquad (13)$$

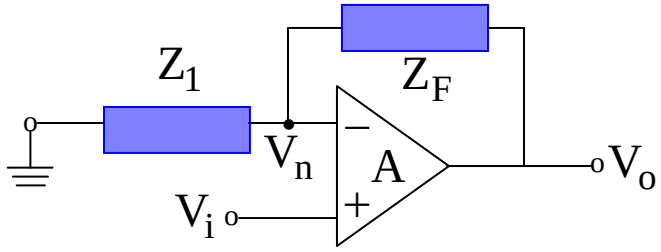
Comparing (13) to (2) we conclude that in a fully balanced system (i.e. with $V_{01} = -V_{02}$) under the architecture in Fig. the transfer funtion T(s) implemented by the CMFF block must be given as follows

$$T(s) = \frac{V_C(s)}{V_{i1}(s) + V_{i2}(s)} = -\frac{K_1(s)}{2K_2(s)}. \qquad (14)$$

CM input voltage (V_{i1}+V_{i2})/2, and an FB system can be implemented with a CM feedforward (CMFF) path, as shown in Fig.

Fully Differential Fully Balanced Circuits

What is the problem with single-input / single-output?



$$V_n = \frac{V_o Z_1}{Z_1 + Z_F}$$

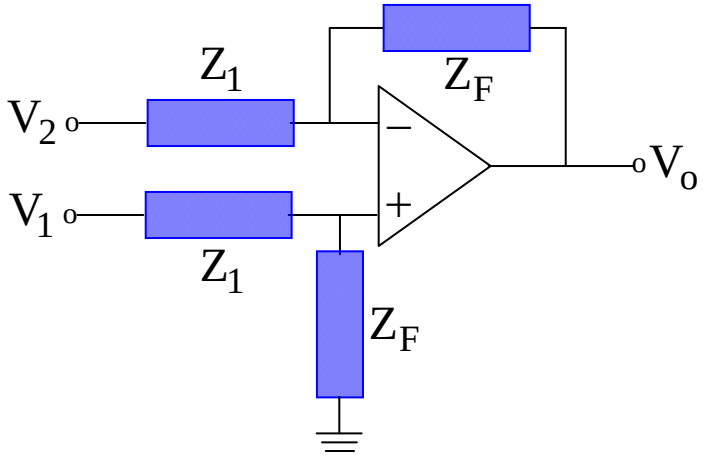
$$V_1 - V_n = \frac{V_o}{A}\Bigg|_{A \to \infty} = 0$$

For $V_i = V_{id} + V_{icm}$

$$V_o = \left(1 + \frac{Z_F}{Z_1}\right)(V_{id} + V_{icm})$$

No elimination of common-mode signal.

How to solve this problem?



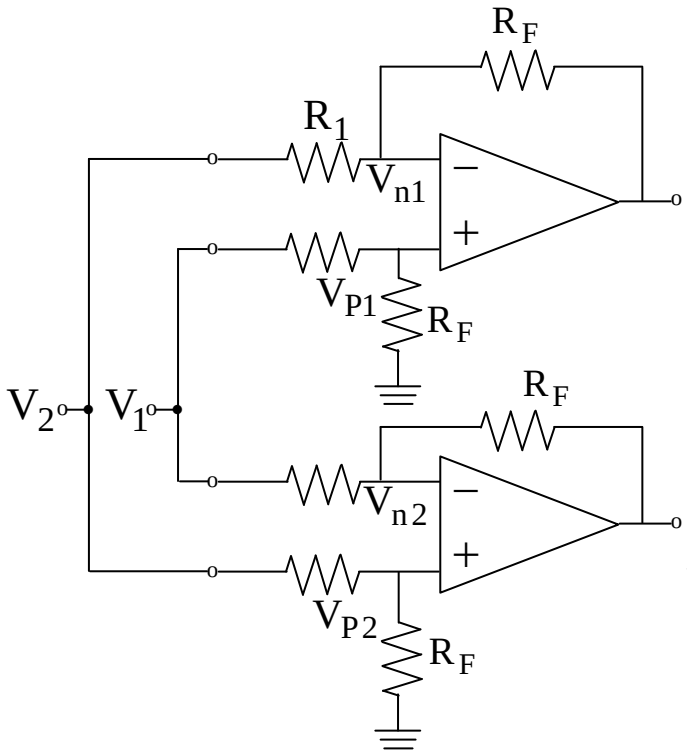
For $V_i = V_{id} + V_{icm} = (V_1 - V_2) + \frac{(V_1 + V_2)}{2}$

$$V_o = \frac{Z_F}{Z_1}(V_1 - V_2)$$

No common-mode output.

How to obtain a fully differential circuit?
We will discuss two potential approaches

Approach 1



$$V_{o1} = -\frac{R_F}{R_1}(V_2 - V_1)$$

$$= \frac{R_F}{R_1}(V_1 - V_2)$$

$$V_{o2} = +\frac{R_F}{R_1}(V_2 - V_1)$$

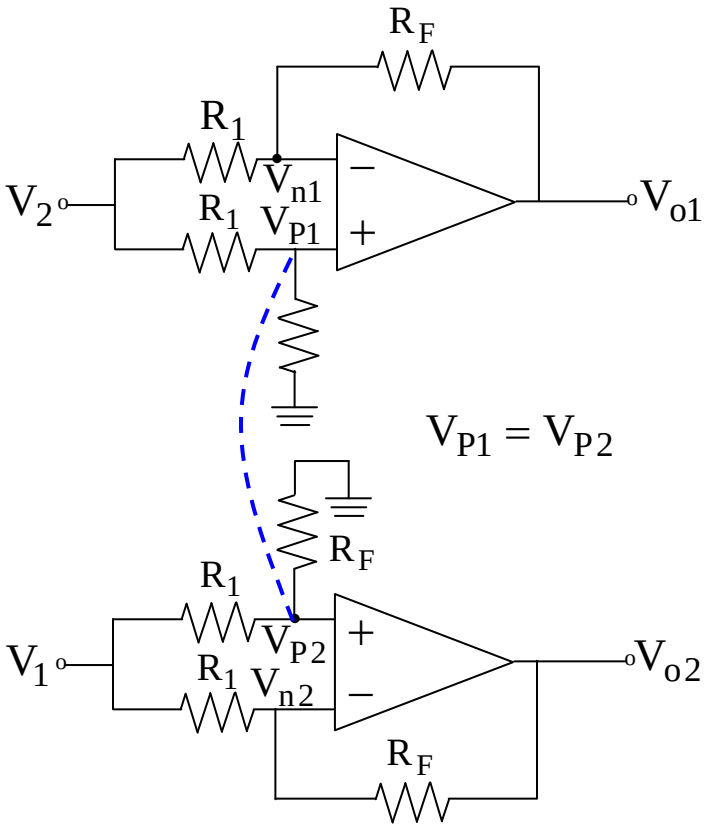
$$V_{o1} - V_{o2} = \frac{R_F}{R_1}(V_1 - V_2 - V_2 + V_1) =$$

$$V_{oD} = \frac{2R_F}{R_1}(V_1 - V_2)$$

conditions $V_{n2} = V_{P2}$; $V_{n1} = V_{P1}$

Remark: sensitive to CM signals

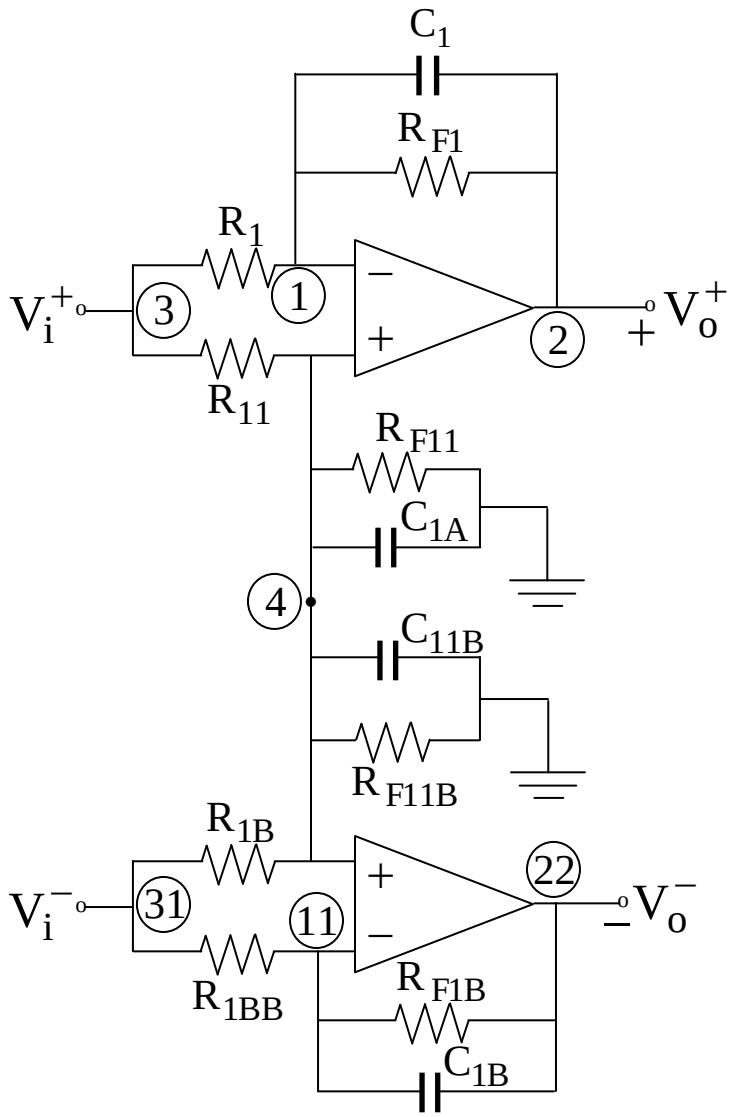
Approach 2



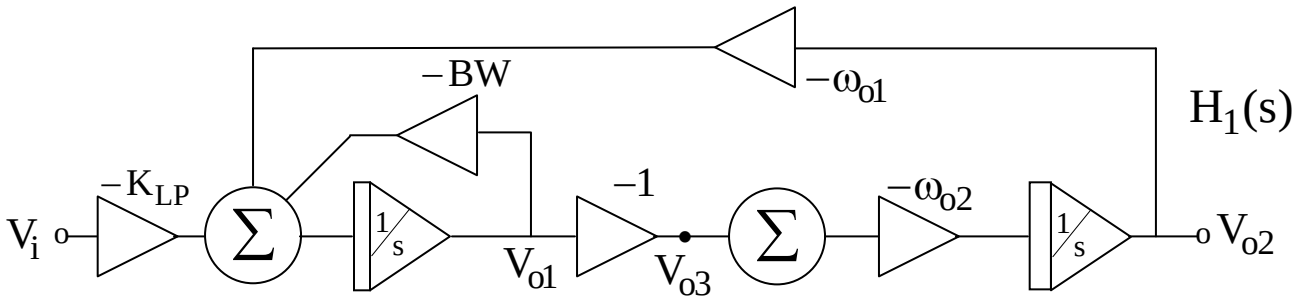
Remark:
More robust to reject
common-mode signals

First-Order FB Low Pass with Op Amp

```
*
.subckt opamp non inv out
rin non inv 100K
egain       1       0       (non, inv)    200K
ropen       1       2       2K
copen  2    0       15.9155u
eout   3    0       (2, 0)   1
rout    3     out    50
.ends
*vin          3      31      ac      1.0
vin      31  0   ac   1.0
x1       4       1       2       opamp
x2       4       11      22      opamp
R1       3       1       1K
R11      3       4       1K
R1B      31      4       1K
R1BB 31      11      1K
RF1      2       1       1K
RF1B 22      11      1K
RF11  4       0       1K
RF11B         4       0       1K
C1       2       1       0.159155u
C1B   22       11      0.159155u
C1A   4        0       0.159155u
C11B 4         0       0.159155u
rdummy  3     31     1
.ac   dec   10    10Hz   10KHz
.probe
.end
```

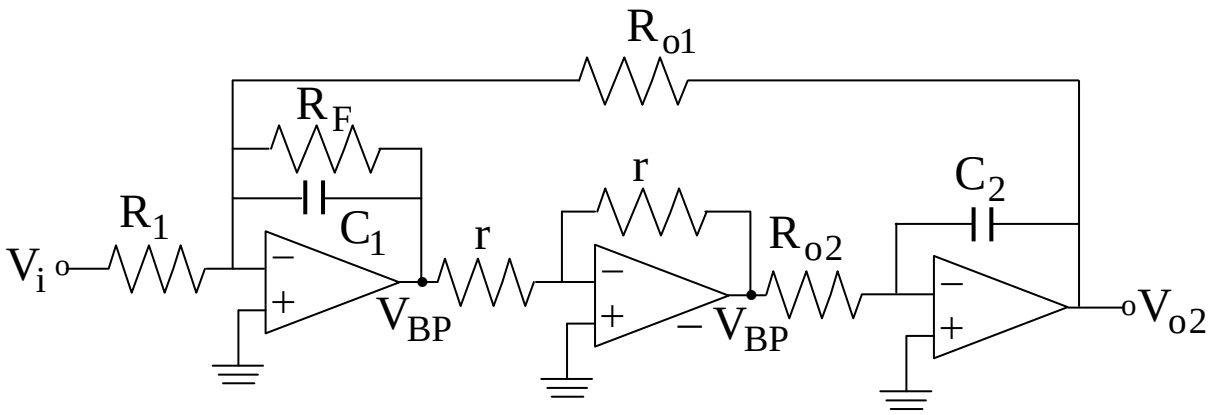


A Two-Integrator Active-RC Filter

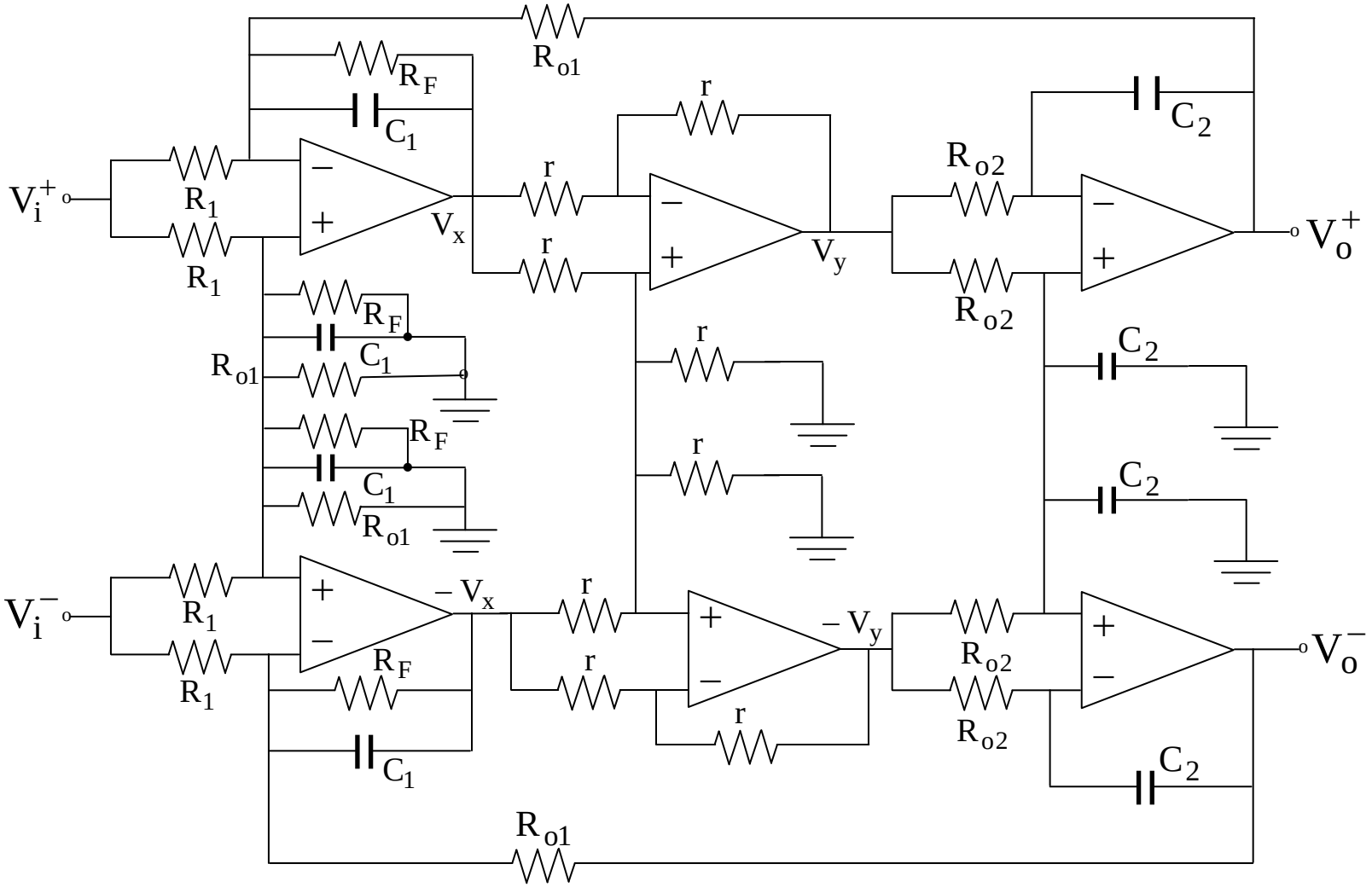


$$H_1(s) = \frac{V_{o2}}{V_i} = \frac{-K_{LP}\omega_{o2}}{s^2 + BWS + \omega_{o1}\omega_{o2}}$$

(a) Block Diagram

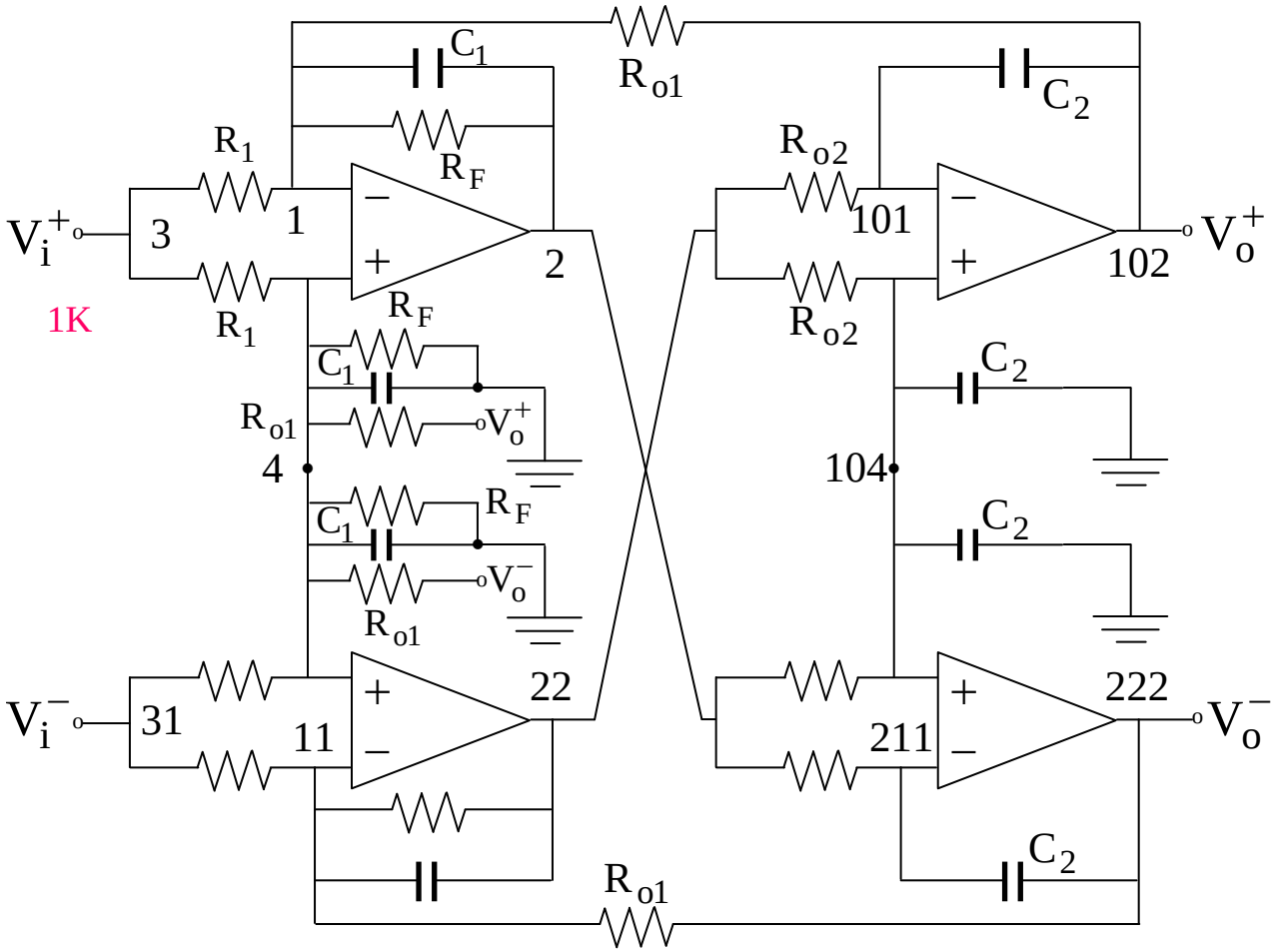


(b) Active RC Implementation (single-ended)



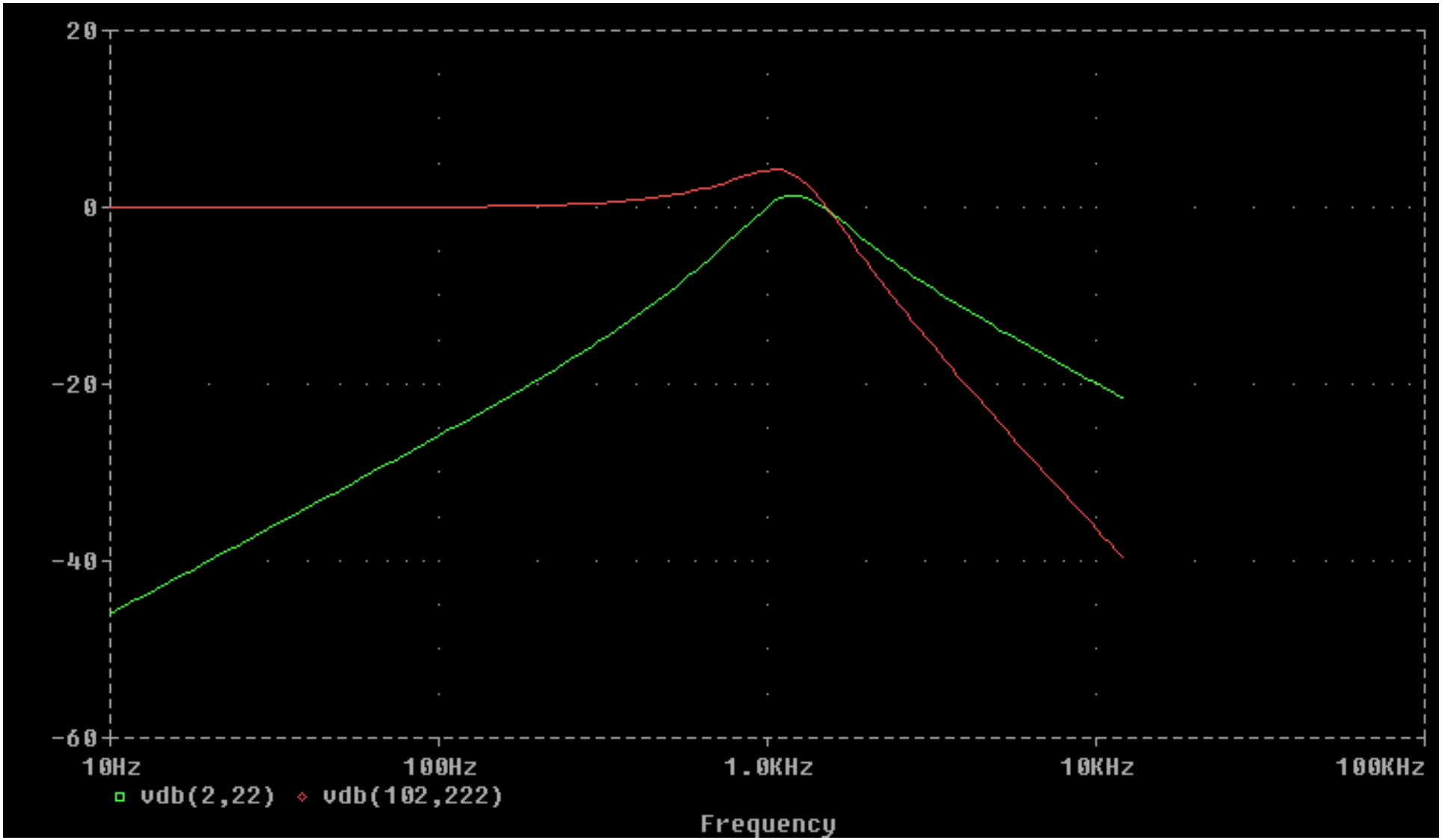
(c) Fully Balanced, Fully-Differential (not simplified)

```
Second-Order FB Low Pass with Op Amp
*
.subckt opamp non inv out
rin non inv 100K
egain     1     0     (non, inv)    200K
ropen     1     2     2K
copen  2  0     15.9155u
eout   3  0     (2, 0)   1
rout   3   out   50
.ends
vin     3     31     ac     1.0
*vin          0     31     ac    1.0
*ein       3  0     (31, 0)      1
x1      4     1     2     opamp
x2      4     11    22    opamp
R1      3     1     1K R11   3     4     1K
R1B    31     4     1K
R1BB 31     11    1K
RF1    2     1     1K
RF1B 22     11    1K
RF11  4     0     1K
RF11B       4     0       1K
C1      2     1     0.159155u
C1B   22     11     0.159155u
C1A   4      0     0.159155u
C11B 4      0     0.159155u
RO1A 4      0     1K
RO1B 4      0      1K
rdummy  3     31    1
Ro11    22     101     1K
Ro11a       22     104     1K
Ro11b       2      211     1K
Ro111       2      211     1K
C2     102     101     0.159155u
C2a    104     0       0.159155u
C2b    104     0       0.159155u
C2bb  222     211     0.159155u
* FEEDBACK RESISTORS
RO1   1       102     1K
RO2   11      222     1K
x3      104     211     222    opamp
x4      104     101     102    opamp
.ac   dec   50    10Hz   12KHz
.probe
.end
```



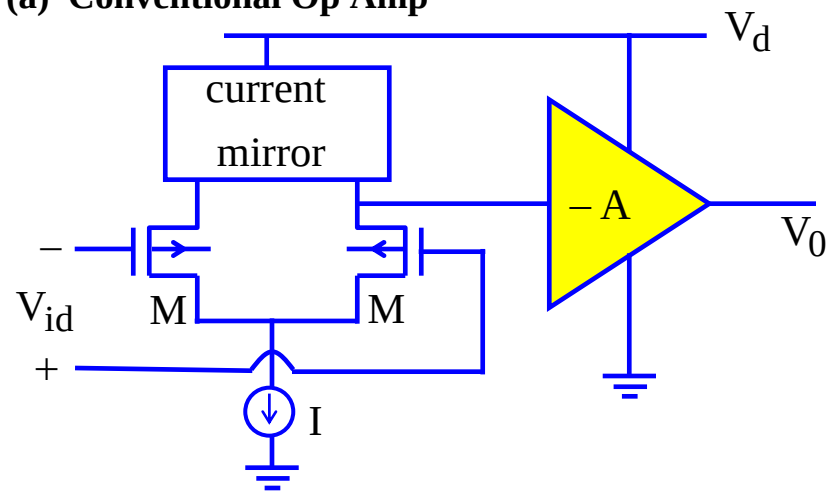
Fully Balanced Active RC Fully Differential, : *Differential outputs*

Ro1 connected to the outputs and middle point cm, + terminal of Op Amps

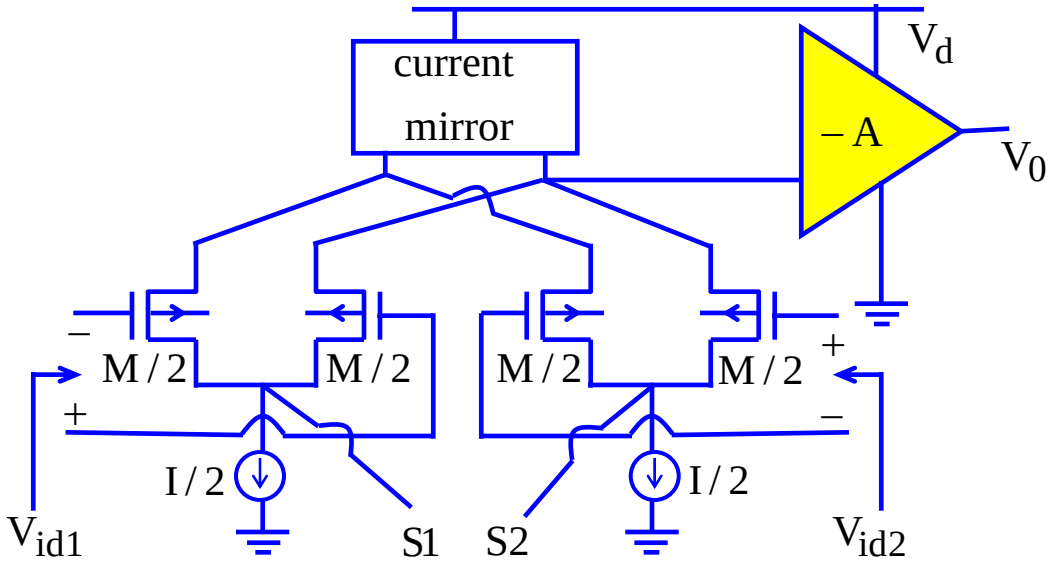


Dual Input Amplifier

(a) Conventional Op Amp



(b) A method of a dual-input amplifier implementation



$$V_0(s) = K(s)V_{id}(s) \text{ with } |K| \to \infty, \tag{15}$$

$$V_0(s) = \frac{K(s)}{2}\left[V_{id1}(s) + V_{id2}(s)\right] \text{with } \frac{|K|}{2} \to \infty \tag{16}$$

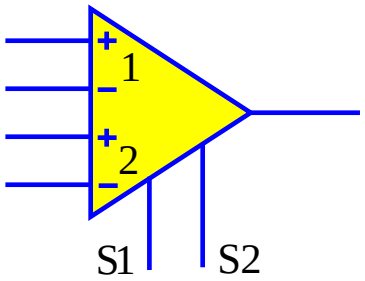
Where V_{id1} and V_{id2} are differential input voltages applied to the first and second input, respectively. If a dual-input opamp is completed with negative feedback (e.g. if V_0 is assumed finite) the sum $V_{id1} + V_{id2}$ is forced to be

$$V_{id1} + V_{id2} = 0 \tag{17}$$

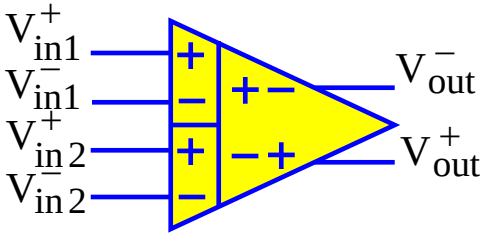
Furthermore, without linearization techniques the following must hold :

$$V_{id1} \to 0 \quad \text{and} \quad V_{id2} \to 0$$

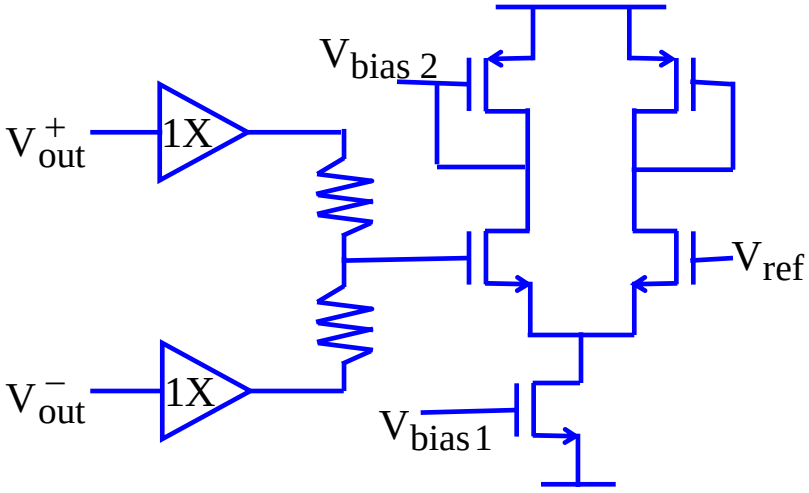
(c) a symbol of a dual-input amplifier.



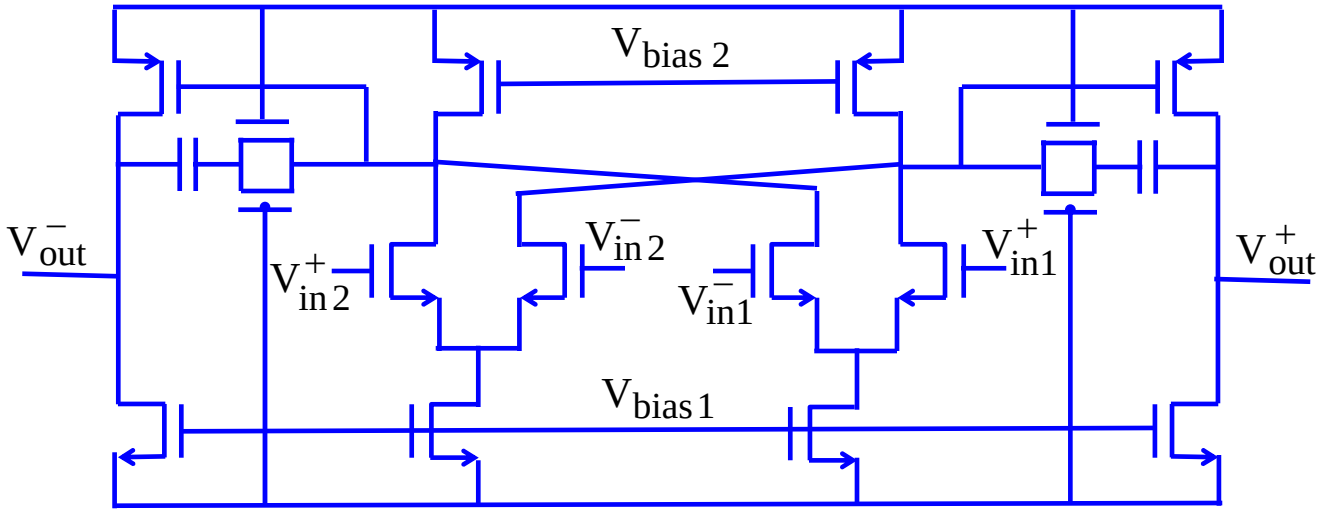
A Multiple Input Op Amp



(a)



(c)

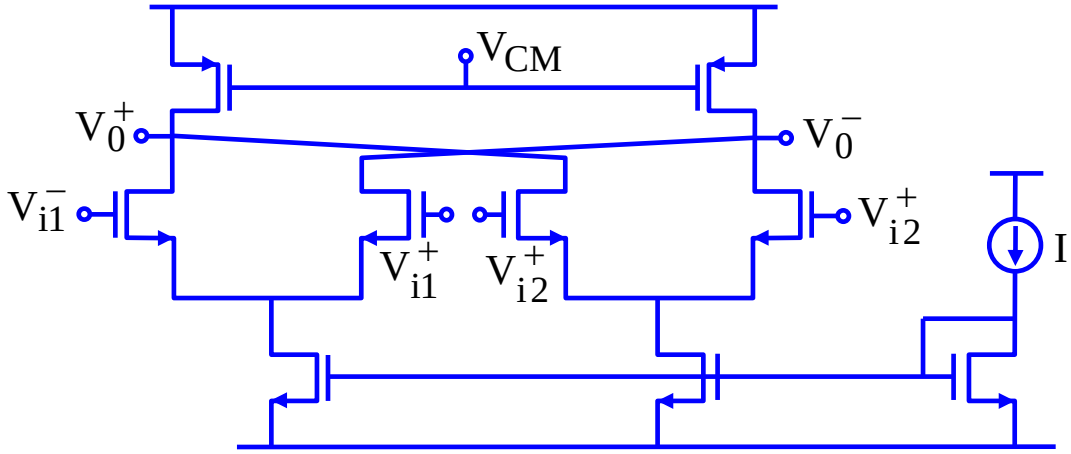


(b)

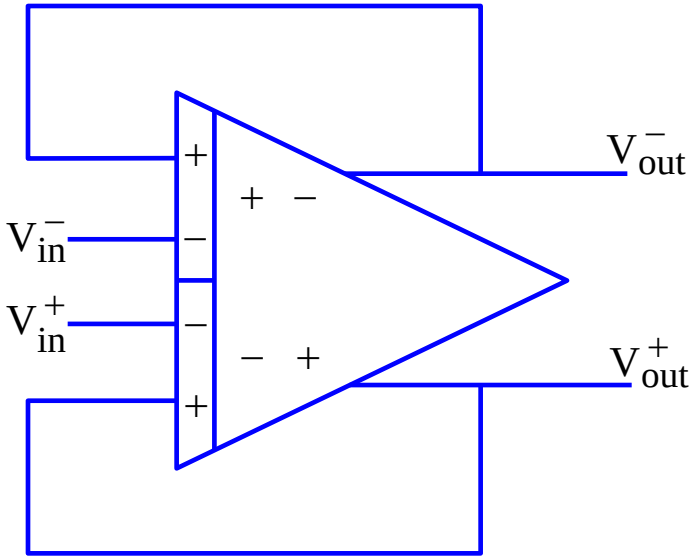
Fully differential difference amplifier (FDDA). (a) Symbol.
(b) Circuit schematic. (c) Common-mode feedback loop (CMFB)

FULLY DIFFERENTIAL BUFFER BASED ON FULLY-DIFFERENTIAL DIFFERENCE AMPLIFIER (FDDA)

Fully-differential difference amplifier (FDDA) scheme:



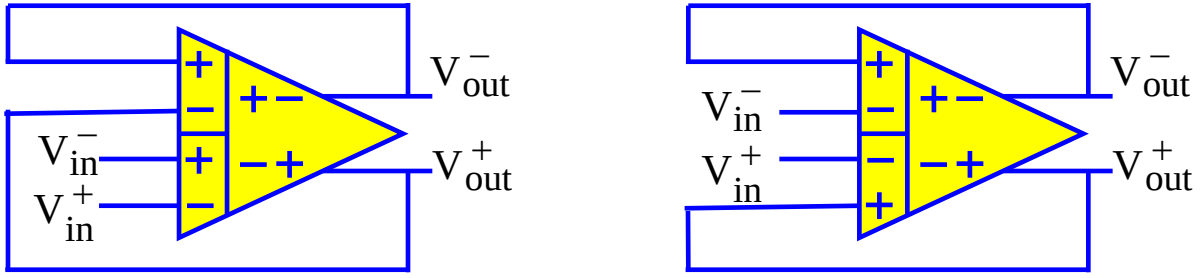
Fully-differential buffer configuration:



Simulation file:

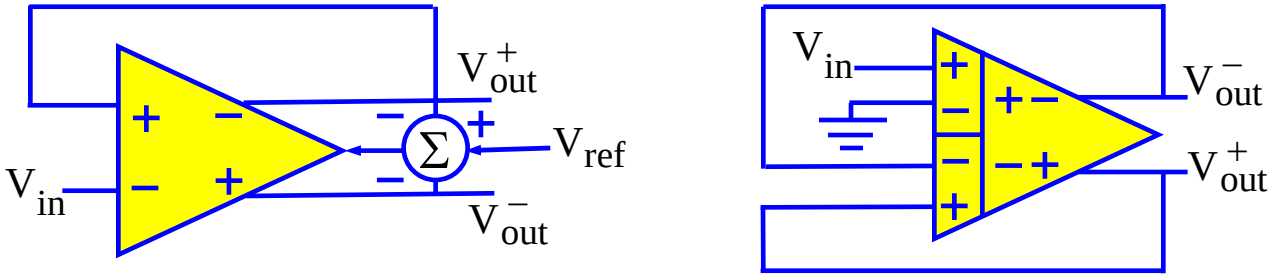
```
*BUFFER WITH SIMPLE DIFFERENTIAL PAIR

*TRANSISTOR MODELS

.MODEL MODN NMOS LEVEL=2
+ CGSO =0.290e-09   CGDO =0.290e-09   CGBO =0.170e-09
+ CJ   =0.360e-03   MJ   =0.430e+00   CJSW =0.250e-09   MJSW =0.190e+00
+ JS   =0.010e-03   PB   =0.960e+00   RSH  =25.50e+00
+ TOX  =23.80e-09   XJ   =0.175e-06   LD   =-.050e-06   WD   =0.398e-06
+ VTO  =0.736e+00   NSUB =33.30e+15   NFS  =0.452e+12   NEFF =5.250e+00
+ UO   =515.0e+00   UCRIT=28.70e+04   UEXP =0.251e+00   UTRA =0.000e+00
+ VMAX =77.30e+03   DELTA=0.000e+00   KF   =0.101e-25   AF   =1.330e+00
.MODEL MODP PMOS LEVEL=2
+ CGSO =0.290e-09   CGDO =0.290e-09   CGBO =0.170e-09
+ CJ   =0.340e-03   MJ   =0.530e+00   CJSW =0.220e-09   MJSW =0.200e+00
+ JS   =0.020e-03   PB   =0.970e+00   RSH  =46.00e+00
+ TOX  =23.80e-09   XJ   =0.056e-06   LD   =0.043e-06   WD   =0.448e-06
+ VTO  =-.751e+00   NSUB =18.00e+15   NFS  =1.300e+12   NEFF =3.090e+00
+ UO   =175.0e+00   UCRIT=21.60e+04   UEXP =0.268e+00   UTRA =0.000e+00
+ VMAX =54.00e+03   DELTA=0.798e+00   KF   =0.390e-27   AF   =1.290e+00

*AMPLIFIER SUBCIRCUIT
.subckt ampli 2 4 5 vdd vss 30
m1 1 2 3 vss MODN w=100u l=10u
m2 5 4 3 vss MODN w=100u l=10u
m3 1 1 vdd vdd MODP w=150u l=5u
m4 5 1 vdd vdd MODP w=150u l=5u
m5 3 30 vss vss MODN w=100u l=10u
m6 30 30 vss vss MODN w=100u l=10u
.ends ampli
*BUFFER
x1 1 2 4 vdd vss 30 ampli
x2 3 4 2 vdd vss 30 ampli
*SUPPLY
ib vdd 30 10u
VDD vdd 0 dc 3v
VSS vss 0 dc -3v
*INPUTS
*DC
*vi+ 1 0 dc 0
*ei- 3 0 1 0 -1
*TRAN
vi+ 1 0 sin(1 0.1 1k)
vi- 3 0 sin(1 -0.1 1k)

*Simulation options
.op
*.dc vi+ -3 3 0.1
.tran 1u 2m
.option post
.end
```

Applications of Multiple Input Op Amp



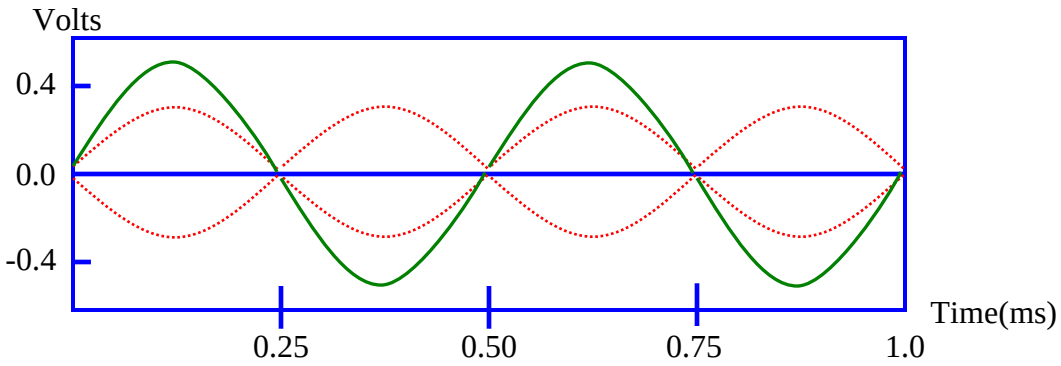
(a) **(b)**

Unity-feedback FD followers. (a) Requires differential pairs with high input DM range. (b) Requires differential pairs with high input CM range.

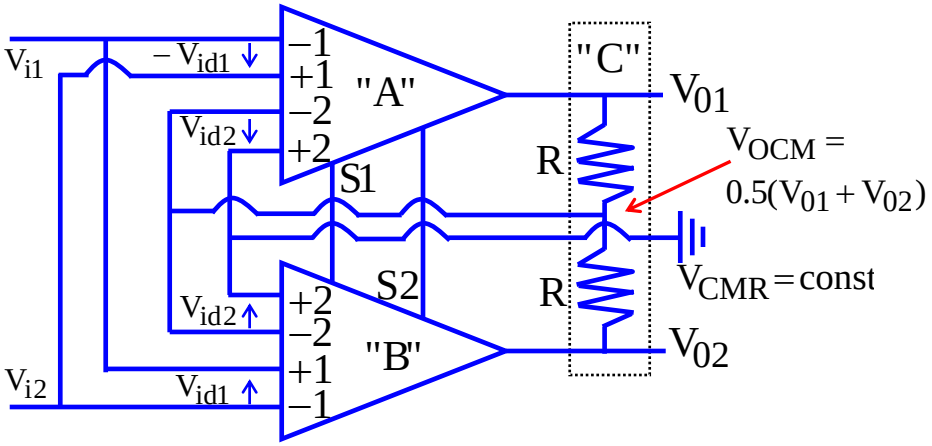


(a) **(b)**

SE-to-DE signal converters. (a) Classic approach based on FDA. (b) Proposed approach based on FDDA.



Double-ended (broken lines) conversion of a single-ended 1 V_{PP} 2kHz signal (solid line).



A new general FB opamp architecture

$$V_{id1} + V_{id2} \to 0 \text{ and } -V_{id1} + V_{id2} \to 0, \qquad (19)$$

where

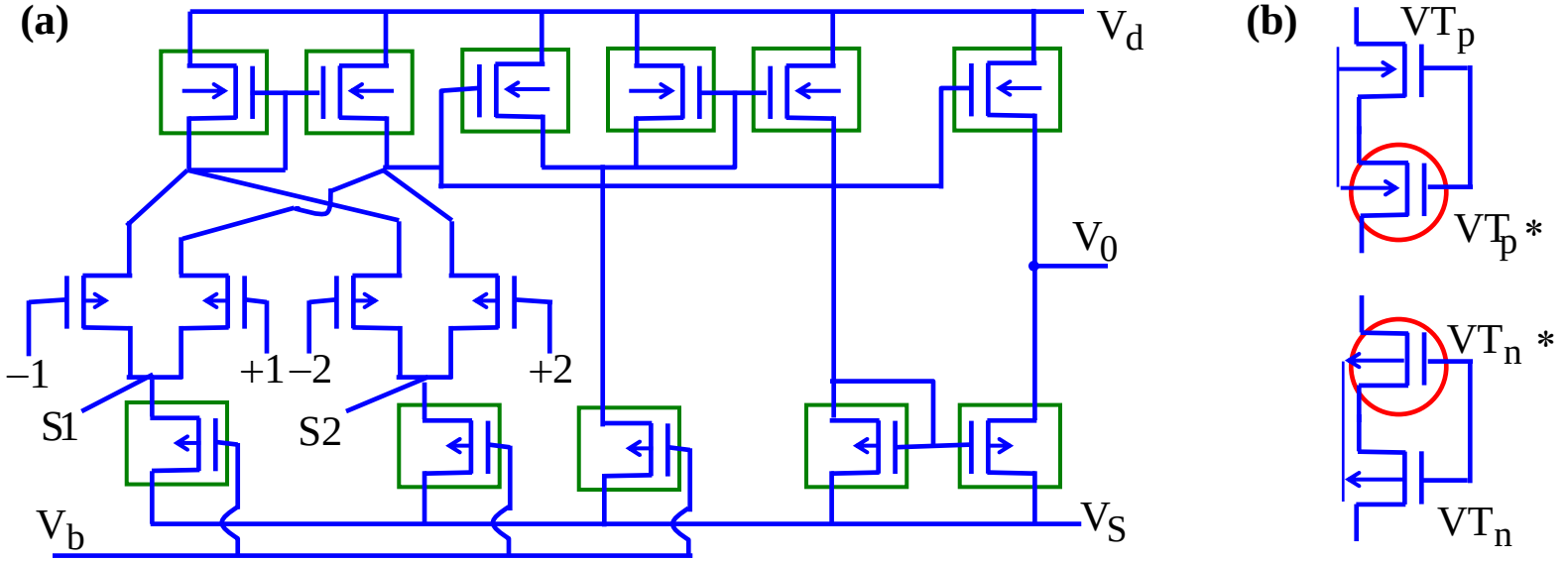
$$V_{id1} = V_{i1} - V_{i2} \text{ and } V_{id2} = V_{CMR} - (V_{01} + V_{02})/2.$$

$$V_{01} - V_{02} = -V_{id}\left[(K_{1A} + K_{1B}) + \frac{(K_{1A} - K_{1B})(K_{2A} - K_{2B})}{1 + (K_{2A} + K_{2B})/2}\right], \qquad (20)$$

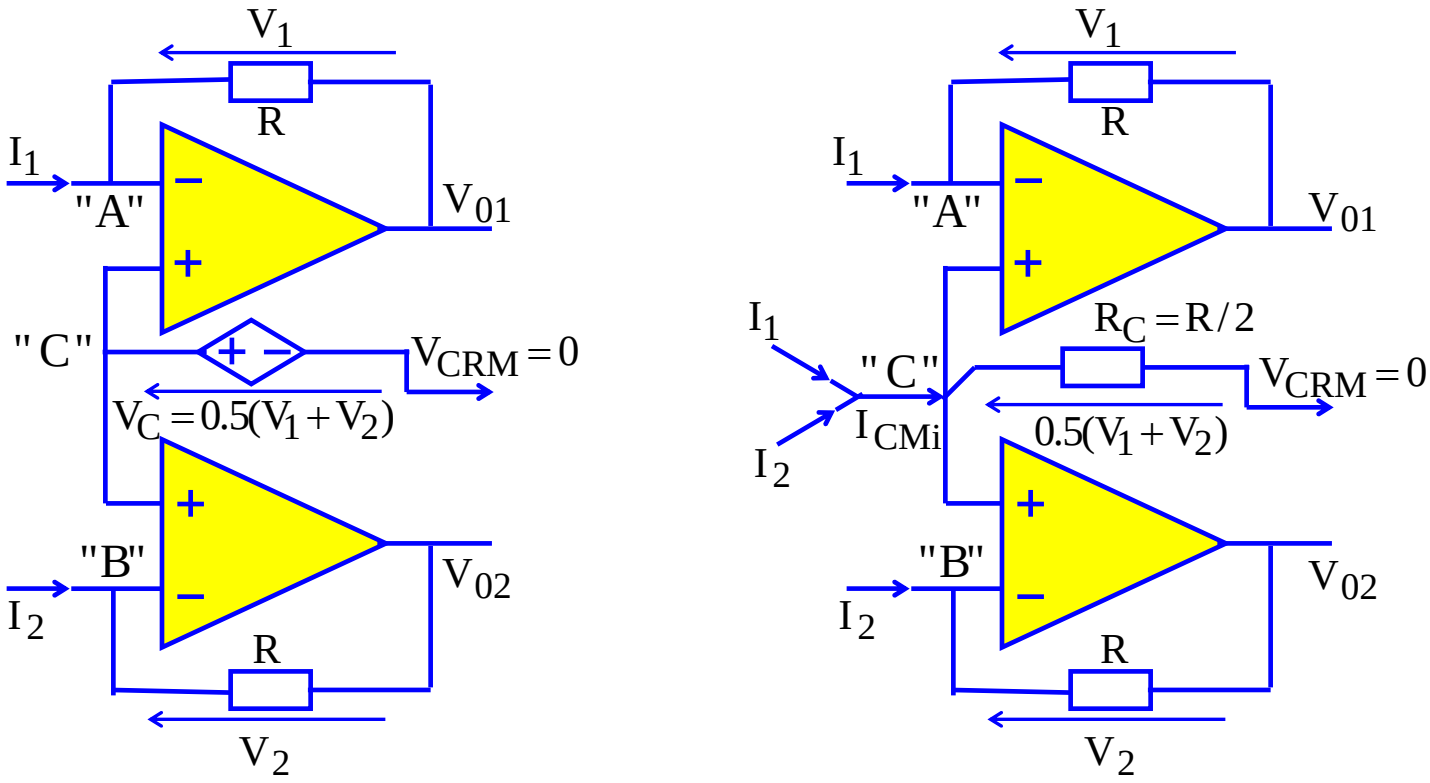
$$V_{01} + V_{02} = -V_{id}\frac{(K_{1A} - K_{1B})}{1 + (K_{2A} + K_{2B})/2}, \qquad (21)$$

where $V_{id} = V_{id1} = V_{i1} - V_{i2}$.

An Example of an Implementation



(a) a detailed shcematic of a dual-input amplifier with self bias cascode transistors (symbols within a square box), (b) implementations of self bias cascode transistors



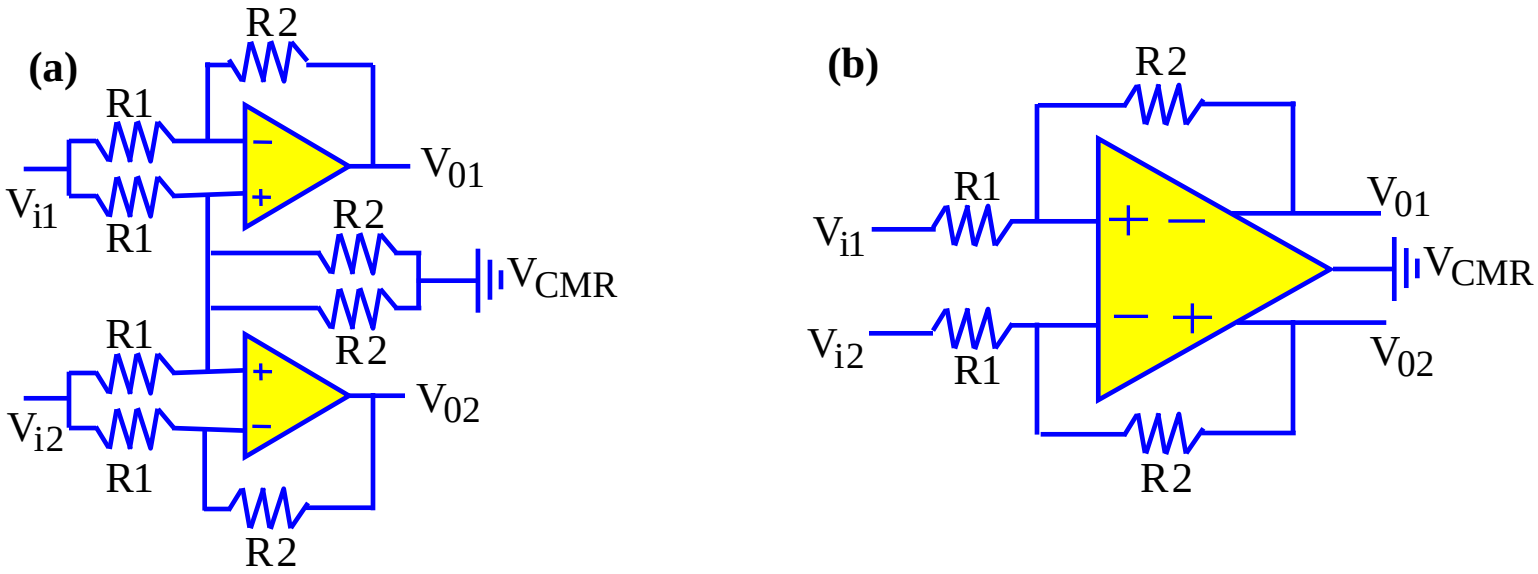
Basic principle of FB architecture with only CM feedforward path.

$$V_C(s) = \frac{V_1(s) + V_2(s)}{2} \qquad (22)$$

is inserted between node "C" and a reference node. Note that a $V_C(s)$ voltage is controlled by the common - mode value of the feedback voltages $V_1(s)$ and $V_2(s)$. Assuming that the input of each amplifier are virtually shorted it allows the output voltages $V_{01}(s)$ and $V_{02}(s)$ to be fully balanced around a constant voltage V_{CMR} (= 0) applied to the reference node. They are given as follows :

$$V_{01}(s) = -\frac{V_1(s) - V_2(s)}{2} = -V_{02}(s). \qquad (23)$$

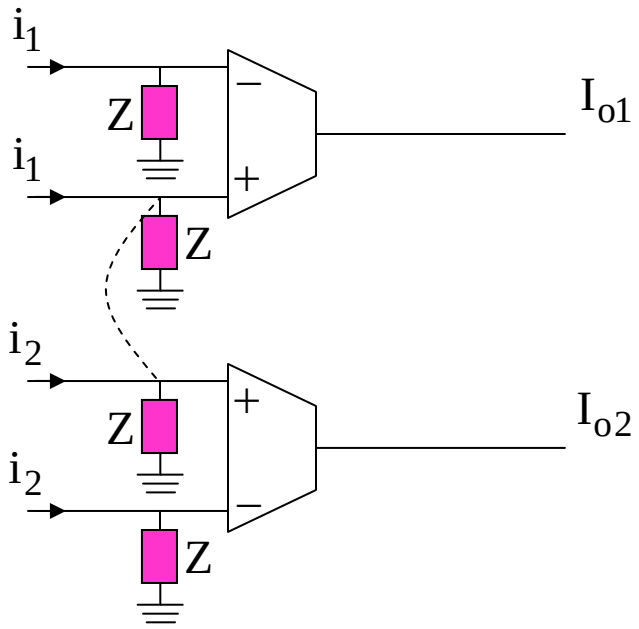
Examples:



An inverting FB amplifier with (a) CM feedforward, and (b) CM feedback

In principle, both circuits realize the same differential and common - mode transfer functions. However, the new FB inverting amplifier in Fig. (a) can be realized more simply, i.e, with only ordinary opamps, than the conventional approach shown in Fig. (b). Its stability is also improved because a CM feedback is not required.

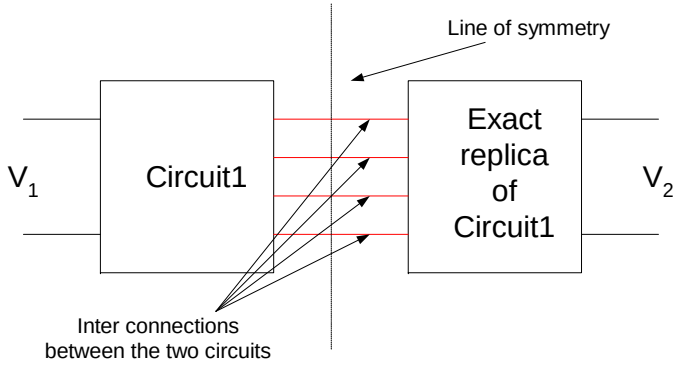
For OTA one solution becomes



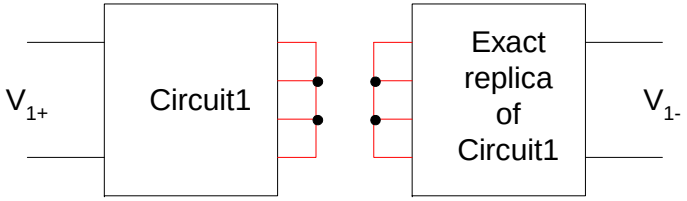
Every input should be in pairs of signal.

Another suggested solution ?

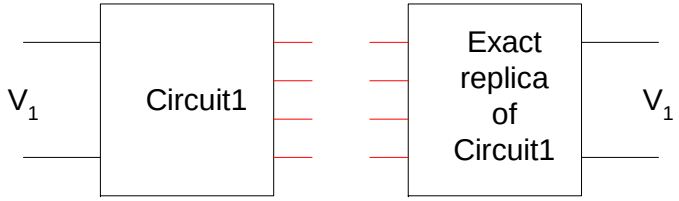
Recall the behavior of symmetric circuits



An example of fully symmetric circuit

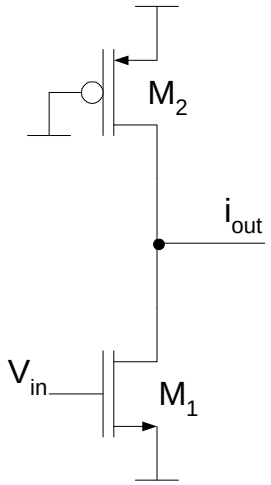


Equivalent circuit for fully differential input

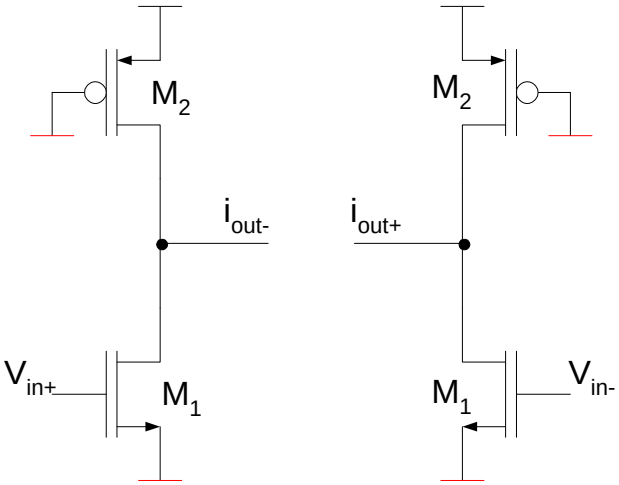


Equivalent circuit for common mode input

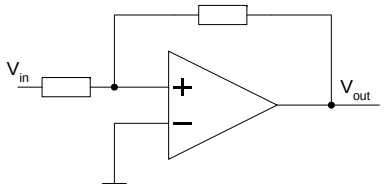
Derivation of CMFF OTA

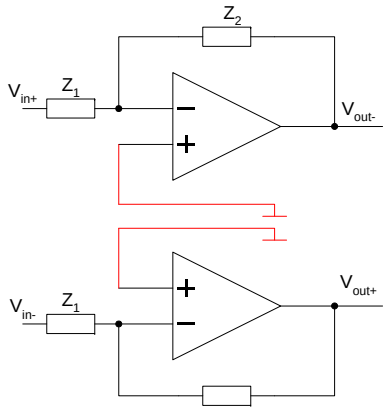


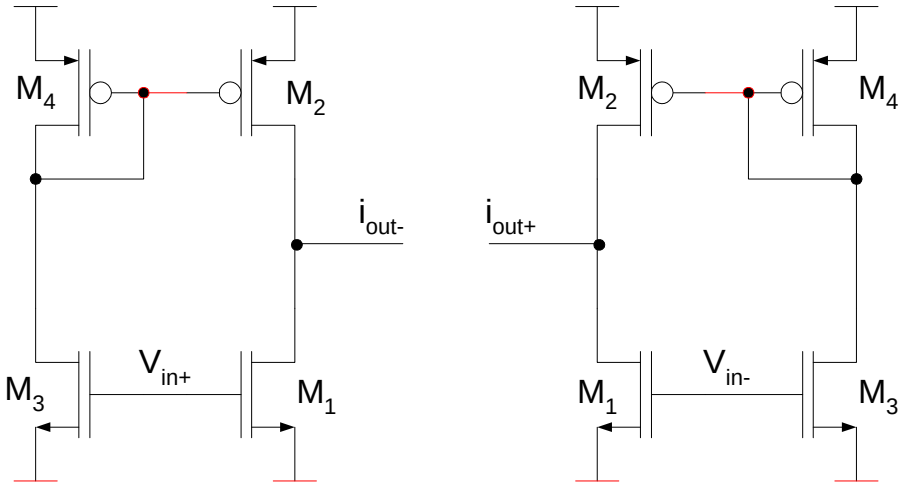
Single ended OTA circuit



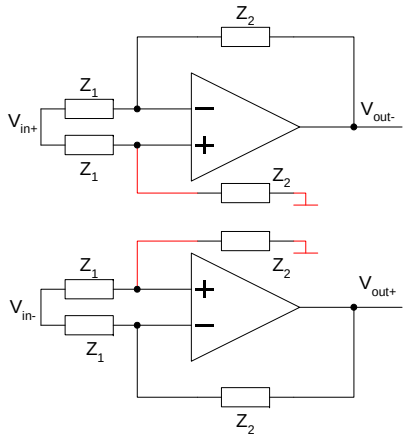
Circuit of OTA for differential input



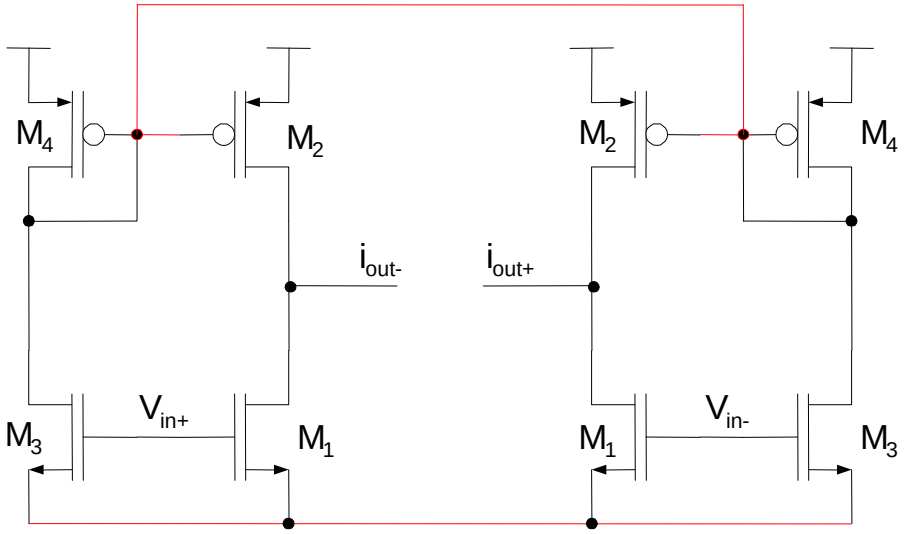


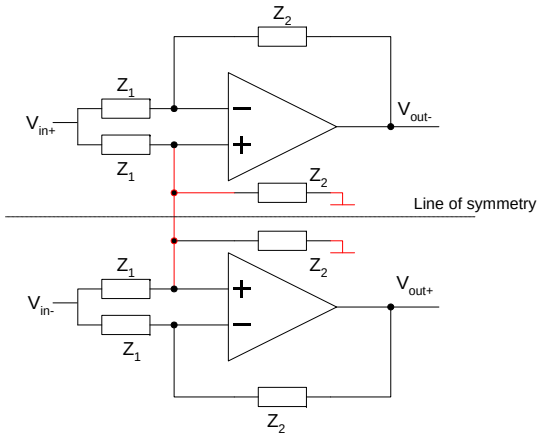


Circuit of OTA for common mode signals

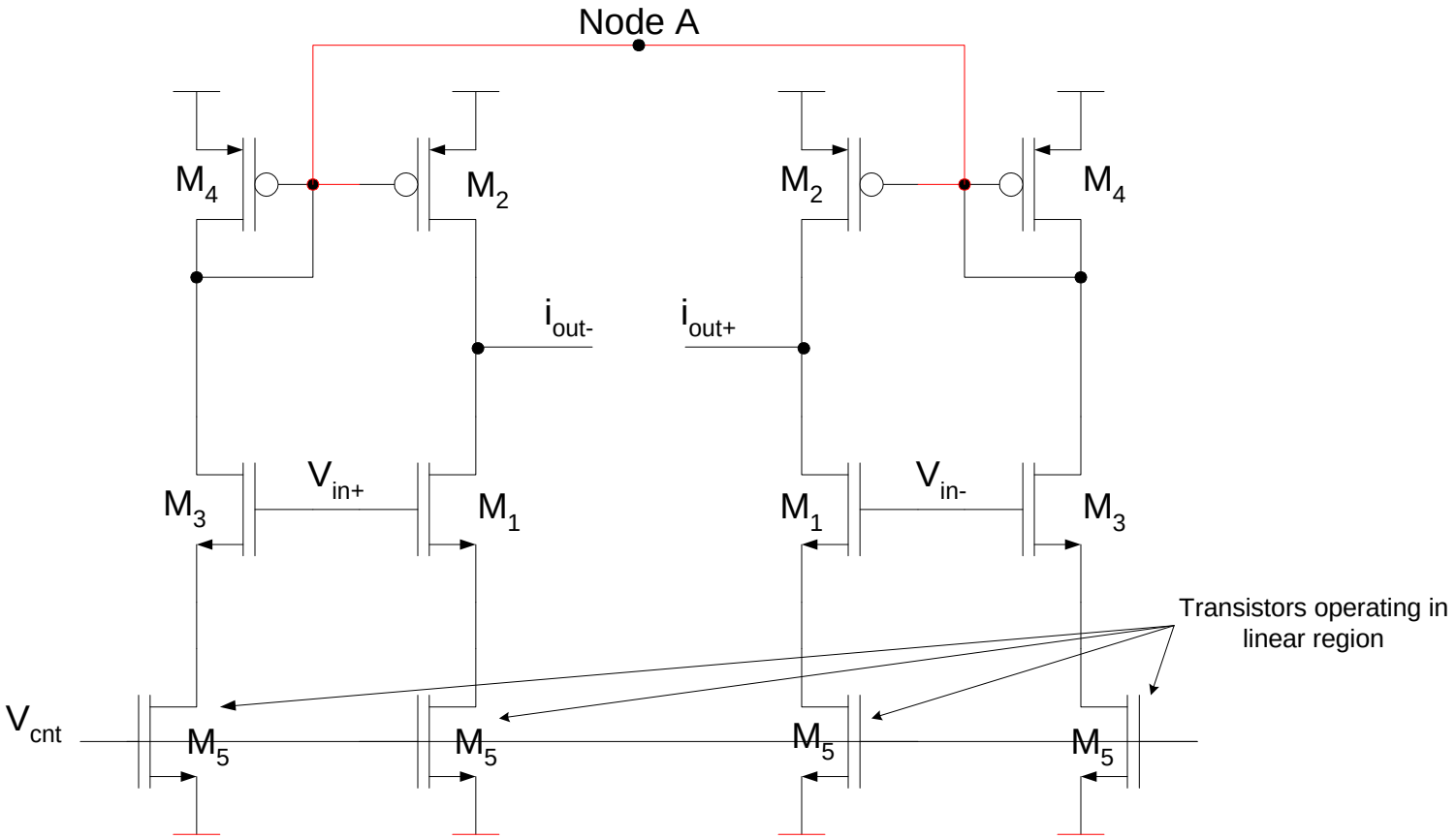


Fully-balanced, fully-symmetric CMFF OTA



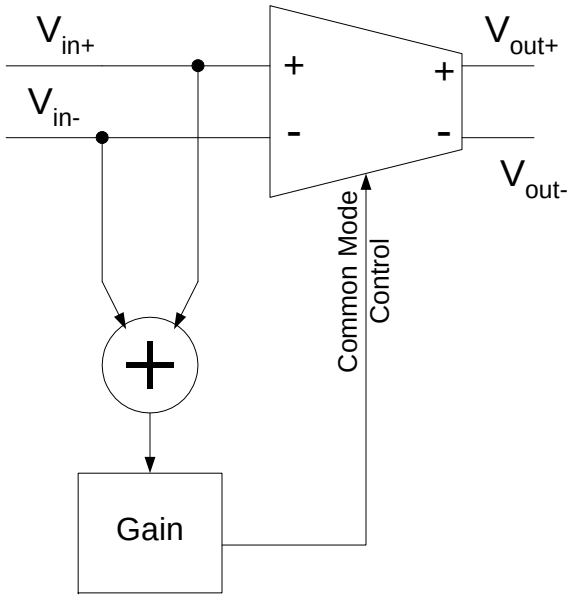


OTA with improved linearity



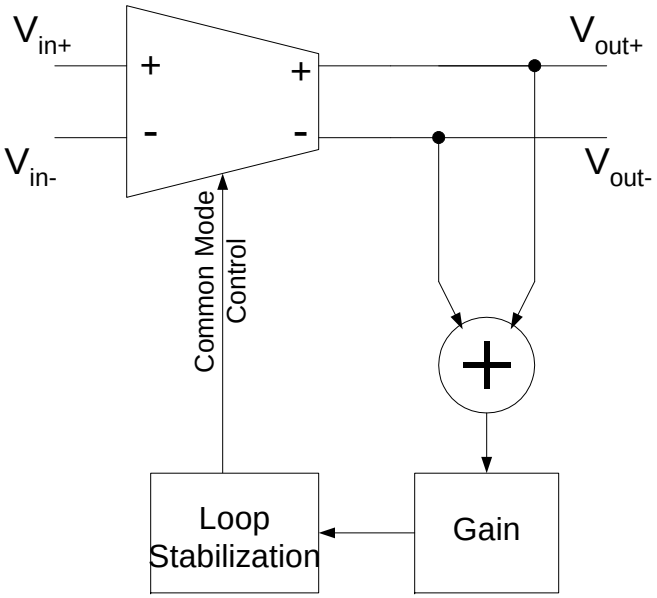
Fully-balanced, fully-symmetric, pseudo differential CMFF OTA

Common Mode Feed Forward



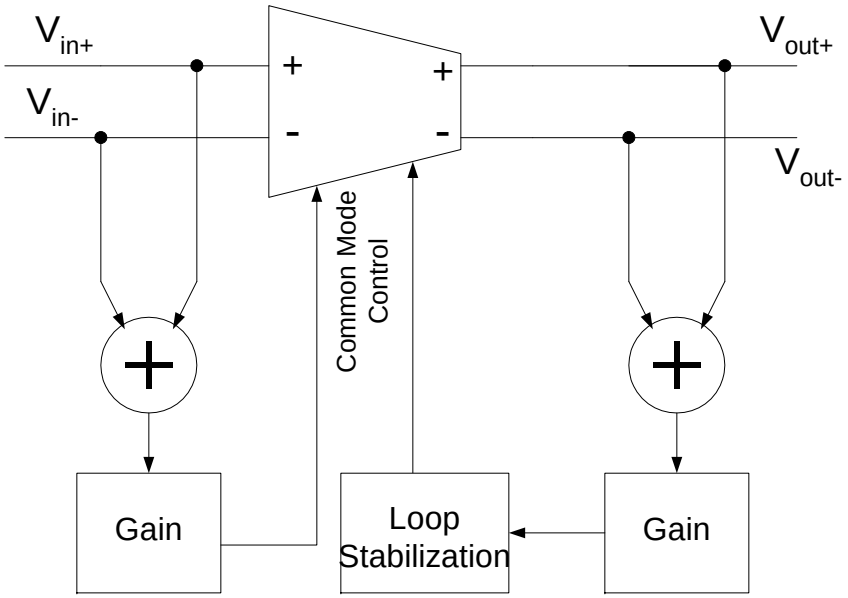
- Can decrease common mode gain even at higher frequencies
- Does not have stability problems
- Cannot stabilize the output DC voltage

Common Mode Feed Back

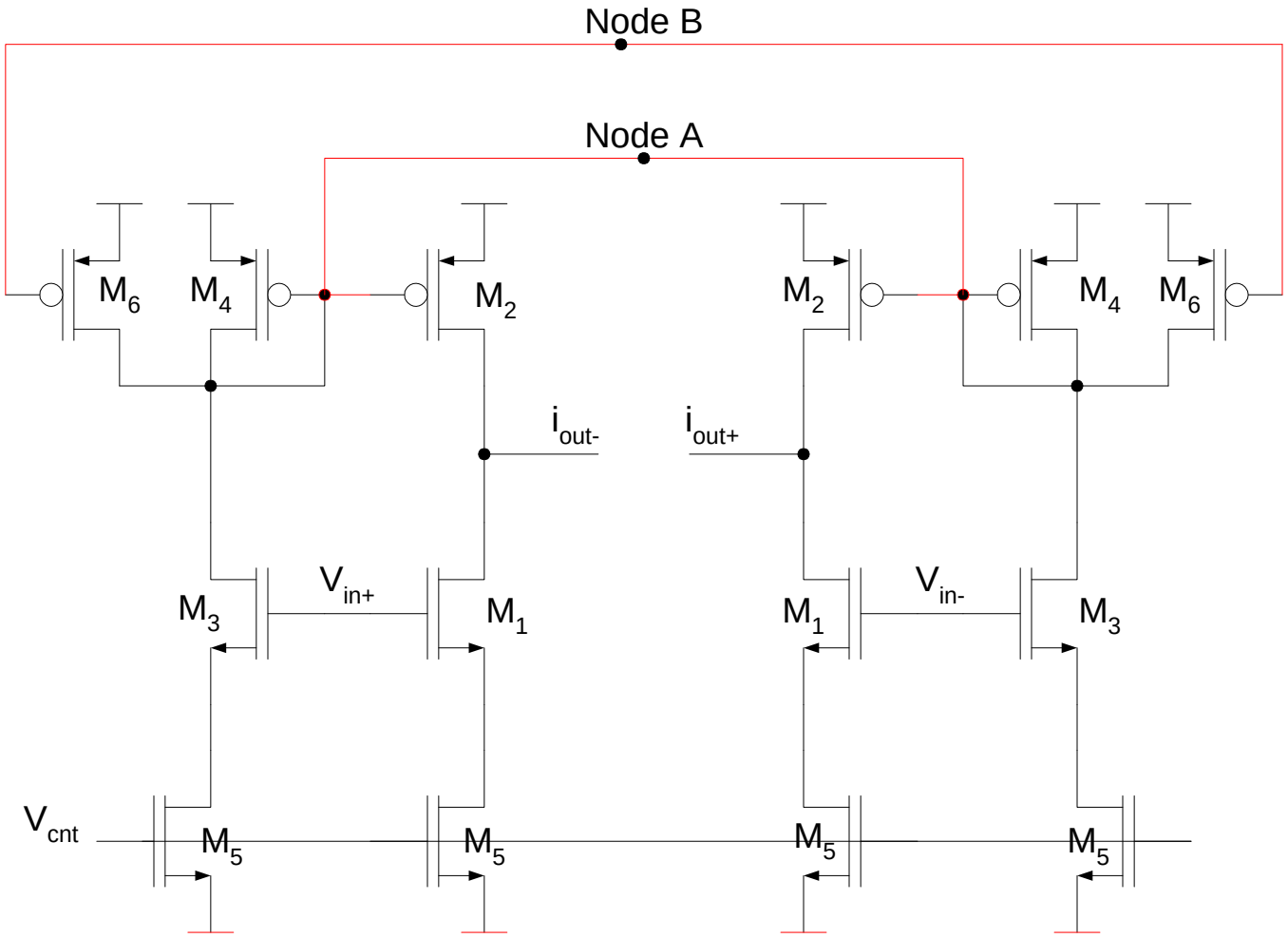


- Stabilizes output DC voltage
- Feedback stability issues make the circuit slow and bulky

CMFF + CMFB

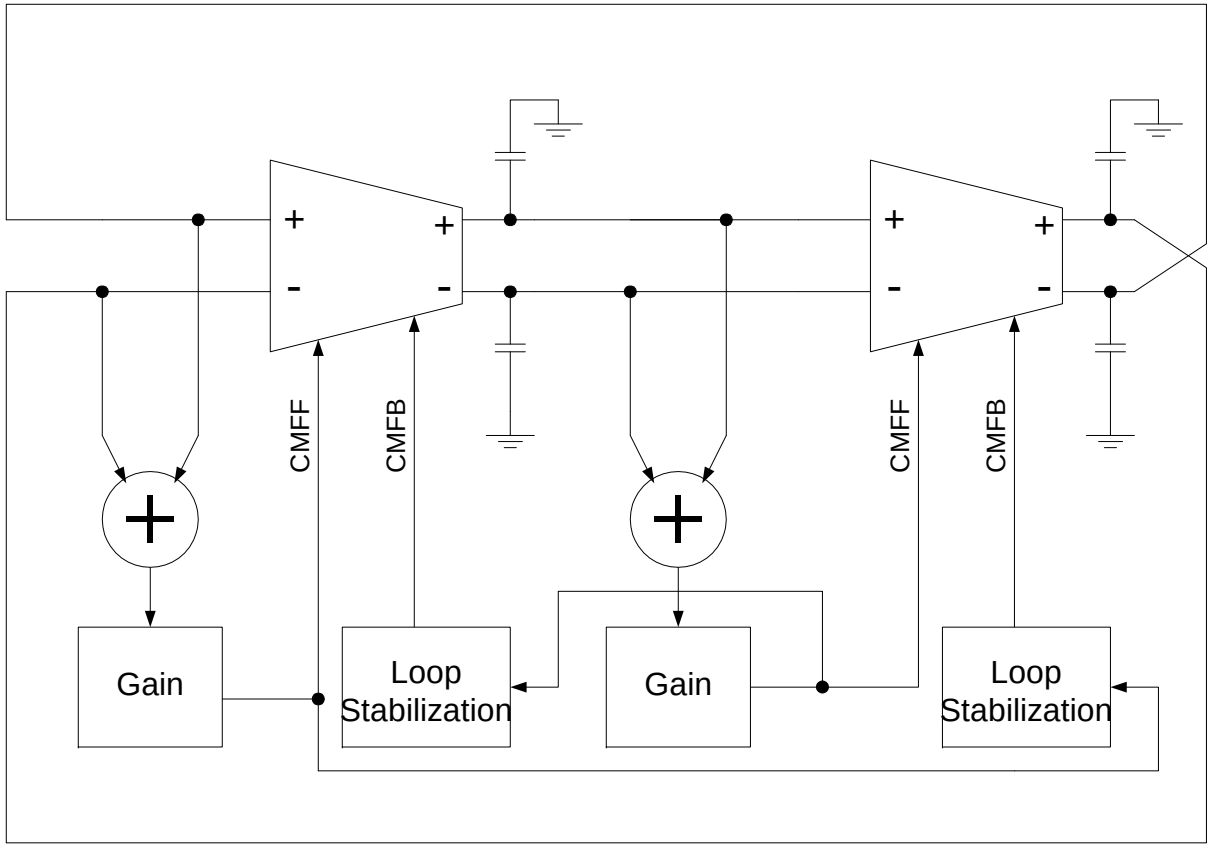

V_{in+}
V_{in-}
+
-
+
-
V_{out+}
V_{out-}
Common Mode Control
Gain
Loop Stabilization
Gain

(CMFF + CMFB) OTA



Fully-balanced, fully-symmetric, pseudo differential (CMFF+CMFB) OTA

Two integrator loop



Characteristics of the OTA

- Let the total capacitance at ‘node A’ be C_{int}
- Let the capacitance used in two integrator loop be C_{ext}
- Effective transconductance= $$g_{m1eff} = \frac{g_{m1}}{1+\frac{g_{m1}}{g_{ds5}}}$$

- CMFB loop gain = $$\frac{g_{m1eff} \cdot g_{m6} \cdot g_{m2}}{g_{m4} \cdot g_{m4} \cdot g_{ds2}} \cdot \frac{1}{\left(1+\frac{sC_{\text{int}}}{g_{m4}}\right)^2 \left(1+\frac{sC_{ext}}{g_{ds2}}\right)}$$

- Gain $(I_o/V_i) = g_{ds5}\left\{2-\left(1+\frac{4\beta_1}{g_{ds5}}(V_G-V_T)\right)^{-\frac{1}{2}}\right\}$

- Gain$(I_o/V_i^3) = \frac{12\beta_1^2}{g_{ds5}}\left[1+\frac{4\beta_1}{g_{ds5}}(V_G-V_T)\right]^{-\frac{5}{2}} = \frac{12\beta_1^2 g_{ds5}^{3/2}}{\left[g_{ds5}+4\beta_1(V_G-V_T)\right]^{5/2}}$

- To improve linearity, use larger resistor for source degeneration.

- Differential gain= $\frac{g_{m1,eff}}{g_{ds2}}$
- Common mode gain = $\left[1-\frac{1}{1+\frac{sC_{\text{int}}}{g_{m4}}}\right]\times\frac{g_{m1,eff}}{g_{ds2}}+\frac{g_{m1,eff}}{g_{m4}}$
- $\text{CMRR}_{(\text{DC})}$ = $\frac{g_{m4}}{g_{ds2}}$

- Gain from +ve supply=1
- Gain from -ve supply= $\left[1-\frac{1}{1+\frac{sC_{\text{int}}}{g_{m4}}}\right]\times\frac{g_{m1,eff}}{g_{ds2}}+\frac{g_{m1,eff}}{g_{m4}}$

- Gain from VSS is less than gain from VDD. So, output should be measured wrt VDD
- PSRR is same as CMRR

Output noise current=

$$i_{n1}^2 \times \left(\frac{1}{1+\frac{g_{m1}}{g_{ds5}}} \right)^2 + 4KTg_{ds5} + 4KTg_{ds5} \times \left(\frac{g_{m2}}{g_{m4}\left(1+\frac{sC_{\text{int}}}{g_{m4}}\right)} \right)^2$$

$$+ i_{n2}^2 + i_{n4}^2 \times \left(\frac{g_{m2}}{g_{m4}} \right)^2 + i_{n6}^2 \times \left(\frac{g_{m2}}{g_{m4}\left(1+\frac{sC_{\text{int}}}{g_{m4}}\right)} \right)^2$$

Simplified noise expression

$$KT\left\{\frac{8g_{m1}}{3\left(1+\frac{g_{m1}}{g_{ds5}}\right)^2}+4g_{ds5}+\frac{4g_{ds5}}{\left(1+\frac{sC_{\text{int}}}{g_{m4}}\right)^2}+\frac{8g_{m2}}{3}+\frac{8g_{m2}}{3\left(1+\frac{sC_{\text{int}}}{g_{m4}}\right)^2}\right\}$$

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