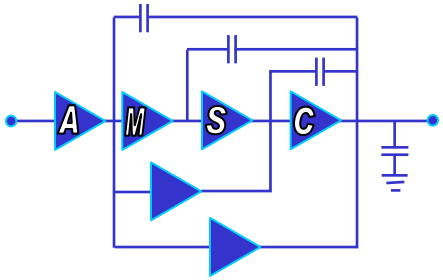
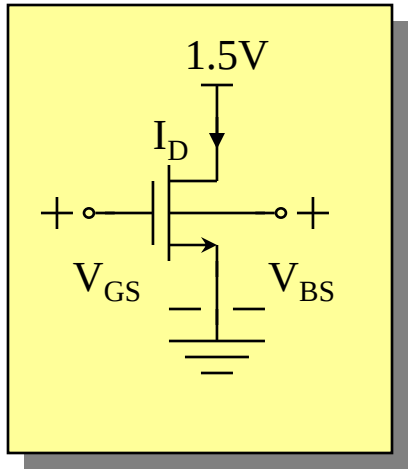
Analog and Mixed-Signal Center





Bulk Driven Transistors

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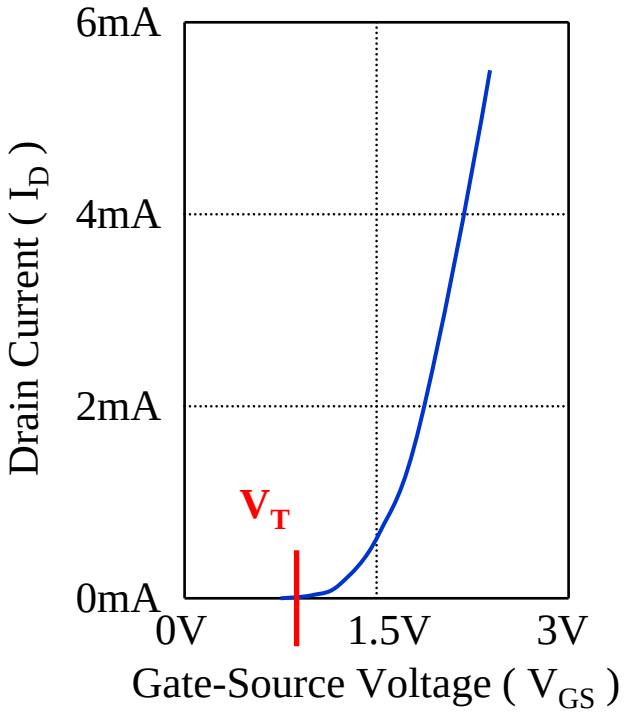
Why Bulk-Driven MOS Transistors?

- We know that if we need a MOS transistor to perform any signal processing task, it should conduct some biasing drain current. For a conventional gate-driven MOS transistor, we have to overcome the threshold voltage V_T to let it operate.
- As the feature size of modern CMOS processes scaling down, the maximum allowable power supply continuously decreases, but the threshold voltage does not scale down with the same rate! Which poses a great challenge to CMOS analog/mixed-signal circuit design. Some circuit structures become obsolete for modern CMOS processes!



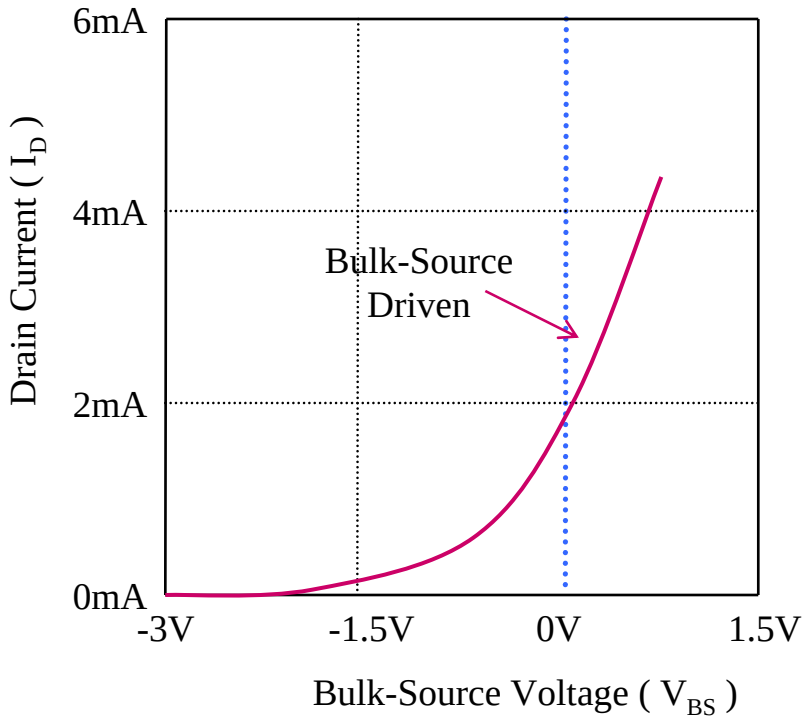
Bulk-Driven MOS Transistors Issues

- In modern CMOS technologies, V_T does not scale down proportionally with the maximum possible power supply -- Please note that the maximum possible power supply is roughly proportional to the gate oxide thickness.

Process	Feature Size (um)	Gate Oxide Thickness (angstroms)	Threshold Voltage (V)	
			V_{TN}	V_{TP}
Obit 2.0u	1	402	0.81	-0.90
AMI 1.2u	0.6	304	0.61	-0.87
HP 0.8u	0.4	169	0.71	-0.88
HP 0.5u	0.3	96	0.70	-0.88
TSMC 0.35u	0.2	76	0.55	-0.76

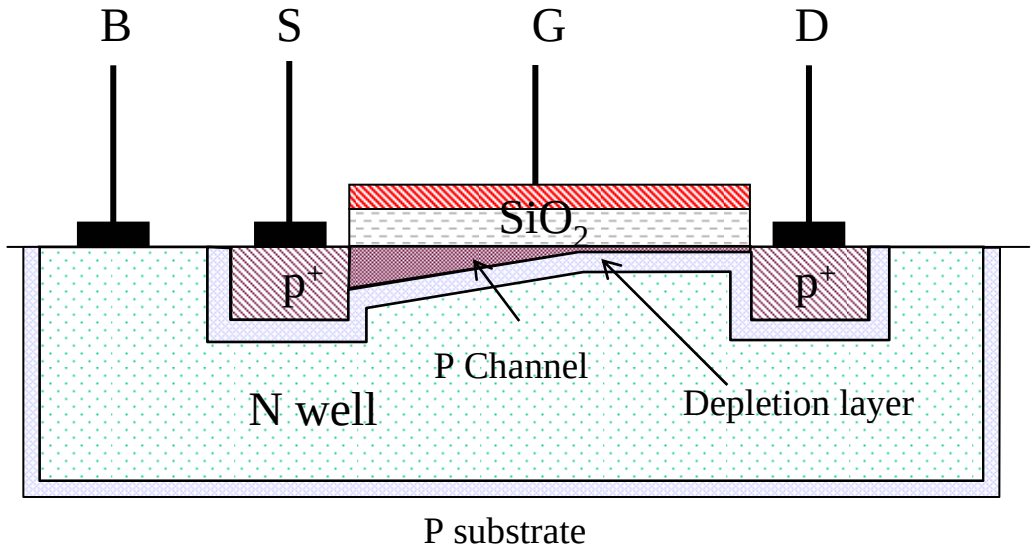
Bulk-Driven MOS Transistors Issues

- The bulk-driven transistor is a good solution to the threshold voltage limitation. Because the bulk-driven transistor is a depletion type device. It can work in negative, zero, or even slightly positive biasing condition!



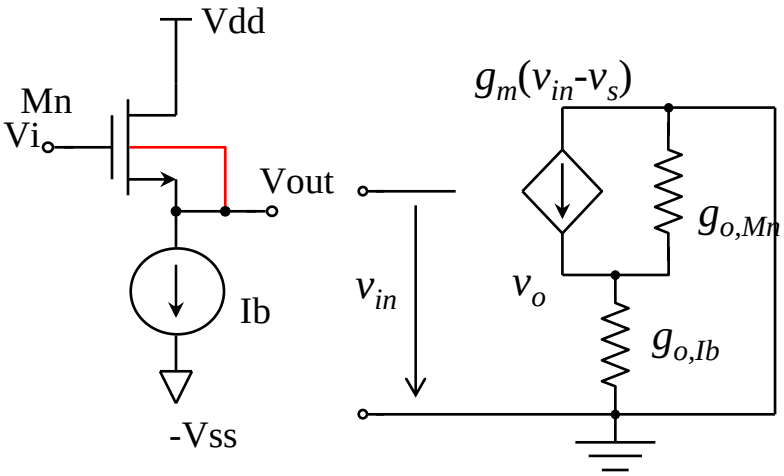
What are Bulk-Driven MOS Transistors?

- For a MOS FET, conductivity is normally controlled by the gate capacitance. The voltage across the gate capacitance, V_{GS}, controls the conductivity of the channel.
- The drain current, I_D, of a MOS FET can also be controlled by bulk-source voltage, V_{BS}. Normally this is a parasitic effect, and may introduce unwanted g_{mb}, which could degrade the signal path. Please refer to the source follower example in the following slide.



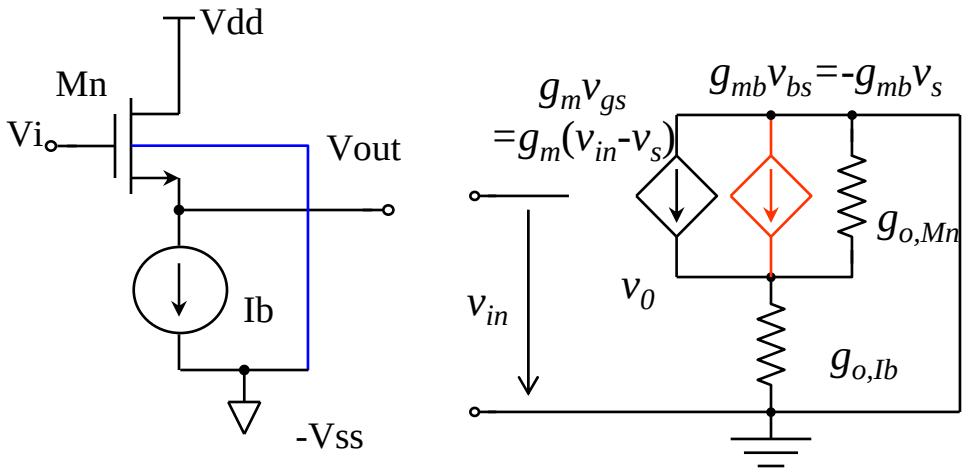
Cross section of p-channel MOS FET in N-well CMOS technology

Small Signal Bulk-Driven MOS Transistors



$$A_v = \frac{v_o}{v_i} = \frac{g_m}{g_m + g_{o,Ib} + g_{o,Mn}} \approx 1$$

(a) Source follower with source and bulk tied together. There is no g_{mb} in signal path, the voltage gain is very close to 1. This N-channel source follower is only available in P-well or twin-well technology.



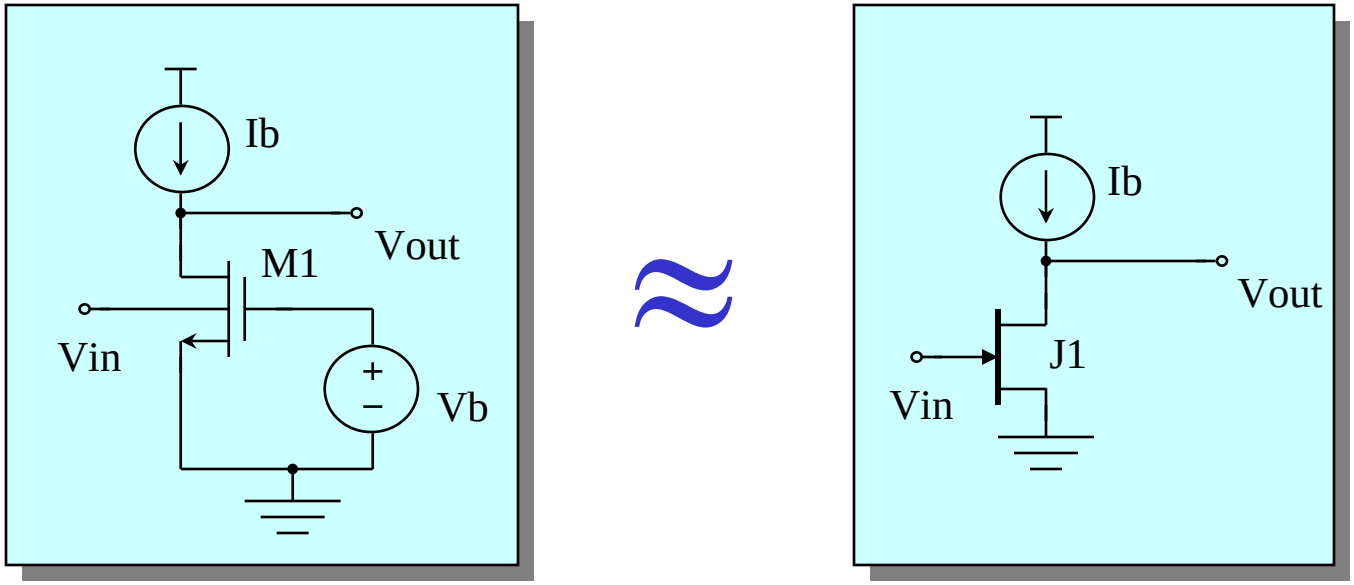
$$A_v = \frac{v_o}{v_i} = \frac{g_m}{g_m + g_{mb} + g_{o,Ib} + g_{o,Mn}}$$

$$\approx \frac{g_m}{g_m + g_{mb}}$$

(b) Source follower with bulk tied to power supply -Vss. Because of g_{mb}, the voltage gain is decreased and usually has a value from 0.6 to 0.85. This N-channel source follower does not depend on the process technology of the chip.

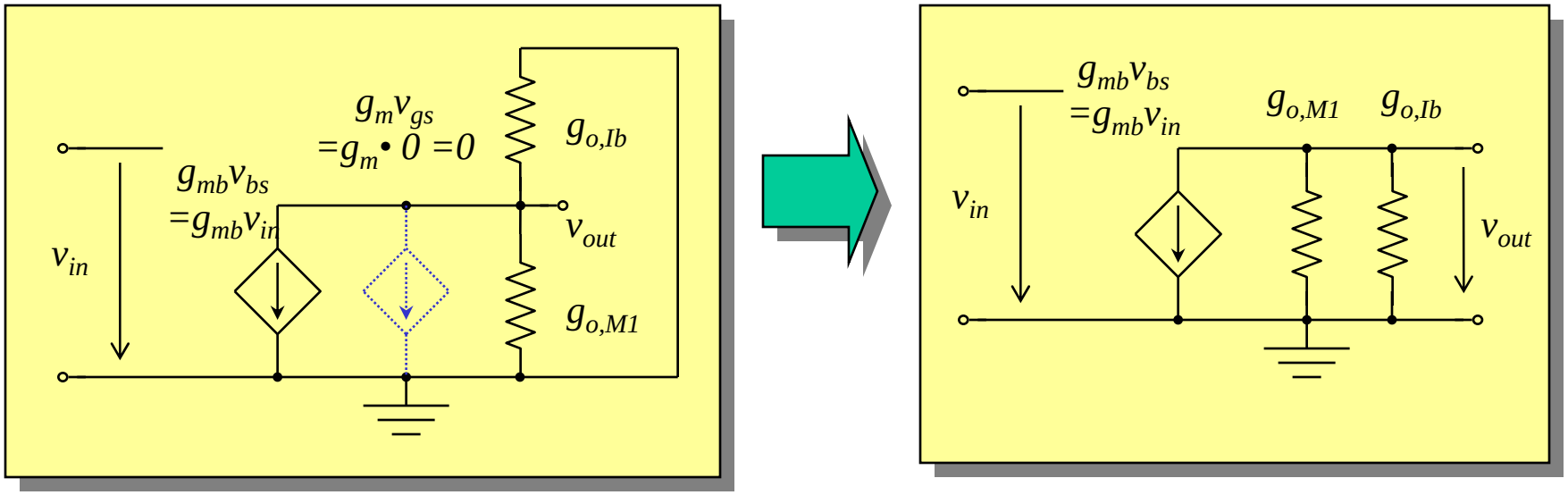
Similarity of Bulk-Driven MOS Transistors to JFETs

- Actually, the g_{mb} is due to the existence of the bottom parasitic JFET (Junction FET) , which is formed by the channel and the bottom depletion layer capacitance.
- We can utilize the parasitic JFET for signal processing purpose. If we apply signal to the bulk, instead of to the gate, and keep V_{GS} constant, then we have a bulk-driven MOS transistor.



Small Signal Bulk-Driven MOS Transistors

Small Signal Equivalent Circuits:



- To apply signal at the bulk, we must have a separate well for the bulk to isolate it from the substrate of the chip.
- As we will discuss, the depletion characteristic is very attractive for low voltage circuit design!

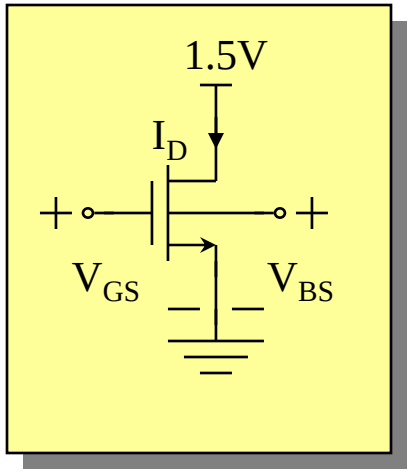
$$Av = \frac{v_{out}}{v_{in}} = \frac{g_{mb}}{g_{o,Ib} + g_{o,M1}},$$

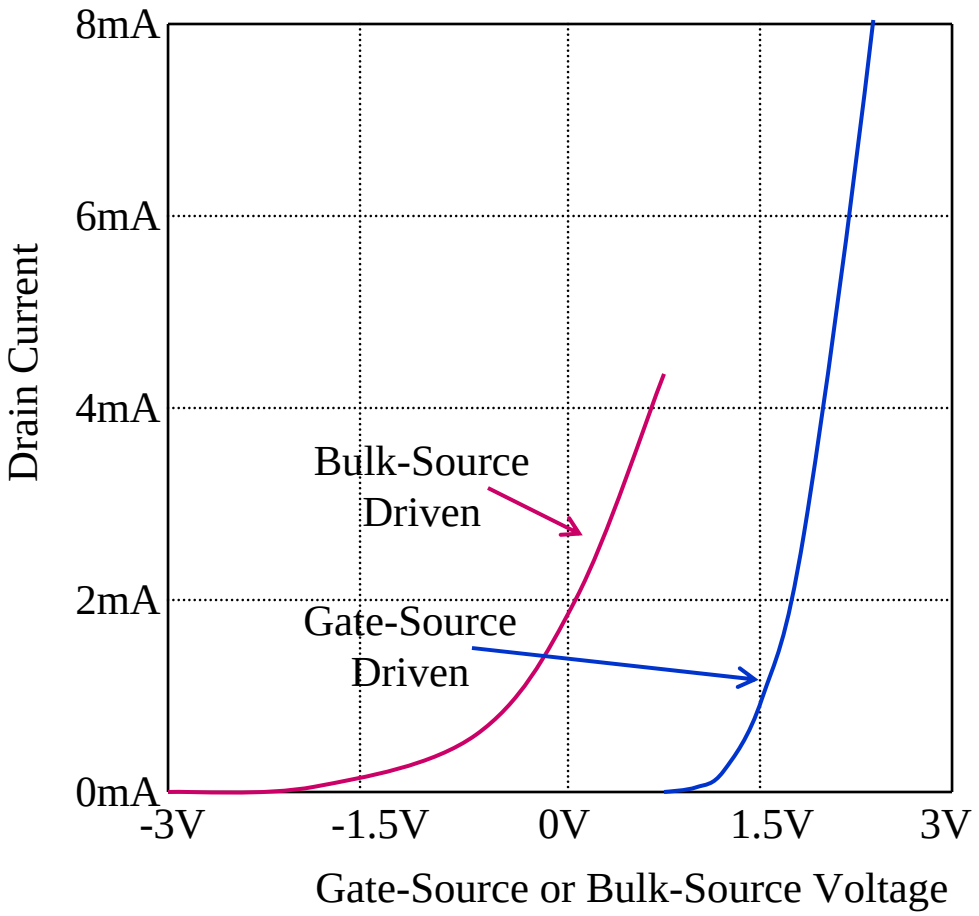
$$Gm_{eff} = g_{mb},$$

$$g_o = g_{o,Ib} + g_{o,M1}$$

Bulk-Driven MOS Transistor Characteristics

- I_D vs. V_{BS} or V_{GS} of bulk-driven and conventional gate-driven MOS transistors





Theoretical Aspects of Bulk-Driven MOS Transistors

- First order theory gives the drain current, i_D, of a MOSFET as

$$i_D = K_P\left(\frac{W}{L}\right)\left(v_{GS} - V_T - \frac{n}{2}v_{DS}\right)v_{DS}, \quad v_{DS} \le V_{DSsat} \qquad (1)$$

and

$$i_D = \frac{K_P}{2n}\frac{W}{L}(v_{GS} - V_T)^2(1 + \lambda v_{DS}), \quad v_{DS} \ge V_{DSsat} \qquad (2)$$

where

$$n = 1 + \frac{\gamma}{2\sqrt{\phi_j - V_{BS}}} = 1 + \eta = 1 + \frac{g_{mb}}{g_m}, \qquad (3)$$

$$V_T = V_{T0} \pm \gamma\left(\sqrt{2\,|\phi_F| - V_{BS}} - \sqrt{2\,|\phi_F|}\right), \qquad (4)$$

and

$$V_{DSsat} = \frac{V_{GS} - V_T}{n}, \qquad (5)$$

Theoretical Aspects of Bulk-Driven MOS Transistors (*cont'd*)

Expand V_T term in expression (1) and (2) we can get

$$i_D = K_P \frac{W}{L}[V_{GS} - V_{T0} + \gamma(\sqrt{2\phi_F} - \sqrt{2\phi_F - v_{BS}}) - \frac{n}{2}v_{DS}]v_{DS}, \quad v_{DS} \le V_{DSsat} \tag{6}$$

and

$$i_D = \frac{K_P}{2}\frac{W}{L}[V_{GS} - V_{T0} + \gamma(\sqrt{2\phi_F} - \sqrt{2\phi_F - v_{BS}})]^2(1 + \lambda v_{DS}), \quad v_{DS} \ge V_{DSsat} \tag{7}$$

Practically, V_{BS} should be less than the turn-on voltage of the bulk-channel PN junction diode, i.e.,

$$V_{BS} < V_{DIODE}$$

Where, V_{DIODE} is normally in the range of 0.6 to 0.7V.

Notice that, when V_{BS} is critically large, latch-up may be incurred because of the parasitic BJTs in CMOS process.

Theoretical Aspects of Bulk-Driven MOS Transistors (*cont'd*)

- Above equations are used for the theoretical predictions of the bulk-driven MOS transistor's drain current, but test results suggest that they need to be re-examined to permit better correlation between experimental and theoretical results.

- Berkeley short-channel insulated-gate (BSIM) model can model bulk-driven operation reasonably well, but BSIM model tends to overestimate the bulk current when the bulk-source junction is forward biased.

- Extensive experimental results show that latch-up has not appeared to be a significant problem.

Advantages of Bulk-Driven MOS Transistors

- The depletion characteristic allows zero, negative, and even small positive values of bias voltage to achieve the desired dc current. This can lead to larger input common mode voltage range and voltage swing that could not otherwise be achieved at low power supply voltages. (Please refer the following example in this section and bulk-driven differential pair discussed in following sections)
- We can use the conventional gate to modulate the bulk-driven MOS transistor.

- Example

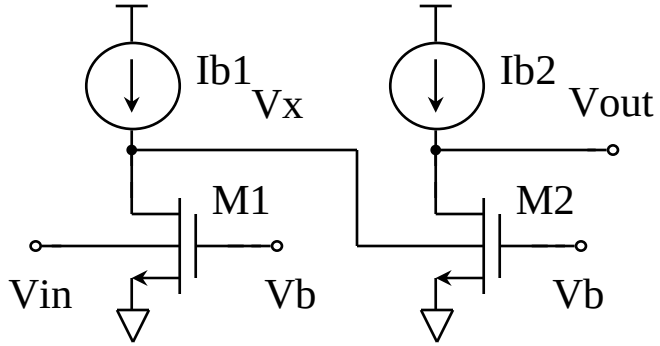
  Assume for the low voltage amplifiers, power supply voltage is

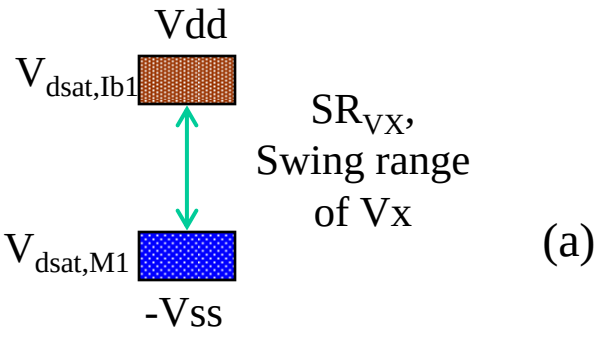
  $V_{sup} = Vdd + |Vss| < V_{DIODE} + V_{dsat}$,

  where V_{DIODE} is the forward Si diode cut-in voltage.

  The voltage swing of Vx (Figure a, the amplifier with bulk-driven MOS FETs) has only $2V_{dsat}$'s decrease over V_{sup}. In such a low voltage, the conventional gate-driven amplifier (Figure b) fails to operate or may be greatly limited in voltage swing.

Overhead of Bulk-Driven MOS Transistors

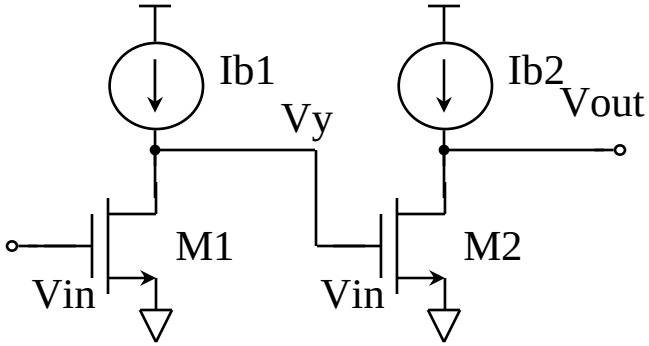


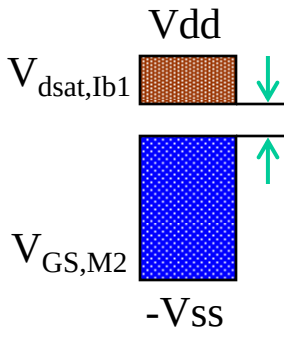


SR_{VX}, Swing range of Vx

(a)

$SR_{VX}=V_{sup}-V_{dsat,Ib1}-V_{dsat,M1}$





Swing range of Vy

(b)

$SR_{VY}=V_{sup}-V_{dsat,Ib1}-V_{GS,M2}$

$= V_{sup}-V_{dsat,Ib1}-V_{dsat,M2}-V_T$

The bulk-driven amplifier is more suitable for low voltage operation. Please notice that the maximum allowable voltage at Vx is V_{DIODE}.

Disadvantages of Bulk-Driven MOS Transistors

- The transconductance of a bulk-driven MOS FET is substantially smaller than a conventional gate-driven MOS transistor. This may result in lower GBW and worse frequency response, but better linearity and smaller power supply requirements.
- For a conventional gate-driven MOSFET, the frequency response capacity is described by its transitional frequency, f_T,

$$f_{T,gate-driven} = \frac{g_m}{2\pi C_{gs}}$$

- For the bulk-driven MOSFET, f_T is given by

$$f_{T,bulk-driven} = \frac{g_{mb}}{2\pi(C_{bs}+C_{bsub})} = \frac{\eta g_m}{2\pi(C_{bs}+C_{bsub})}$$

where η is the ratio of g_{mb} to g_m and typically has a value in the range of 0.2 to 0.4.

Disadvantages of Bulk-Driven MOS Transistors (*cont'd*)

- For typical saturated strong inversion MOSFET operation, the following approximation stands,

$$f_{T,bulk-driven} \approx \frac{\eta}{3.8} f_{T,gate-driven}$$

- Another disadvantage of bulk-driven MOSFETs is that the polarity of the bulk-driven MOSFETs is process related. For an P well CMOS process, we only have N channel bulk-driven MOSFETs available, and for N well CMOS process, only P channel MOSFETs. This limits its application. We can not use bulk-driven MOS transistors in some circuit structures which requires both N and P MOSFETs.

Disadvantages of Bulk-Driven MOS Transistors (*cont'd*)

- We know that if MOS transistors can be laid out in the same well instead than in differential wells, they will match better. Bulk driven transistors are in differential wells, it is inconvenient to design some circuits which require tight matching between transistors. For bulk-driven MOSFETs, it is not easy to utilize some layout techniques such as interdigitized and common centroid layout to make good matching.

- Potentials to turn on the parasitic BJT transistors which may result in latch-up problem

- The equivalent noise of a bulk-driven MOS amplifier is larger than a conventional gate-driven MOS amplifier.

Disadvantages of Bulk-Driven MOS Transistors (*cont'd*)

Obviously, the channel noise current is identical for a conventional gate-driven MOSFET and a bulk-driven MOSFET. But because g_{mb} is much smaller than g_m, the equivalent input noise for a bulk driven MOSFET is much larger than that of a conventional gate-driven MOSFET.

The channel noise current is identical in gate-driven and bulk-driven cases, which is given by

$$\overline{di_{DS}^2} = \frac{8kT}{3} g_m df ,$$

The equivalent input noise voltage of a conventional gate-driven MOS amplifier is

$$\overline{dv_{ieq,gate-driven}^2} = \frac{8kT}{3} \frac{1}{g_m} df ,$$

Disadvantages of Bulk-Driven MOS Transistors (*cont'd*)

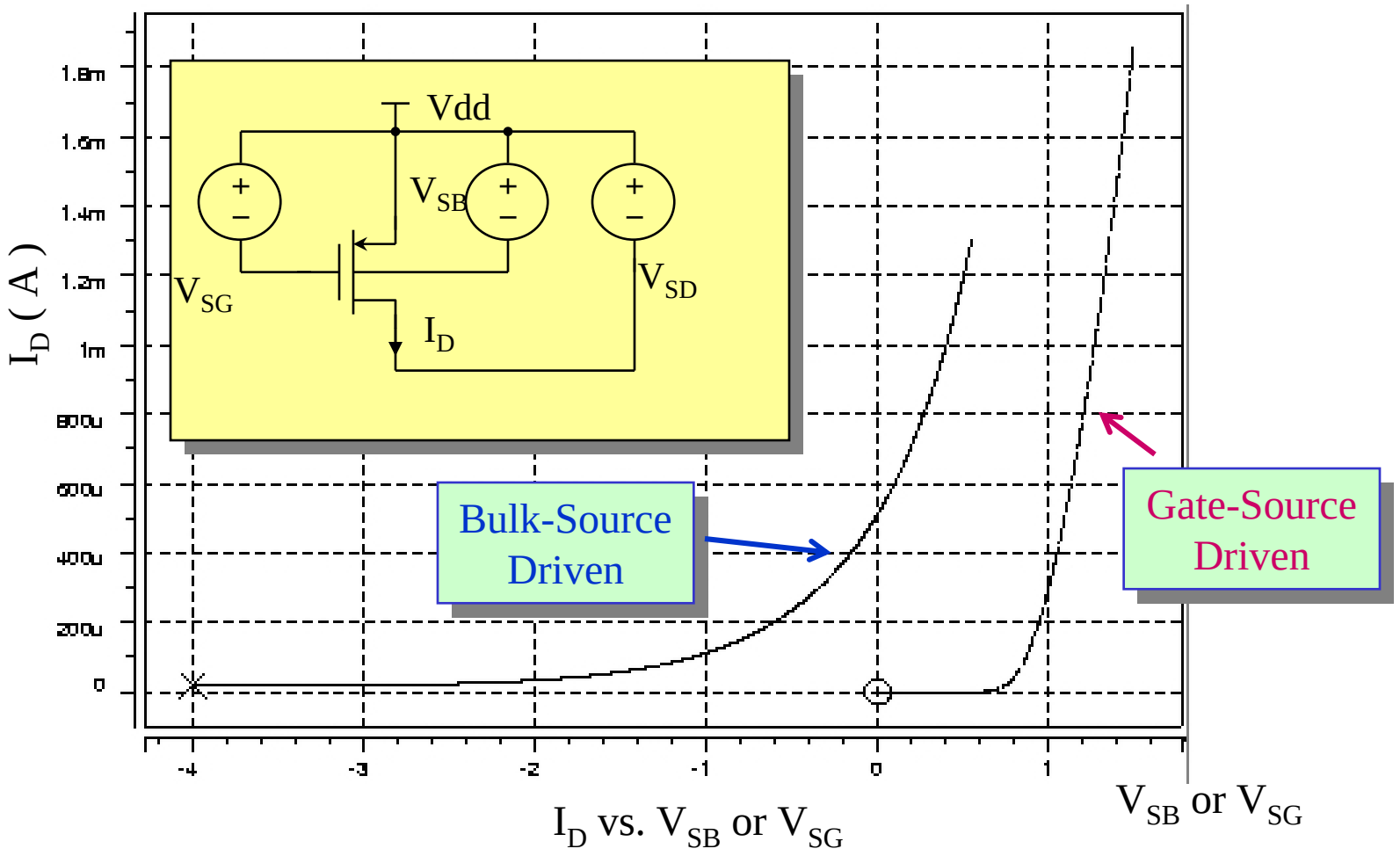
For bulk-driven MOS amplifier, the equivalent input noise voltage is

$$\overline{dv_{ieq,bulk-driven}^2} = \frac{8kT}{3}\frac{g_m}{g_{mb}^2}df = \frac{8kT}{3}\frac{1}{\eta^2 g_m}df = \frac{1}{\eta^2}\overline{dv_{ieq,gate-driven}^2},$$

which is $\frac{1}{\eta^2}$ times larger than the equivalent input noise of the conventional gate-driven MOS amplifier, $\overline{dv_{ieq,gate-driven}^2}$

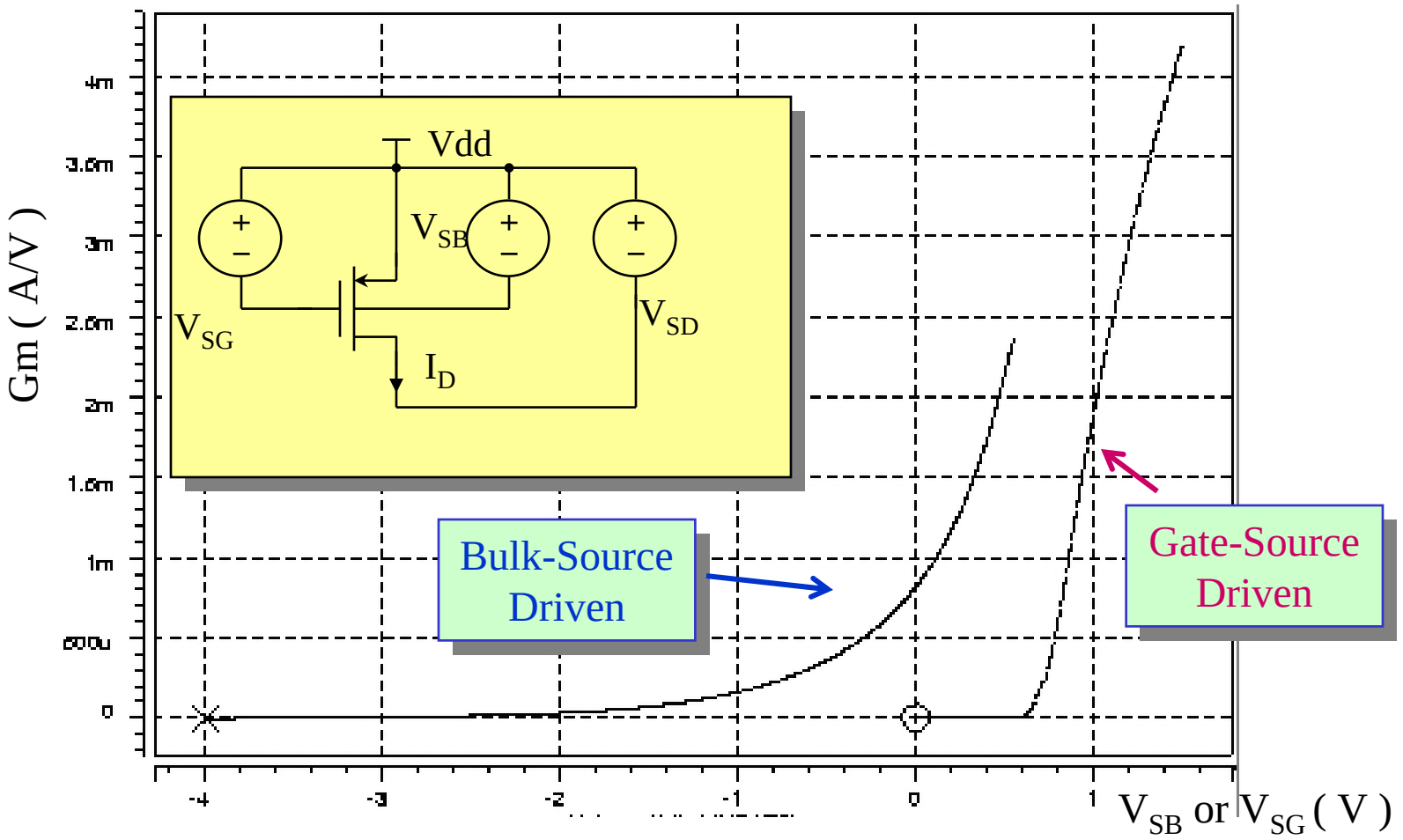
Simulation of Bulk-Driven Transistors

- We select Orbit 2.0 technology as our CMOS process for the simulation
- Orbit 2.0 CMOS process is an N-well process, we can only use P channel transistors as bulk-driven MOSFETs



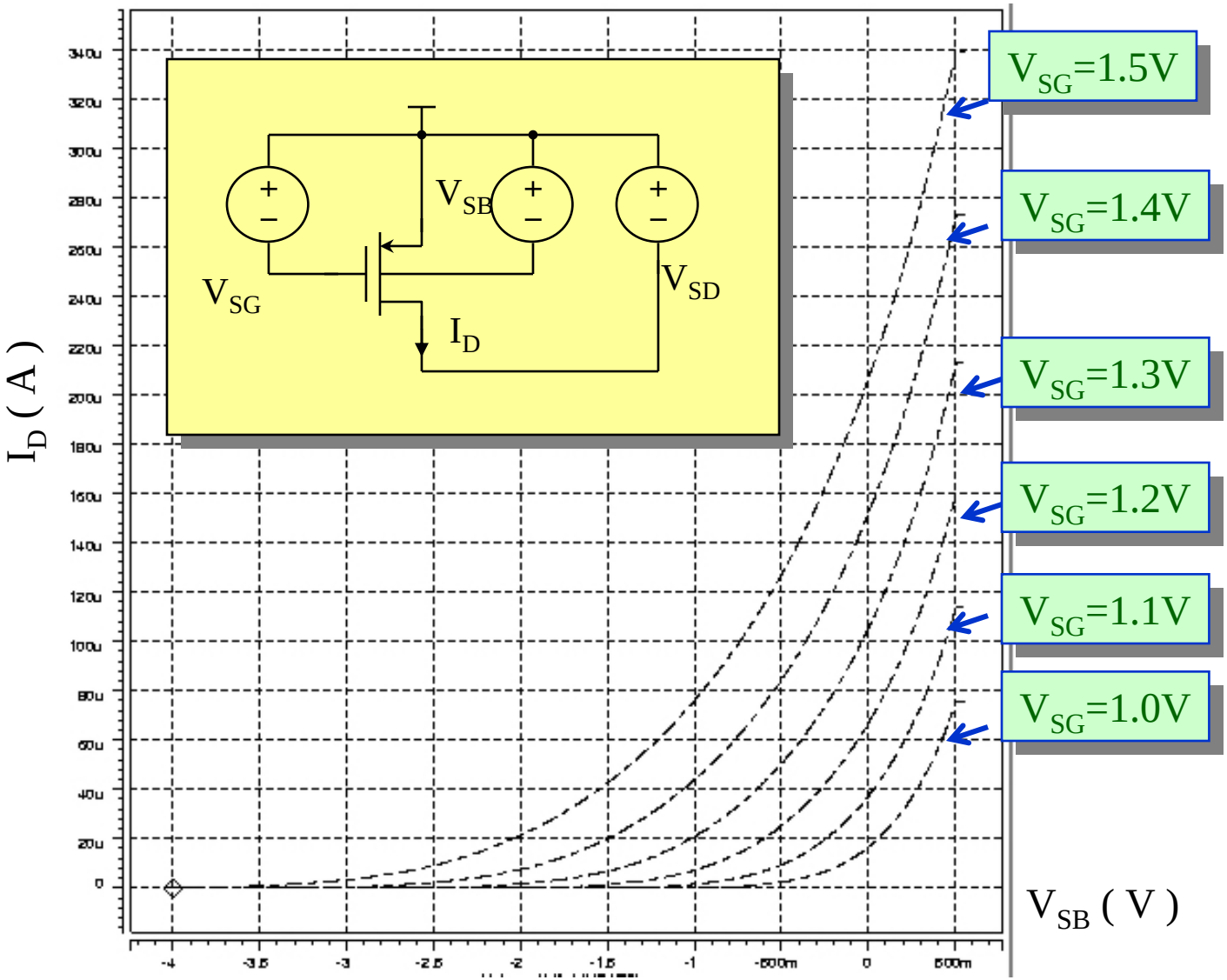
Simulation of Bulk-Driven Transistors (*cont'd*)

- Transconductance vs. V_{SB} or V_{SG}



Simulation of Bulk-Driven Transistors (*cont'd*)

- $I_D \sim V_{SB}$ Characteristic for different V_{SG}



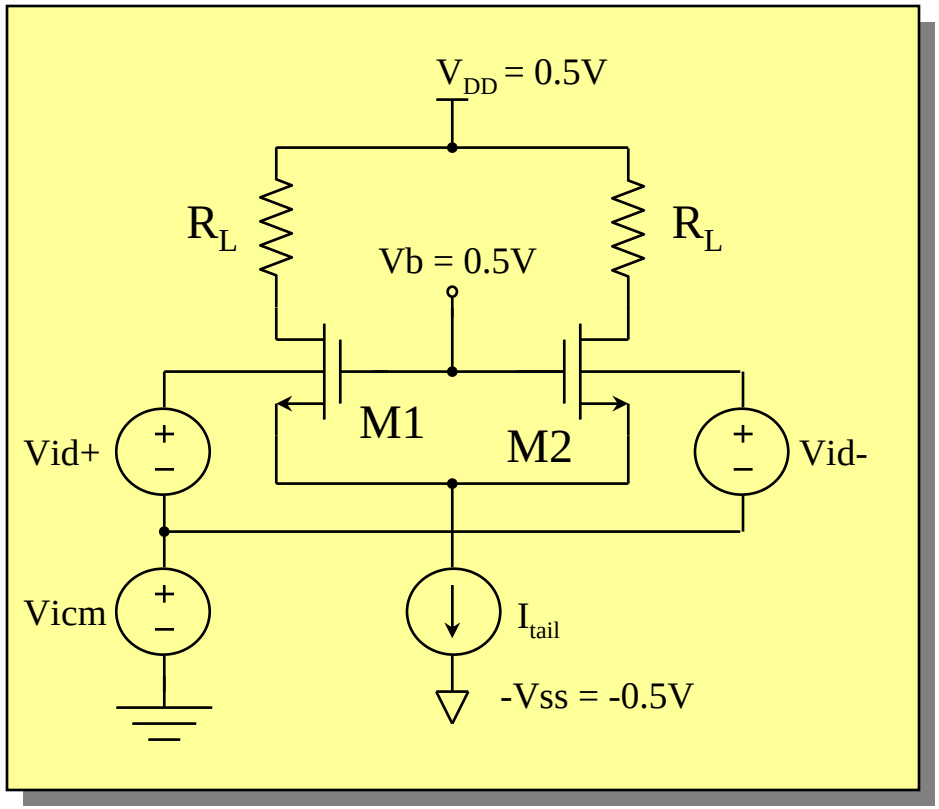
Simulation of Bulk-Driven Transistors (*cont'd*)

- We may notice that the transfer characteristic of the bulk-driven MOS FET changes greatly with different V_{GS}, because I_D is more sensitive to V_{GS} than to V_{BS}. The typical value of bias voltage V_{GS} is dependent on a specific process and working conditions of the MOS transistors. For our Orbit 2.0 process, we can select $|V_{GS}|$ from 0.9 to 1.5V.

- The tuning range of g_{mb} is very large, but please notice that with very small g_{mb}, we may have a very large reverse biasing voltage across the bulk-source PN junction, which is not practical for low voltage circuit design.

Bulk-Driven Differential Amplifier

- One of the key building blocks of analog circuits is the differential amplifier.
- The bulk-driven differential pair is shown below.



Bulk-driven MOS FET differential pair

Bulk-Driven Differential Amplifier (*cont'd*)

- The differential transconductance is given by

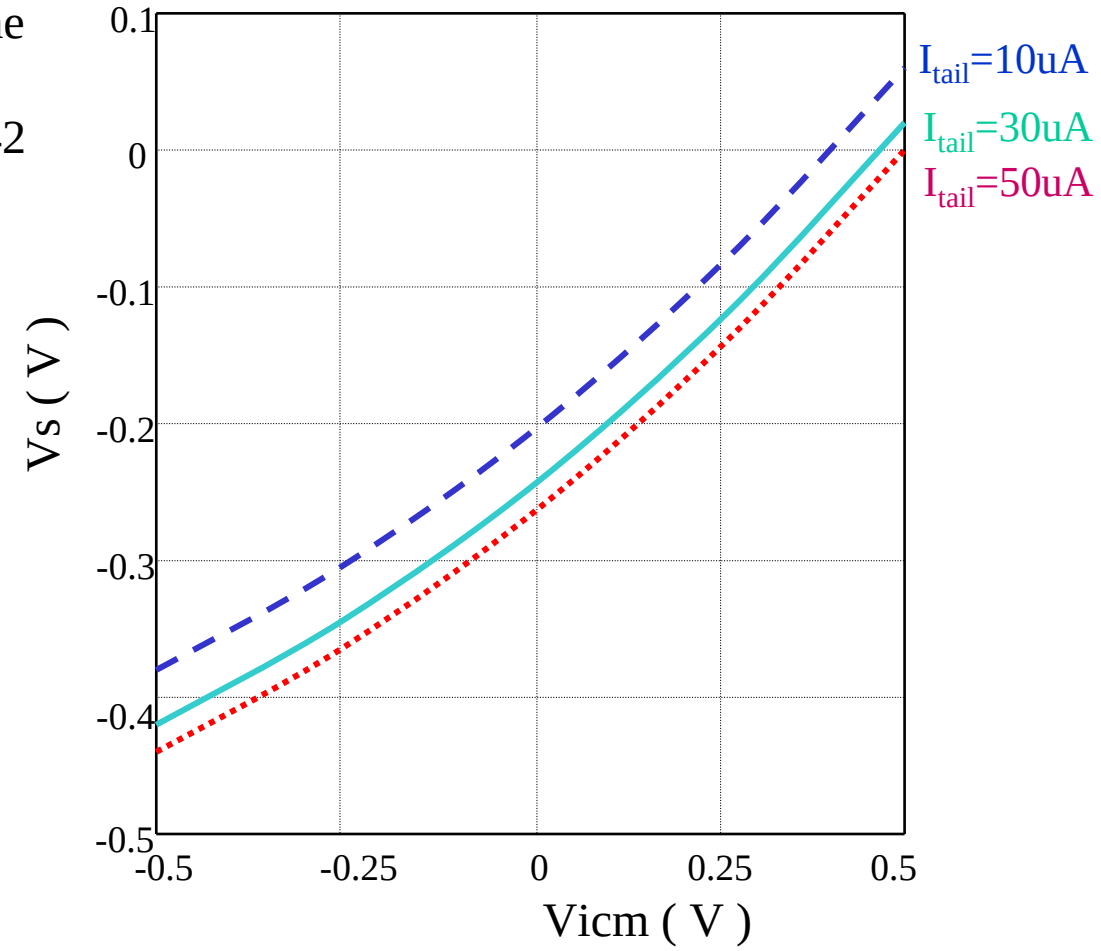
$$G_{mb} = \frac{\gamma g_m}{2\sqrt{2\phi_F - V_{icm} + V_S}} \approx \frac{\gamma\sqrt{\frac{K_P}{n}\frac{W}{L} I_{tail}}}{2\sqrt{2\phi_F - V_{icm} + V_S}}$$

  where V_S is the source-coupled node voltage.

- When the Vicm moves towards V_{DD}, V_S also moves towards V_{DD}, like conventional differential pair. But the variation of V_S is much less than Vicm, so even Vicm moves rail-to-rail, V_S only changes part of the power supply voltage range to keep current source I_{tail} in saturation region.

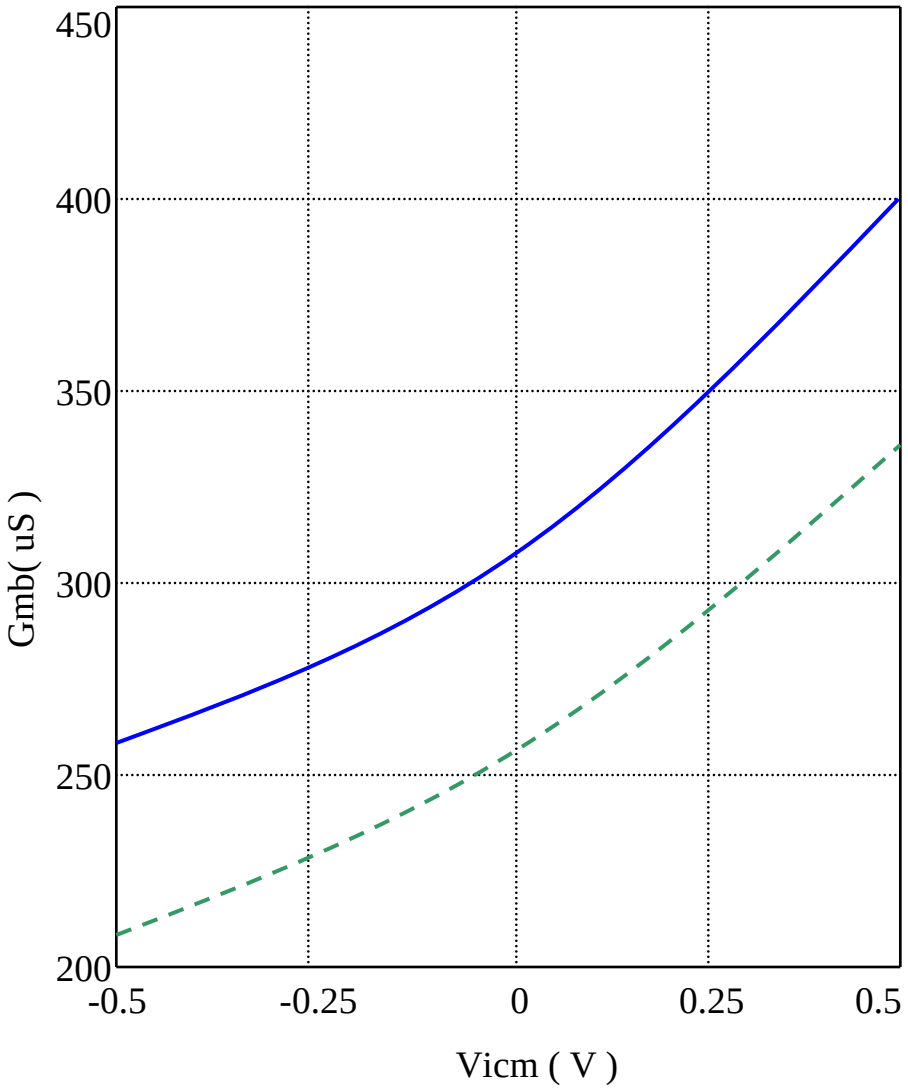
Vs (Source Voltage) vs. Vicm (Common Mode Input Voltage)

- From the Vs vs. Vicm figure, the 30 uA tail current bias corresponds to Vs reaching -0.42 when Vicm=-0.5V, leaving 80 mV across the tail current sink. When using a simple single MOSFET to provide the tail current, proper design of bulk driven differential pair can maintain saturated operation over the entire rail-to-rail common mode range.



Gm (Transconductance) vs. Vicm (Common Mode Input Voltage)

- Measured transconductance vs. common mode input voltage



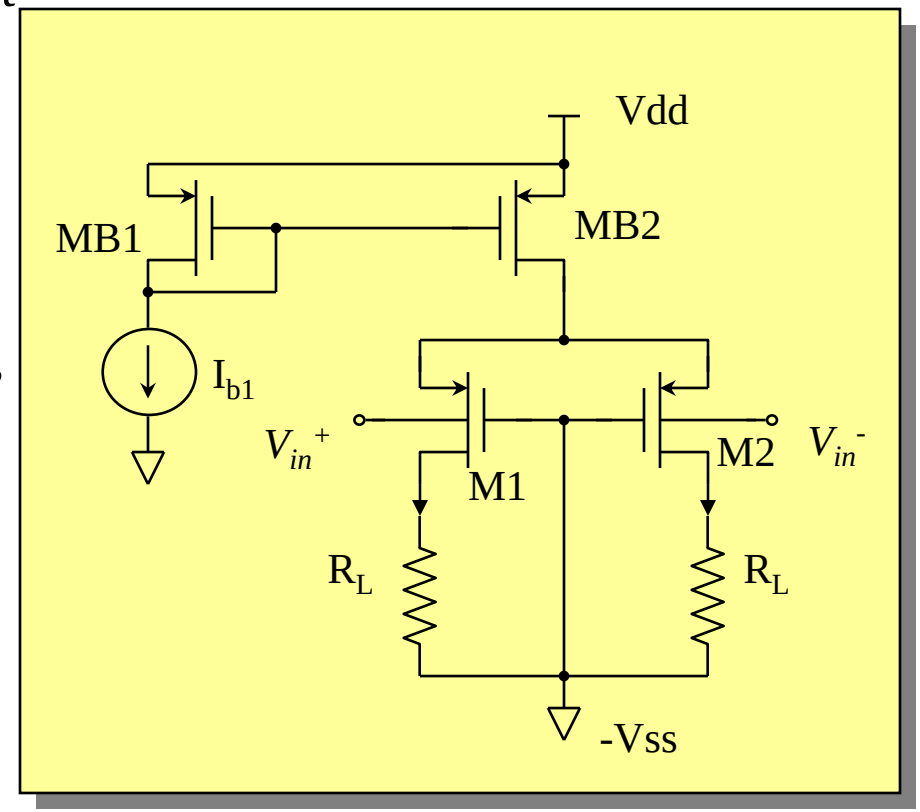
- The measured results demonstrate that Gmb increases when Vicm moves from negative power supply rail to the positive rail.
- Suppose the Gmb when Vicm = 0 is the nominal Gmb.

For Itail = 50uA case, when Vicm =-Vss, the Gmb is 16.3% below its nominal value. When Vicm=Vdd, Gmb is 30% above its nominal value.

For Itail = 40uA case, when Vicm =-Vss, the Gmb is 16.5% below its nominal value. When Vicm=Vdd, Gmb is 28% above its nominal value.

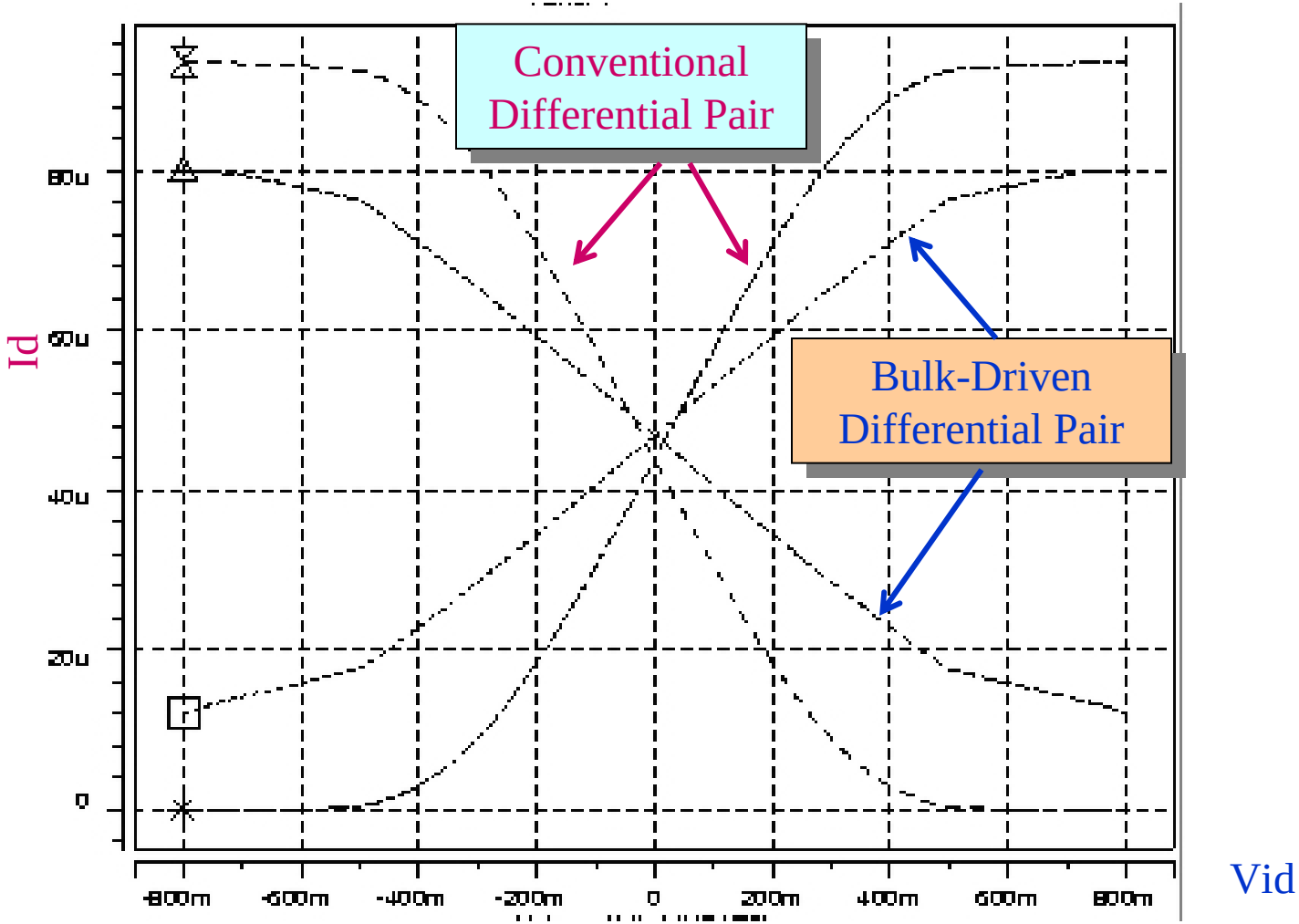
HSPICE Bulk-Driven DP Simulation

- The schematic of simulated circuit
- HSPICE Model file is MOSIS Orbit 2.0 BSIM1
- As Orbit 2.0 is an N-well process, we can only use P channel MOS transistors as bulk-driven transistors.
- M1 and M2 are the input bulk-driven differential pair
- Mb2 provides the tail current of the differential pair



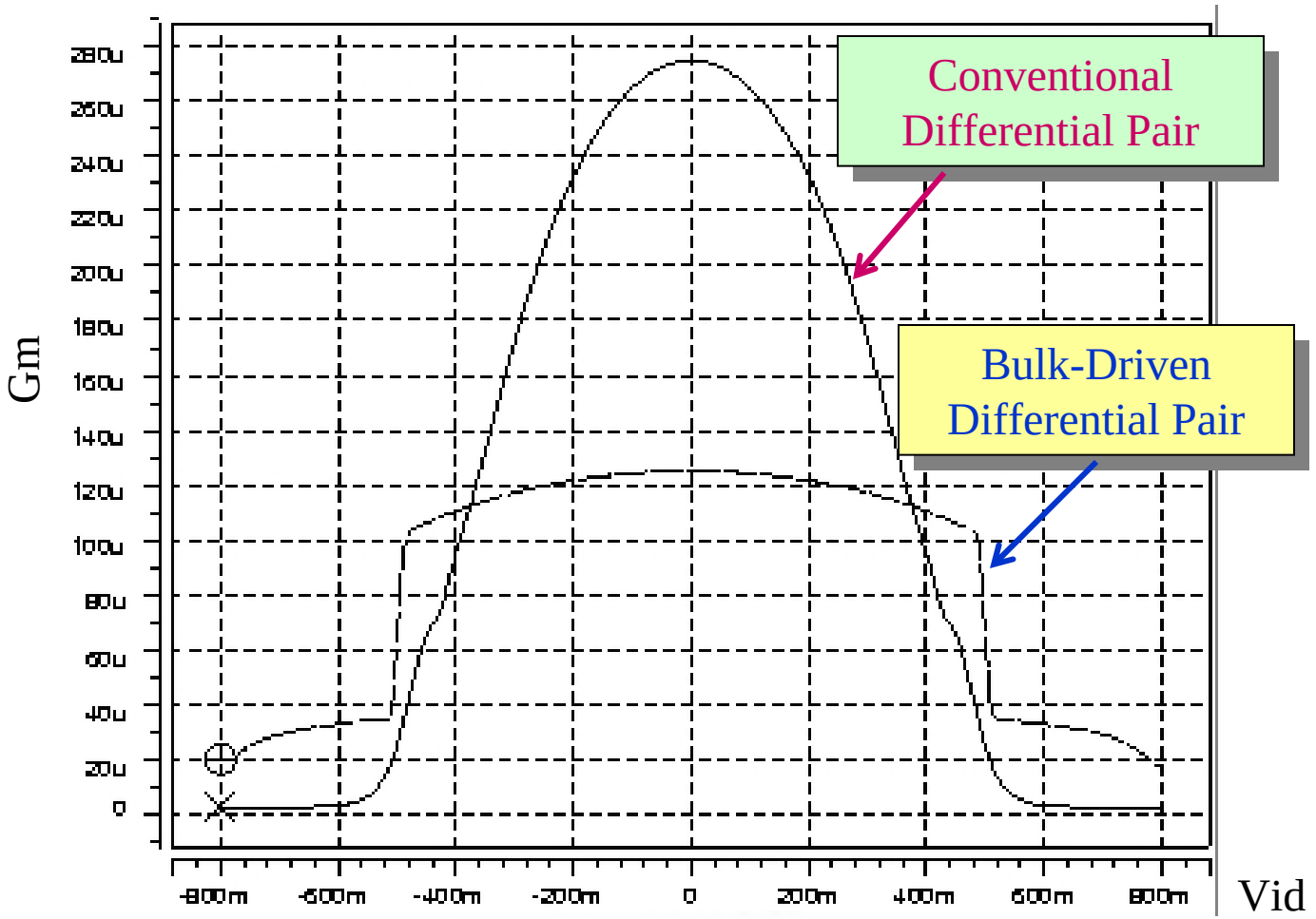
Simulation Results

- Drain Currents vs. Differential Input Voltage (compared with conventional differential pair)



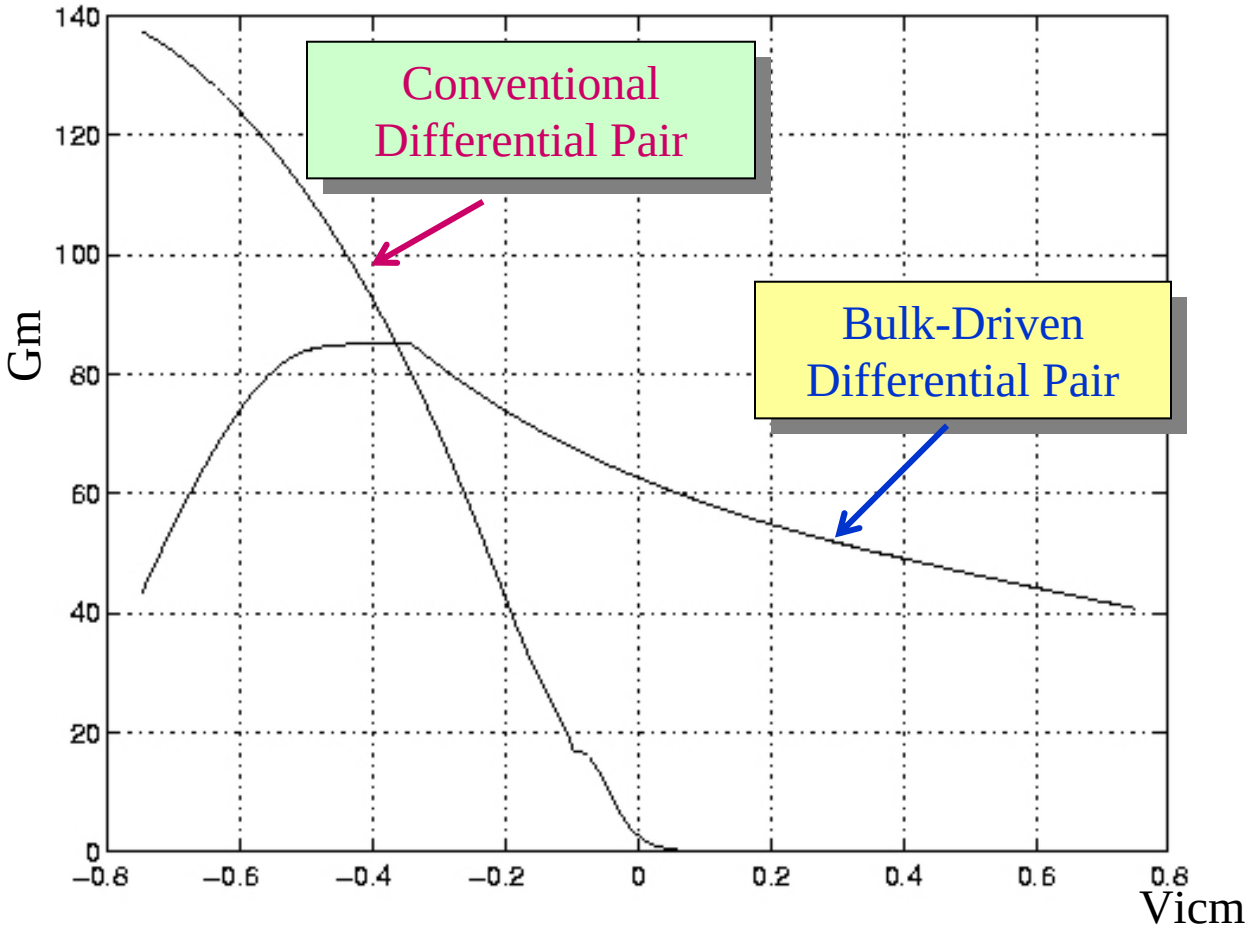
Simulation Results (*cont'd*)

- Transconductance vs. Differential Input Voltage (compared with conventional differential pair)



Simulation Results (*cont'd*)

- Transconductance vs. Common Mode Input Voltage (compared with conventional differential pair)



Simulation Results (*cont'd*)

- From the figure of "Transconductance vs. Differential Input Voltage", we notice that,
  - the $G_{m,gate\text{-}driven}$ is more than 2 times larger than $G_{m,bulk\text{-}driven}$ when Vid=0.

    I.e., Vid = 0, $G_{m,gate\text{-}driven}$ = 272 uA/V, and $G_{m,bulk\text{-}driven}$ = 126 uA/V
  - The $G_{m,bulk\text{-}driven}$ curve is flatter than $G_{m,gate\text{-}driven}$ curve.

- From the figure of "Transconductance vs. Common Mode Input Voltage", we observe that,
  - The $G_{m,gate\text{-}driven}$ changes greatly with the common mode input voltage. Conventional gate-driven differential has very narrow common mode range when working in low voltage environment.
  - Although $G_{m,bulk\text{-}driven}$ changes with the common mode input voltage, the bulk-driven differential has a rail-rail-rail common mode input range. $G_{m,bulk\text{-}driven}$ changes about +14% -32% among rail-to-rail.

HSPICE File for Simulation

```
bulk driven MOS transistor differential pair

.options list node post * captab
.include orbit_bsim.mod

* parameters
.param lam = 1u ln = 4u wn1 = 200u wnb = 400u
+ lp=4u wp1=200u

* power supply
vdd nvdd 0 0.75
vss nvss 0 -0.75

* Transistors of the differential pair
m01 nd1 nvgb 2 ninp cmosp W=wp1 L=lp AD='5*lam*wp1' AS='5*lam*wp1'
+ PS='2*wp1+10*lam' PD='2*wp1+10*lam'
m02 nd2 nvgb 2 ninm cmosp W=wp1 L=lp AD='5*lam*wp1' AS='5*lam*wp1'
+ PS='2*wp1+10*lam' PD='2*wp1+10*lam'

* Bias current mirror
mb1 10 10 nvdd nvdd cmosp W=wp1 L=lp AD='5*lam*wp1' AS='5*lam*wp1'
+ PS='2*wp1+10*lam' PD='2*wp1+10*lam'
mb2 20 10 nvdd nvdd cmosp W=wp1 L=lp AD='5*lam*wp1' AS='5*lam*wp1'
+ PS='2*wp1+10*lam' PD='2*wp1+10*lam'
```

HSPICE File for Simulation (*cont'd*)

```
* bias current source
ib 10 nvss 100u

* Bias voltage for the float gate
vgb nvdd nvgb 1.5

rl1 nd1 nd1a 1k
rl2 nd2 nd2a 1k

* Curent detector
vd1 nd1a nvss 0
vd2 nd2a nvss 0

* Tail current detector
vtail 20 2 0

* differential input signal source with common mode voltage source
einp ninp ncm input 0 0.5
einm ninm ncm input 0 -0.5
vcm ncm 0 0
vin input 0 0 ac=1
```

HSPICE File for Simulation (*cont'd*)

```
* test cards
.op
.dc vin -0.8 0.8 0.01
.dc vcm -0.75 0.75 0.01
.ac dec 400 10k 1000x

.end
```

HSPICE CMOS Model File

```
*PROCESS=ORBIT
*RUN=n83r
*WAFER=02
*Gate-oxide thickness= 412 angstroms
*DATE=9-Jun-1998
*
*NMOS PARAMETERS
*
.MODEL cmosn NMOS LEVEL=13 VFB0=
+ -9.52053E-01, 3.09754E-01,-2.90042E-01
+  7.61488E-01, 0.00000E+00, 0.00000E+00
+  1.39014E+00,-4.45856E-01, 6.81180E-01
+  2.89611E-01,-6.30567E-02,-1.23498E-02
+ -1.00639E-02, 4.33896E-02,-1.38631E-02
+  6.25492E+02,6.61066E-001,3.55486E-001
+  5.31010E-02, 3.07728E-02,-3.78445E-02
+  4.67028E-02, 1.02339E+00,-7.10990E-01
+  7.66255E+00,-4.29386E+00, 6.33325E+01
+ -2.10460E-03,-8.33750E-03,-4.08386E-03
+  7.86650E-04,-2.75358E-03,-7.99349E-03
+  1.36249E-03,-4.33134E-04, 2.20404E-02
+ -5.22311E-02, 7.66167E-02, 4.64562E-02
+  7.98013E+02, 4.92507E+02,-3.56656E+02
+ -6.07056E+00, 3.35698E+01, 1.30904E+02
+  6.36014E+00, 9.18969E+01,-8.58680E+01
```

HSPICE CMOS Model File (*cont'd*)

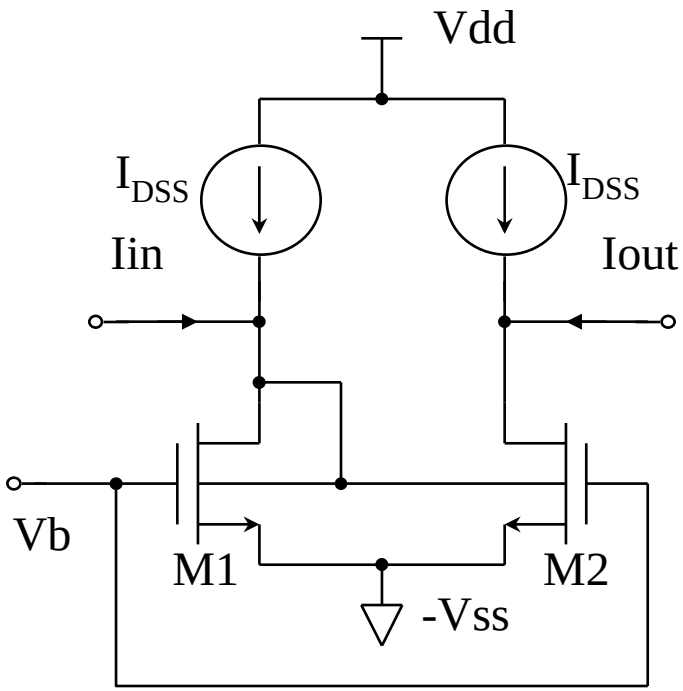
```
+ -9.64235E-03, 1.04318E-01,-9.96489E-02
+ 4.12000E-002, 2.70000E+01, 5.00000E+00
+ 4.15550E-010,4.15550E-010,4.33574E-010
+ 1.00000E+000,0.00000E+000,0.00000E+000
+ 1.00000E+000,0.00000E+000,0.00000E+000
+ 0.00000E+000,0.00000E+000,0.00000E+000
+ 0.00000E+000,0.00000E+000,0.00000E+000
+ 31.3,    1.361100e-04,    4.958500e-10,    1e-08,    0.42381
+ 0.42381,    0.6332,    0.2586,    0,    0
*
* Gate Oxide Thickness is 412 Angstroms
*
*
*PMOS PARAMETERS
*
.MODEL cmosp PMOS LEVEL=13 VFB0=
+ -3.63272E-01, 1.23277E-01, 4.76372E-03
+  6.76709E-01, 0.00000E+00, 0.00000E+00
+  6.54925E-01,-1.46643E-01, 1.59960E-01
+ -3.60661E-03, 4.25677E-02,-2.66194E-03
+ -1.33179E-02, 6.35318E-02,-3.99366E-03
+  2.13547E+02,9.04938E-001,4.12013E-001
+  1.10154E-01, 4.66882E-02,-7.57936E-02
+  1.87314E-02, 1.92437E-01,-8.25287E-02
```

HSPICE CMOS Model File (*cont'd*)

```
+  9.61742E+00,-4.70240E+00, 5.16601E+00
+  1.07426E-06,-4.68539E-03,-3.18683E-03
+  1.05708E-03,-3.48960E-03,-2.53423E-03
+  5.34803E-03,-2.92210E-03, 3.12185E-03
+ -2.35848E-03, 3.10802E-03, 1.19112E-02
+  2.19780E+02, 1.17617E+02,-2.17783E+01
+  7.40832E+00, 5.43904E-01, 1.34420E+01
+  3.63925E-01, 1.46265E+01,-1.76783E+00
+ -1.68680E-03,-7.70387E-04, 1.20730E-03
+ 4.12000E-002, 2.70000E+01, 5.00000E+00
+ 5.68850E-010,5.68850E-010,4.47609E-010
+ 1.00000E+000,0.00000E+000,0.00000E+000
+ 1.00000E+000,0.00000E+000,0.00000E+000
+ 0.00000E+000,0.00000E+000,0.00000E+000
+ 0.00000E+000,0.00000E+000,0.00000E+000
+ 61.8,    3.186100e-04,    3.098500e-10,    1e-08,    0.9
+ 0.9,    0.60597,    0.18698,    0,    0
```

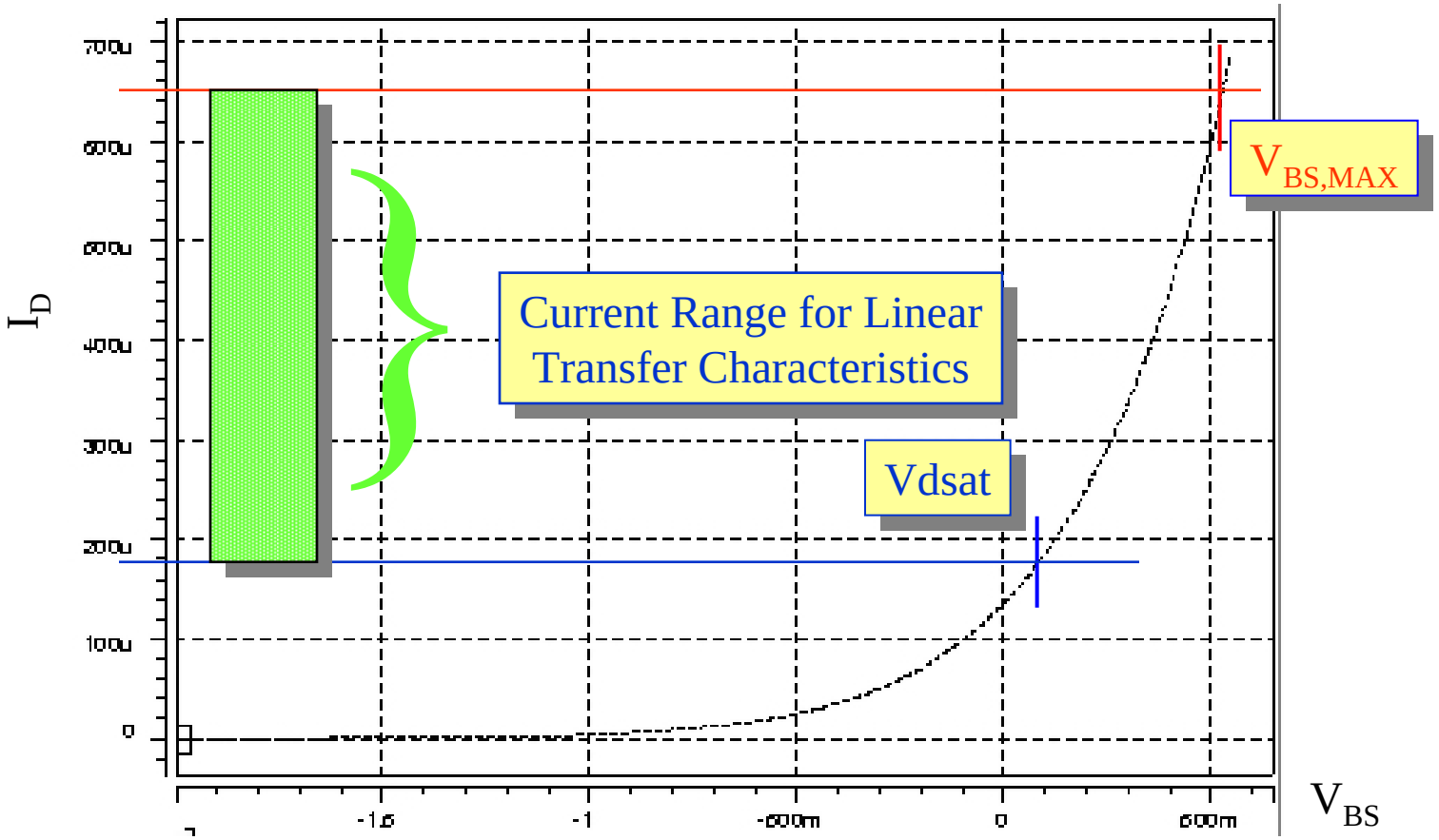
Bulk-Driven Current Mirrors

- One of the problems with conventional CMOS current mirrors is that a significant voltage must dropped across the input device. If the bulk-driven MOSFET is operating with the bulk-source junction slightly forward biased, this voltage drop is minimized.
- The simple bulk-driven current mirror (N channel MOS, P well process) is shown below.



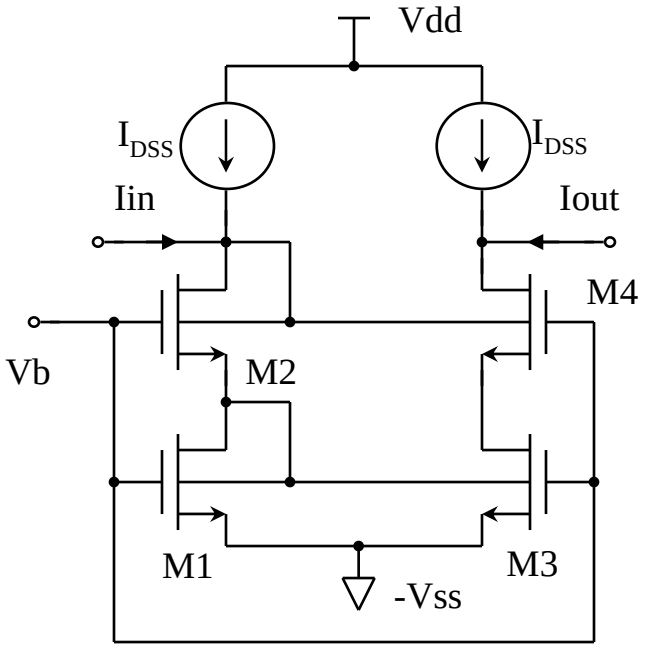
Bulk-Driven Current Mirrors (*cont'd*)

- Please observe the I_D vs. V_{GS} characteristic curve of the bulk driven transistor.
- For M1, as the bulk and drain are tied together, V_{BS} should be greater than Vdsat to ensure saturated operation. And at the same time, V_{BS} must be less than $V_{BS,MAX}$, or the bulk-channel PN junction will be hard forward biased and latchup may result!

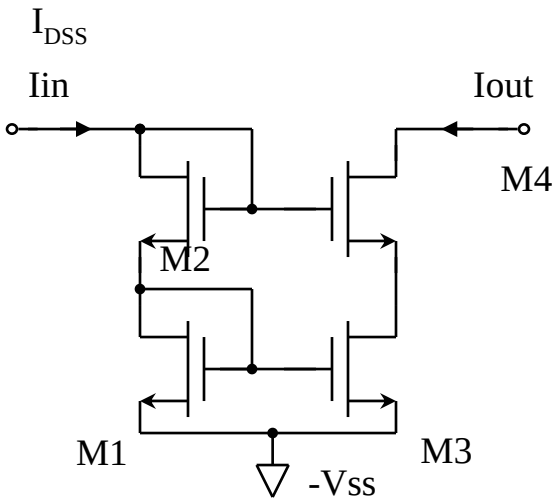


Bulk-Driven Current Mirrors (*cont'd*)

- Cascode Bulk-Driven Current Mirror as shown in Figure (a) which is a direct translation of conventional cascode current mirror (Figure (b)).
- I_{DSS} bias current is to ensure the current flows through the current is in linear range, which we discussed in the previous slide.



(a)



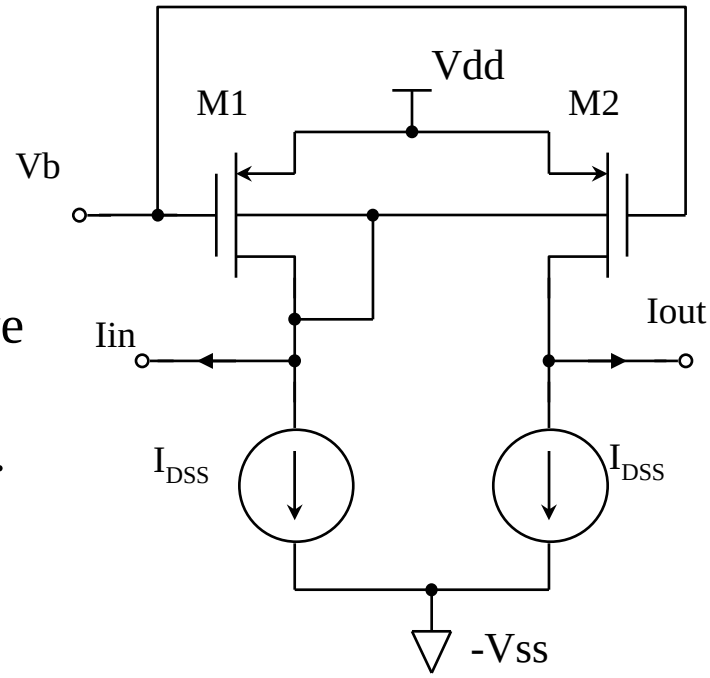
(b)

Simulation of Simple Bulk-Driven Current Mirror

- The schematic of simulated circuit

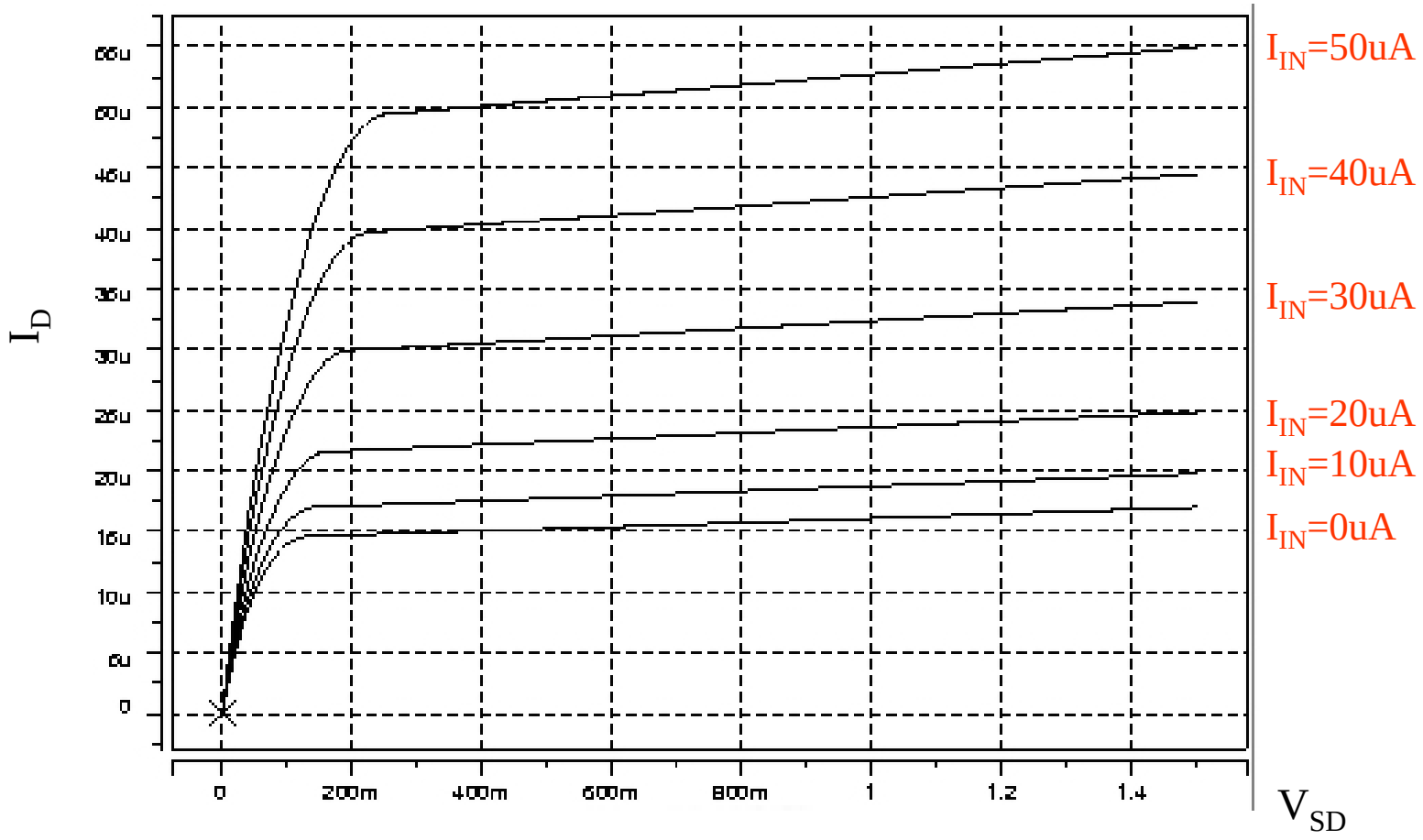
- HSPICE Model file is MOSIS Orbit 2.0 BSIM1

- As Orbit 2.0 is an N-well process, we can only use P channel MOS transistors as bulk-driven transistors. We have to revise the circuit shown in previous slide to P-channel MOS transistors.



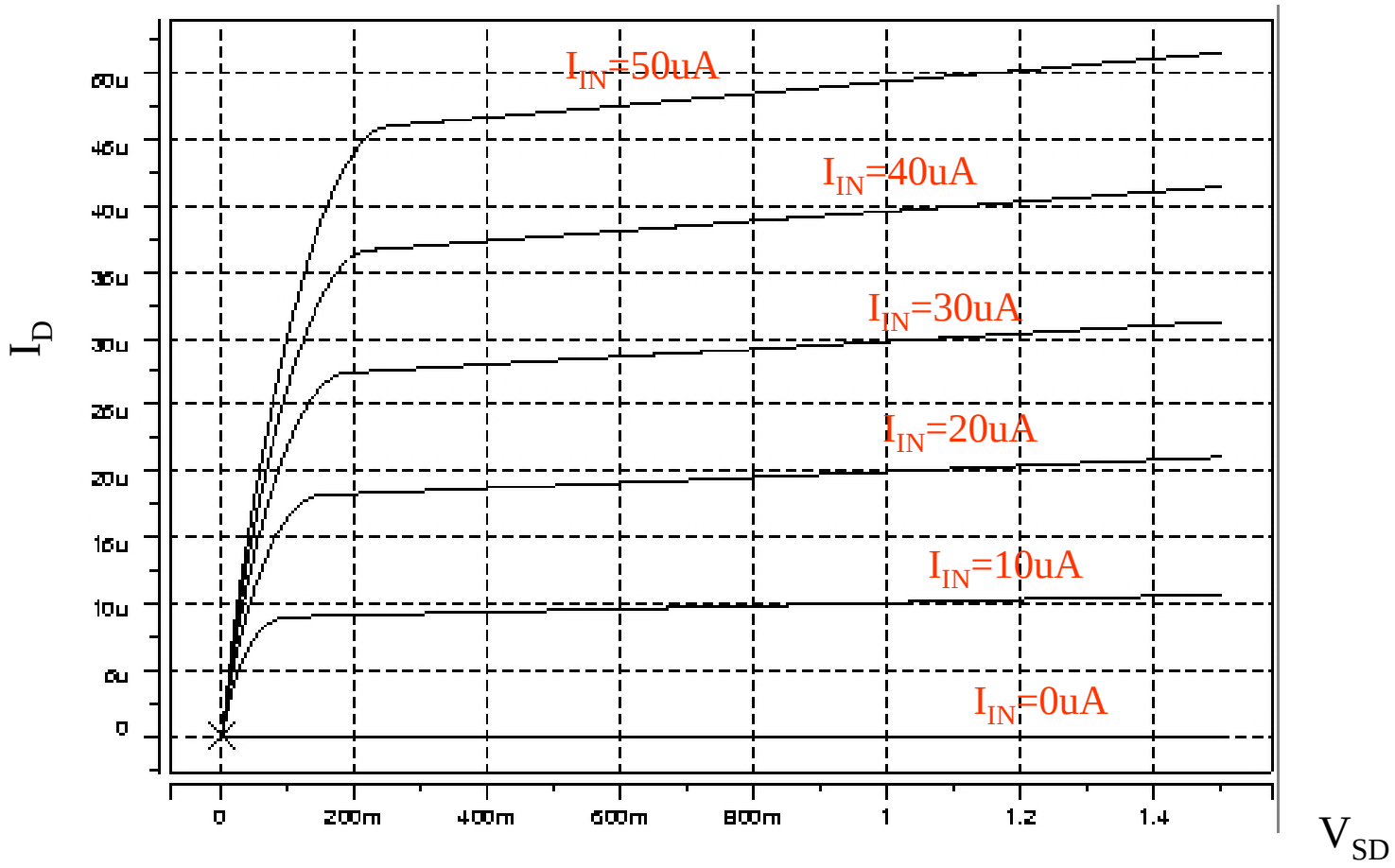
Simulation of Simple Bulk-Driven Current Mirror (*cont'd*)

- DC Sweep of Simple Bulk-Driven Current Mirror



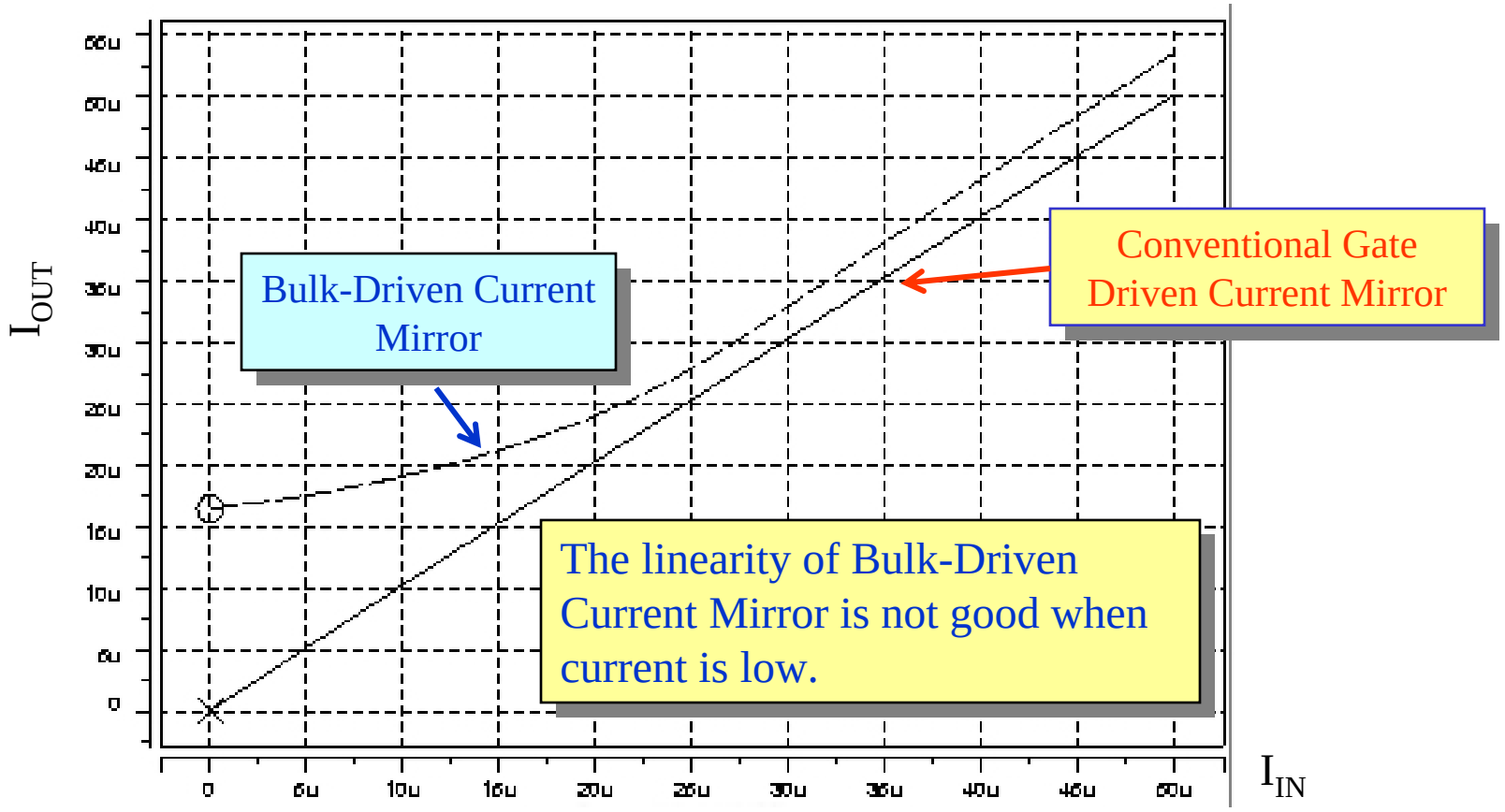
Simulation of Simple Bulk-Driven Current Mirror (*cont'd*)

- DC Sweep of Conventional Gate-Driven Current Mirror



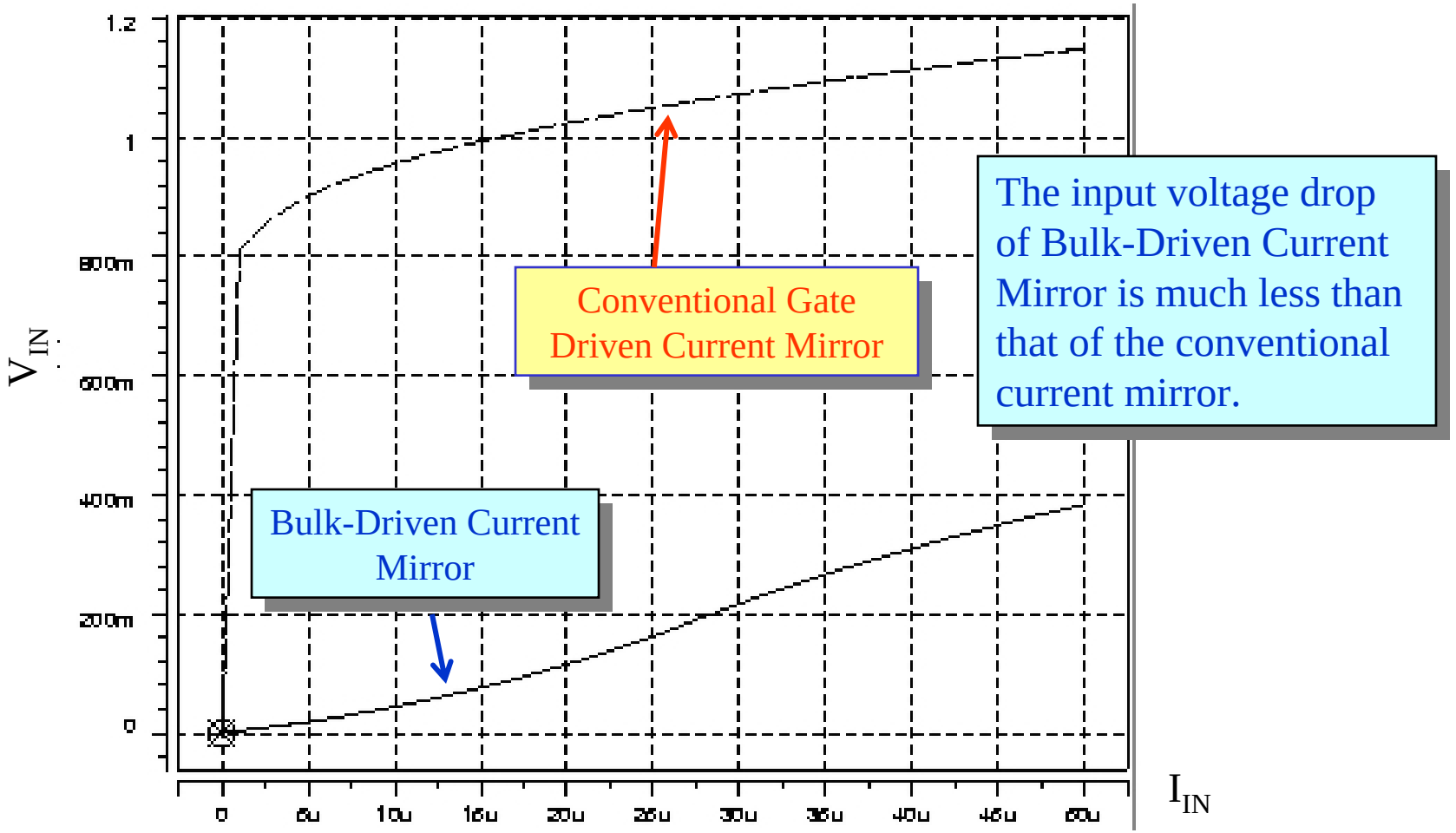
Simulation of Simple Bulk-Driven Current Mirror (*cont'd*)

- Input Output Transfer Characteristics



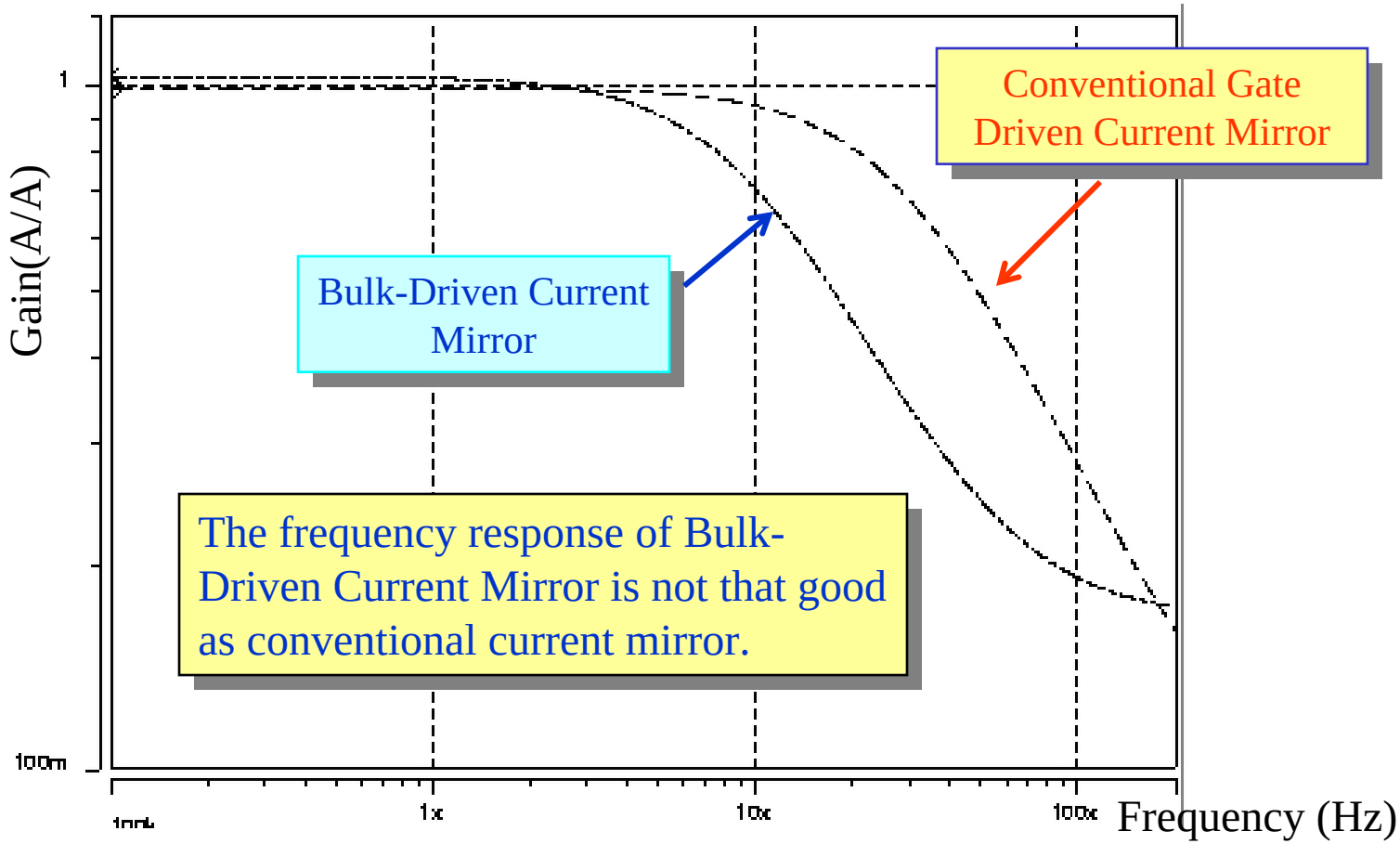
Simulation of Simple Bulk-Driven Current Mirror (*cont'd*)

- Input Voltage vs. Input Current Characteristics



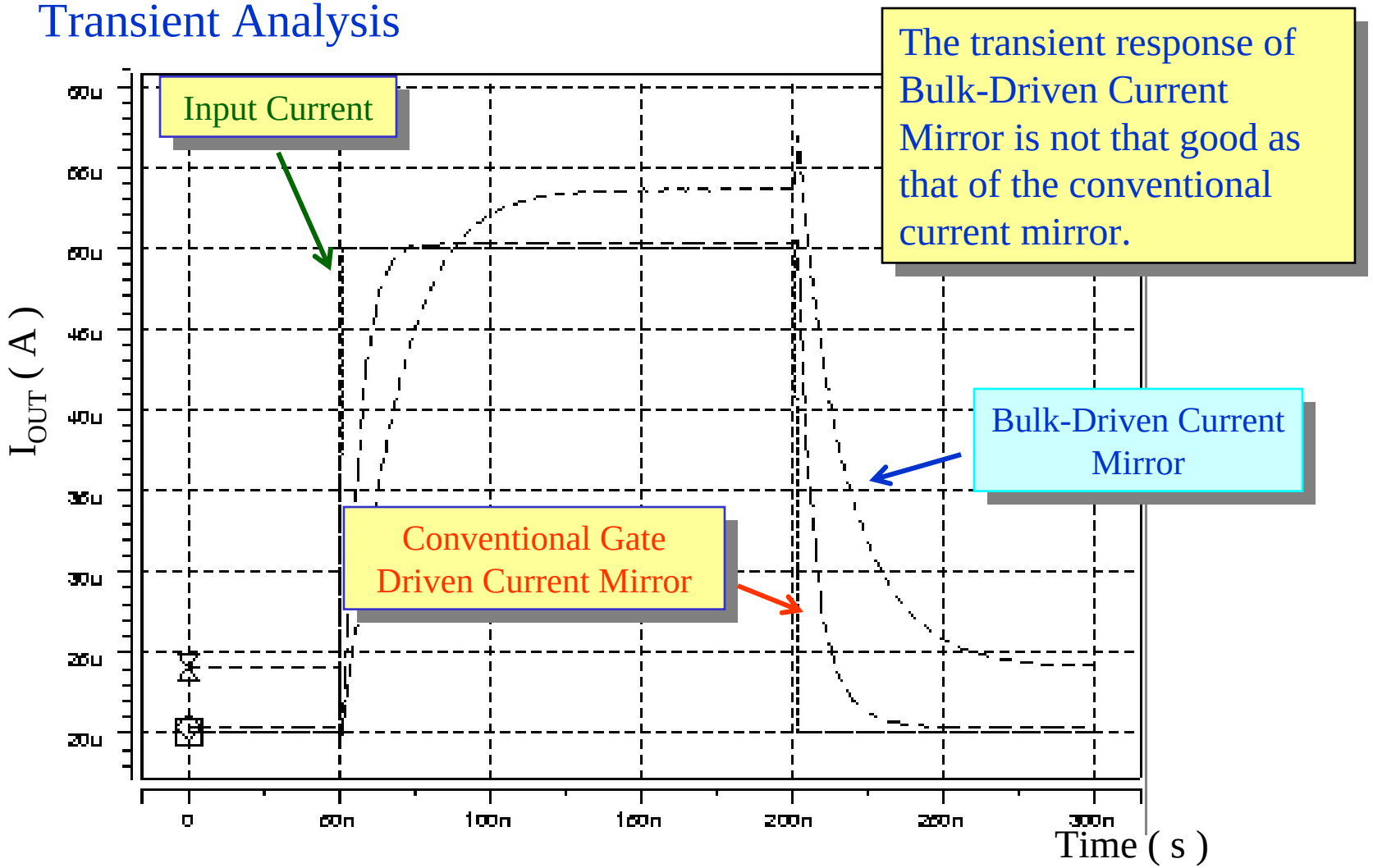
Simulation of Simple Bulk-Driven Current Mirror (*cont'd*)

- Frequency Response



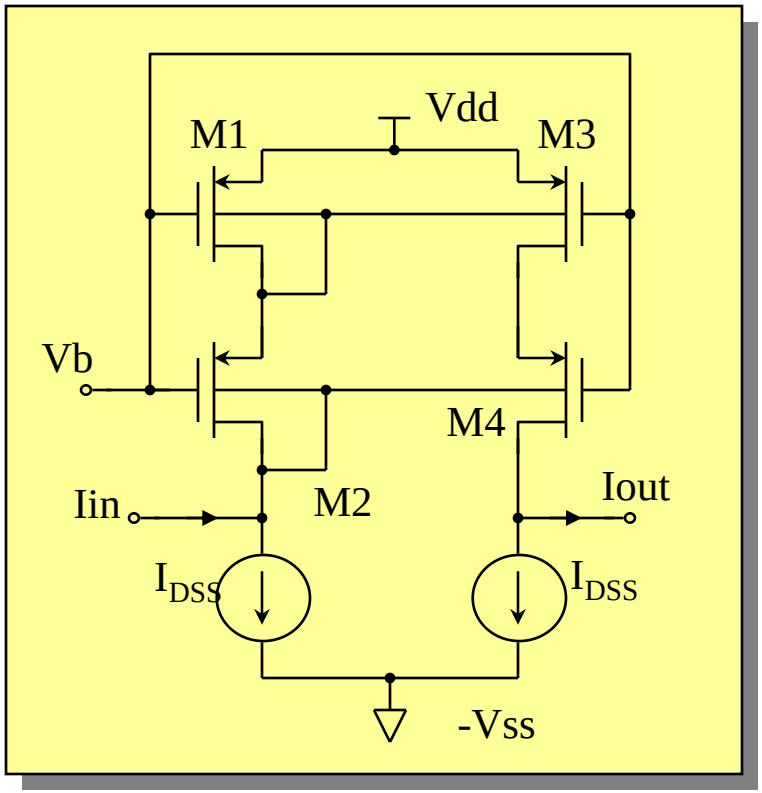
Simulation of Simple Bulk-Driven Current Mirror (*cont'd*)

- Transient Analysis

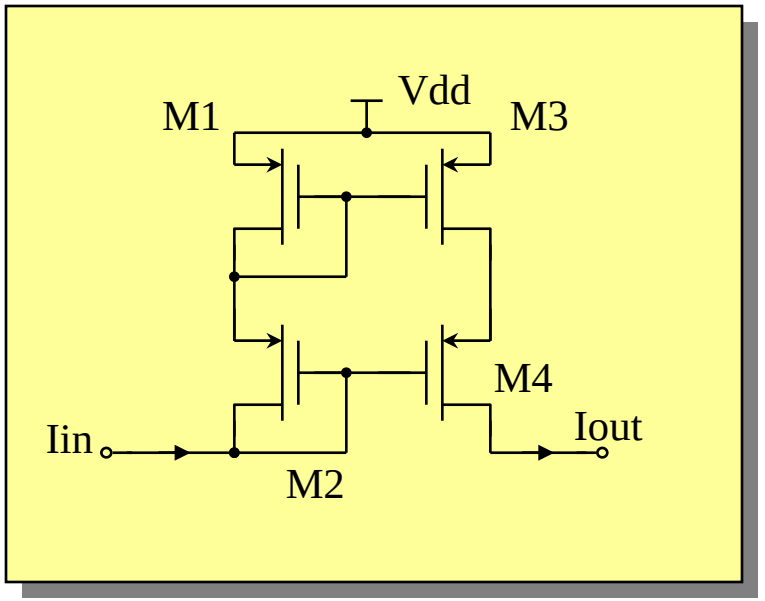


Simulation of Cascode Bulk-Driven Current Mirror

- The schematics of simulated circuits
- HSPICE Model is MOSIS Orbit 2.0 BSIM1



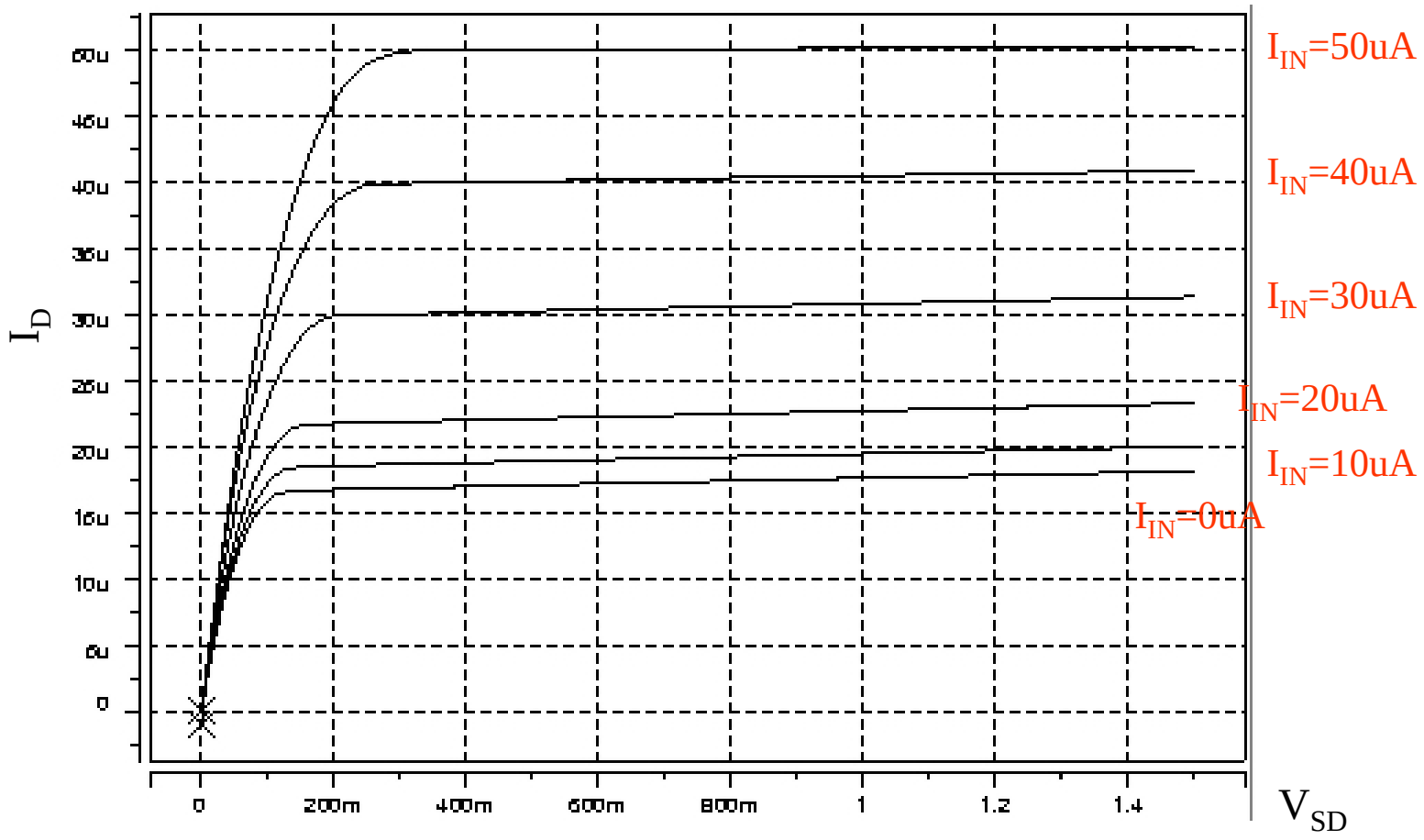
(a) Cascode Bulk-Driven Current Mirror



(b) Cascode Conventional Current Mirror

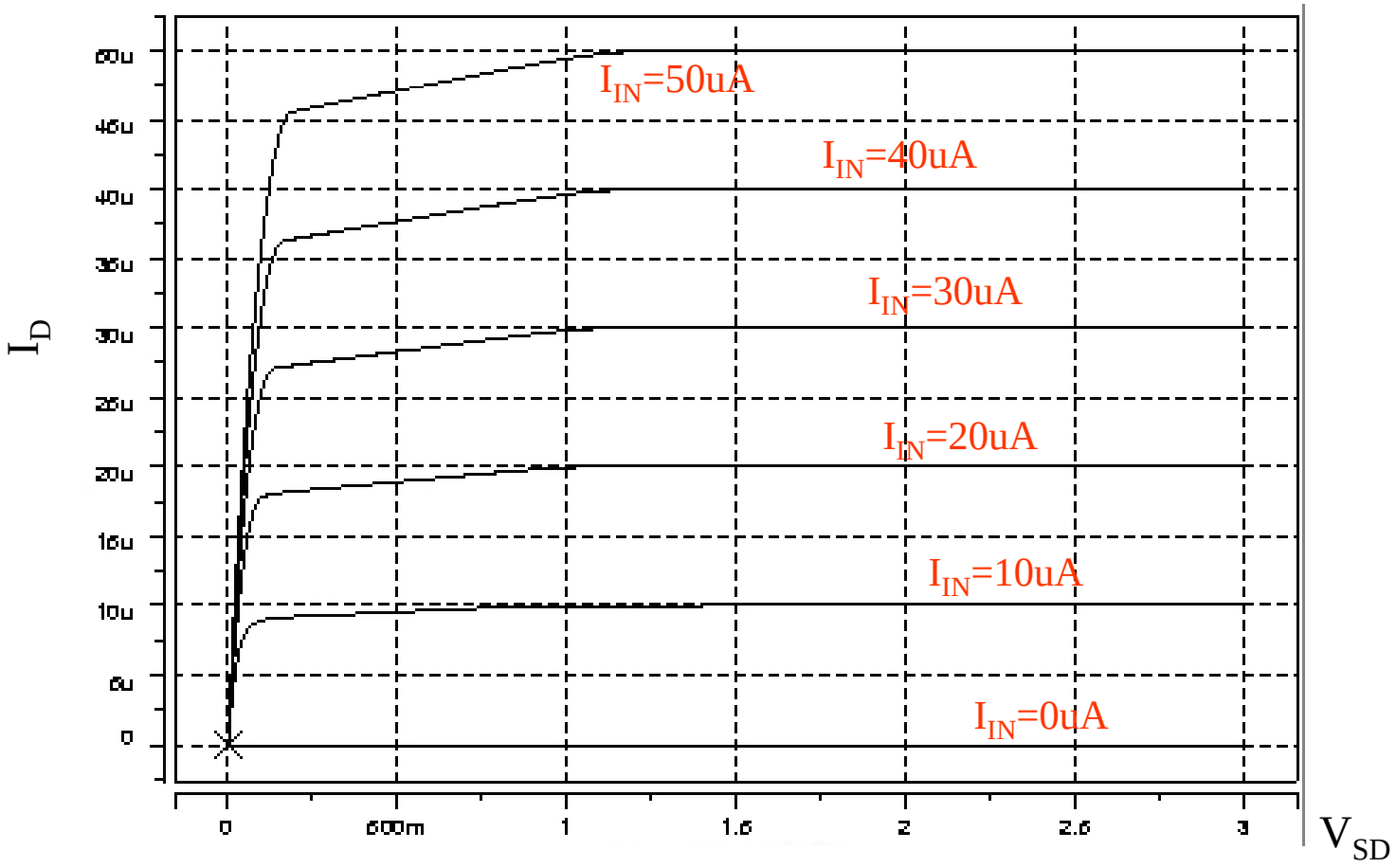
Simulation of Cascode Bulk-Driven Current Mirror (cont'd)

- DC Sweep of Cascode Bulk-Driven Current Mirror



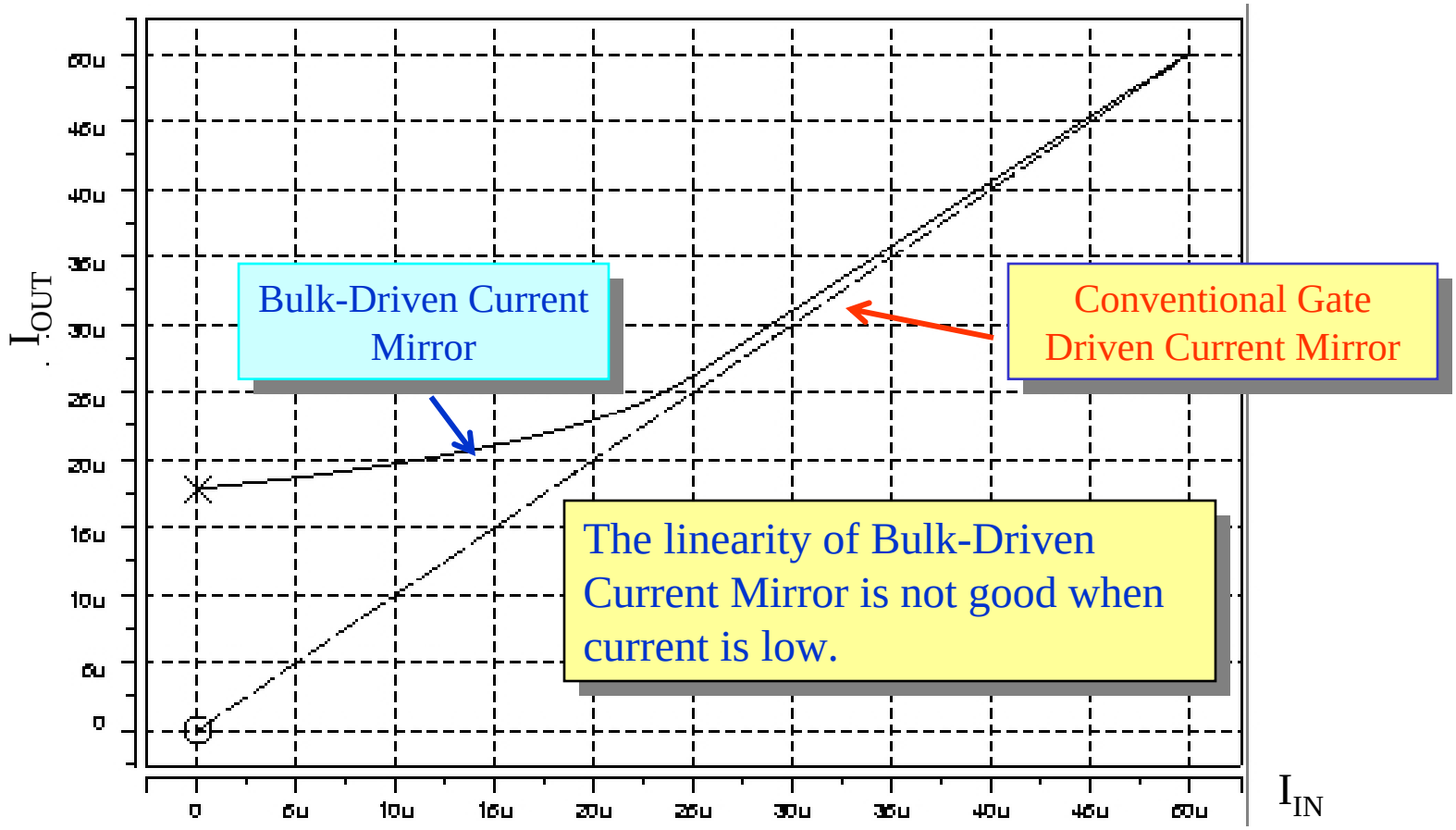
Simulation of Cascode Bulk-Driven Current Mirror (*cont'd*)

- DC Sweep of Conventional Gate-Driven Cacode Current Mirror



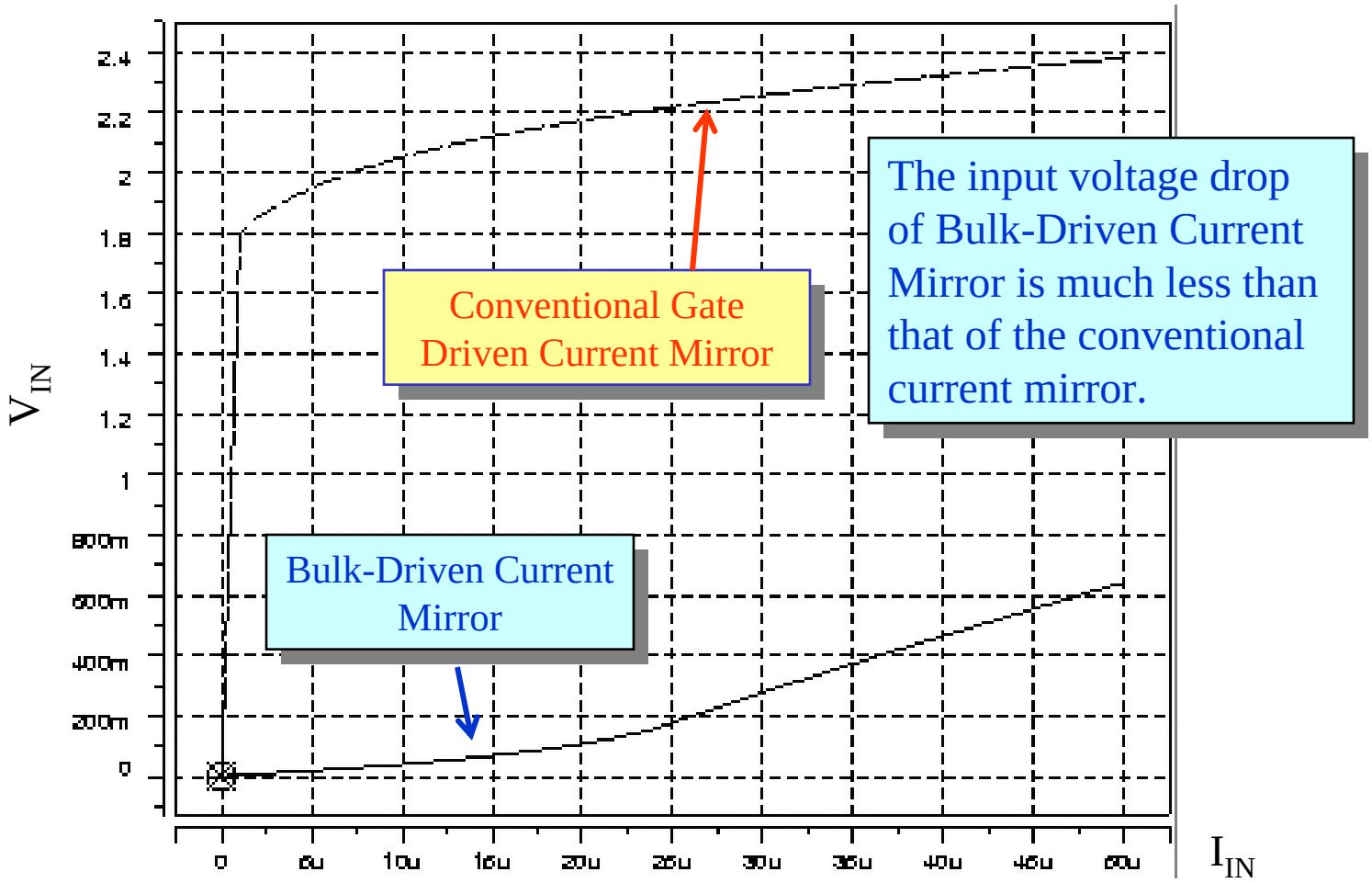
Simulation of Cascode Bulk-Driven Current Mirror (*cont'd*)

- Input Output Transfer Characteristics



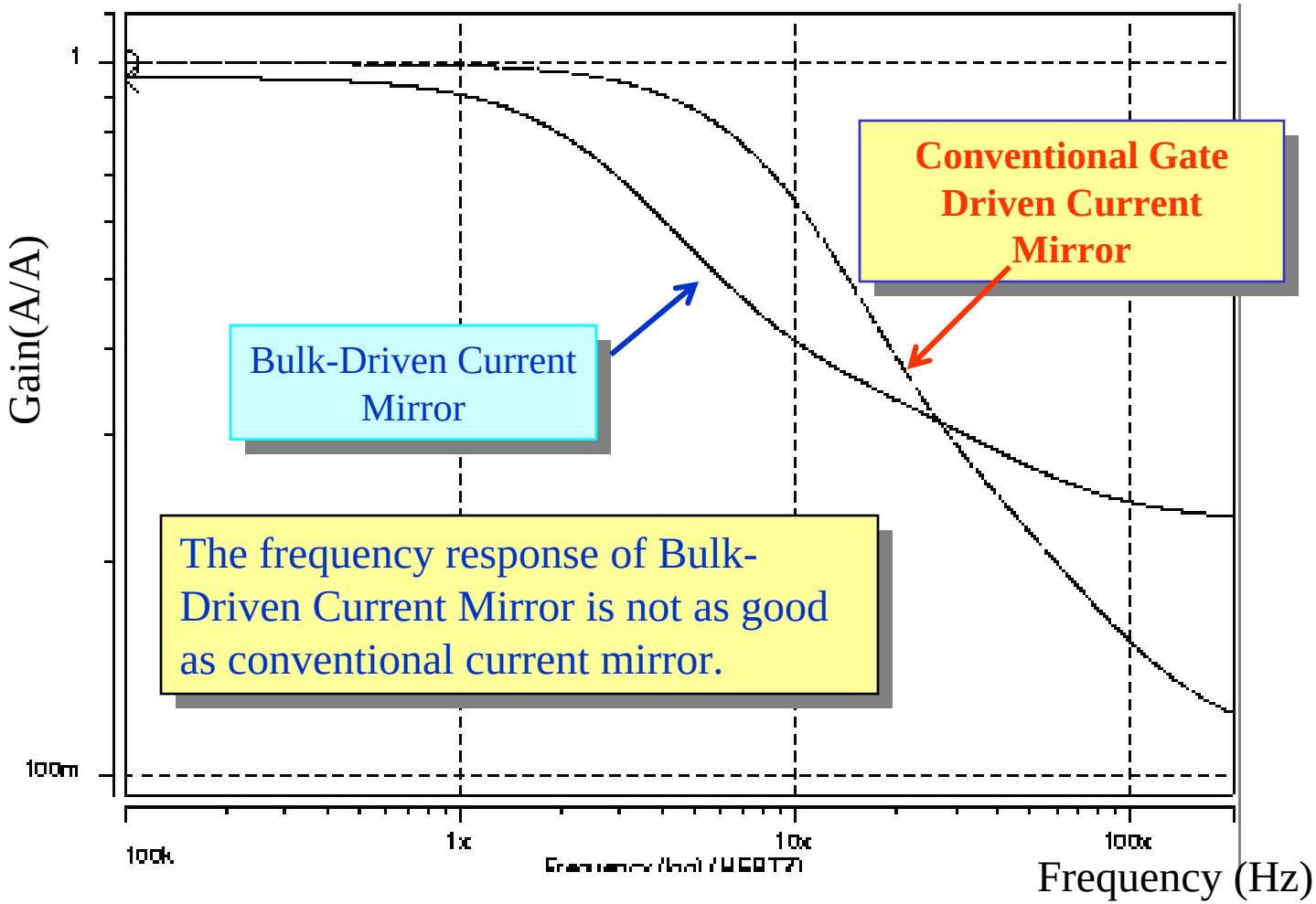
Simulation of Cascode Bulk-Driven Current Mirror (*cont'd*)

- Input Voltage vs. Input Current Characteristics



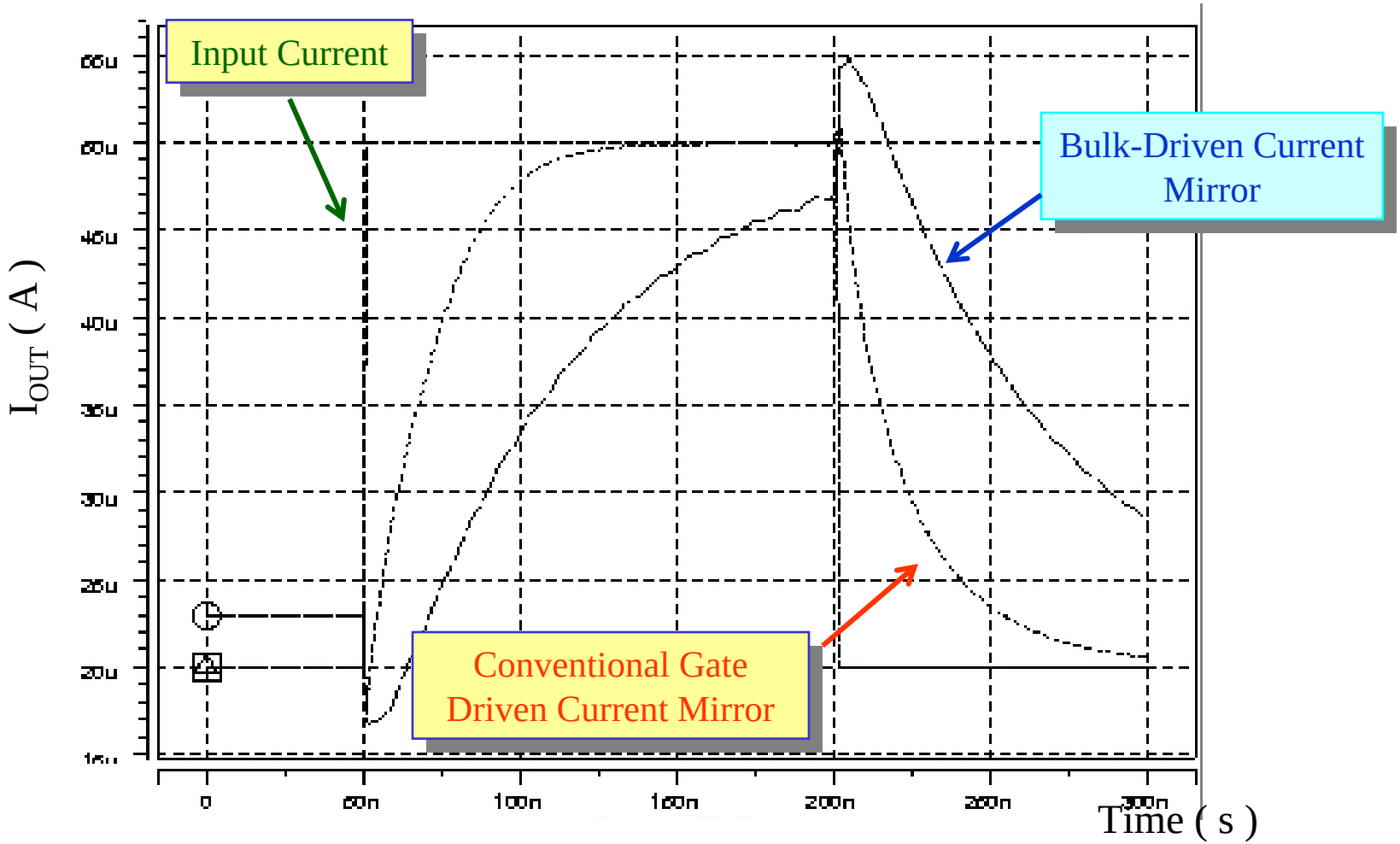
Simulation of Cascode Bulk-Driven Current Mirror (*cont'd*)

- Frequency Response



Simulation of Cascode Bulk-Driven Current Mirror (*cont'd*)

- Transient Analysis



Conclusion

- The bulk-driven technique removes the threshold voltage requirement of MOS FETs from the signal path, and a device which is similar to the JFET transistor with depletion characteristics is obtained.
- Bulk-driven MOS transistors can work even the power supply voltage drops to 0.9V. With such a low power supply voltage, designing analog circuit using conventional gate-driven MOS transistors is difficult.
- By bulk-driven MOS transistors, a differential pair with rail-to-rail common mode input voltage is obtained. The bulk-driven MOS current mirror shows a low input voltage drop.
- Of course, the frequency response, transient response and noise performance is degraded compared with conventional gate-driven MOS FETs, because g_{mb} is much less than g_m in normal condition.
- The bulk-driven technique is a good solution for very low voltage analog circuit design without CMOS processes with low V_T MOS FETs.

References

[1] B. J. Blalock, P. E. Allen, and G. A. Rincon-Mora, "Design 1-V Op Amps Using Standard Digital CMOS Technology," *IEEE Trans. Circuits and Systems – II : Analog and Digital Signal Processing*, pp. 769-780, Vol. 45, No. 7, July 1998

[2] P. E. Allen, B. J. Blalock, and G. A. Rincon, "A 1 V CMOS op amp using bulk-driven MOSFET's", in *Proc. 1995 ISSCC*, Feb. 1995, pp. 192-193

[3] B. J. Blalock, and P. E. Allen, "A one-volt, 120-uW, 1-MHz OTA for standard CMOS technology", in *Proc. 1996 ISCAS*, vol. 1, pp. 305-307

[4] B. J. Blalock, and P. E. Allen, "A low-voltage, bulk-driven MOSFET current mirror for CMOS technology", in *Proc. 1995 ISCAS*, vol. 3, pp. 1972-1975

[5] Kenneth R. Laker and Willy M. C. Sansen, *Design of Analog Integrated Circuits and Systems*, McGraw-Hill, Inc., 1994

[6] J. M. Carrillo, G. Torelli, R. Perez-Aloe, J. F. Duque-Carrillo, " 1-V Rail-to-Rail CMOS Op Amp With Improved Bulk-Driven Input Stage" *IEEE J. Solid State Circuits*, vol. 42, no 3, March 2007

[7] A. Veeravalli, E. Sanchez-Sinencio, and J. Silva-Martinez, " Transconductance amplifier structures with very small transconductances: a comparative study design approach," *IEEE J. Solid-State Circuits*, Vol. 37, pp. 770-775, June 2002.