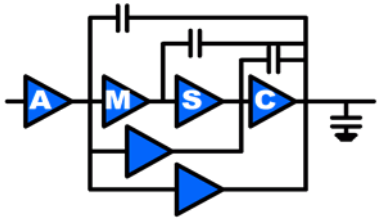

Negative Impedance Converter (NIC) and Applications

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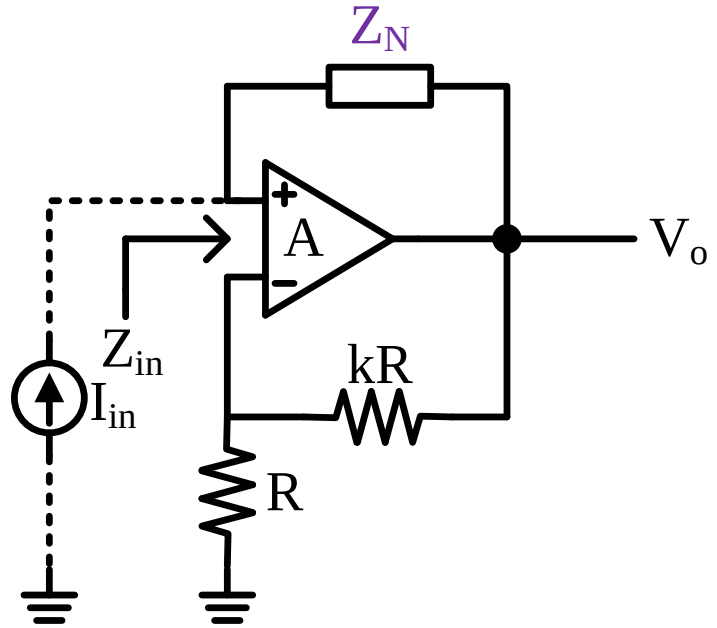
Negative Impedance Converter (NIC)



$$\frac{V+}{Z_N} - \frac{V_o}{Z_N} = I_{in} \qquad (1)$$

$$-\frac{V_o}{kR} + \left(\frac{1}{R} + \frac{1}{kR}\right)V- = 0 \qquad (2)$$

$$V_o = (A)(V+ - V-) \qquad (3)$$

Yields

$$Z_{in}\Big|_{A\to\infty} \cong -\frac{Z_N}{k}$$

$$Z_{in} = -Z_N \frac{1+k+A}{k(A-1)-1} = -Z_N \frac{1+\frac{1+k}{A}}{k-\frac{1+k}{A}}$$

For $A(s) \cong \frac{GB}{s}$

$$Z_{in} = -\frac{Z_N}{k}\frac{1+s/\omega_Z}{1-s/\omega_p} \quad ; \quad \omega_Z = \frac{GB}{1+k} \quad ; \quad \omega_p = \frac{GB}{1+\frac{1}{k}}$$

Negative Impedance Implementations

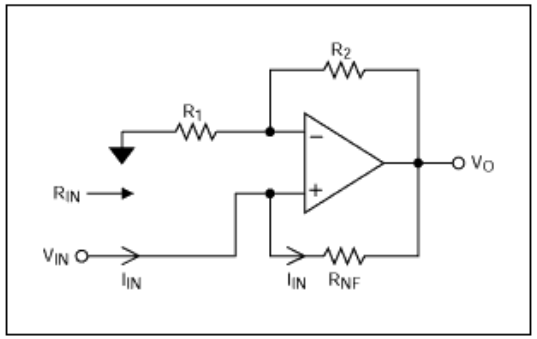


Figure 1. This circuit produces a negative resistance of Rin = -Rnf(R1/R2).

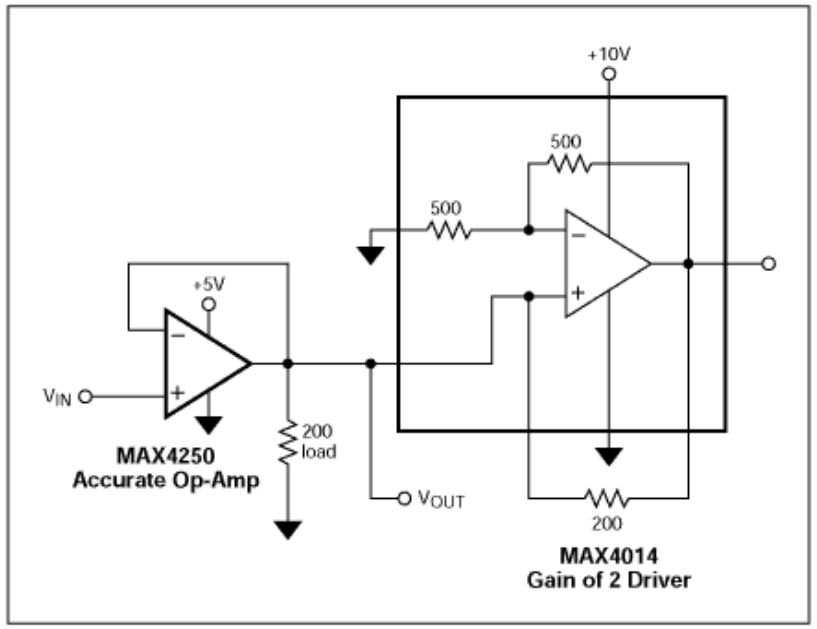
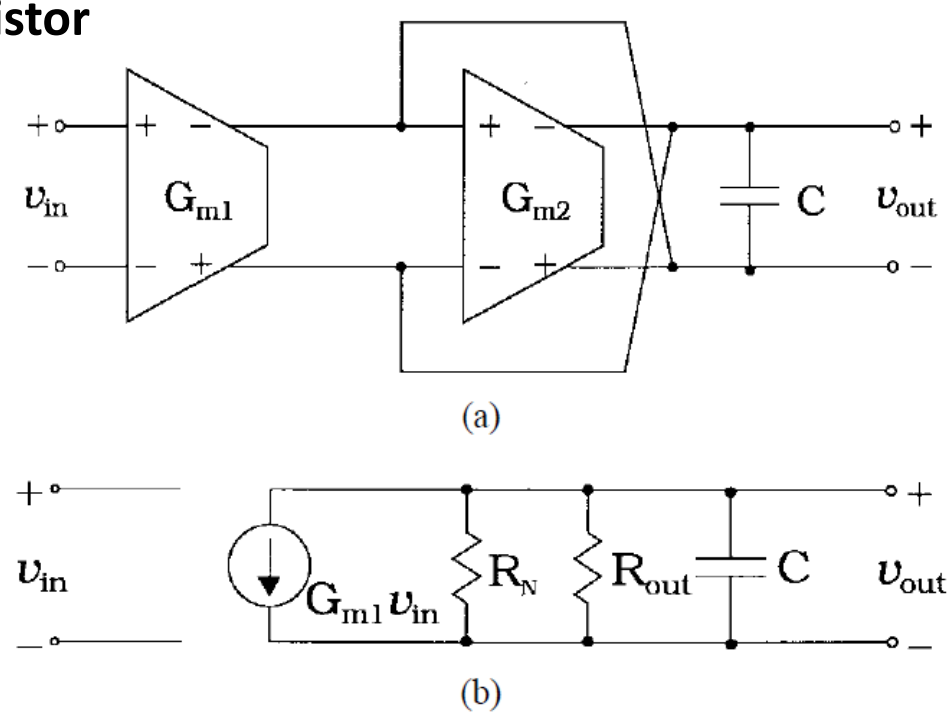


Figure 2. Connecting a load-cancelling negative resistor in parallel with the load

Reference:
https://www.maximintegrated.com/en/app-notes/index.mvp/id/1868

Negative Resistance Applications

Gm with negative resistor

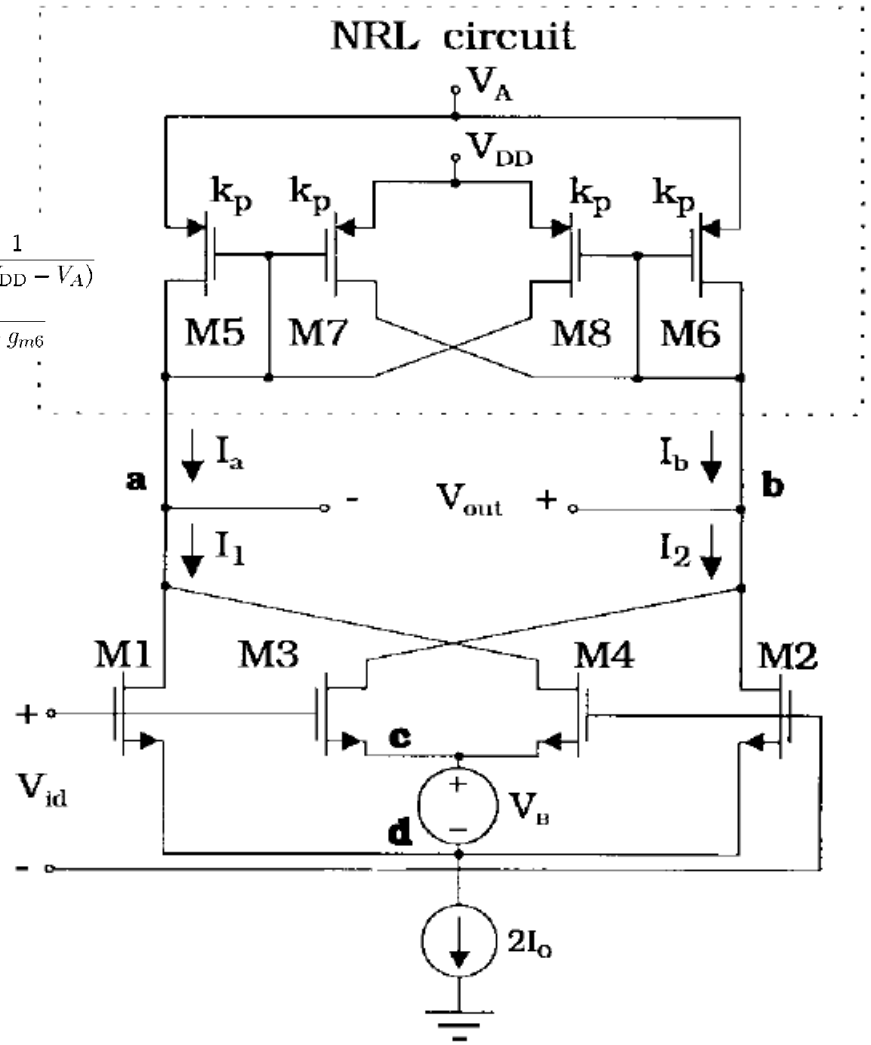


$$\frac{V_{\text{out}}}{V_{\text{in}}} = -\frac{G_{m1}}{sC - G_{m2} + 1/R_{\text{out}}}.$$

Fig. 1. (a) Conceptual block diagram of the OTA-C integrator with high dc gain. (b) Small-signal macromodel including parasitic output resistance R_{out} in parallel with a negative resistance R_N.

Reference: S. Szczepanski, J. Jakusz and R. Schaumann, "A linear fully balanced CMOS OTA for VHF filtering applications," in IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, vol. 44, no. 3, pp. 174-187, Mar 1997.

$$R_N = \frac{1}{G_{m2}} = \frac{V_{\text{out}}}{I_R} = -\frac{1}{2k_p(V_{\text{DD}} - V_A)} = -\frac{1}{g_{m8} - g_{m5}} = -\frac{1}{g_{m7} - g_{m6}}$$



$$I_1 = I_0 + \frac{I_{\text{out}}}{2} = k_n(V_P - V_{Tn})^2 + k_n(V_Q - V_B - V_{Tn})^2 \tag{4}$$

$$I_2 = I_0 - \frac{I_{\text{out}}}{2} = k_n(V_Q - V_{Tn})^2 + k_n(V_P - V_B - V_{Tn})^2 \tag{5}$$

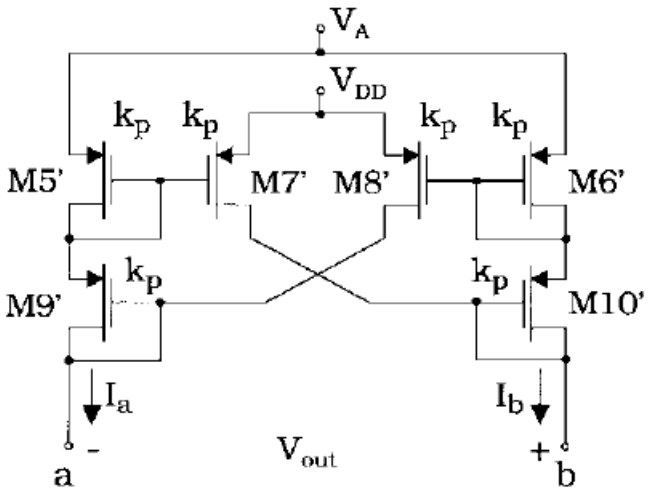
$$I_{\text{out}} = I_1 - I_2 = 2k_n V_B(V_P - V_Q) = 2k_n V_B V_{id} \tag{6}$$

$$I_{\text{out}} = 2k_n[V_{B\text{oc}} + r_{\text{out}B}(I_{d3} + I_{d4})]V_{id} \tag{7}$$

$$|V_{id}| \le \sqrt{I_o/k_n - 3V_B^2/4} - V_B/2 \tag{9}$$

which requires that the common-mode voltage $V_{ic} \ge V_{Tn} + V_B + V_{\text{DSsat}}$, where V_{DSsat} is the minimum voltage required for the current source $2I_o$ to operate in saturation.

Fig. 3. Simplified scheme of the proposed CMOS OTA with a voltage-variable NRL circuit.



(a)

(b)

Fig. 11. (a) Modified topology of the NRL element in Fig. 3.

$$I_R = I_a - I_b = 2k_{\text{eff}}(V_C - V_{\text{DD}})V_{\text{out}} \tag{35}$$

$$R_N = \frac{V_{\text{out}}}{I_R} = -\frac{1}{2k_{\text{eff}}(V_{\text{DD}} - V_C)}. \tag{39}$$

To keep this circuit working linearly, the following conditions should be satisfied

$$|V_{\text{out}}| \le \sqrt{\frac{I_o}{k_{\text{eff}}} - \frac{3}{4}(V_{\text{DD}} - V_C)^2} - \frac{V_{\text{DD}} - V_C}{2} \tag{40}$$

$$|V_{\text{out}}| \le V_{T\Sigma} \tag{41}$$

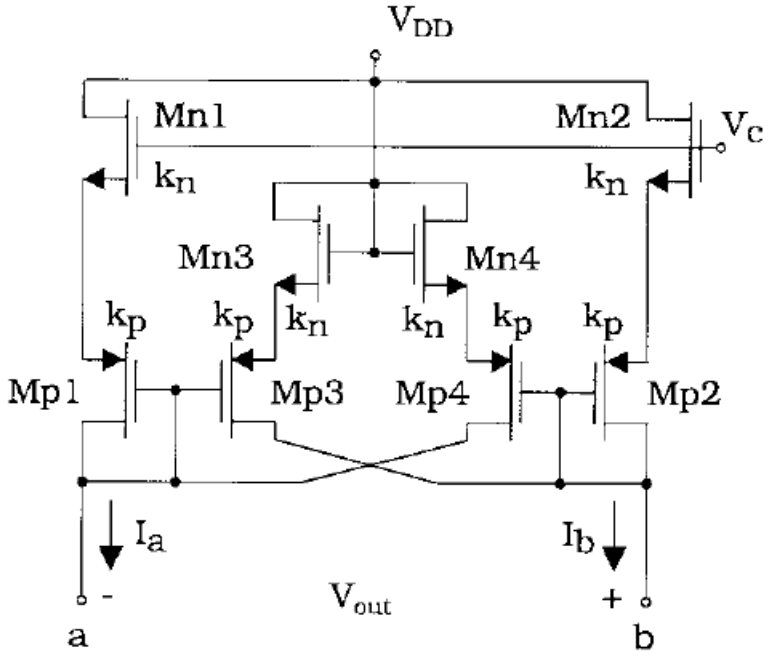


Fig. 12. Alternative topology for an NRL element based on two CMOS double pairs.

Floating bias source: Ma1-Ma3 & Mb1-Mb3

$$V_B = V_{\mathrm{gsMa3}} + \sqrt{\frac{I_{\mathrm{CF}}}{k_{n\mathrm{Ma2}}}} - \sqrt{\frac{I_S - I_{\mathrm{CF}}}{k_{n\mathrm{Ma1}}}}. \qquad (50)$$

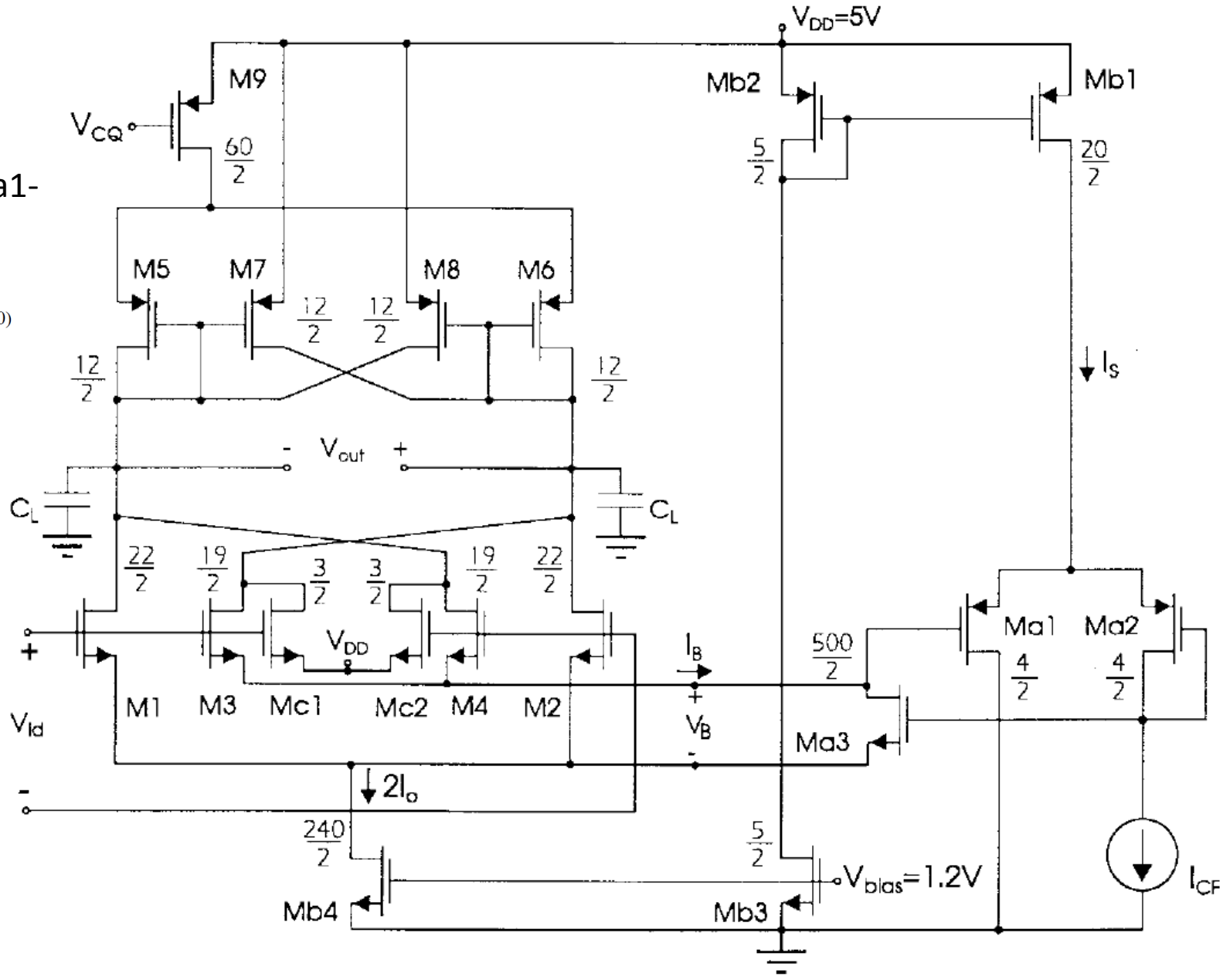
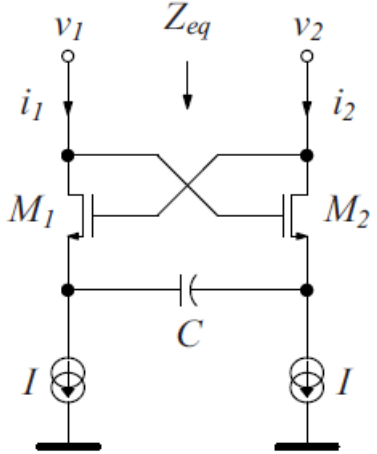


Fig. 14. Complete circuit diagram of the CMOS OTA with the NRL.



The simple negative capacitance generator

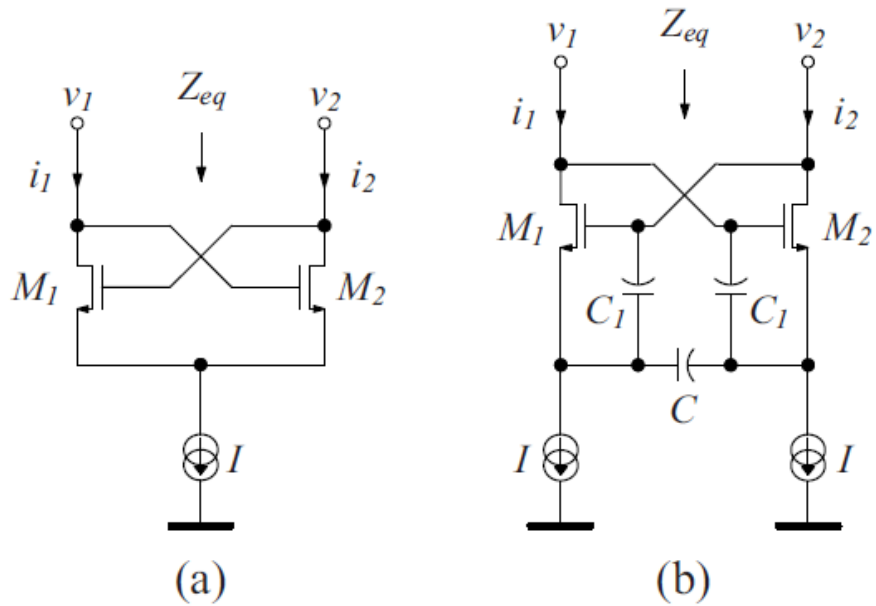
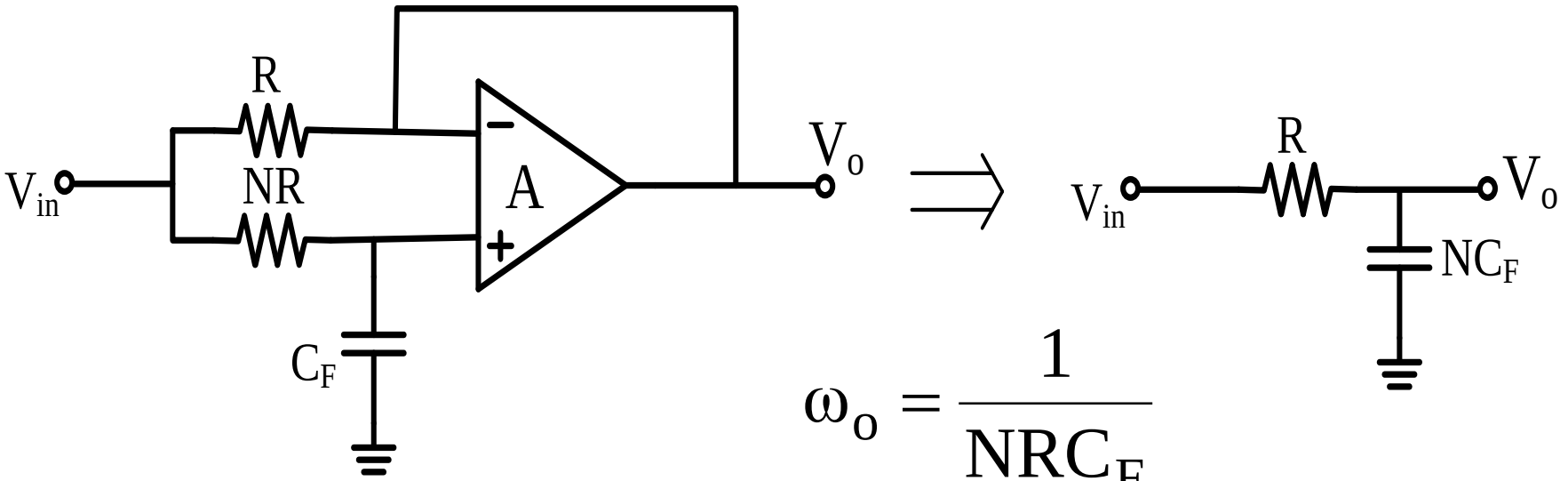


Figure 2. Schematic diagrams of (a) negative resistance and (b) negative inductance generators

$$Z_{equ} = -\frac{1}{sC}\frac{g_m + s(C_{GS} + 2C)}{g_m - sC_{GS}}$$

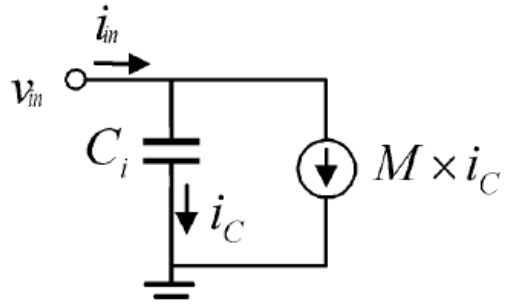
Capacitance Multiplier

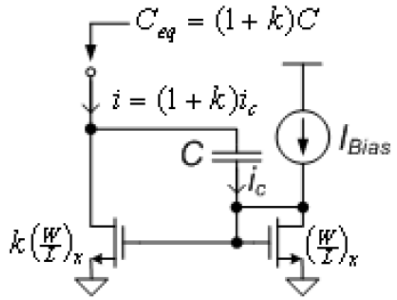


$$\omega_o = \frac{1}{NRC_F}$$

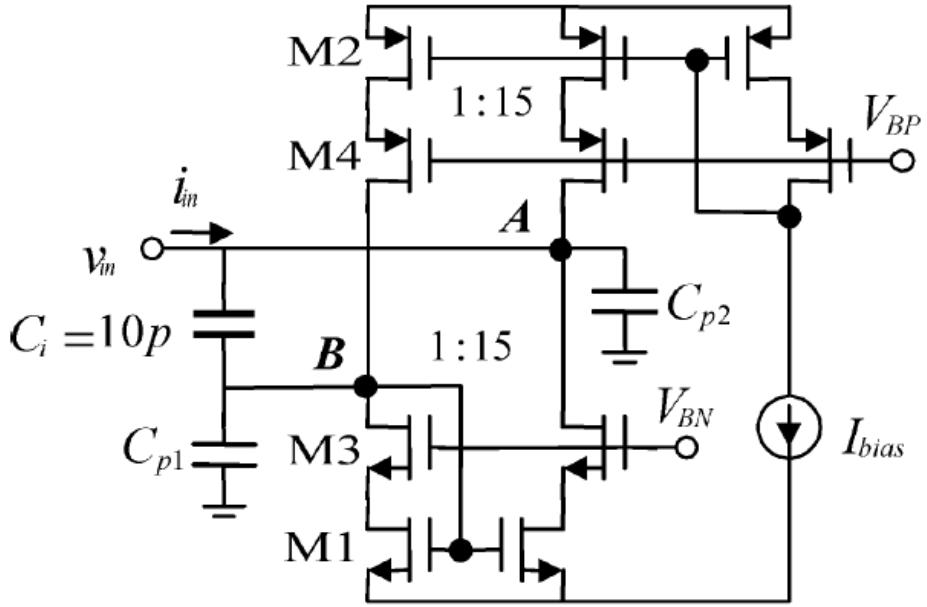
$$\frac{V_O}{V_{in}} = \frac{1}{(1+sR(NC_F))(1+1/A)}$$

CAPACITANCE MULTIPLIER

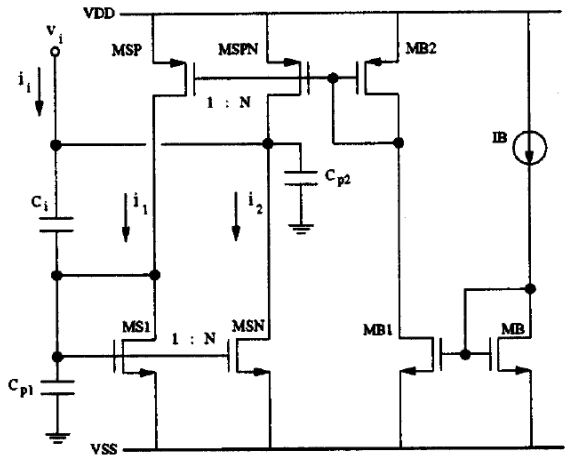


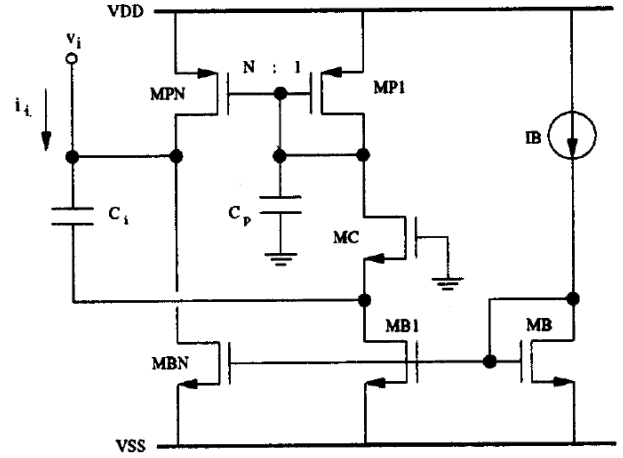


(a)



(b)





(a) (b)

Scaling up a grounded capacitance. (a) Basic circuit. (b) Capacitance scaler using a cascode transistor.

Fig. 6. Capacitance multiplier. (a) Principle. (b) Circuit implementation.

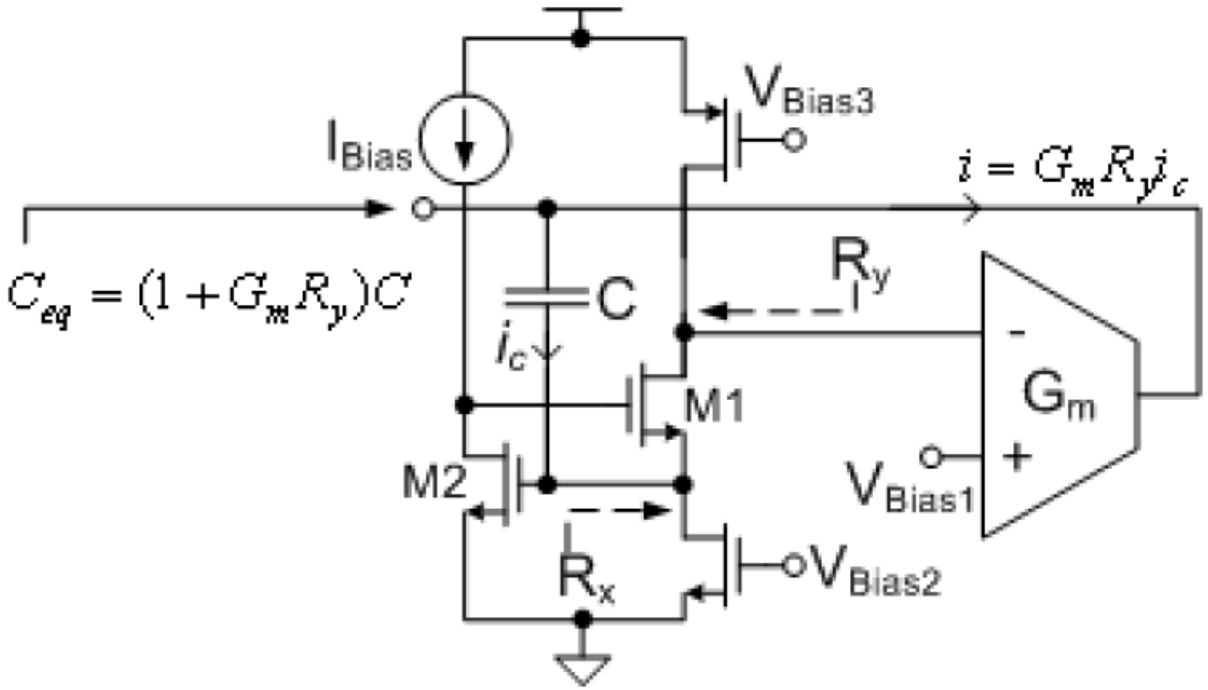


Figure 3. Linearly bidirectional current-mode capacitor multiplier

Reference:
http://users.ece.gatech.edu/rincon-mora/publicat/trade_jrnls/pmdl_0706_cx.pdf

Using negative capacitance for LDO applications

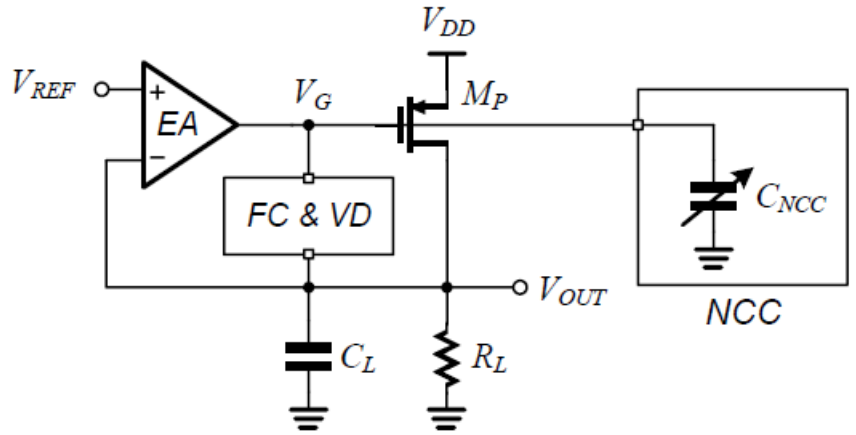


Fig. 1. Fundamental blocks of the proposed LDO regulator

If C_{NCC} cancels out the parasitic capacitances C_p and C_{gd} as

$$C_{NCC} = -\left(C_p + C_{gd}\right), \tag{3}$$

then v_g can be simply approximated as

$$v_g \cong \frac{C_{gs}}{C_{gs} + C_p + C_{gd} - (C_p + C_{gd})} v_{dd} = v_{dd}. \tag{4}$$

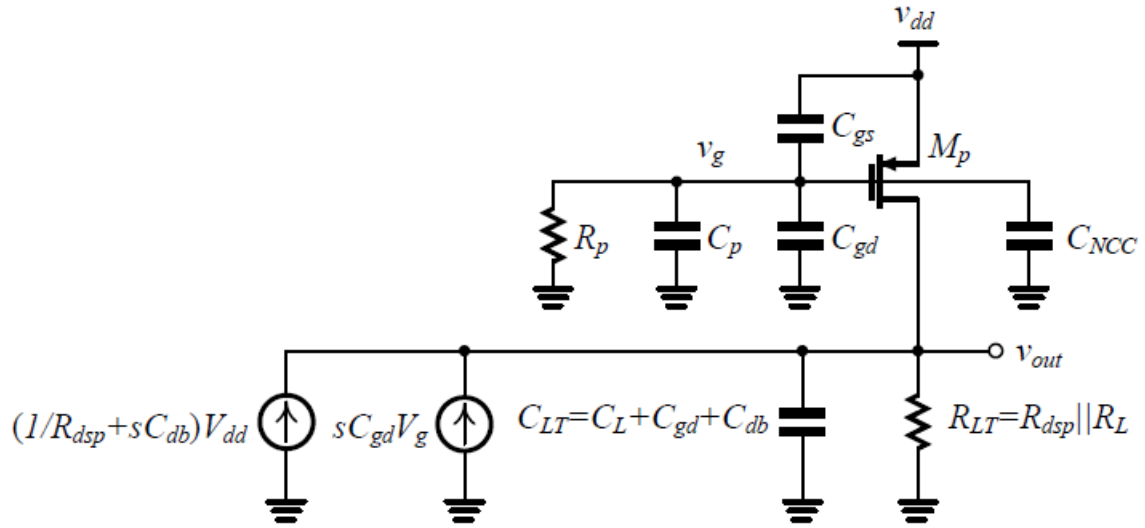


Fig. 2. Small-signal equivalent circuit of the proposed LDO regulator

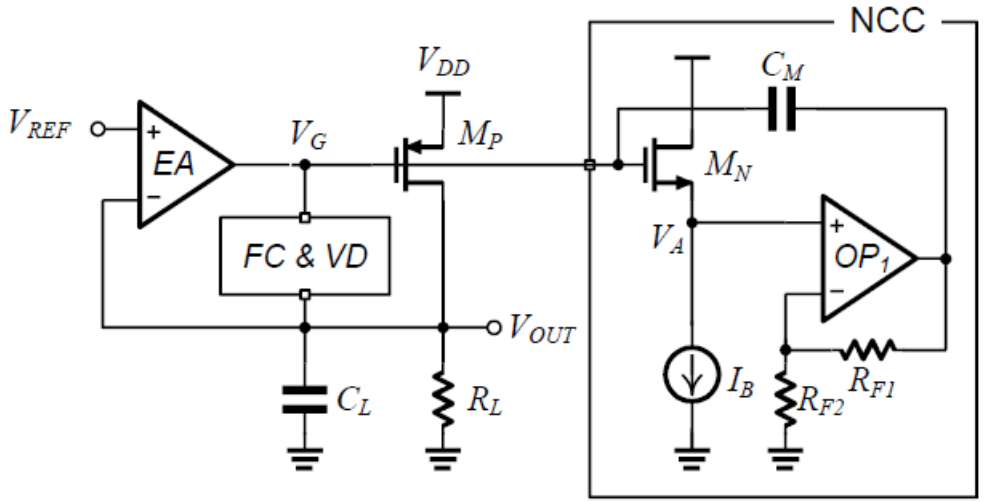


Fig. 3. Implementation of NCC with fundamental blocks

S. J. Yun; J. S. Kim; Y. S. Kim, "Capless LDO Regulator Achieving -76 dB PSR and 96.3 fs FOM," in IEEE Transactions on Circuits and Systems II: Express Briefs , vol.PP, no.99, pp.1-1