ELEN 607 (ESS) **Due: February 28, 2017**
Spring 2017

Homework Assignment #4

Problem 1 a) Design a FD amplifier with two stages for the following specs using

0.13μm technology

$V_{DD} = 1.2V$ or $V_{DD} = -V_{SS} = 0.6V$

$SR > 2V/\mu sec$

$A_{o,DC} \geq 90dB$

DC CMRR $\geq 85dB$

$GBW > 4MHz$

$PM > 60^o$

$C_L // R_L = 25pF // 47K\Omega$

Power to be minimum

$1\%\ T_s < 160nS$

Describe your design procedure for the differential and common-mode gains and bandwidths. Use two different CM detectors and compare results. Provide a summary table including IIP3, 1% THD and indicate the bandwidths and gains of A_{DM} and A_{CM}.

b) Provide the output step response for a common-mode step of 0.5V. What is the Ts?

c) Force a transistor mismatch of 2% in the differential pair and study its effects on the performance. In particular the linearity.

Problem 2. Design the single output op amp to meet the following specs when it is connected as an inverter amplifier. Describe procedure to set the op amp specs.

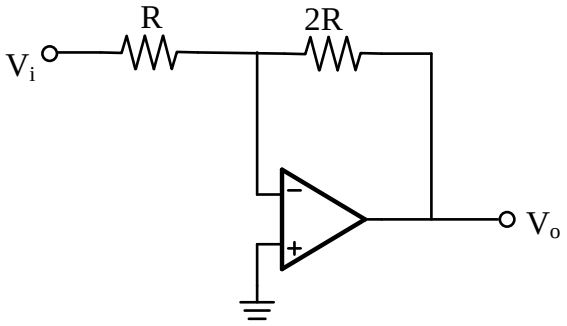
$H_{CL}(o) = -2$

$BW = 1.3MHz$

$SR > 1.5V/\mu s$

Technology $0.13\ \mu$m

$V_{DD} = 1.2V$



The accuracy error of the DC gain of the inverter should be less than 1.1%

— What are poles and zero locations?

— What is ROC and phase margin?