Low Power Multistage Amplifiers For Large Capacitive Loads

By

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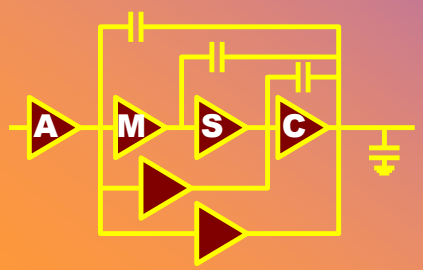


See March 2005 issue in the IEEE JSSC

Outline

- Introduction
- Design Considerations
- Existing approaches
- Proposed Approach (1)
- Proposed Approach (2)
- Experimental Results
- Discussion
- Conclusion

Introduction

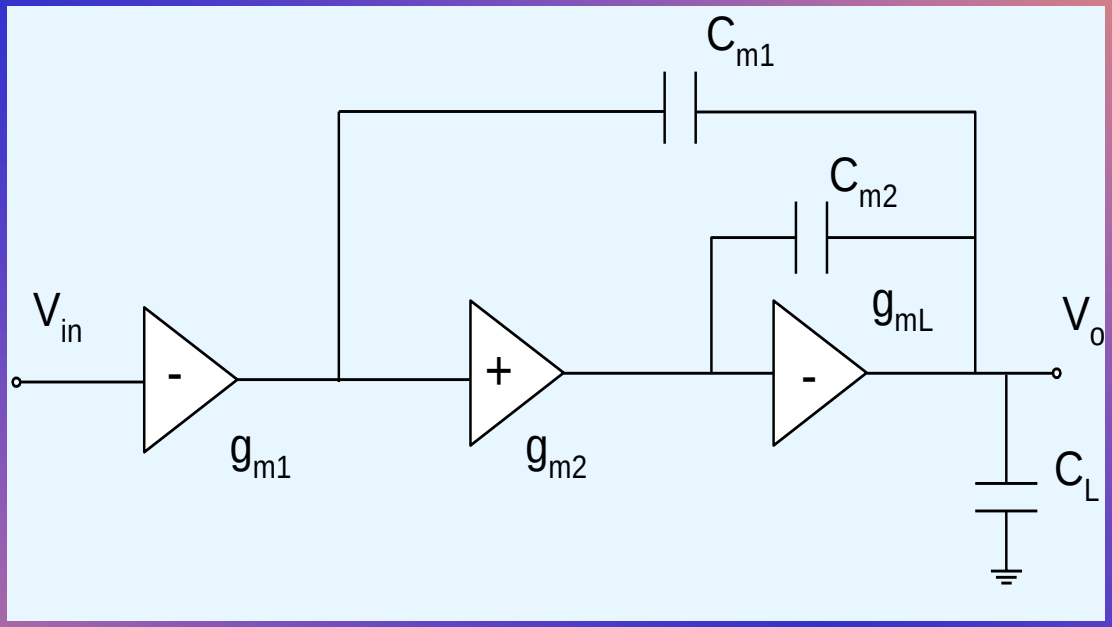
- Need for Low voltage Low power amplifier.
- High gain + low voltage ⟶ multistage architecture
- High capacitive loads are required in error amplifiers in a linear regulator which is a part of low power portable devices.
- Large capacitive loads degrade the frequency response.
- Robust Phase compensation technique required.

Design Considerations

- Large Capacitive Load
- Low Power
- Less Area
- High Gain
- Moderate GBW and PM

Existing solutions in the literature?

Nested Miller Compensation



$$A_V = \frac{g_{m1} g_{m2} g_{mL}}{g_{p1} g_{p2} g_L}$$

$$GBW = \frac{1}{4}\left(\frac{g_{mL}}{C_L}\right)$$

[4] R. G. H. Eschauzier etal. “A 100-MHz 100-dB operational amplifier with multipath nested miller compensation structure,” *IEEE Journal of Solid State Circuits*, Vol. 27, pp. 1709-1717, Dec. 1992.

NMC (contd..)

Stability analysis:

$$GBW \leq \frac{1}{2} p_2 \leq \frac{1}{4} p_3$$

$$\frac{g_{m1}}{C_{m1}} \leq \frac{1}{2}\frac{g_{m2}}{C_{m2}} \leq \frac{1}{4}\frac{g_{mL}}{C_L}$$

Stability condition:

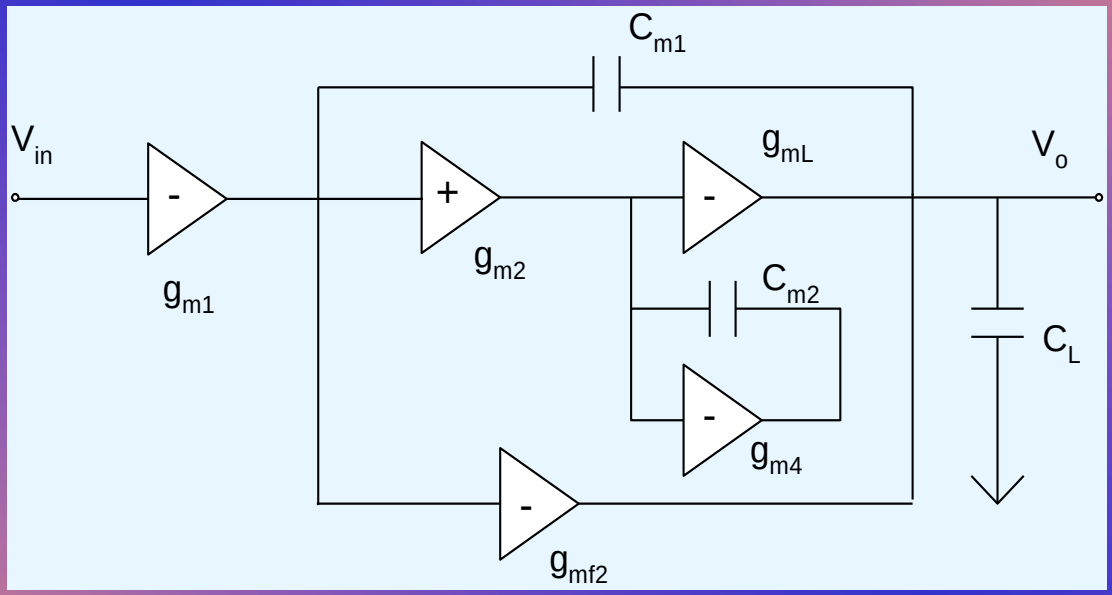
$$g_{mL} >> g_{m1}, g_{m2}$$

$$C_{m1} = 4\left(\frac{g_{m1}}{g_{mL}}\right)C_L$$

$$C_{m2} = 2\left(\frac{g_{m2}}{g_{mL}}\right)C_L$$

C_{m1} and C_{m2} very large for large load!!

Damping Factor-Control Frequency Compensation (DFCFC)



[2] K. N. Leung et al., “Three Stage Large Capacitive Load Amplifier with Damping-Factor Control Frequency Compensation,” *IEEE Journal of Solid State Circuits,* Vol.35, No.2, February 2000.

DFCFC (contd.)

Stability condition:

$$g_{mf2} = g_{mL}$$

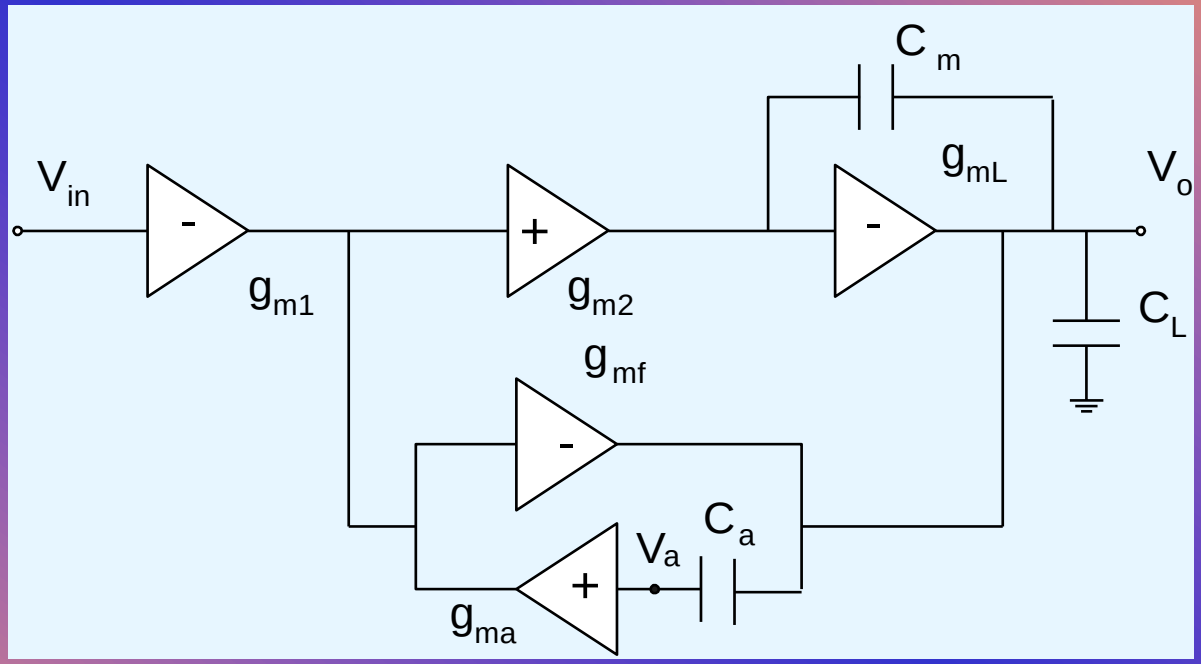
$$C_{m1} = \frac{4}{\beta}\left(\frac{g_{m1}}{g_{mL}}\right)C_L$$

$$C_{m1} \geq C_{m2} > C_{p2}$$

$$g_{m4} = \beta\left(\frac{C_{p2}}{C_L}\right)g_{mL}$$

$$where \beta = 1 + \sqrt{1 + 2\left(\frac{C_L}{C_{p2}}\right)\frac{g_{m2}}{g_{mL}}}$$

Active Feedback Frequency Compensation(AFFC)



[1] H. Lee, P. K .T Mok. , “Active-feedback frequency compensation technique for low-power multistage amplifiers, “ *IEEE Journal of Solid State Circuits*, Vol. 38, pp- 511-520, March, 2003.

AFFC (contd.)

Stability condition:

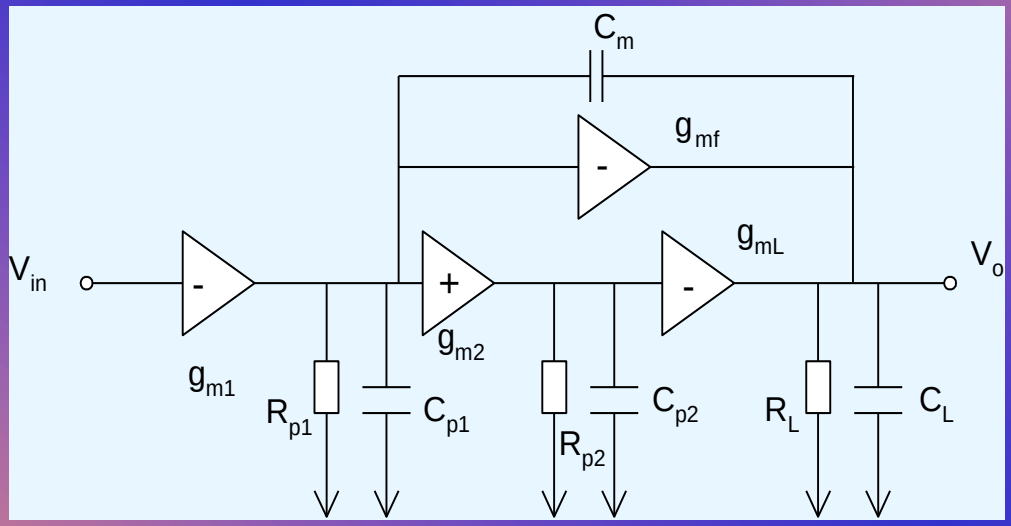
$$g_{ma} = 4g_{m1}$$

$$g_{mf} > g_{m2}$$

$$C_a = C_m = \frac{1}{N} C_{m1(NMC)}$$

$$where N = \sqrt{8\left(\frac{C_L}{C_1}\right)\left[\frac{g_{m1}\left(g_{mf} - g_{m2}\right)}{g_{mL}^2}\right]}$$

Proposed Solution 1
Single Miller Capacitor (SMC)



SMC (contd.)

Transfer function analysis

$$\begin{cases} g_{m2}V_1 - g_{p2}V_2 - sC_{p2}V_2 = 0 \\ -g_{m3}V_2 - g_L V_{out} - sC_L V_{out} + sC_m(V_1 - V_{out}) = 0 \end{cases} \quad (V_{out} - V_1) = 0$$

$$H(s) \approx \frac{\dfrac{g_{m1}g_{m2}g_{mL}}{g_{p1}g_{p2}g_L}\left[1 - s\dfrac{C_m}{G_{meff}} - s^2\dfrac{C_m C_{P2}}{g_{m2}g_{mL}}\right]}{\left(1 + s\dfrac{g_{m2}g_{mL}C_m}{g_{p1}g_{p2}g_L}\right)\left[1 + s\dfrac{C_L}{G_{meff}} + s^2\dfrac{C_{p2}C_L}{g_{m2}g_{mL}}\right]}$$

$$G_{meff} = \frac{g_{m2}}{g_{p2}}g_{mL}$$

SMC (contd.)

Poles and Zeros:

Poles:

$$p_1 = \frac{g_{p1} g_{p2} g_L}{g_{m2} g_{mL} C_m}$$

$$p_2 = \frac{g_{p2}}{C_{p2}} - \frac{G_{meff}}{C_L}$$

$$p_3 = \frac{G_{meff}}{C_L}$$

Zeros:

$$z_1 = \frac{G_{meff}}{C_m} \quad \text{RHP}$$

$$z_2 = \frac{g_{p2}}{C_{p2}} + \frac{G_{meff}}{C_m} \quad \text{LHP}$$

$$z_2 > z_1 >> p_{1,2,3}$$

P_1: Dominant Pole P_2: Non-dominant Pole P_3: Non-Dominant Pole

$$A_V = \frac{g_{m1} g_{m2} g_{mL}}{g_{p1} g_{p2} g_L}$$

$$PM = 180^o - \tan^{-1}\left(\frac{GBW}{p_1}\right) - \tan^{-1}\left(\frac{GBW}{p_2}\right) - \tan^{-1}\left(\frac{GBW}{p_3}\right)$$

$$GBW = \frac{1}{2} p_2 = \frac{1}{4} p_3 \qquad PM = 180^0 - 90^0 - \tan^{-1}\left(\frac{1}{2}\right) - \tan^{-1}\left(\frac{1}{4}\right) = 49.4^0$$

SMC (contd.)

Stability analysis:

$$GBW \le \frac{1}{2} p_2 \le \frac{1}{4} p_3$$

$$\frac{g_{m1}}{C_m} \le \frac{1}{2}\left(\frac{g_{p2}}{C_{p2}} - \frac{G_{meff}}{C_L} \right) \le \frac{1}{4} \frac{G_{meff}}{C_L}$$

Stability condition:

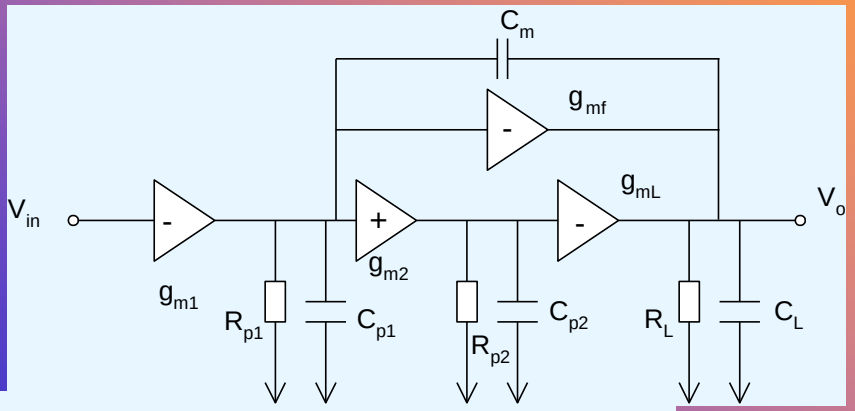
$$C_m \ge \frac{4 g_{m1} C_L}{G_{meff}}$$

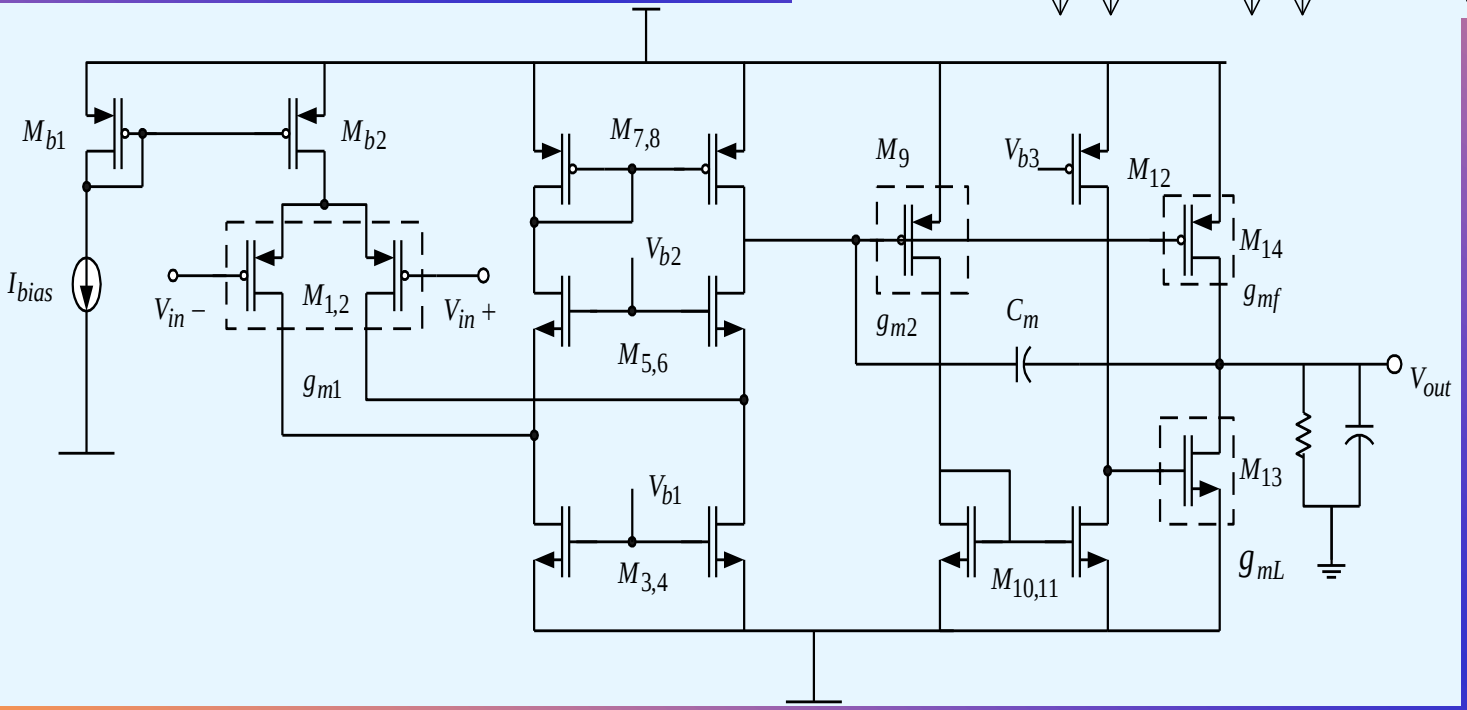
$$g_{mL} \approx 4 g_{m1} \Rightarrow C_m \ge \frac{C_L}{A_{v2}}$$

$$\frac{g_{p2}}{C_{p2}} > \frac{G_{meff}}{C_L}$$

C_m is small even for large load!!

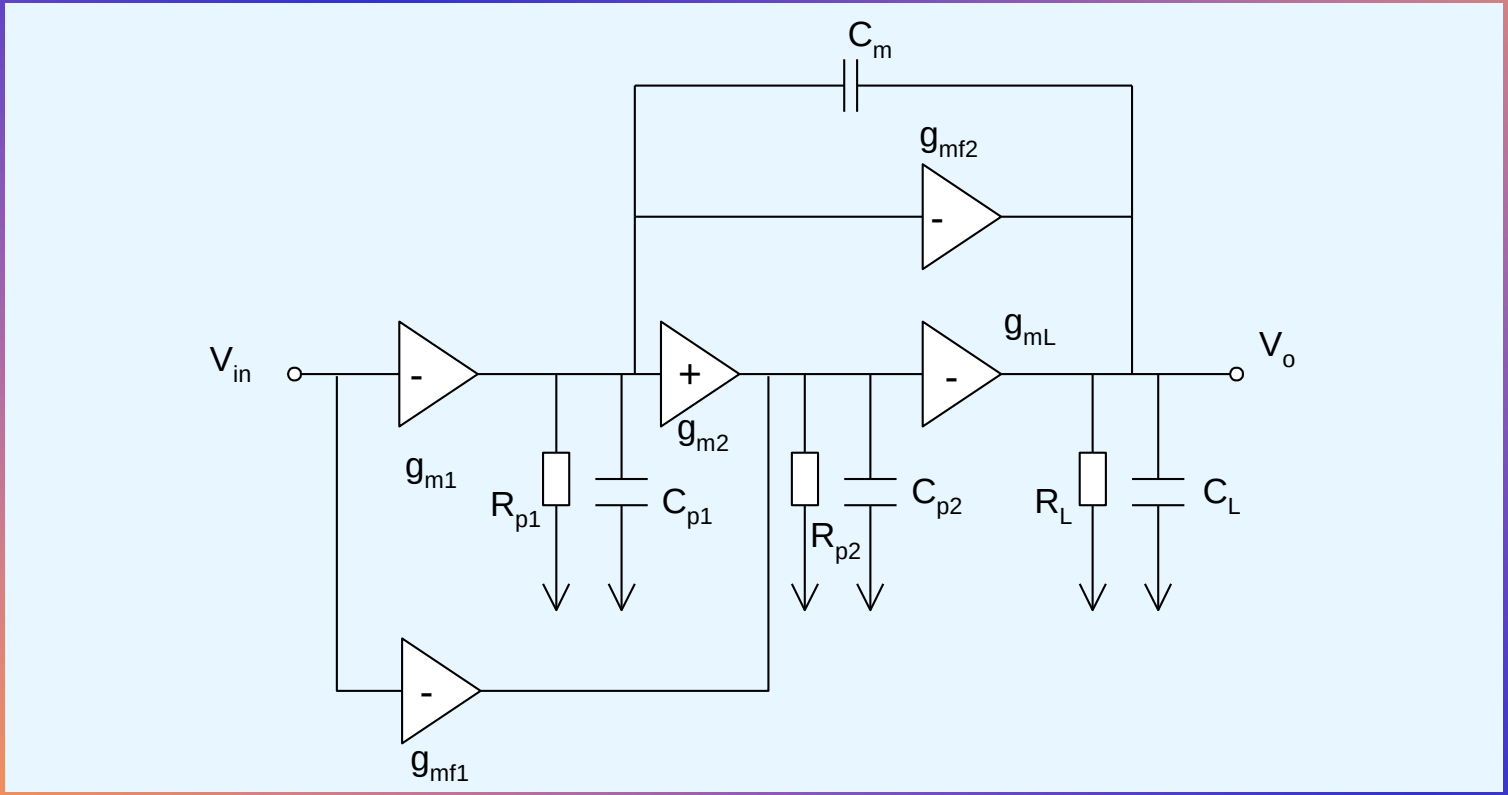
SMC (contd.)





g_{mf} and g_{mL} form a push-pull output stage for better slew rate and settling time.

Proposed Solution 2
Single Miller Capacitor Feedforward Compensation (SMFFC)



SMFFC (contd.)

Transfer function analysis

$$\begin{cases} -g_{mf1}V_{in} + g_{m2}V_1 - g_{p2}V_2 - sC_{p2}V_2 = 0 \\ -g_{mf2}V_1 - g_{mL}V_2 - g_L V_{out} - sC_L V_{out} + sC_m(V_1 - V_{out}) = 0 \end{cases}$$

$$H(s) \approx \frac{\dfrac{g_{m1}g_{m2}g_{mL}}{g_{p1}g_{p2}g_L}\left[1 + s\dfrac{g_{mf1}C_m}{g_{m1}g_{m2}} - s^2\dfrac{C_m C_{P2}}{g_{m2}g_{mL}}\right]}{\left(1 + s\dfrac{g_{m2}g_{mL}C_m}{g_{p1}g_{p2}g_L}\right)\left[1 + s\dfrac{C_L g_{p2}}{g_{m2}g_{mL}} + s^2\dfrac{C_{P2}C_L}{g_{m2}g_{mL}}\right]}$$

SMFFC (contd.)

Poles and Zeros:

Poles:

$$p_1 = \frac{g_{p1} g_{p2} g_L}{g_{m2} g_{mL} C_m}$$

$$p_2 = \frac{g_{p2}}{C_{p2}} - \frac{G_{meff}}{C_L}$$

$$p_3 = \frac{G_{meff}}{C_L}$$

Zeros:

$$z_1 = \frac{g_{m1} g_{m2}}{g_{mf1} C_m} \quad \text{LHP}$$

$$z_2 = \frac{g_{mf1} g_{mL}}{g_{m1} C_{p2}} + \frac{g_{m1} g_{m2}}{g_{mf1} C_m} \quad \text{RHP}$$

$$z_2 > z_1$$

P_1: Dominant Pole P_2: Non-dominant Pole P_3: Non-Dominant Pole

$$A_V = \frac{g_{m1} g_{m2} g_{mL}}{g_{p1} g_{p2} g_L} \qquad GBW = \frac{1}{2} p_2 = \frac{1}{4} p_3$$

$$PM = 180^o - \tan^{-1}\left(\frac{GBW}{p_1}\right) - \tan^{-1}\left(\frac{GBW}{p_2}\right) - \tan^{-1}\left(\frac{GBW}{p_3}\right) + \tan^{-1}\left(\frac{GBW}{z_1}\right)$$

$$PM = 180^0 - 90^0 - \tan^{-1}\left(\frac{1}{2}\right) - \tan^{-1}\left(\frac{1}{4}\right) + \tan^{-1}\left(\frac{1}{2}\right) = 75^0$$

SMFFC (contd.)

Stability analysis:

$$GBW \le \frac{1}{2} p_2 \le \frac{1}{4} p_3$$

$$\frac{g_{m1}}{C_m} \le \frac{1}{2}\left(\frac{g_{p2}}{C_{p2}} - \frac{G_{meff}}{C_L}\right) \le \frac{1}{4}\frac{G_{meff}}{C_L}$$

Stability condition:

$$C_m \ge \frac{4 g_{m1} C_L}{G_{meff}}$$

$$g_{mL} \approx 4 g_{m1} \Rightarrow C_m \ge \frac{C_L}{A_{v2}}$$

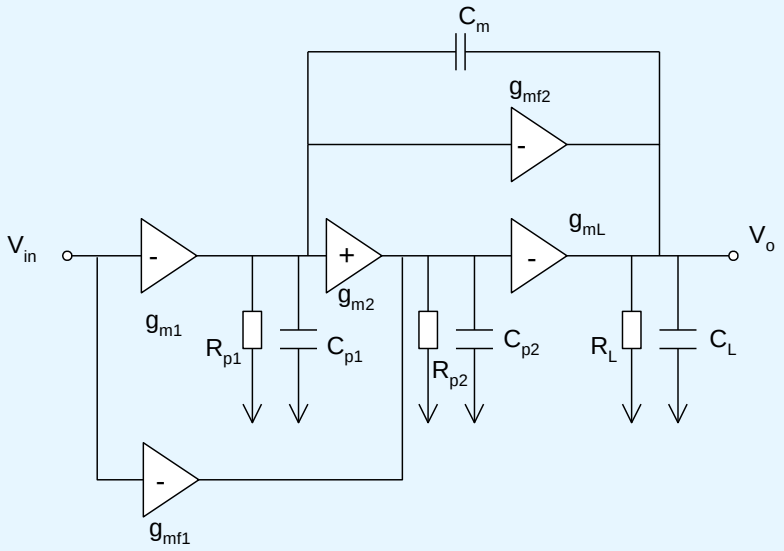
$$\frac{g_{p2}}{C_{p2}} > \frac{G_{meff}}{C_L}$$

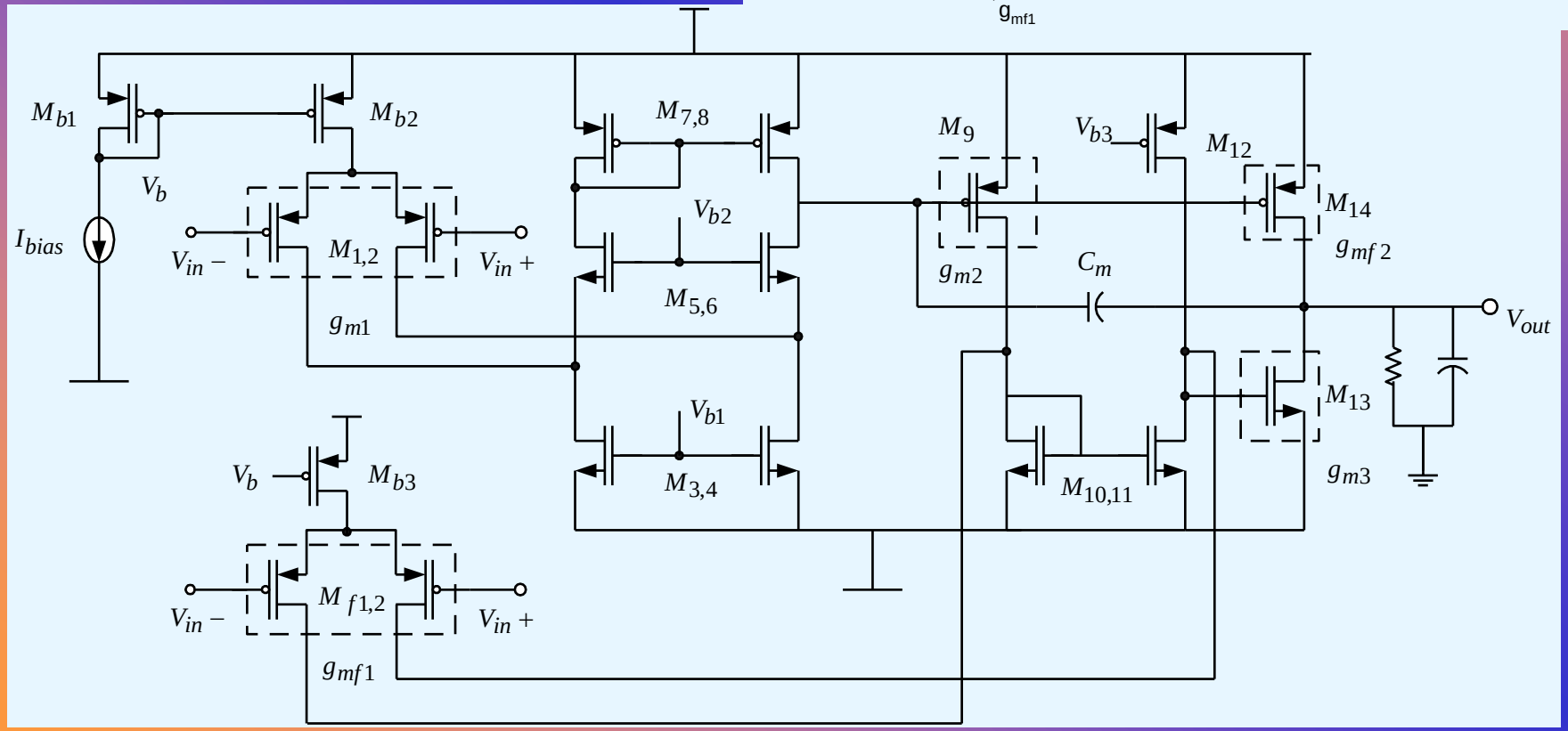
$$g_{mf1} = \frac{g_{m1} g_{m2} g_{02} C_{p2} C_L}{(g_{02}^2 C_L - g_{m2} g_{m3} C_{p2}) C_m}$$

C_m is much smaller even for large load!!

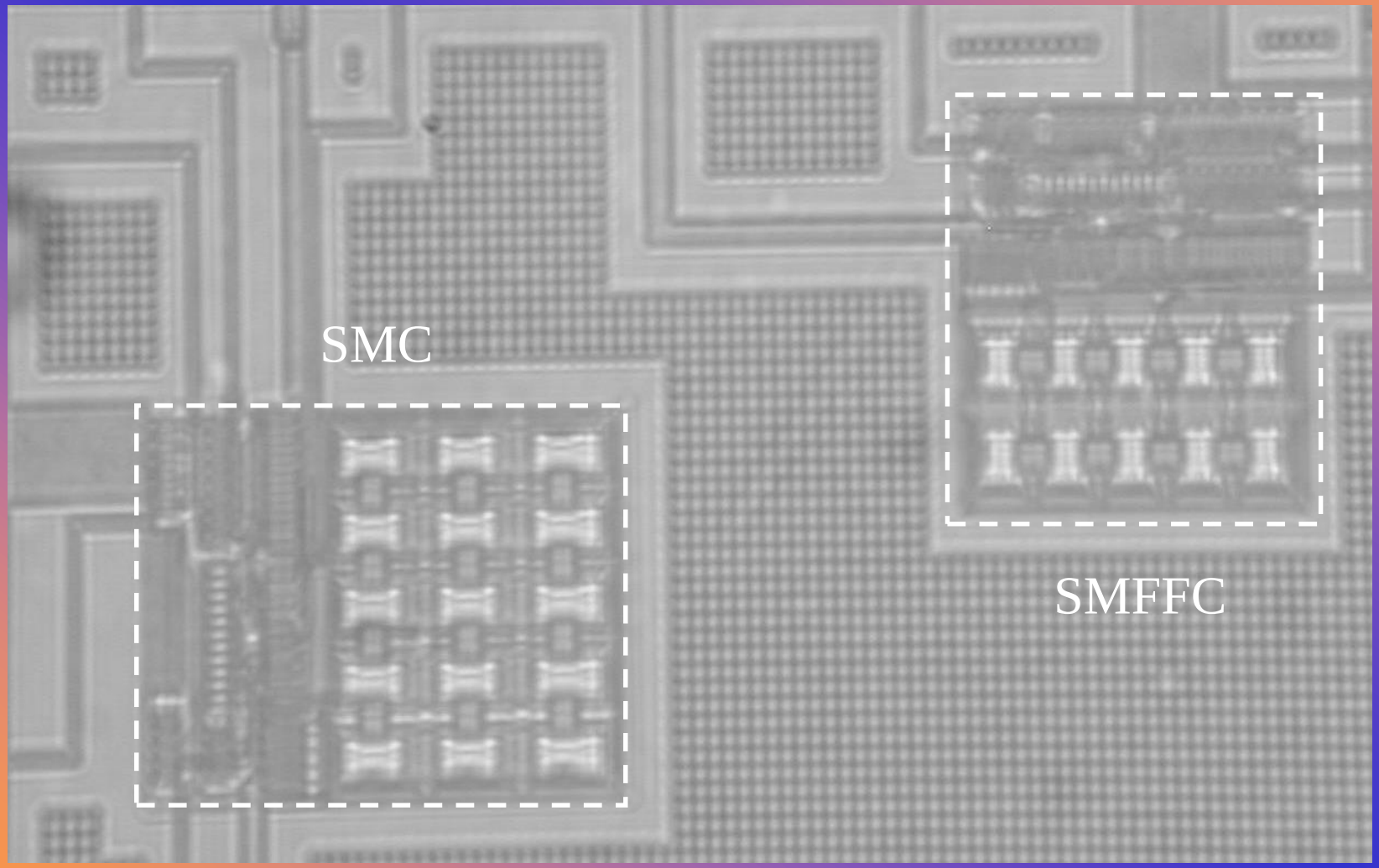
SMFFC (contd.)

Schematic

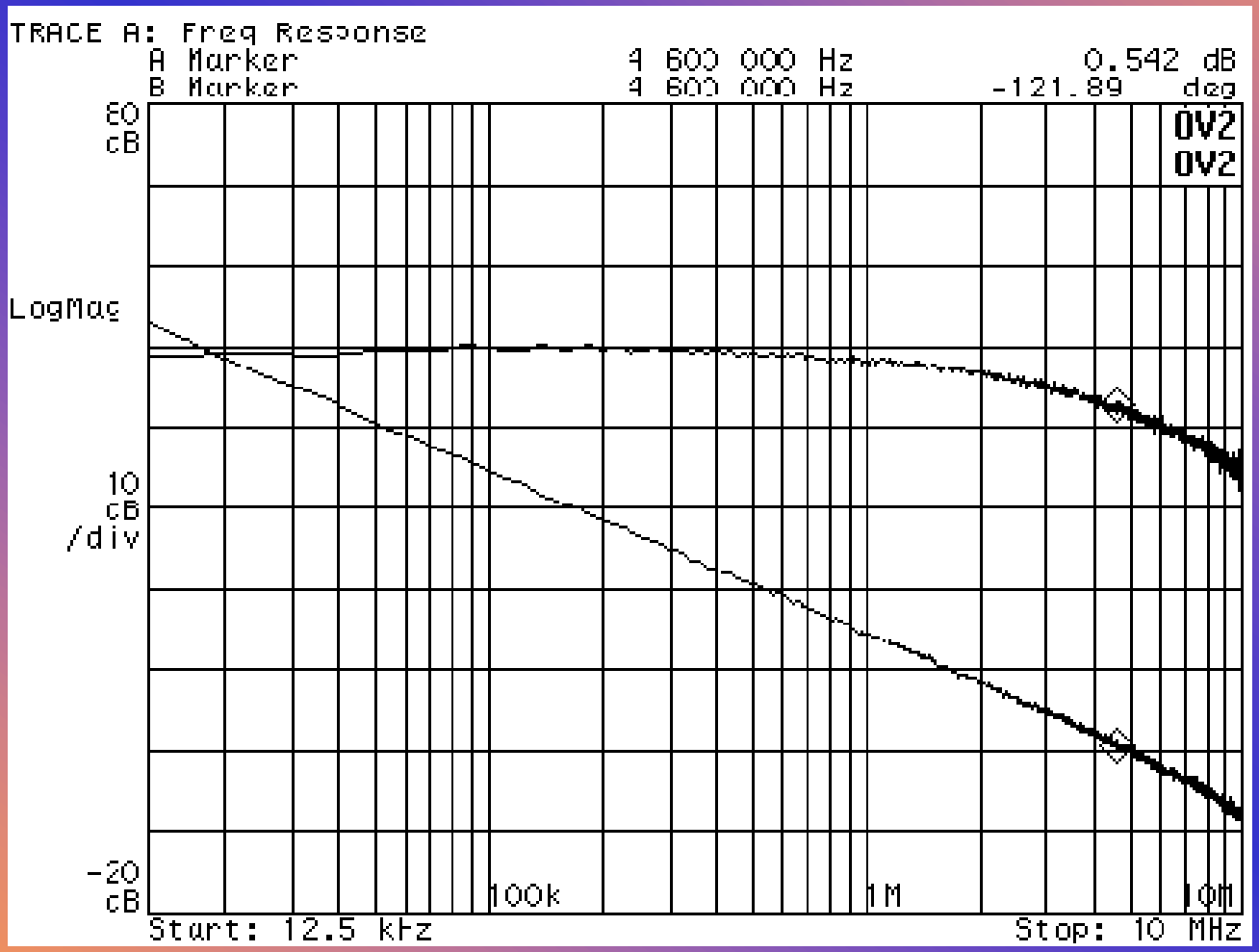




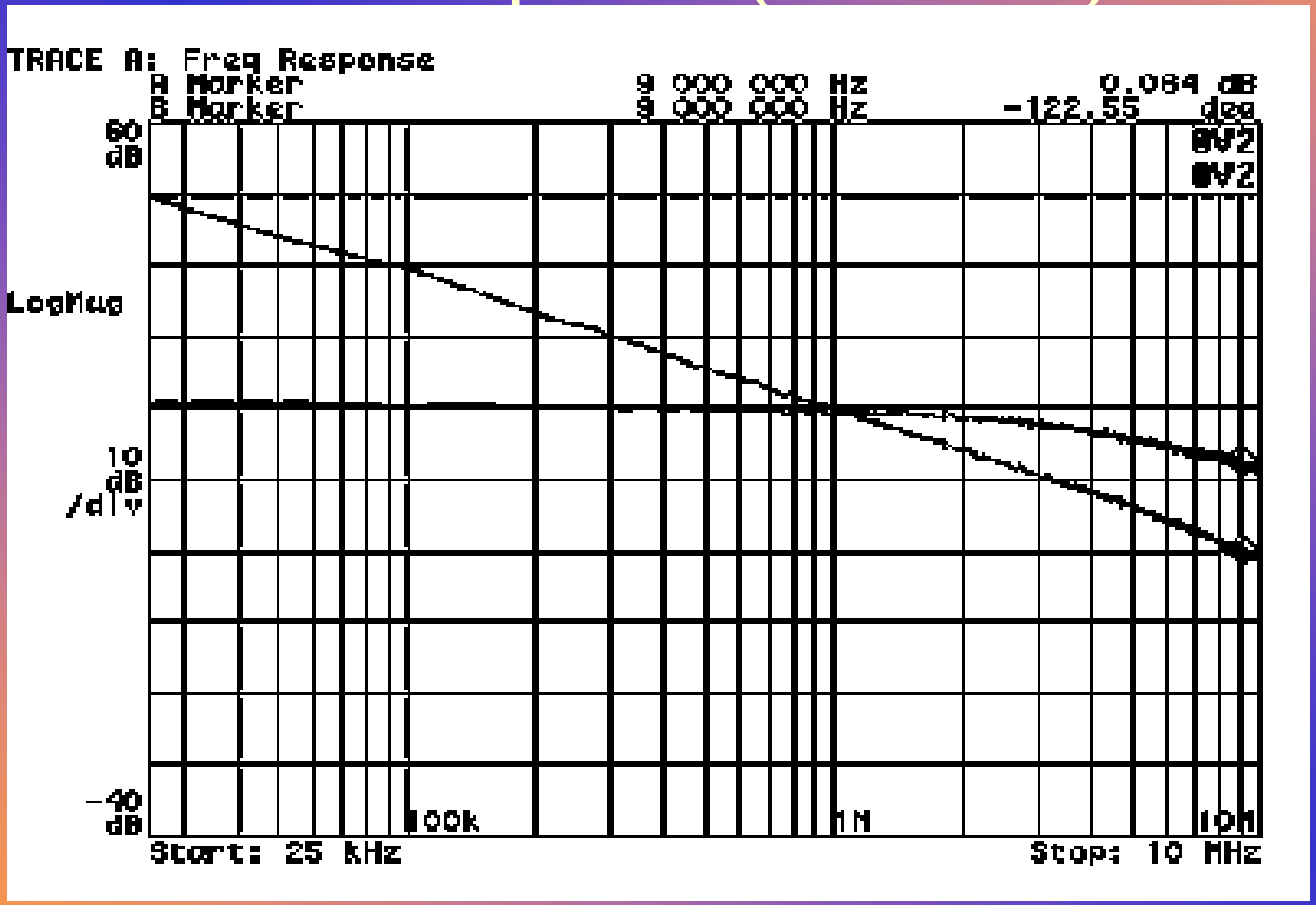
Chip Micrograph



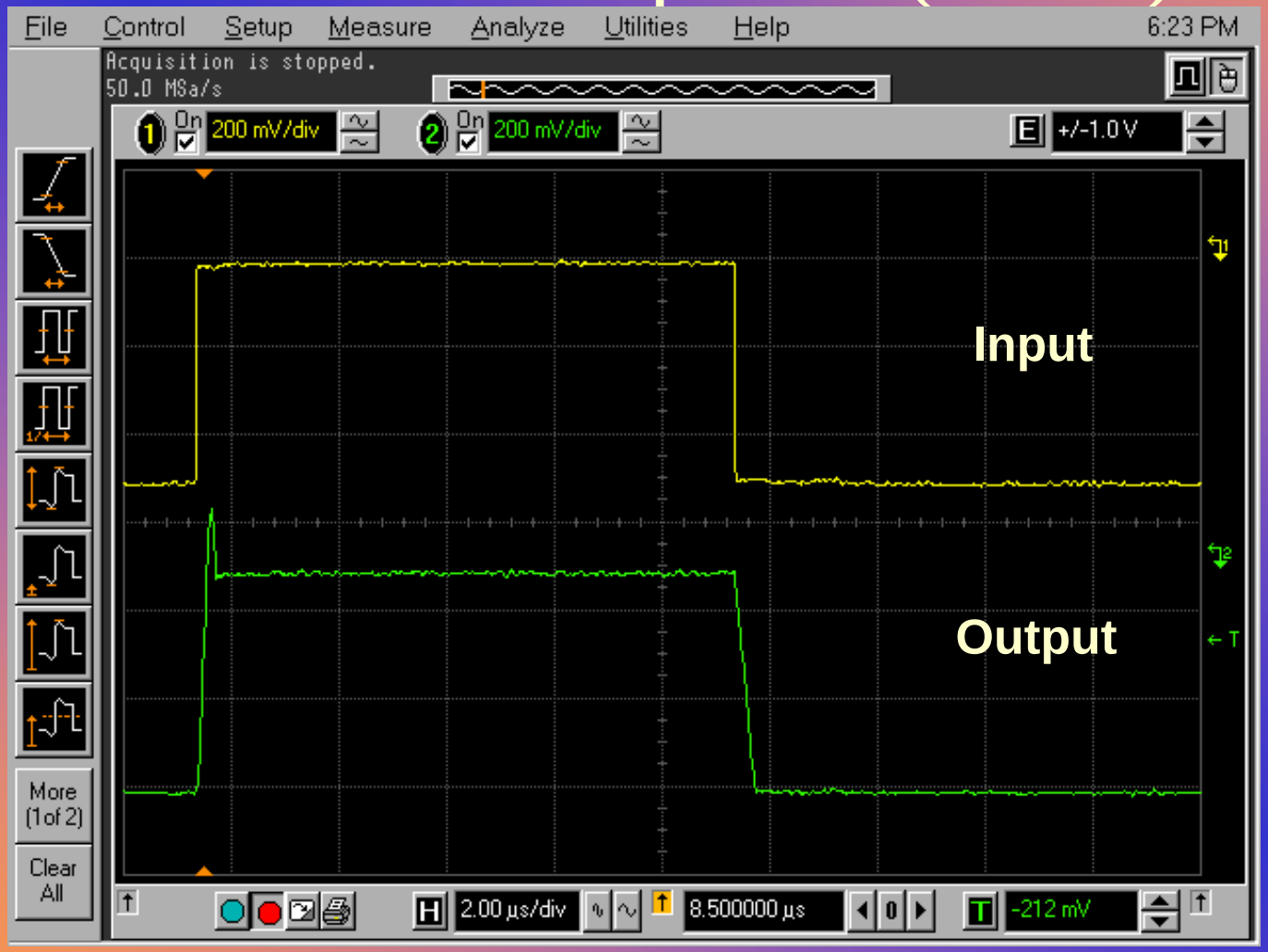
AC Response (SMC)



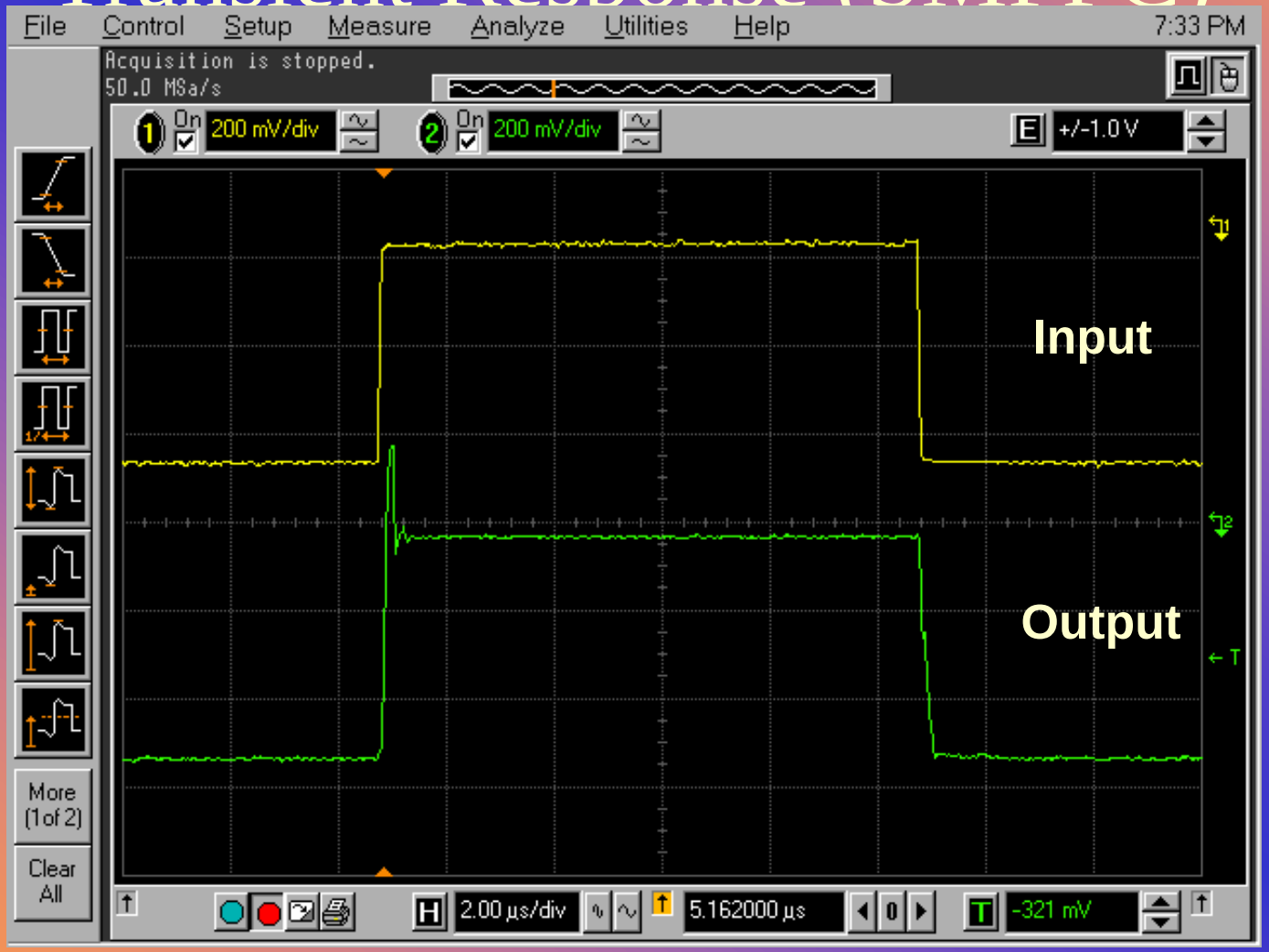
AC Response (SMFFC)



Transient Response (SMC)



Transient Response (SMFFC)



Comparison Table

	NMC	DFCFC	AFFC	SMC This Work	SMFFC This Work
Load pF/KΩ	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	±1V				
DC gain (dB)	>100	>100	>100	>100	>100
GBW (MHz)	0.4	2.6	4.5	4.6	9
Phase margin	61°	43°	65°	57°	57°
Power (mW@Vdd)	0.38 @2	0.42 @2	0.4 @2	0.38@2	0.41@2
Capacitor Value (pF)	C_{m1}=88 C_{m2}=11	C_{m1}=18 C_{m2}=3	C_m=3 C_a=7	C_m=7	C_m=4
Slew Rate SR+/ SR- (V/μS)	0.15/0.13	1.36/1.27	2.20/0.78	3.28/1.31	4.8/2
Settling Time TS^+/TS^- (μs) (to 1%)	4.9/4.7	0.96/1.37	0.42/0.85	0.53/0.4	0.58/0.43
FOM_S(MHz.pF/mW)	127	619	1350	1453	2634
FOM_L(V/μs.pF/mW)	45	314	447	726	996
Area (mm^2)	0.14	0.11	0.06	0.02	0.015
Normalized Area	9.33	7.33	4	1.33	1
Technology	0.8μm CMOS			0.5μm CMOS	

Note: Average value of the slew rate is used in the calculation of FOM_L parameter

$FOM_S = \frac{GBW * C_L}{Power}$ and $FOM_L = \frac{SR * C_L}{Power}$, where C_{Total} = Total value of compensation capacitors

Conclusions

→ **Two low power multistage amplifier topologies are introduced for large capacitive loads.**

→ **Pole splitting and feedforward approaches are combined for better performance.**

→ **Performance parameters such as GBW and Area are improved without sacrificing same power consumption.**

→ **The proposed approaches have better small-signal and large-signal performances than other reported compensation topologies .**

A Robust Feedforward Compensation Scheme for Multi-Stage OTA's with no Miller capacitors

Thanks to Bharath Kumar Thandri and

Dr José-Silva Martínez for the material provided

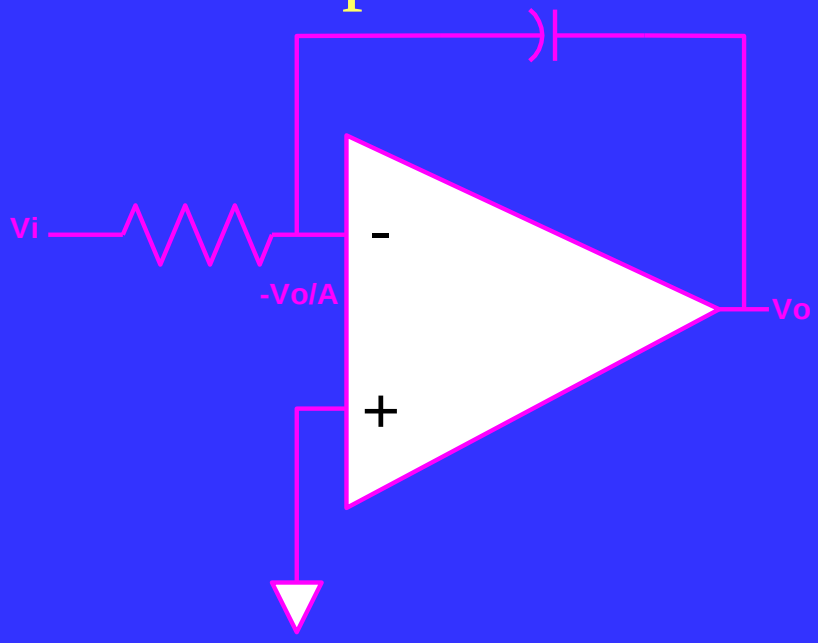
ELEN 607 (ESS)

Outline

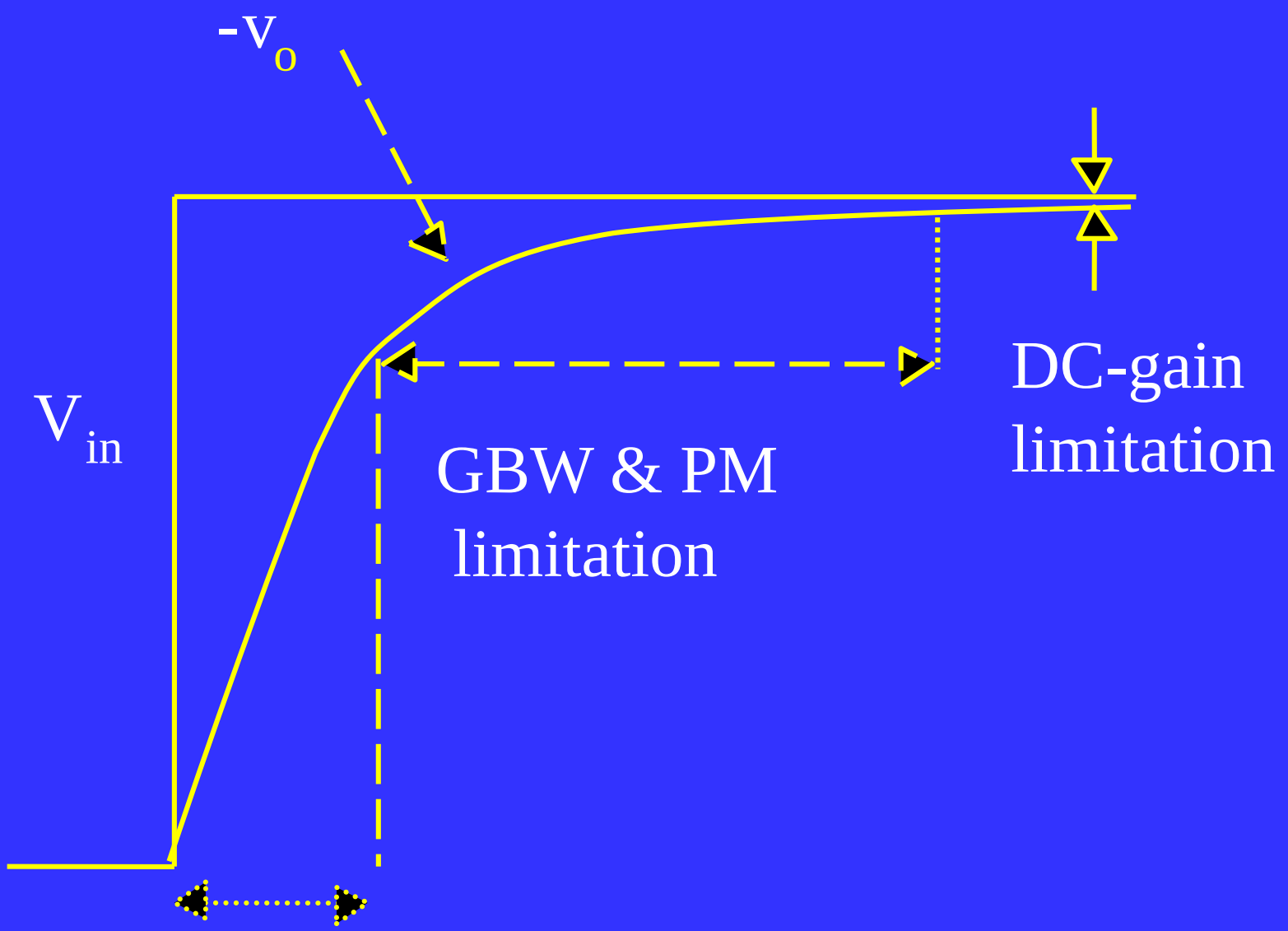
- Need for high performance amplifiers
- Conventional approaches and problems
- Proposed NCFF compensation scheme
- Pole-zero mismatch effects
- OTA design
- Simulation and Experimental results
- Conclusion

Need for high performance amplifiers

- Performance of integrator degrades because of the amplifier characteristics
- Output deviates from ideal value due to finite gain
- Settling time increases with decreasing GBW
- Amplifiers with high gain and GBW are required in high precision ADC's (pipelined, sigma-delta etc) and switched capacitor filters.



$$V_o = \frac{\left(\frac{-V_i}{sRC}\right)}{\left(\frac{1}{A}\left(1+\frac{1}{sRC}\right)+1\right)}$$

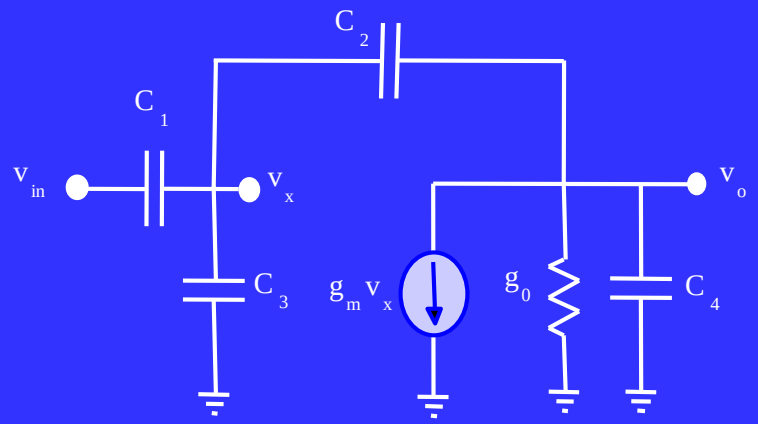


Step response of an amplifier with sufficient phase margin.

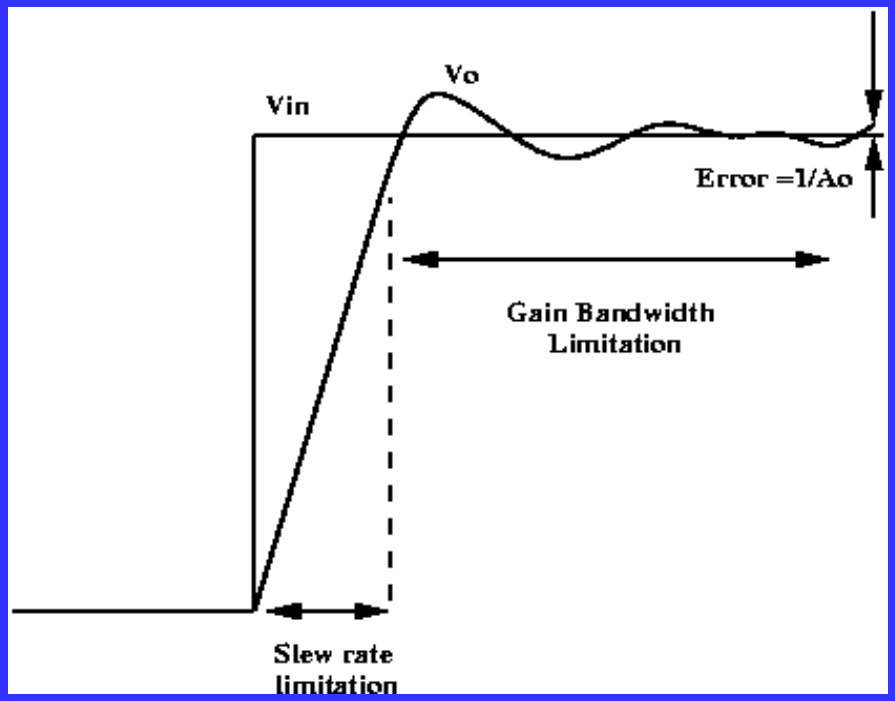
$$V_o(t) = V_o(t_0) - \frac{\alpha V_i}{1 + \frac{1}{\beta A_v}}\left[1 - e^{-\omega_{GBW} t}\right]$$

$$\omega_{GBW} = \frac{\beta g_m}{C_4 + \frac{C_2(C_1 + C_3)}{C_1 + C_2 + C_3}}$$

α (=C1/C2) is the ideal amplifier gain, β (=C2/ (C1+C2+C3)) is the feedback factor and Av (=gm/g0)



Step response of an amplifier (continues)



$$V_o(t) = V_{in}(1 - k_1 e^{-\omega_{gbw} t})$$

$k_1 \cong 1$

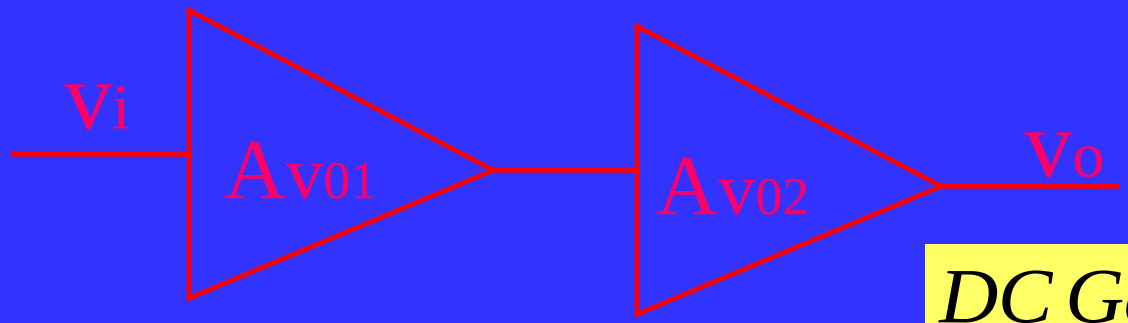
ω_{gbw} is gainband width of amplifier

- Two phases - slewing phase and quasi-linear phase
- Slew rate is limited by current available to charge/discharge the load capacitor. Response is usually dominated by second phase
- High GBW => fast settling time ; High gain => accuracy ; sufficient phase margin => no ringing or overshoot
- Best settling performance requires high performance amplifier

Contradicting requirements for Gain vs Bandwidth ?

- High gain amplifiers => multistage architectures, low bias currents, large channel lengths
- High bandwidth amplifiers => single stage, high bias currents, minimum channel lengths
- Difficult to obtain high gain and bandwidth simultaneously
- Previous architectures settle for an optimal tradeoff between speed and accuracy requirements

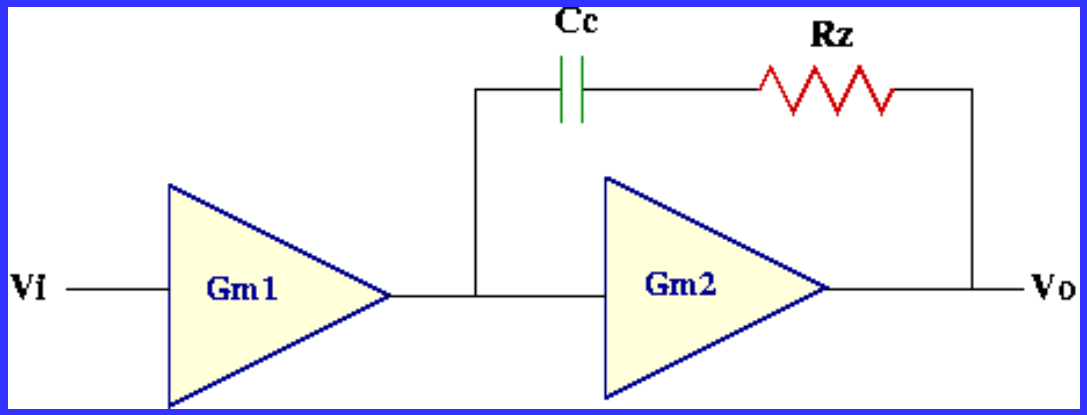
Cascaded amplifiers

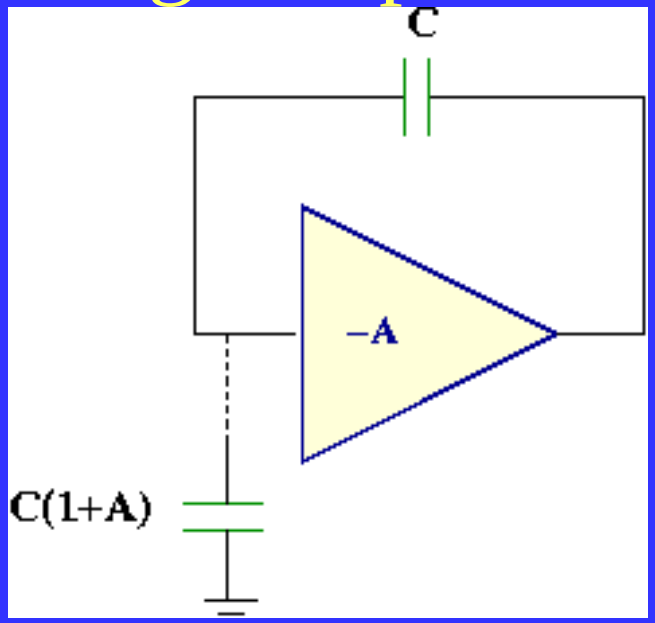


$$DC\,Gain = A_{v01} * A_{v02}$$

- Cascade of individual gain stages gives high gain
- Poles created by each stage degrade phase response by -90°
- Stable closed loop operation => phase margin > 45°
- Robust phase compensation scheme is required for multi-stage amplifiers
- Miller compensation (pole splitting/lead compensation) used for two stage amplifiers has been extended for multi-stage amplifiers

Miller compensation for 2-stage amplifier





Disadvantages

- Miller effect of C_c pushes dominant pole to lower frequencies => low GBW
- Non-dominant pole is pushed to higher frequencies => more power consumption
- RHP zero is created by addition of C_c which creates negative phase shift
- R_z is used to cancel RHP zero

$$w_{p,d} = \frac{1}{r_{ds1} A_{v02} C_c}$$

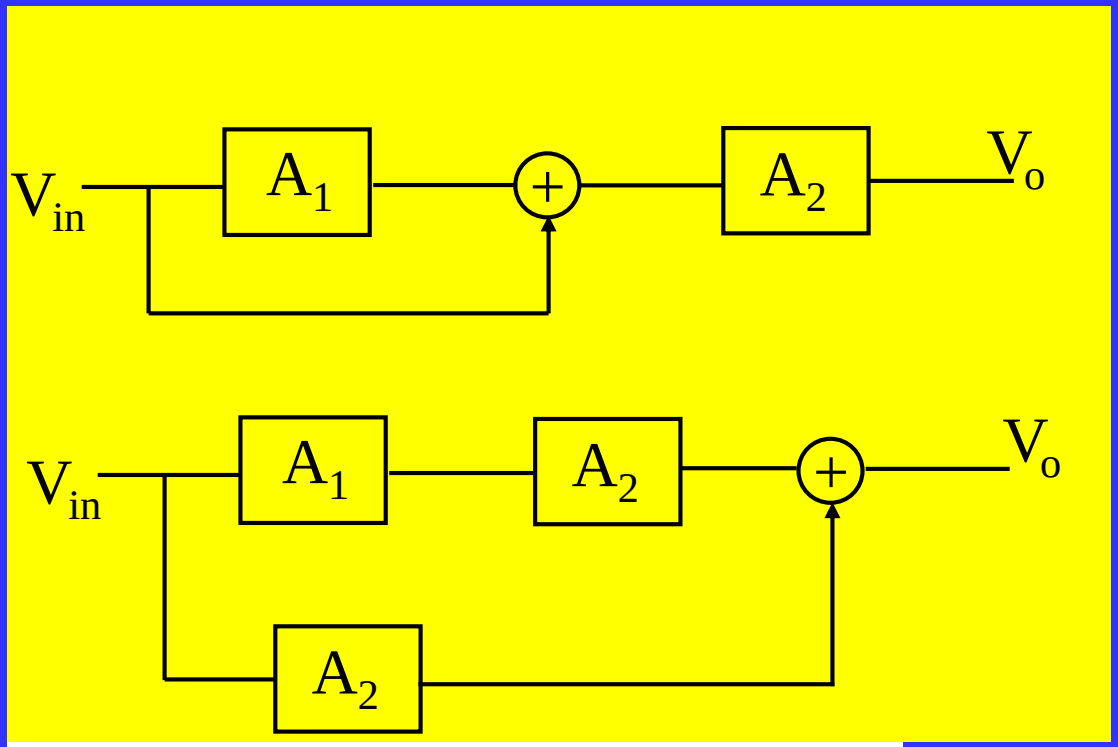
$$w_{z,rhp} = \frac{g_{m2}}{C_c}$$

$$w_z = \frac{1}{C_c\left(R_z - \frac{1}{g_{m2}}\right)}$$

Reported compensation schemes(cont)

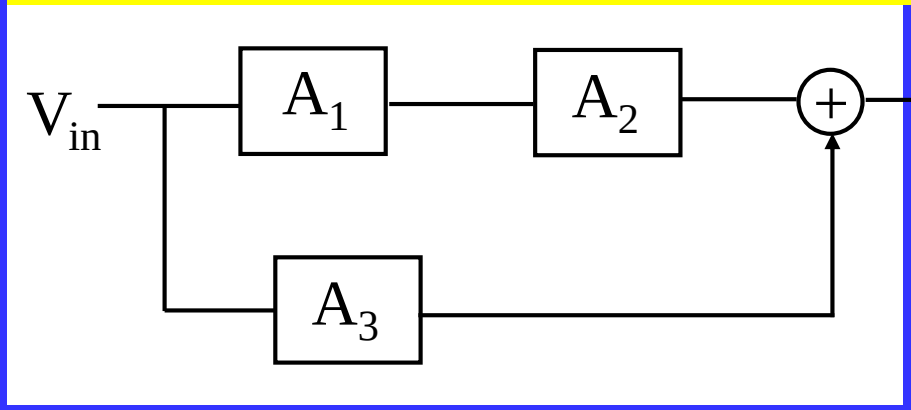
- Damping factor frequency controlled compensation (DFCFC) and embedded frequency compensation schemes have also been reported.
- All reported schemes are often a variant of the two-stage miller compensation and have similar disadvantages
- A multistage feedforward compensated amplifier has been reported by Cirrus Logic for low-noise application, but it also uses compensation capacitor

Equivalent Block Diagrams



$$V_o = (A_1A_2 + A_2)V_{in}$$

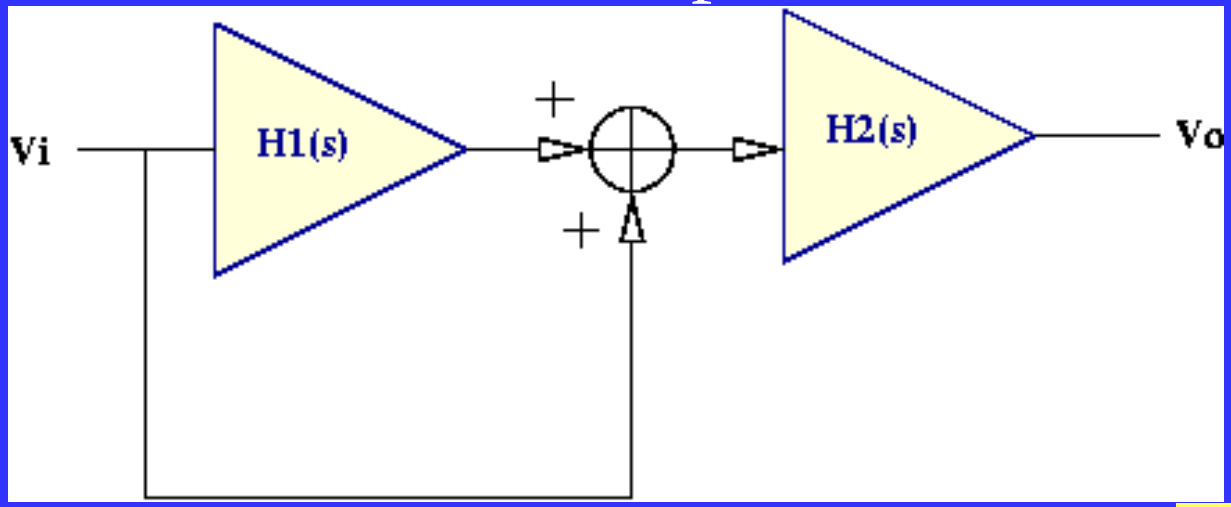
$$V_o = (A_1A_2 + A_2)V_{in}$$



$$V_o = (A_1A_2 + A_3)V_{in}$$

- A_2 and A_3 must have only one pole. Different gains are okay.
- The number of poles of A_1 determines the number of poles of the system.

No-Capacitor FeedForward (NCFF) compensation scheme



$$H1(s) = \frac{A_1}{1 + \frac{s}{w_{p1}}}$$

$$H2(s) = \frac{A_2}{1 + \frac{s}{w_{p2}}}$$

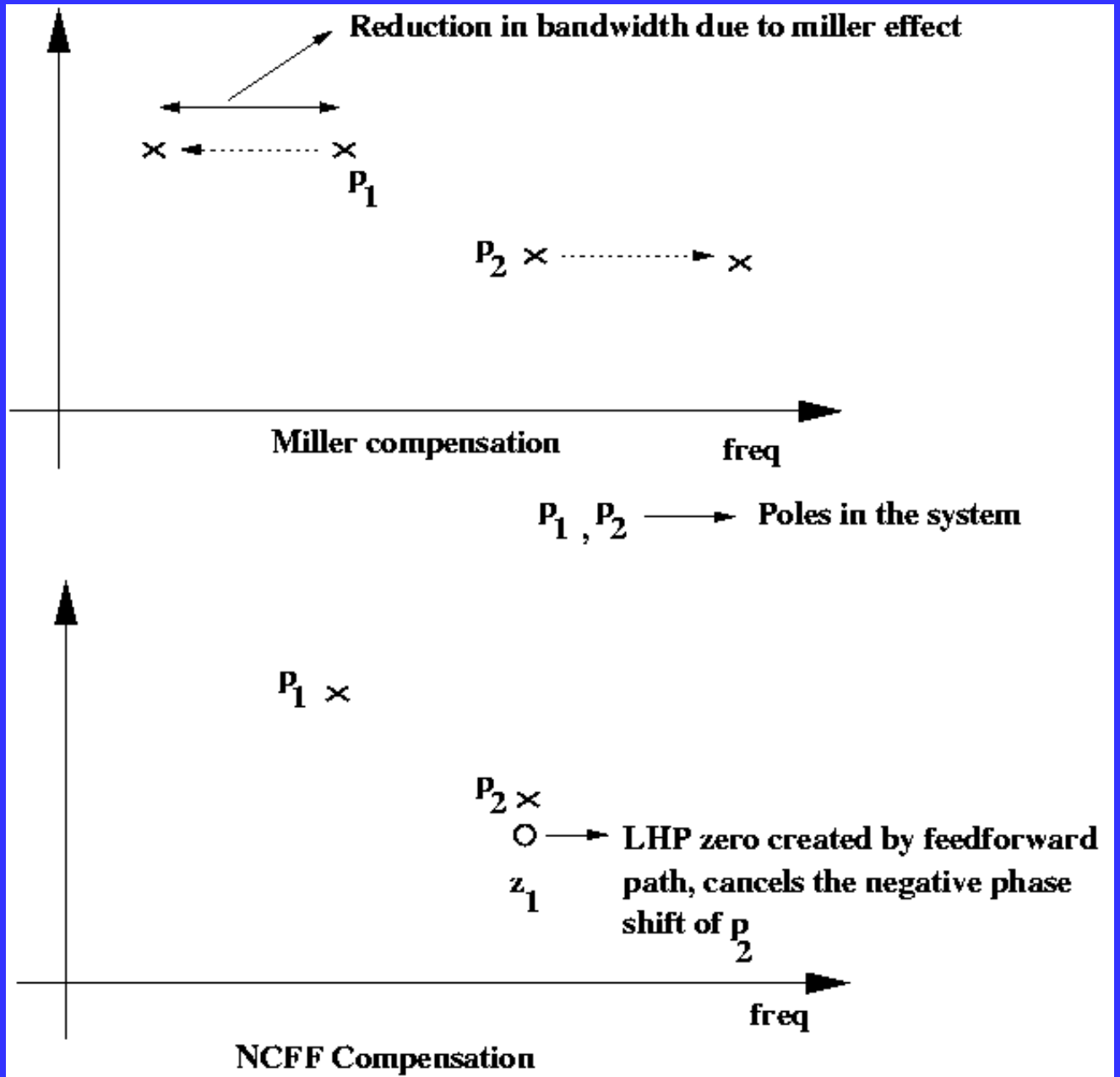
- Main concept : Feedforward path with same phase shift as compared to the normal path produces LHP zeros.
- LHP zeros create positive phase shift and cancels the negative phase shift of poles
- No pole splitting => improvement in BW
- Combines high gain, high GBW and good phase margin

$$\frac{V_o}{V_i} = \frac{A_2\left(A_1 + 1 + \frac{s}{w_{p1}}\right)}{\left(1 + \frac{s}{w_{p1}}\right)\left(1 + \frac{s}{w_{p2}}\right)}$$

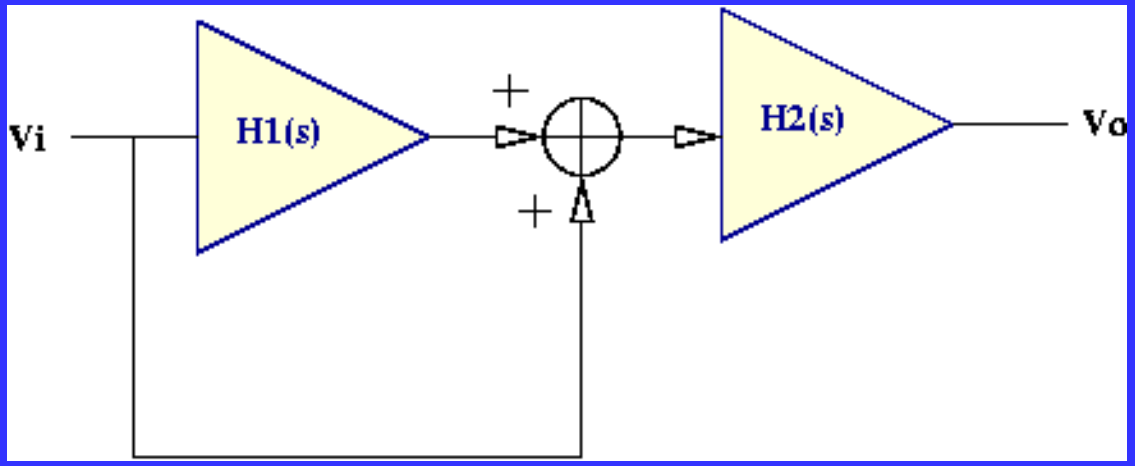
$$A_{vo} = A_1 A_2 + A_2$$

$$z_1 = -(A_1 + 1) w_{p1}$$

Miller vs NCFF compensation:Why the difference?



Effect of non-dominant pole



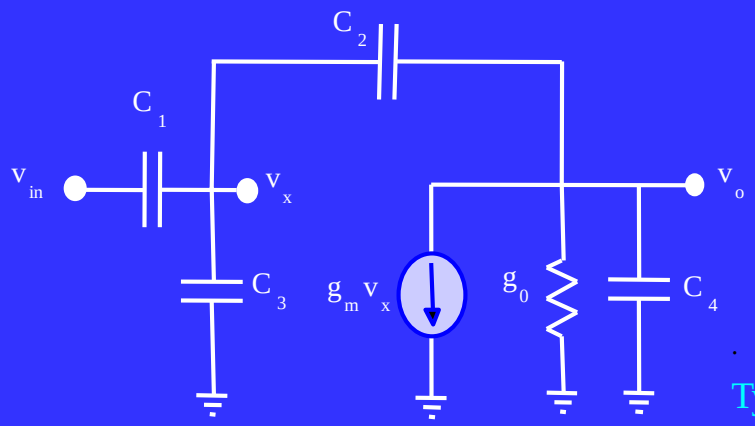
$$H1(s) = \frac{A_1}{(1+\frac{s}{w_{p1,d}})(1+\frac{s}{w_{p1,nd}})}$$

$$H2(s) = \frac{A_2}{1+\frac{s}{w_{p2}}}$$

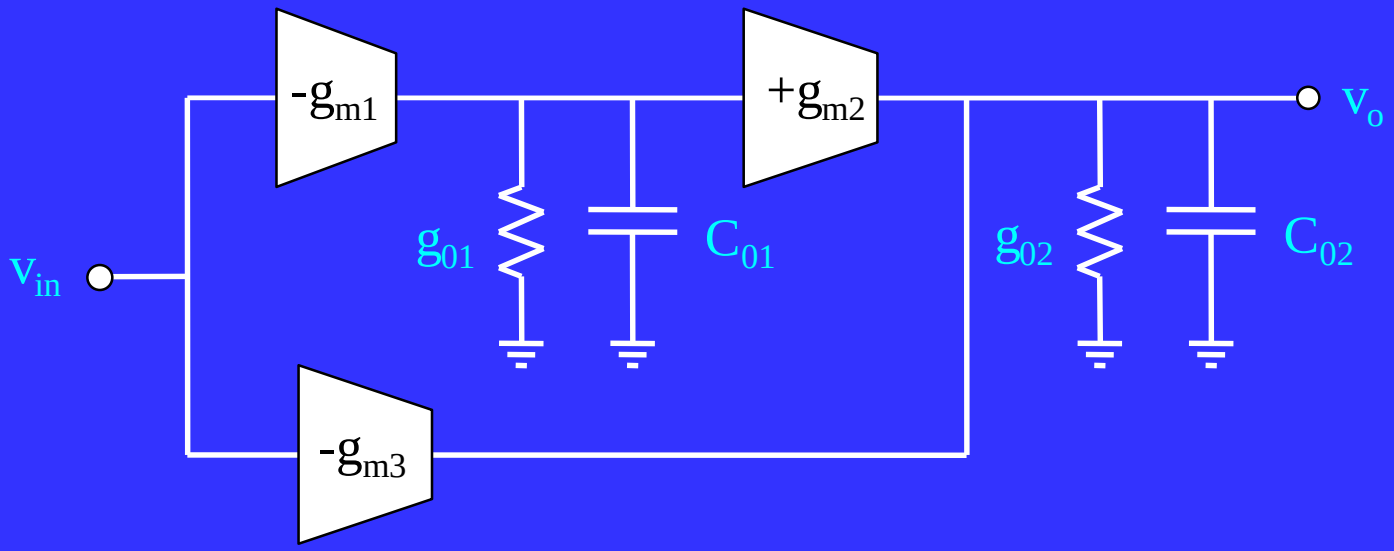
- Number of LHP zeros created is equal to the order of the first stage
- Main constraint - No non-dominant pole of second stage before the overall GBW
- For N poles in the system, (N-1) LHP zeros are created => overall amplifier's response is effectively a single pole phase response

$$\frac{V_o}{V_i} = \frac{A_2\left(A_1 + (1+\frac{s}{w_{p1,d}})(1+\frac{s}{w_{p1,nd}})\right)}{\left(1+\frac{s}{w_{p1,d}}\right)\left(1+\frac{s}{w_{p1,nd}}\right)\left(1+\frac{s}{w_{p2}}\right)}$$

$$A_2\left[A_1 + (1+\frac{s}{w_{p1,d}})(1+\frac{s}{w_{p1,nd}})\right] = 0$$



Typical OTA based capacitor amplifier



Block diagram of basic NCFF compensation scheme for 2-stage amplifier.

$$H(s) \cong -\frac{A_{v1}A_{v2} + A_{v3}\left(1+\dfrac{s}{\omega_{p1}}\right)}{\left(1+\dfrac{s}{\omega_{p1}}\right)\left(1+\dfrac{s}{\omega_{p2}}\right)} = -\frac{\left(A_{v1}A_{v2} + A_{v3}\right)\left(1+\dfrac{A_{v3}s}{\left(A_{v1}A_{v2} + A_{v3}\right)\omega_{p1}}\right)}{\left(1+\dfrac{s}{\omega_{p1}}\right)\left(1+\dfrac{s}{\omega_{p2}}\right)}$$

$$z_1 = -\omega_{p1}\left(1+\frac{A_{v1}A_{v2}}{A_{v3}}\right) \cong -\frac{g_{m1}}{C_{01}}\left(\frac{g_{m2}}{g_{m3}}\right)$$

Optimization of Loop Equations

$$\frac{v_0(s)}{v_i(s)} \cong -\left(\frac{\frac{C_1}{C_2}}{1+\frac{1}{\beta A_V}}\right)\left(\frac{1+\frac{s}{\omega_Z}}{\left(1+\frac{s}{\omega_1}\right)\left(1+\frac{s}{\omega_2}\right)}\right)$$

$$\omega_1 = \frac{\beta g_{m3} + g_0}{2C_L'}\left[1-\sqrt{1-\frac{4\beta C_L' g_{m1} g_{m2}}{C_{01}(\beta g_{m3}+g_0)^2}}\right] \quad (7)$$

$$\omega_2 = \frac{\beta g_{m3} + g_0}{2C_L'}\left[1+\sqrt{1-\frac{4\beta C_L' g_{m1} g_{m2}}{C_{01}(\beta g_{m3}+g_0)^2}}\right]$$

$$\omega_z = \frac{g_{m3}}{2C_2}\left[\sqrt{1+\frac{4C_2 g_{m1} g_{m2}}{C_{01} g_{m3}^{\ 2}}}-1\right]$$

$$v_0(t) = v_0(t_0) - \left(\frac{\frac{C_1}{C_2} V_i}{1 + \frac{1}{\beta A_V}} \right) \left(1 + \frac{1 - \frac{\omega_1}{\omega_2}}{1 - \frac{\omega_1}{\omega_Z}} e^{-\omega_1 t} + \frac{\frac{\omega_2}{\omega_Z} - 1}{\frac{\omega_2}{\omega 1} - 1} e^{-\omega_2 t} \right)$$

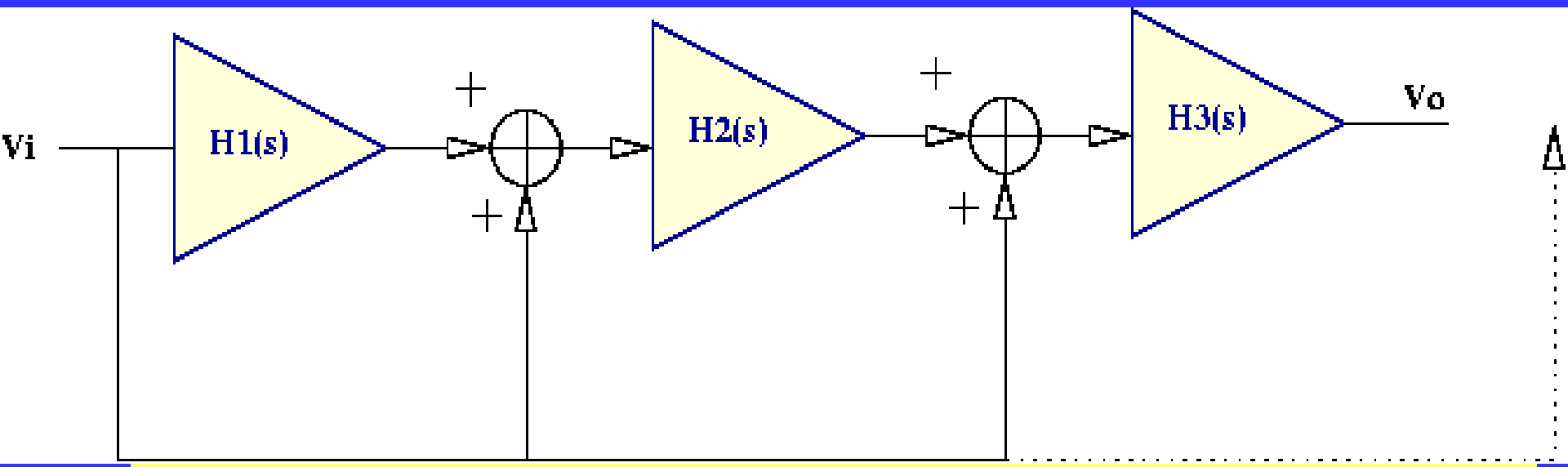
4bCL'gm1gm2/(C01(bgm3+g0)2) < 0.5,

$$\omega_z \cong \left(\frac{g_{m2}}{g_{m3}} \right) \left(\frac{g_{m1}}{C_{01}} \right) \quad (10)$$

$$\omega_1 \cong \frac{\beta g_{m1} g_{m2}}{C_{01}(\beta g_{m3} + g_0)} \quad (11)$$

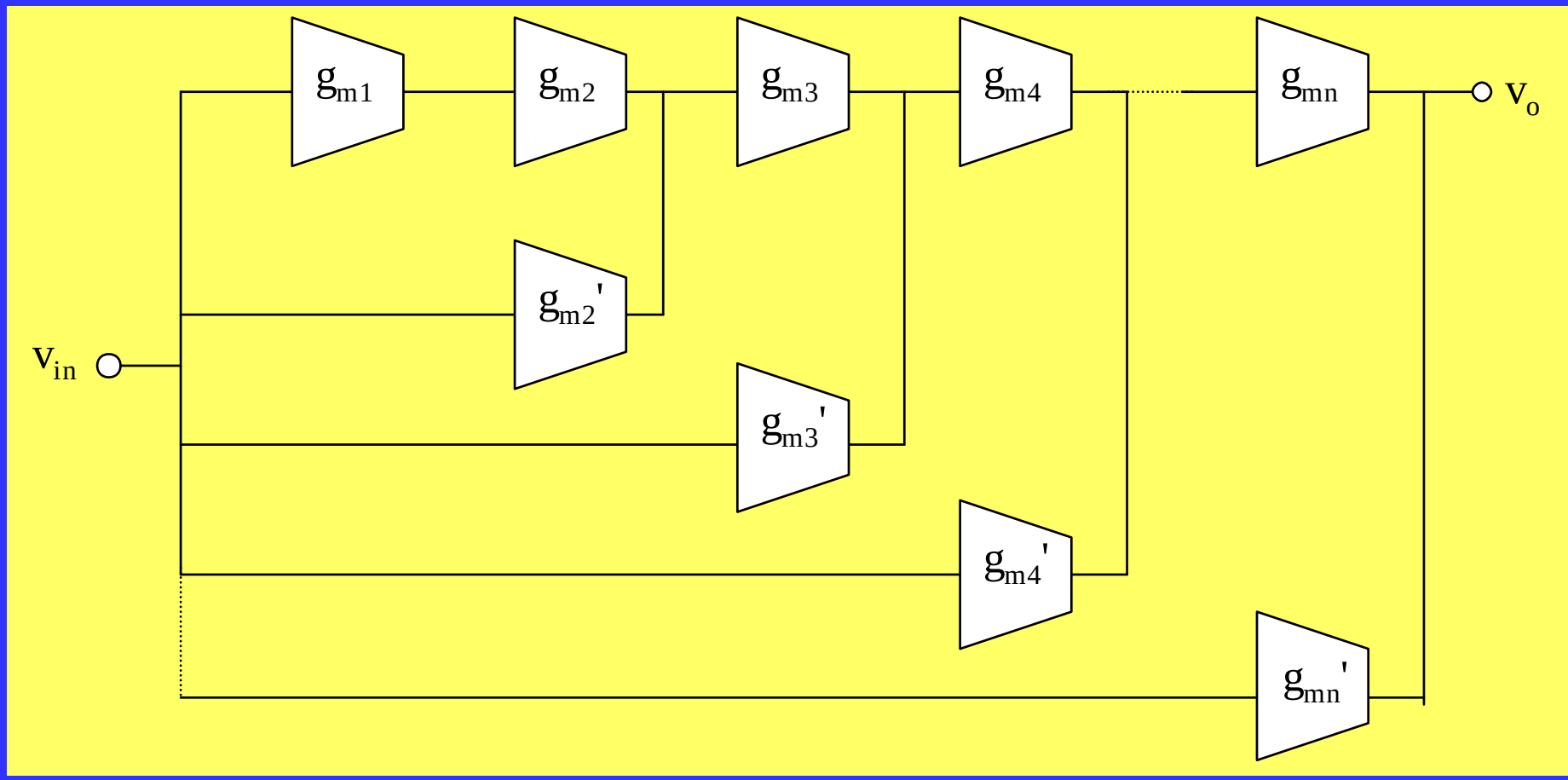
$$\omega_2 \cong \frac{\beta g_{m3} + g_0}{C_L'}$$

Extending the scheme to multi-stage amplifiers: Conceptual Representation



- Constraint - Last stage should not have non-dominant pole before overall GBW
- Number of LHP zeros is one less than the total number of poles in the system

NCFF compensation scheme for N-Stage Amplifier Implementation



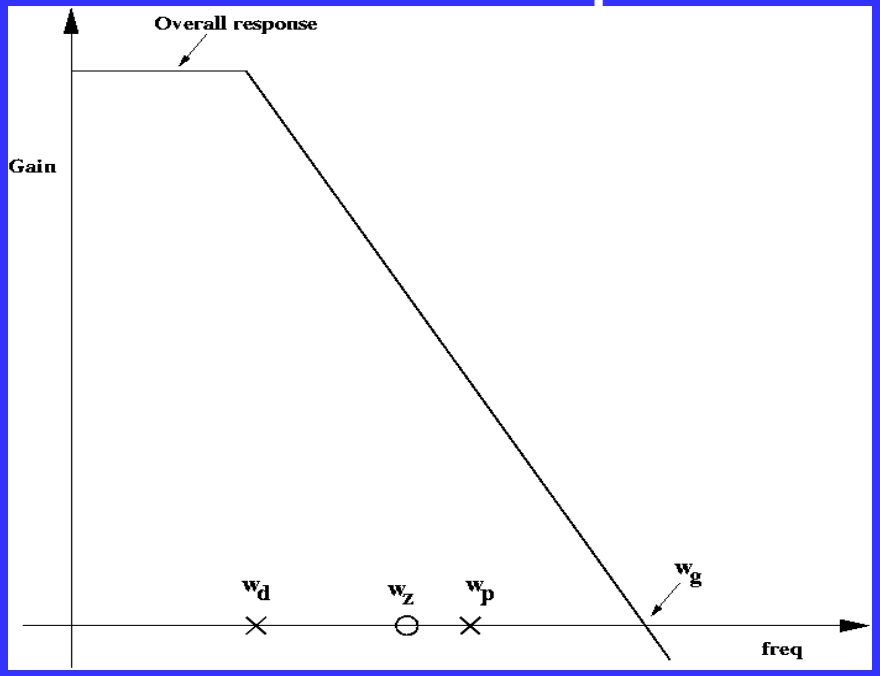
Main features of NCFF compensation scheme

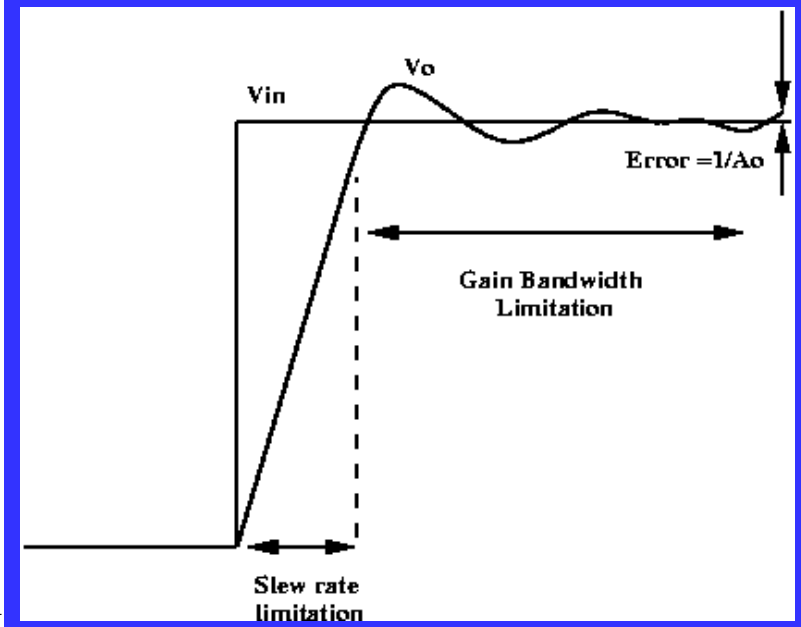
- Combines high gain and GBW, resulting in a good settling time and accurate final value
- Good phase margin - when zero exactly cancels the pole, phase margin is 90°
- No compensation capacitors => lot of reduction in area, esp for multi-stage amplifiers with 2 or more compensation capacitors
- Disadvantage - pole-zero mismatch due to process variations. Pole-zero doublet affects settling time and phase margin

Effect of pole-zero doublet

- Pole zero doublet causes minor change in frequency response, but may degrade the settling time based on their spacing and the zero frequency
- For more accuracy (0.01%), lower frequency doublet causes more degradation in settling time because of higher time constant
- For lesser accuracy(0.1%) higher frequency doublet will cause more degradation because of its larger amplitude, though it decays faster

Effect of pole-zero mismatch





A) Settling time

- Settling time depends on pole-zero mismatch and zero frequency
- When pole-zero cancellation is at high frequencies , effect is very minimal

$$V_o(t) = V_{in}\left(1 - k_1 e^{-w_g t} + k_2 e^{\left(\frac{-t}{\tau_2}\right)}\right)$$

$$k_2 = \frac{w_z - w_p}{w_g} \; ; \tau_2 = \frac{1}{w_z}$$

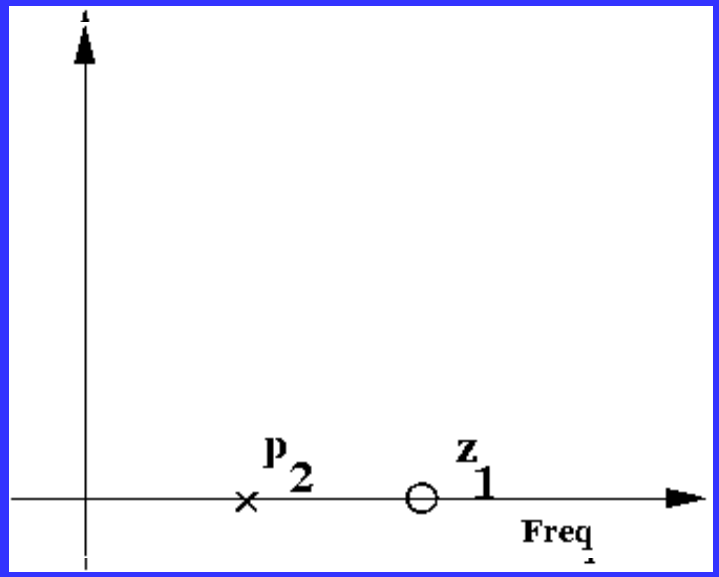
$$w_g \rightarrow \text{GBW}$$

$$w_z \rightarrow \text{zero} \; ; w_p \rightarrow \text{pole}$$

Effect of pole-zero mismatch(cont)

$$z_1 = -(A_1 + 1)w_{p1} \qquad z_1 \cong p_2$$

$$Overall\ GBW = A_2(A_1 + 1)w_{p1}$$

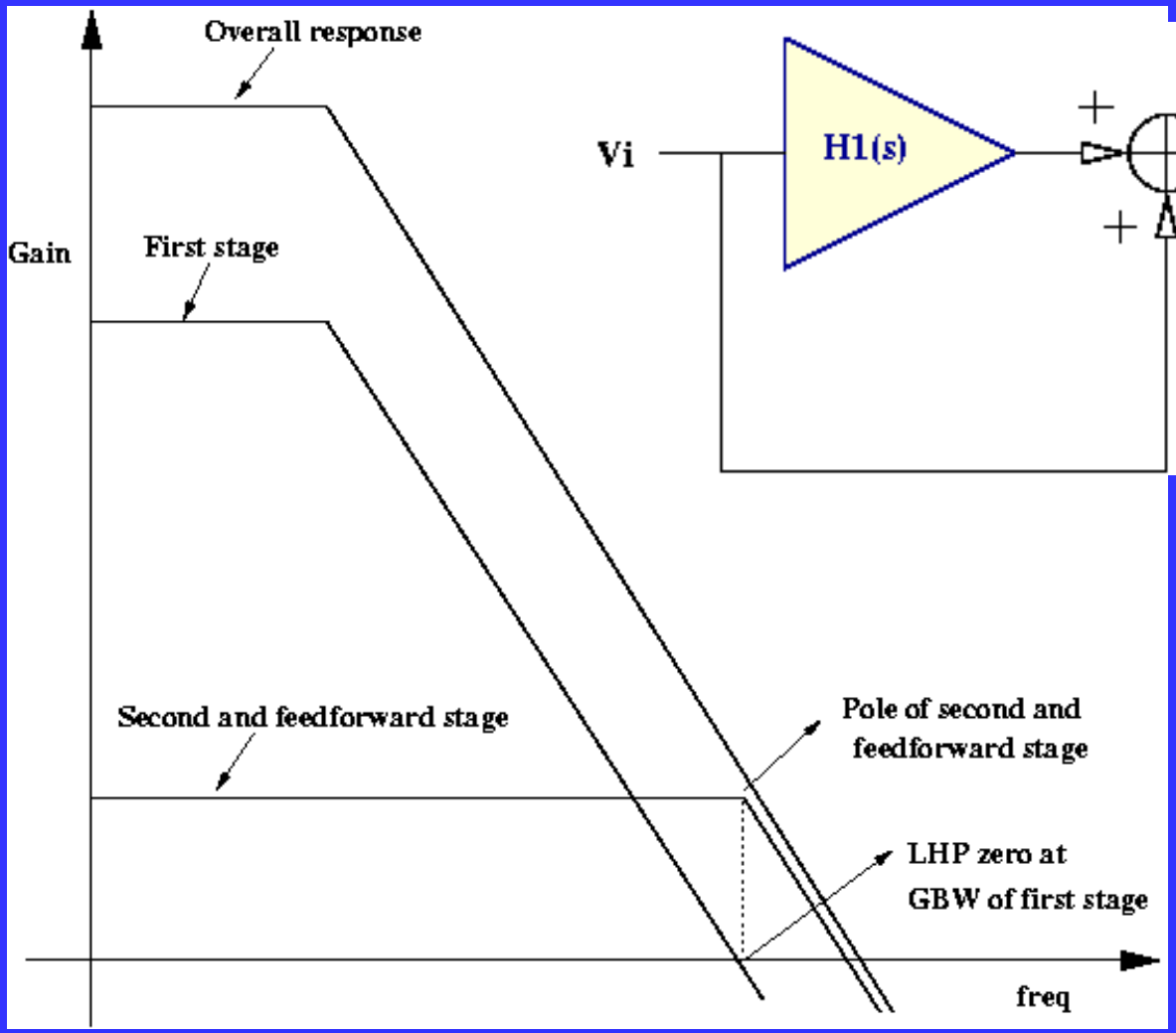


B) Phase margin and stability

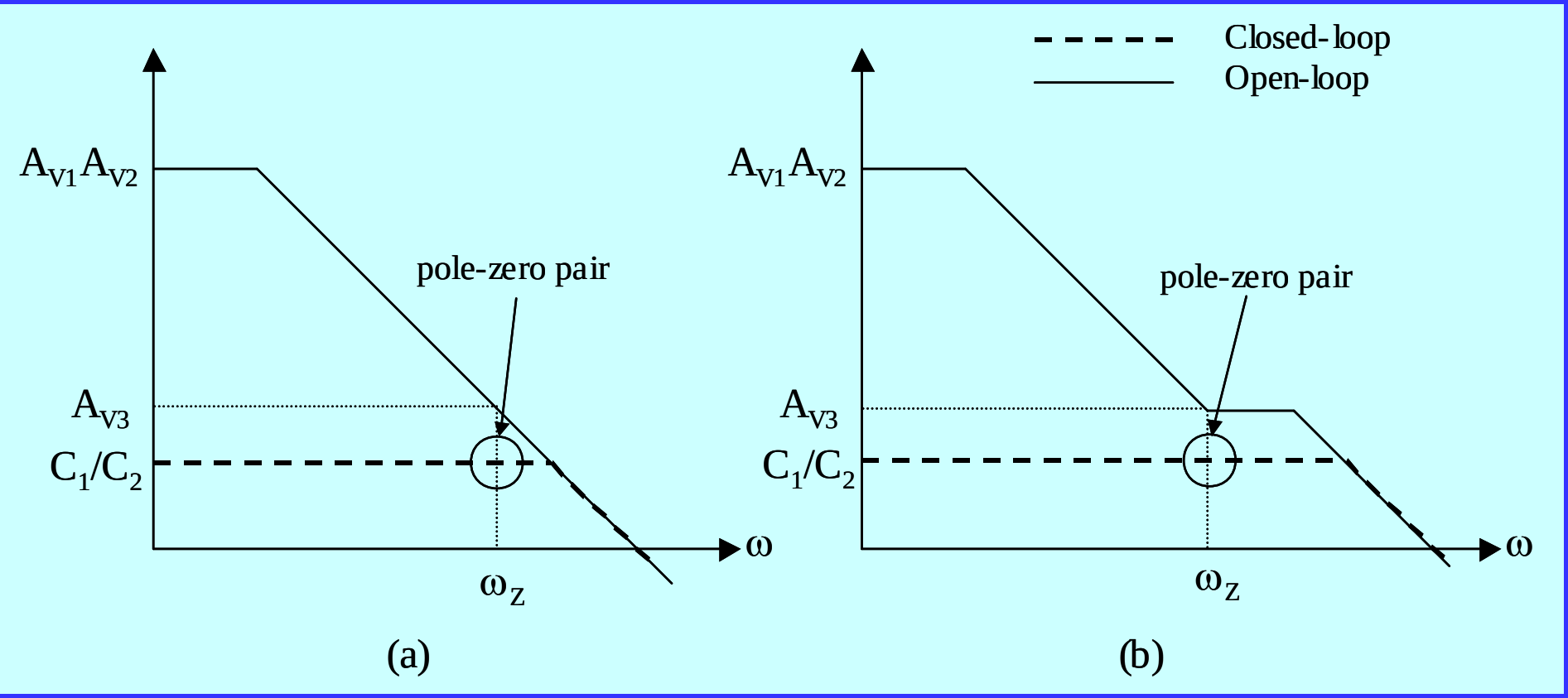
Two scenarios

- When zero occurs before the pole, it improves the phase margin
- When pole occurs before zero : It is always stable when the gain of the second stage > 1. It can be unstable when the second stage is an attenuator
- Since cancellation is done at high frequencies, percentage change due to process variations is relatively small

Gain distribution

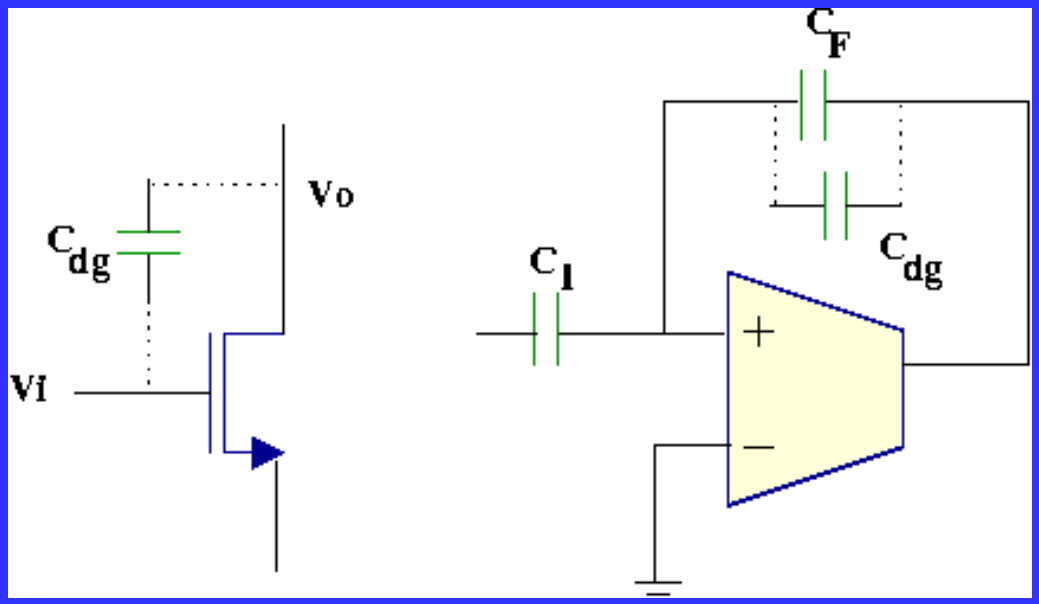


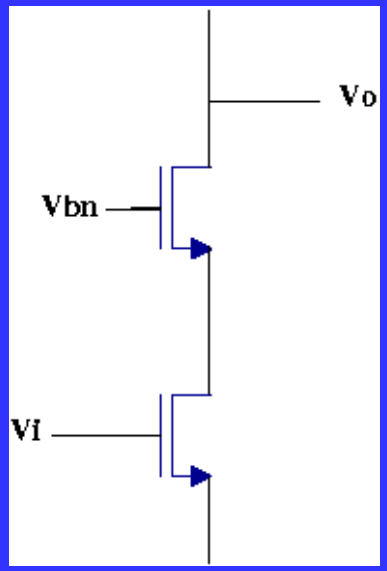
- First stage - High gain and low bandwidth
- Feedforward and second stage - low gain and high bandwidth



Amplifier frequency response and pole-zero locations in open and closed loop.
a) Perfect pole-zero cancellation b) Pole-zero mismatch.

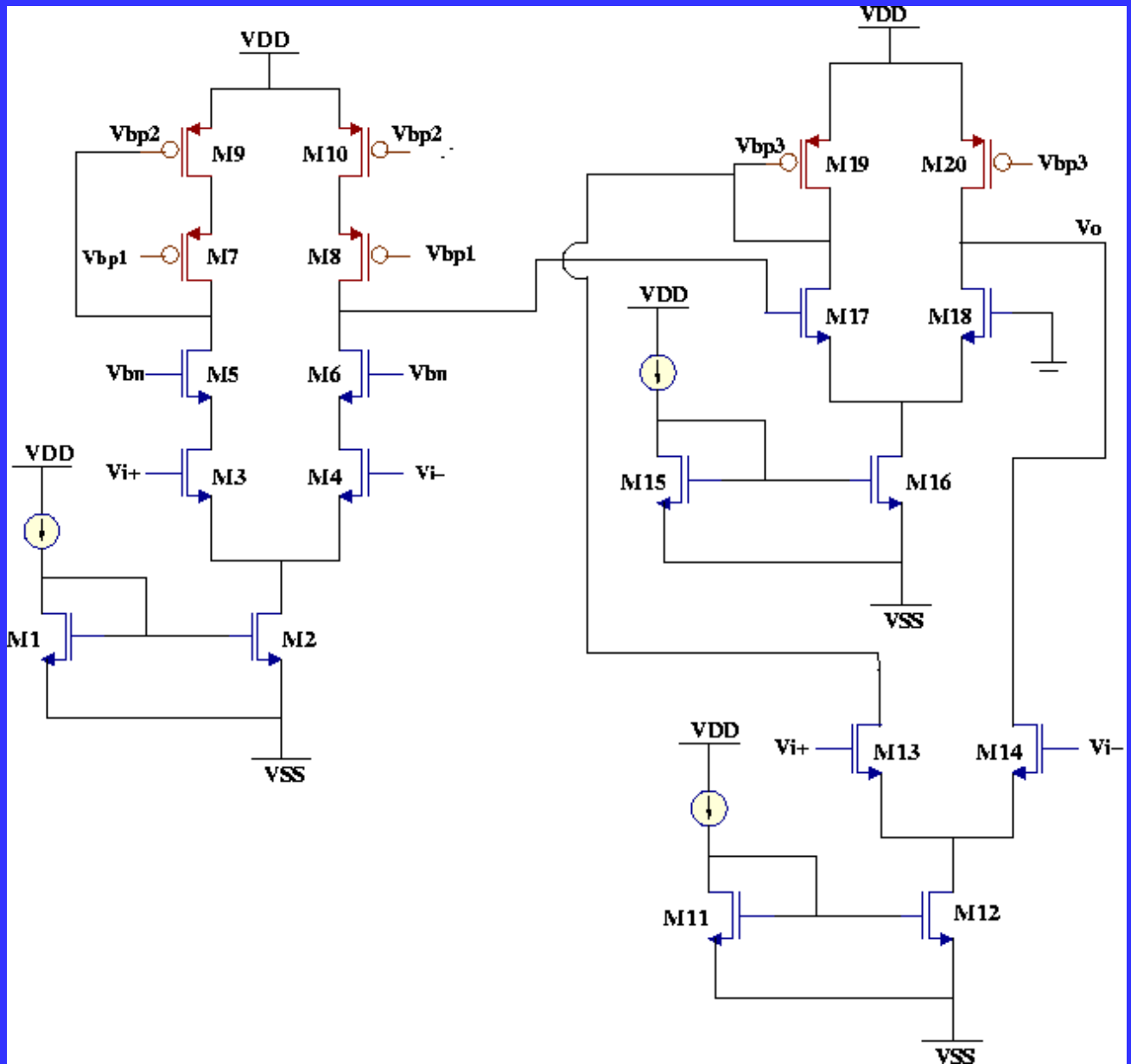
Parasitic capacitance in feedforward path

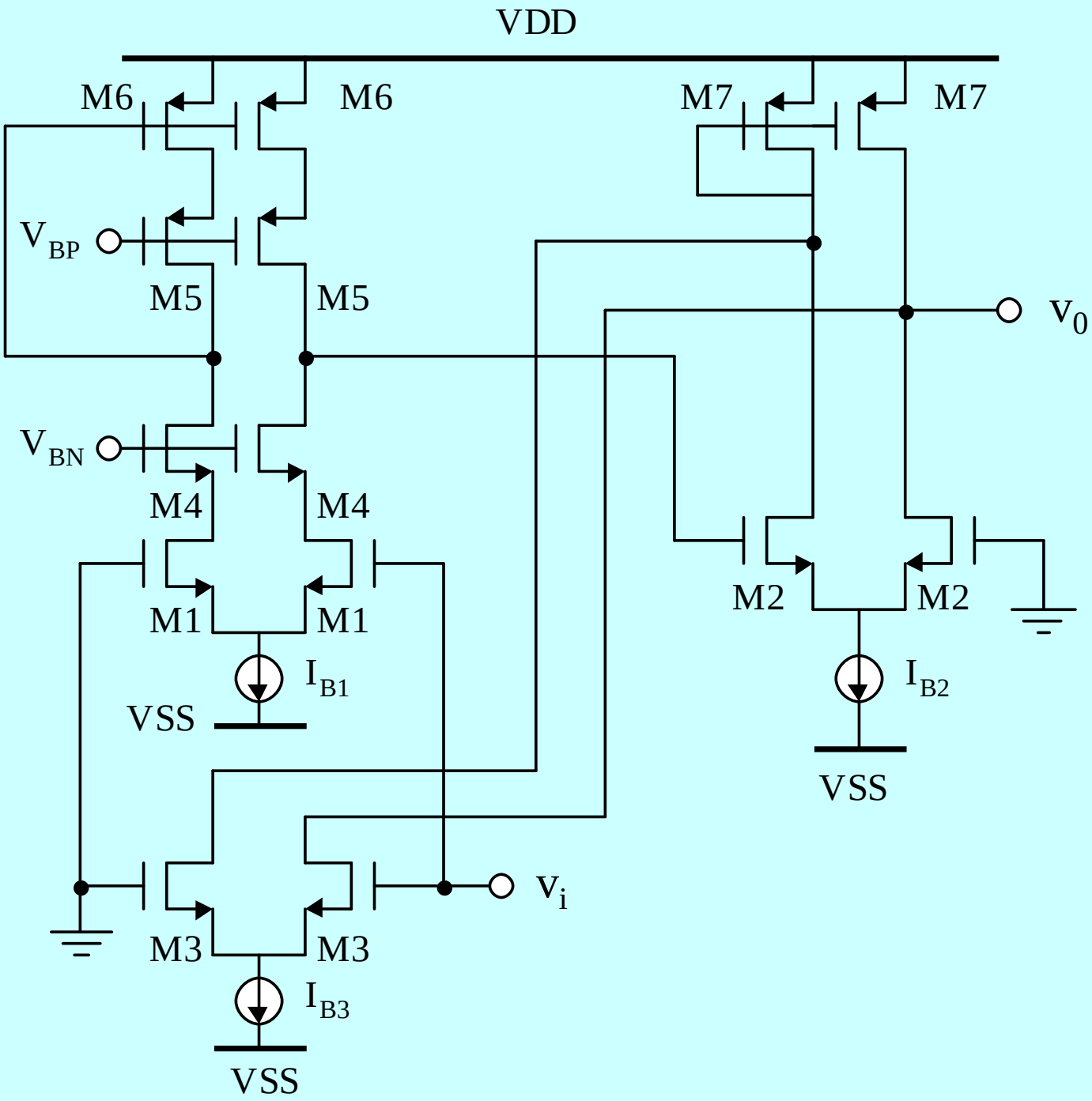




- Parasitic C_{gd} capacitance in the feedforward path exists from input to output node
- When used in closed loop, it is in parallel to feedback capacitor and attenuates the signal
- Possible solution - use cascode amplifier in the feedforward stage

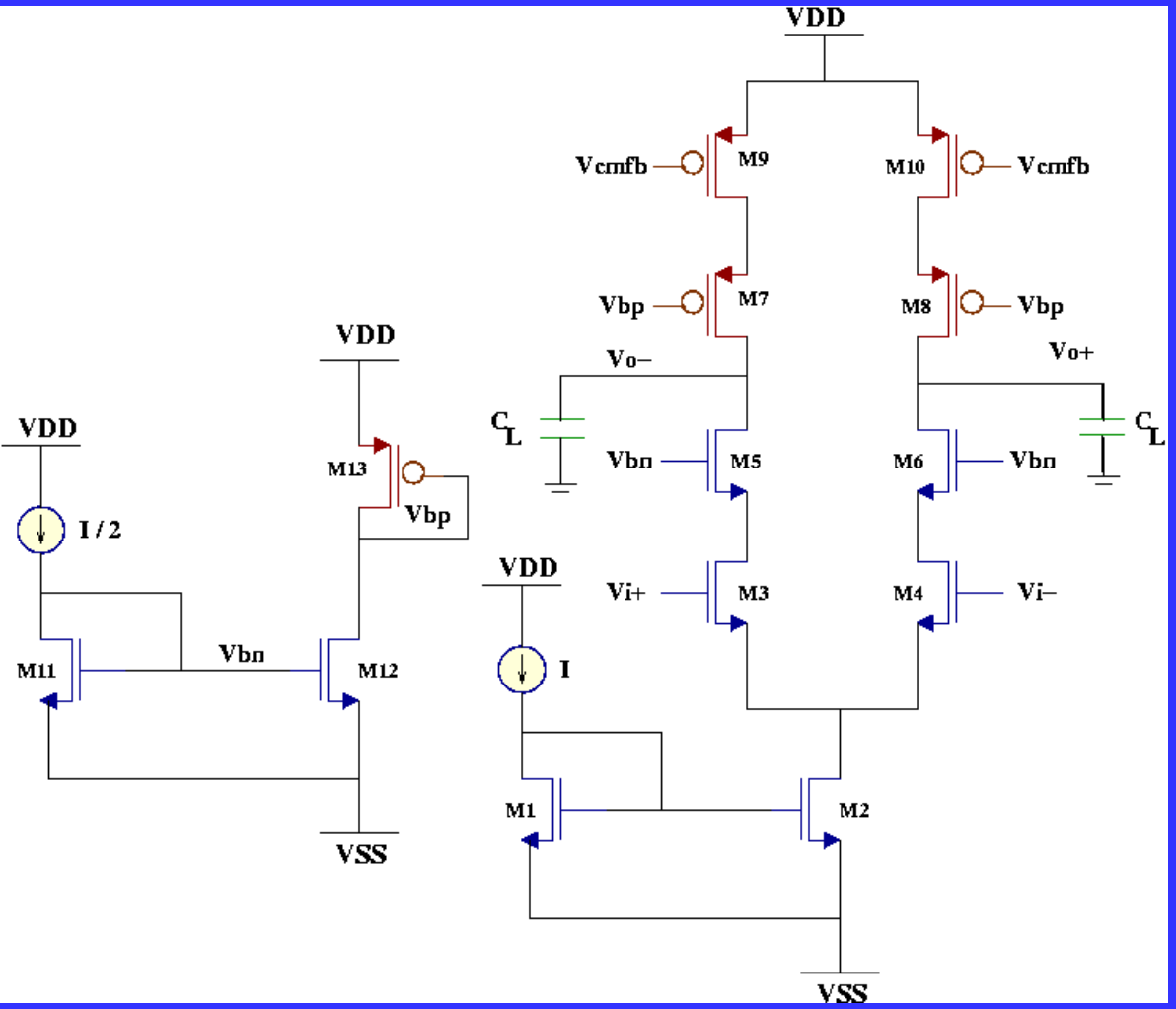
Single-ended amplifier (first try)



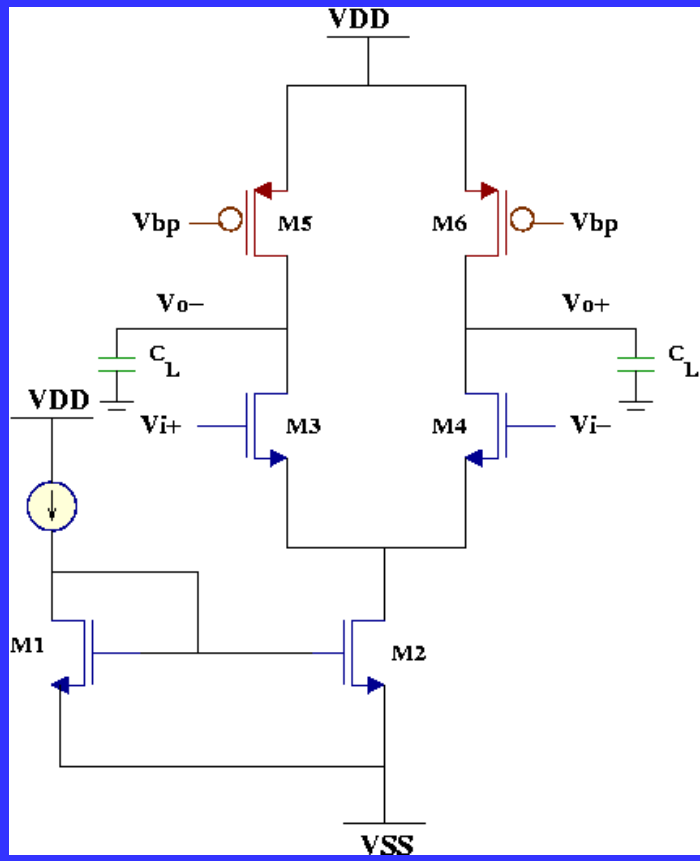


Single-ended amplifier with NCFF compensation scheme

Fully Differential Amplifier

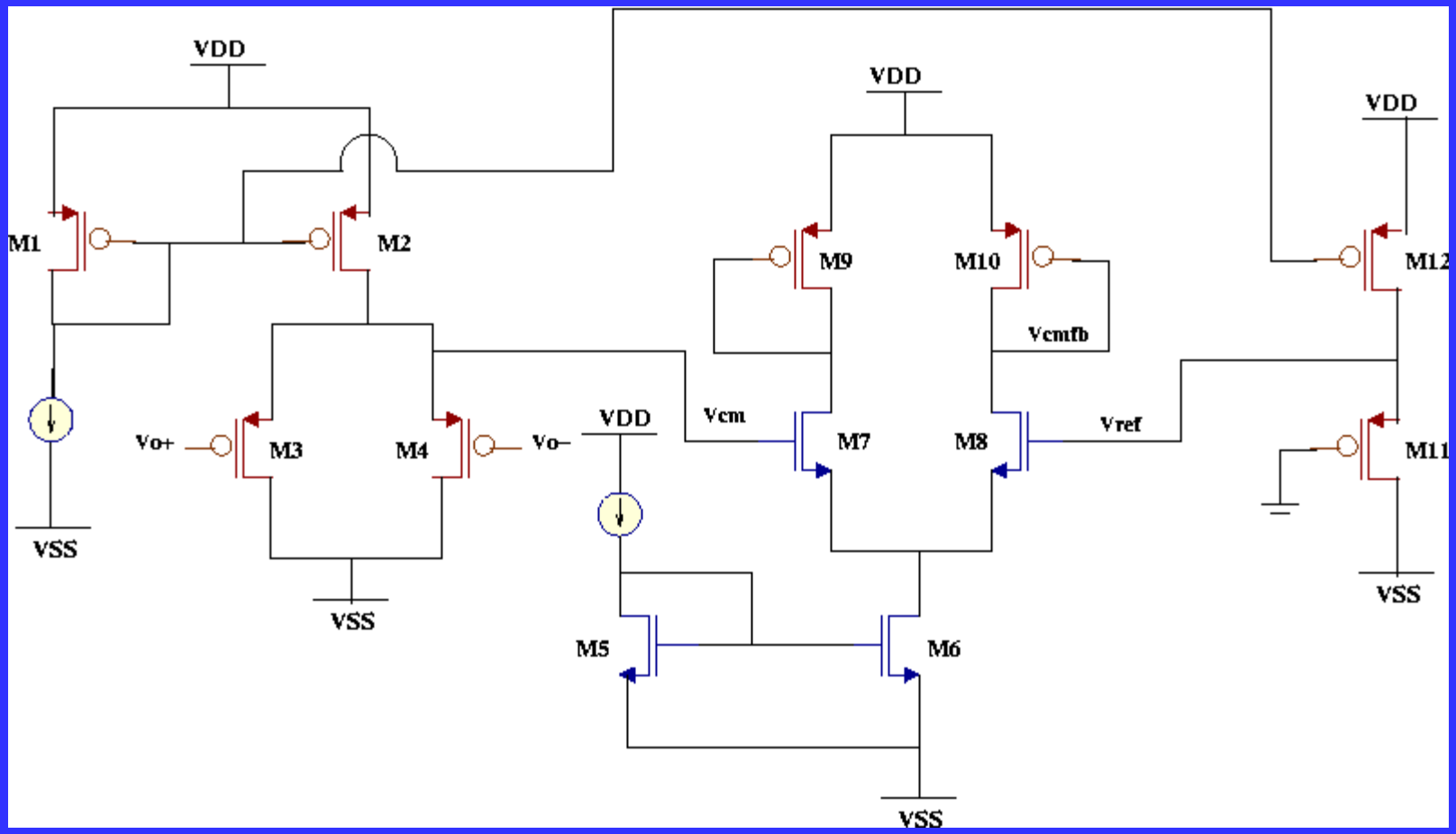


First stage - High gain telescopic cascode



Second and feedforward stage Differential amplifier

Fully differential amplifier (cont.)



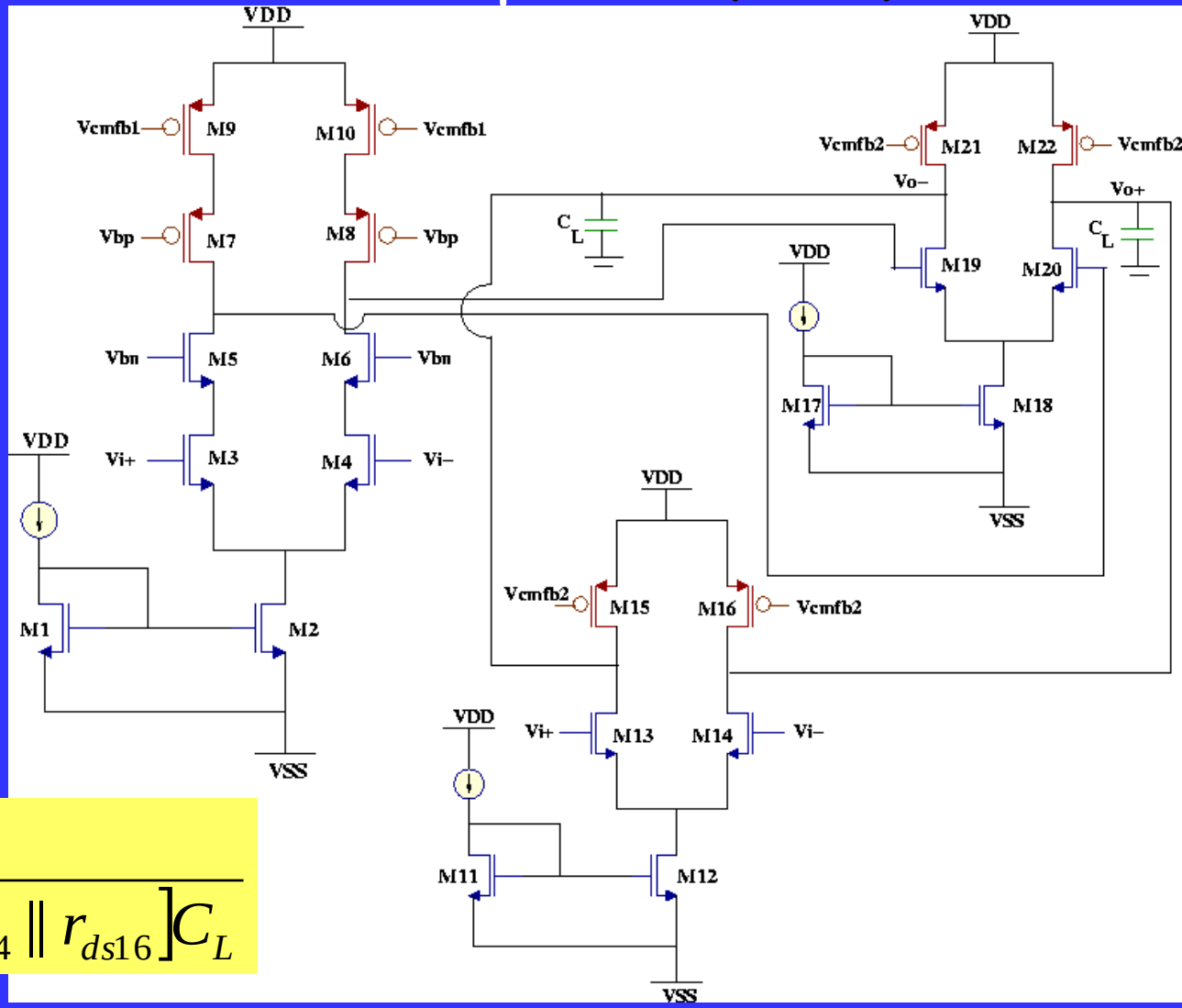
Common-mode feedback for first stage

Fully differential amplifier (cont)

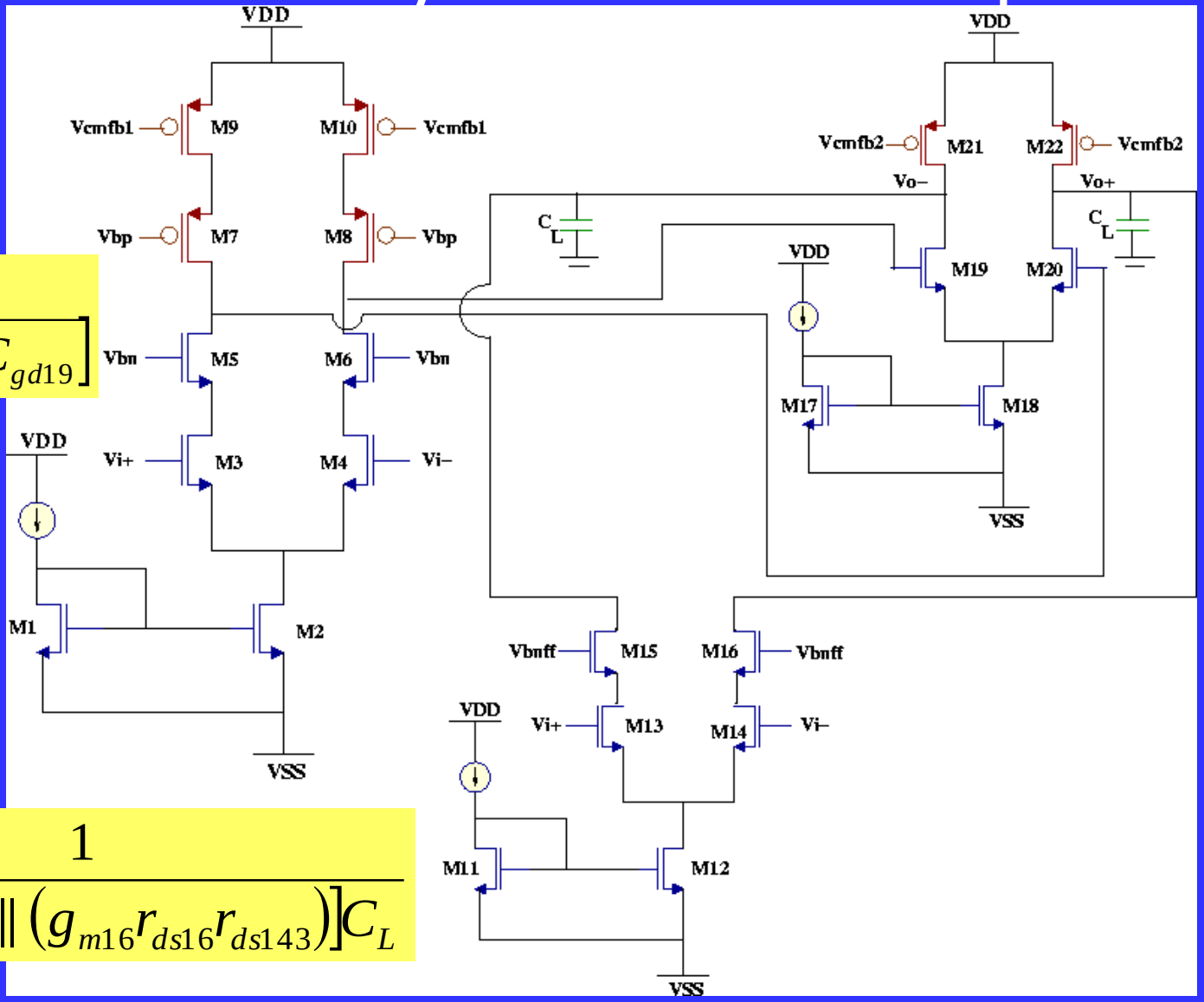
$$\omega_{z1} = \frac{g_{m4}}{\left[C_{gs19} + A_{v2} C_{gd19}\right]}$$

$$\omega_{p2} = \frac{1}{\left[r_{ds22} \parallel r_{ds20} \parallel r_{ds14} \parallel r_{ds16}\right] C_L}$$

$$\omega_{p1} = \frac{1}{\left[\left(g_{m6} r_{ds6} r_{ds4}\right) \parallel \left(g_{m8} r_{ds8} r_{ds10}\right)\right]\left[C_{gs19} + A_{v2} C_{gd19}\right]}$$



Modified fully differential amplifier

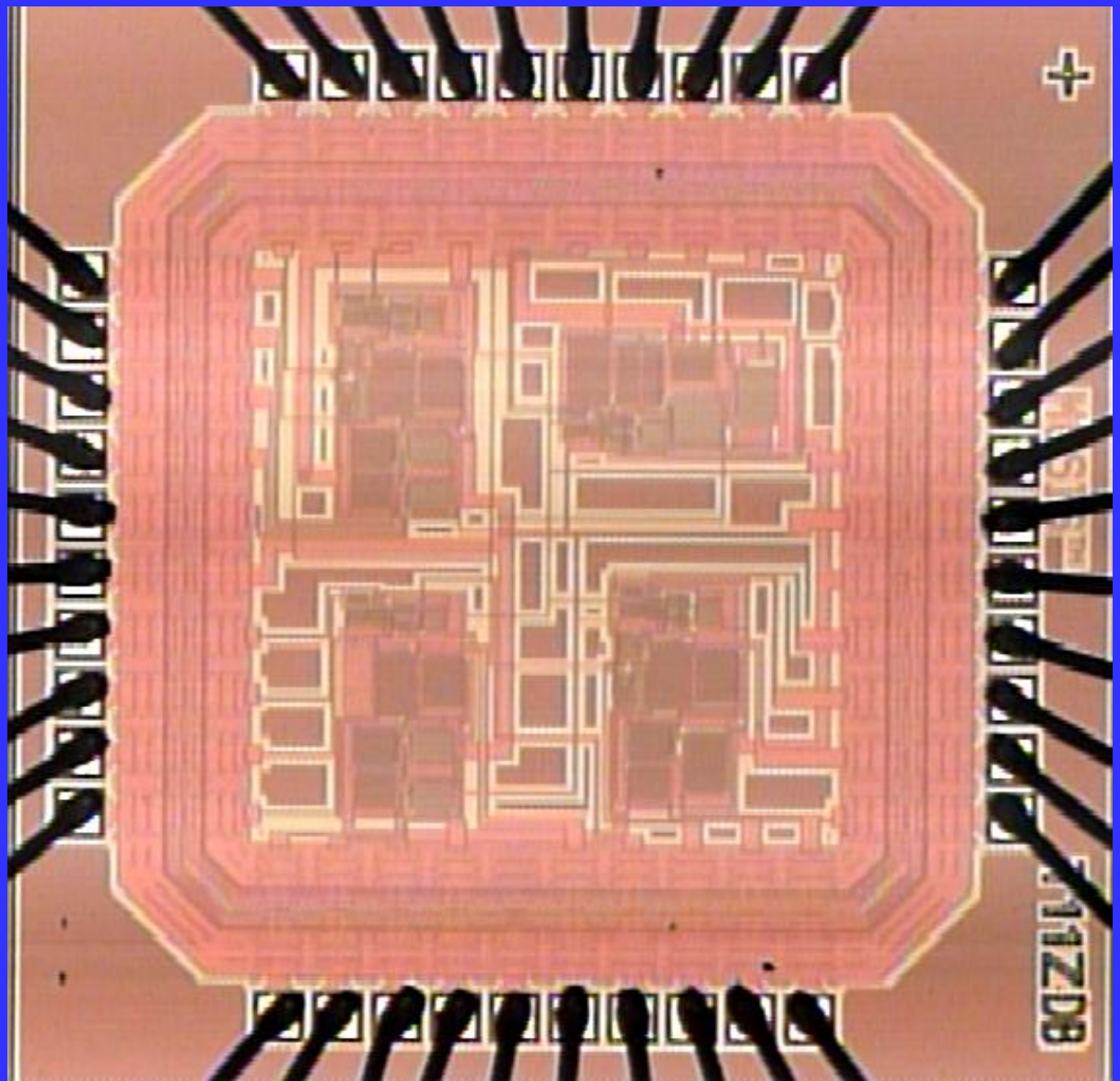


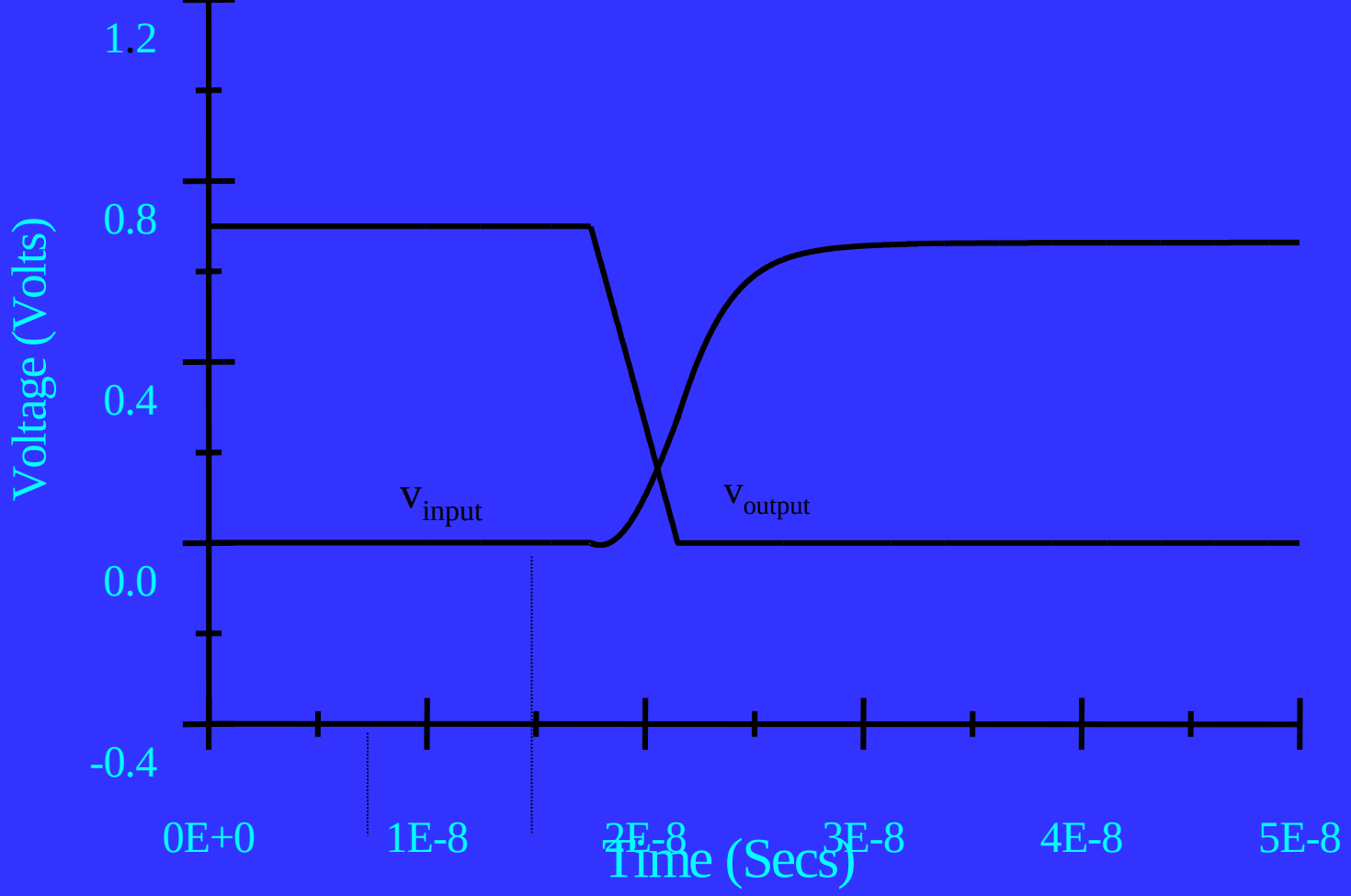
$$\omega_{z1} = \frac{g_{m4}}{\left[C_{gs19} + A_{v2} C_{gd19}\right]}$$

$$\omega_{p2} = \frac{1}{\left[r_{ds22} \parallel r_{ds20} \parallel \left(g_{m16} r_{ds16} r_{ds143}\right)\right] C_L}$$

$$\omega_{p1} = \frac{1}{\left[\left(g_{m6} r_{ds6} r_{ds4}\right) \parallel \left(g_{m8} r_{ds8} r_{ds10}\right)\right]\left[C_{gs19} + A_{v2} C_{gd19}\right]}$$

Chip microphotograph (AMI 0.5µm technology)





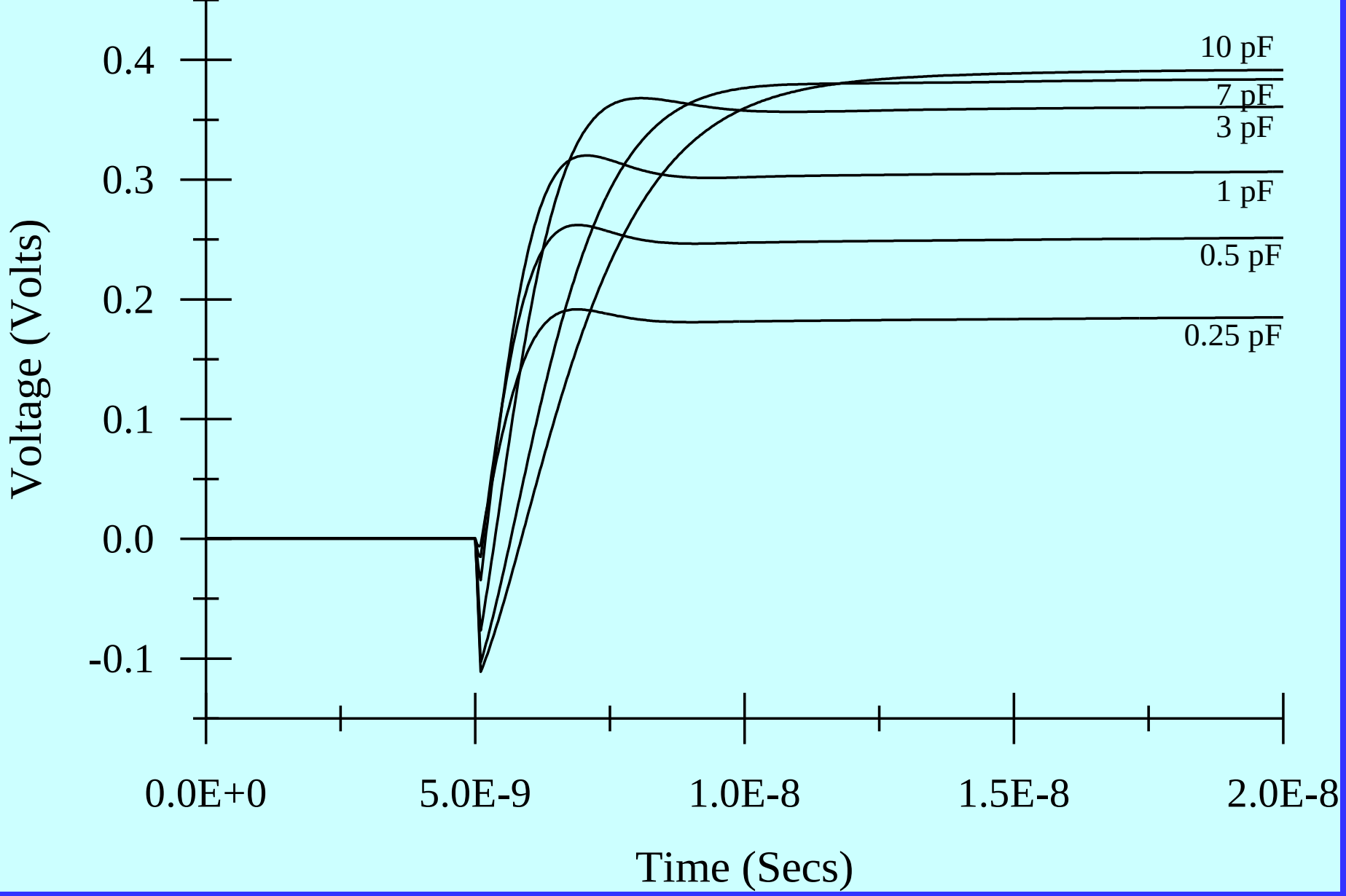
Post-layout simulation results for the capacitive amplifier. Pulse response with a real input signal, including all parasitic capacitors. 1 % settling time is around 14 ns.

Post-layout simulations for OTA's designed in AMI 0.5μm technology

Parameter	Single-ended OTA	Fully differential OTA
DC gain (dB)	94	97
Gainbandwidth (MHz)	300	350
Phase Margin (deg)	74	90
1% settling time (ns) *	6.3	5.1
Current consumption (mA)	5.36	7.16
Power supply	±1.25	±1.25

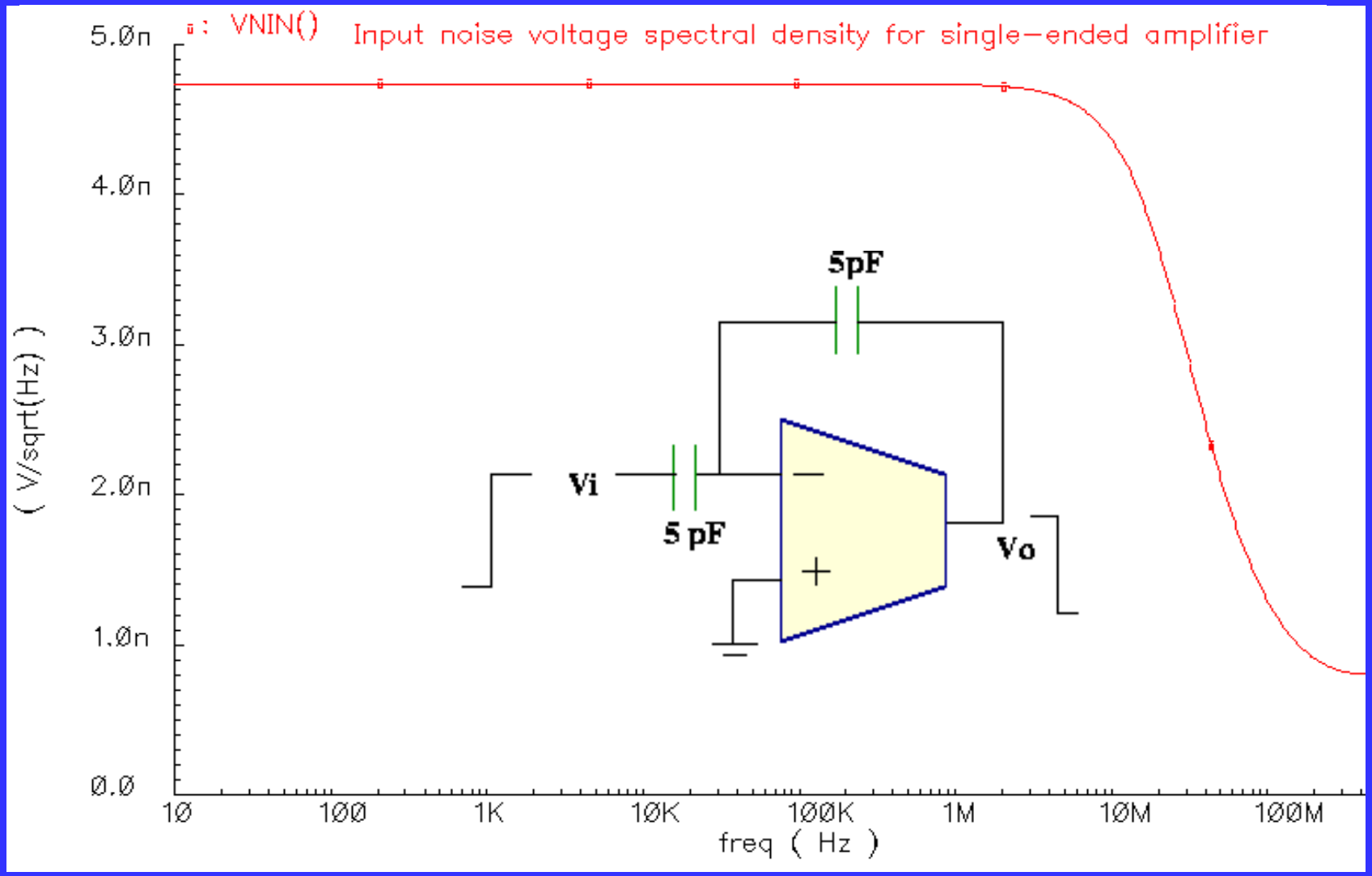
Load capacitor = 12 pF

*** PCB and probe parasitics not included; ideal step input**

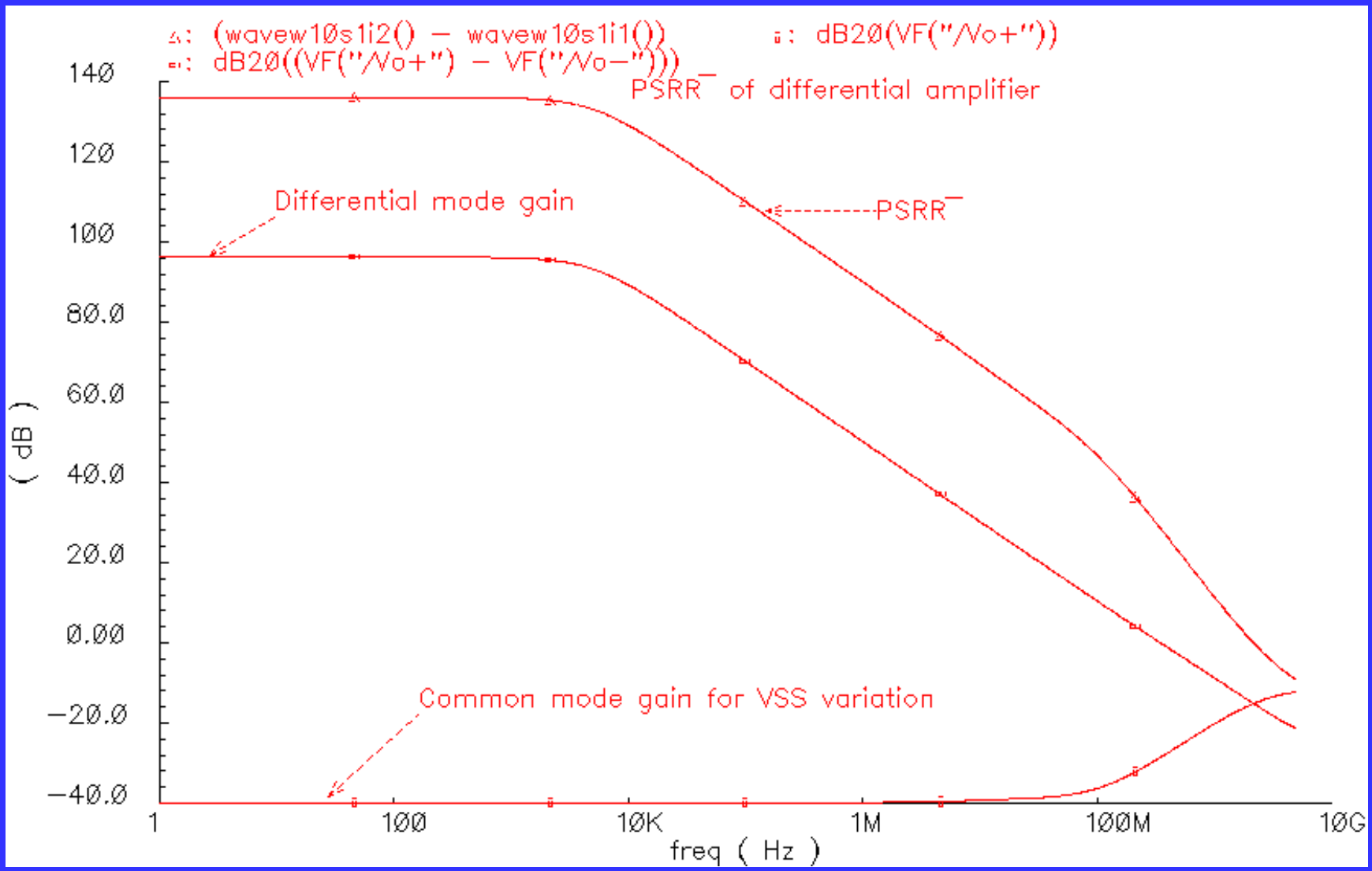


Pulse response post-layout simulation – parametric sweep of feedback and load capacitors.

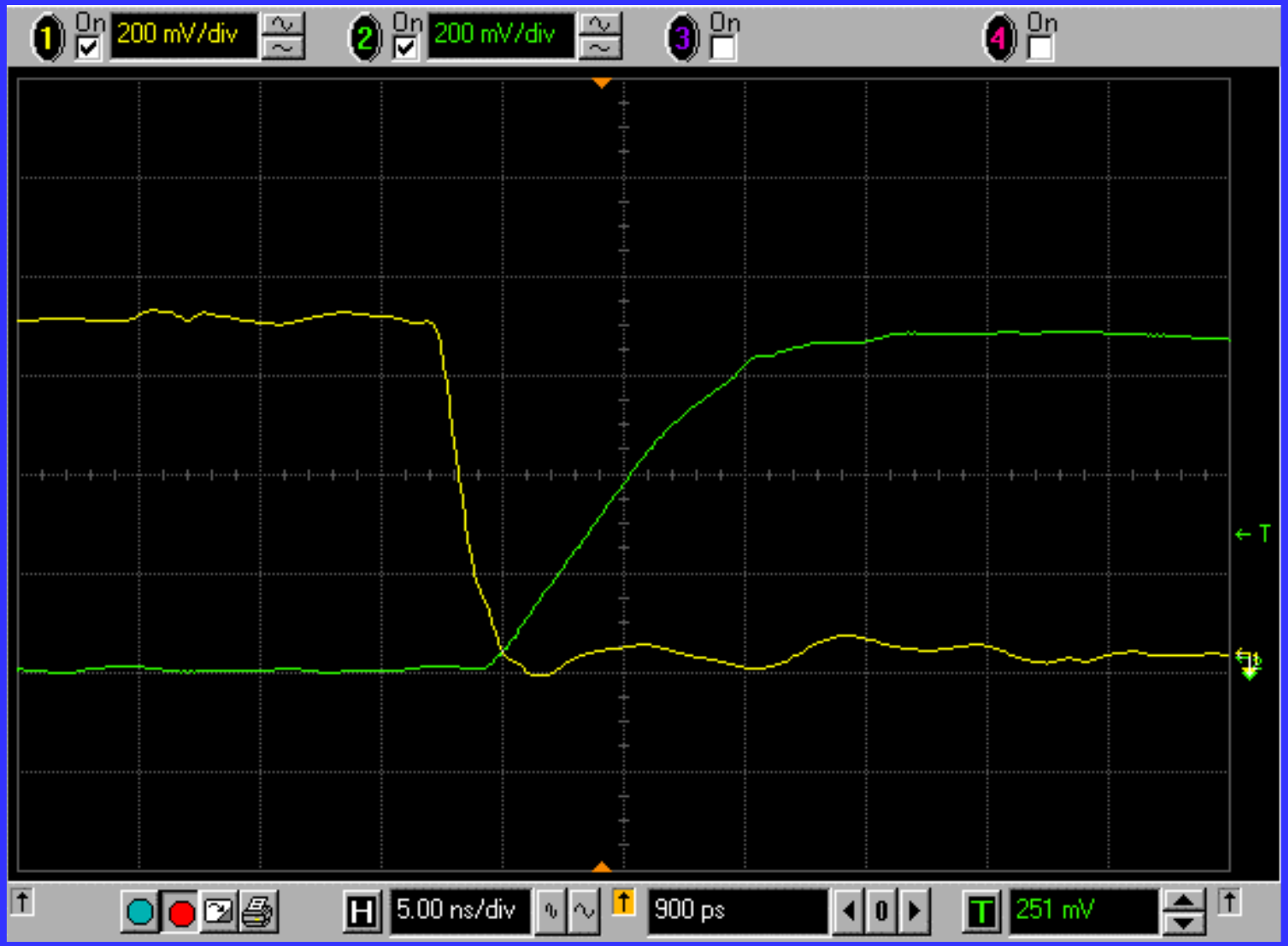
Simulation plots for single-ended amplifier

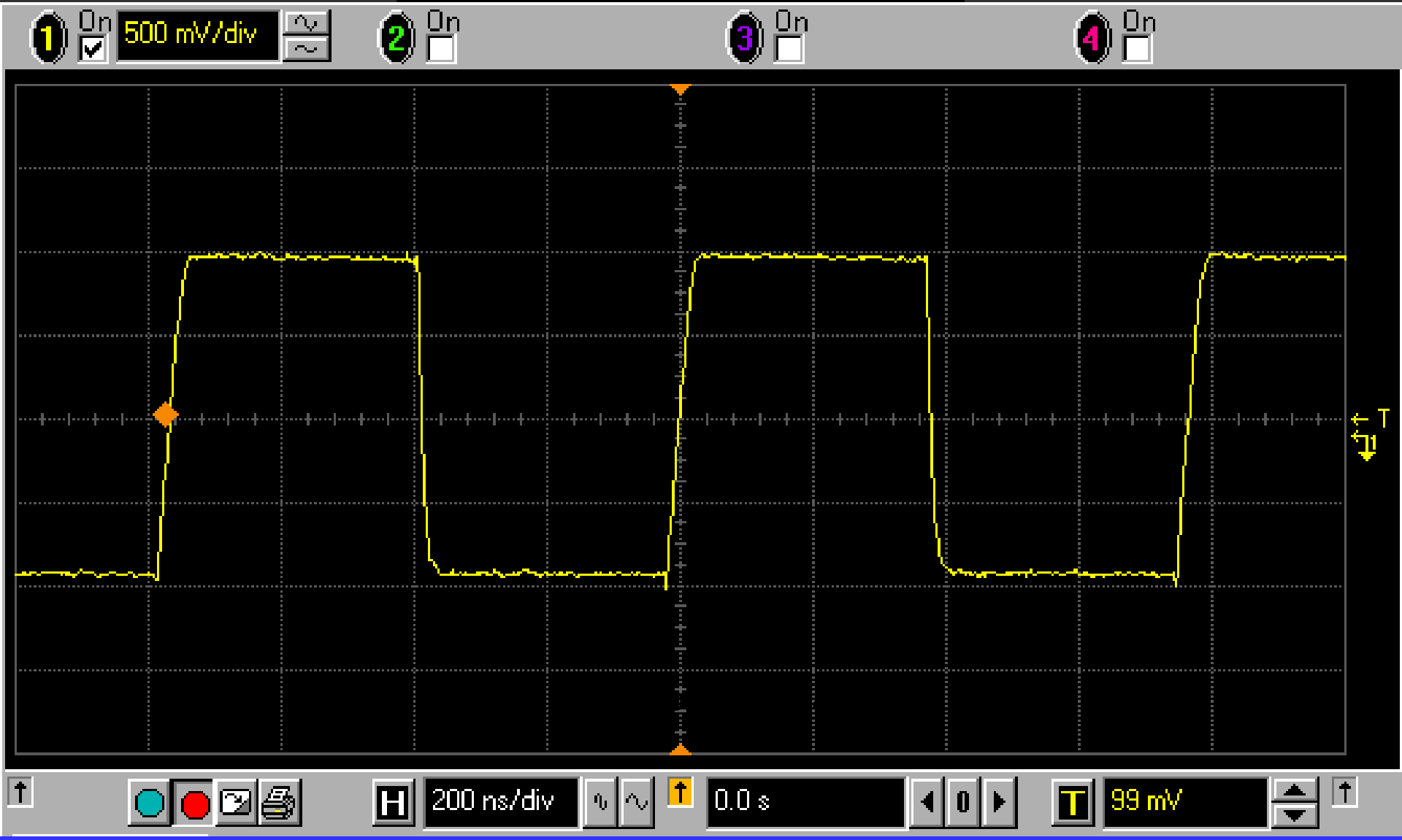


Simulation plots for differential amplifier



Experimental results :Step response of amplifier (Falling step input)




1 On
500 mV/div
2 On
3 On
4 On
T
H
200 ns/div
0.0 s
0
T
99 mV

Remarks

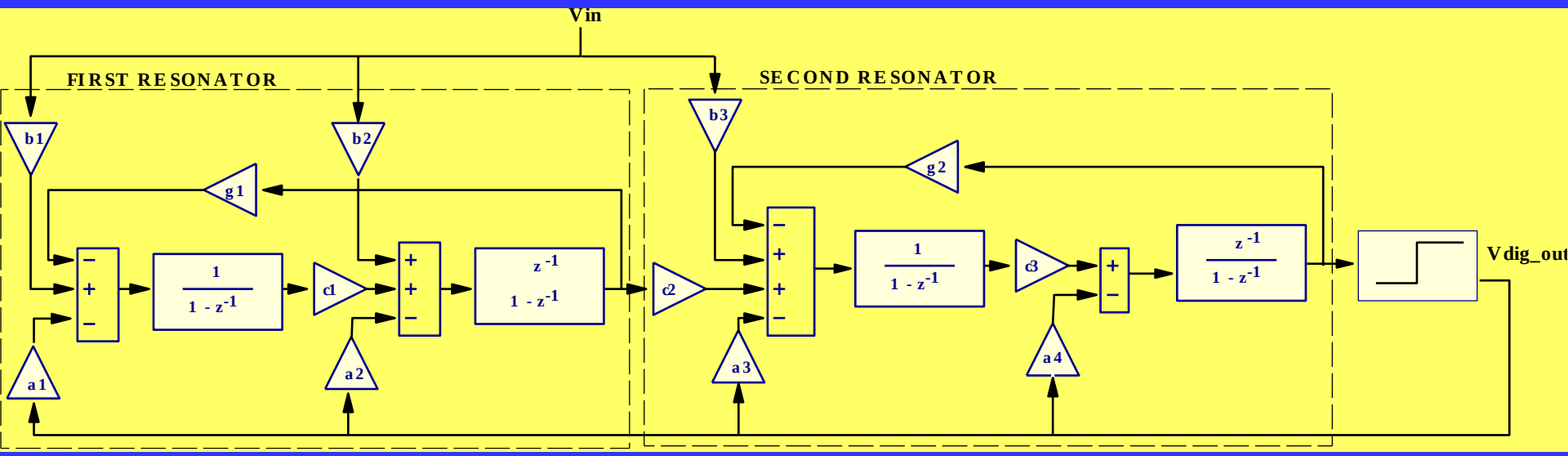
- NCFF compensation scheme for multi-stage amplifiers was presented.
- Compensation scheme uses positive phase shift of LHP zeros to cancel negative phase shift of poles. It combines high gain, GBW and good phase margin
- Other potential optimal NCFF implementations are possible by meeting the poles and number of poles of individual blocks conditions.
- How much saving in power and area versus other schemes such as DFCFC need to be explored

A 92 MHz 80 dB peak SNR SC Bandpass ΣΔ ADC based on NCFF OTA's in 0.35µm CMOS technology

Bharath Kumar Thandri and Jose Silva Martinez
AMSC, Texas A&M University
College Station, Texas
Presented at CICC 2003

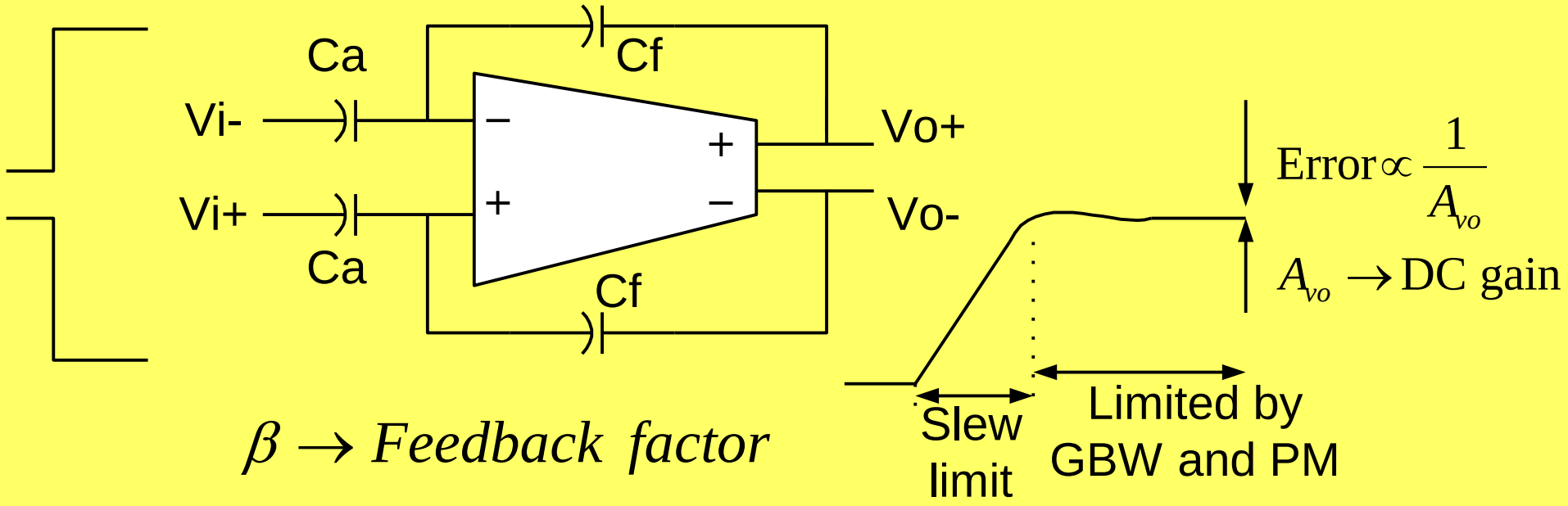
Reference: A 92MHz, 80dB peak SNR SC bandpass Sigma Delta modulator based on a high GBW OTA with no Miller capacitors in 0.35 um CMOS technology
Thandri, B.K.; Martinez, J.S.; Rocha-Perez, J.M.; Wang, J.; Custom Integrated Circuits Conference, 2003. Proceedings of the IEEE 2003 , 21-24 Sept. 2003 Pages:123 - 126

Modulator architecture



- 4th order cascade of resonators in feedback
- Resonator – inverting and non-inverting integrator with local feedback
- For stability, out-of-band gain of NTF =1.5
- Simulations in Matlab/Simulink
- Signal swing, capacitance spread and SNR

Amplifier requirements



$$\frac{\beta \omega_{GBW}}{2} > 5 f_{clock} \qquad \omega_{GBW} \rightarrow Gain\ bandwidth$$

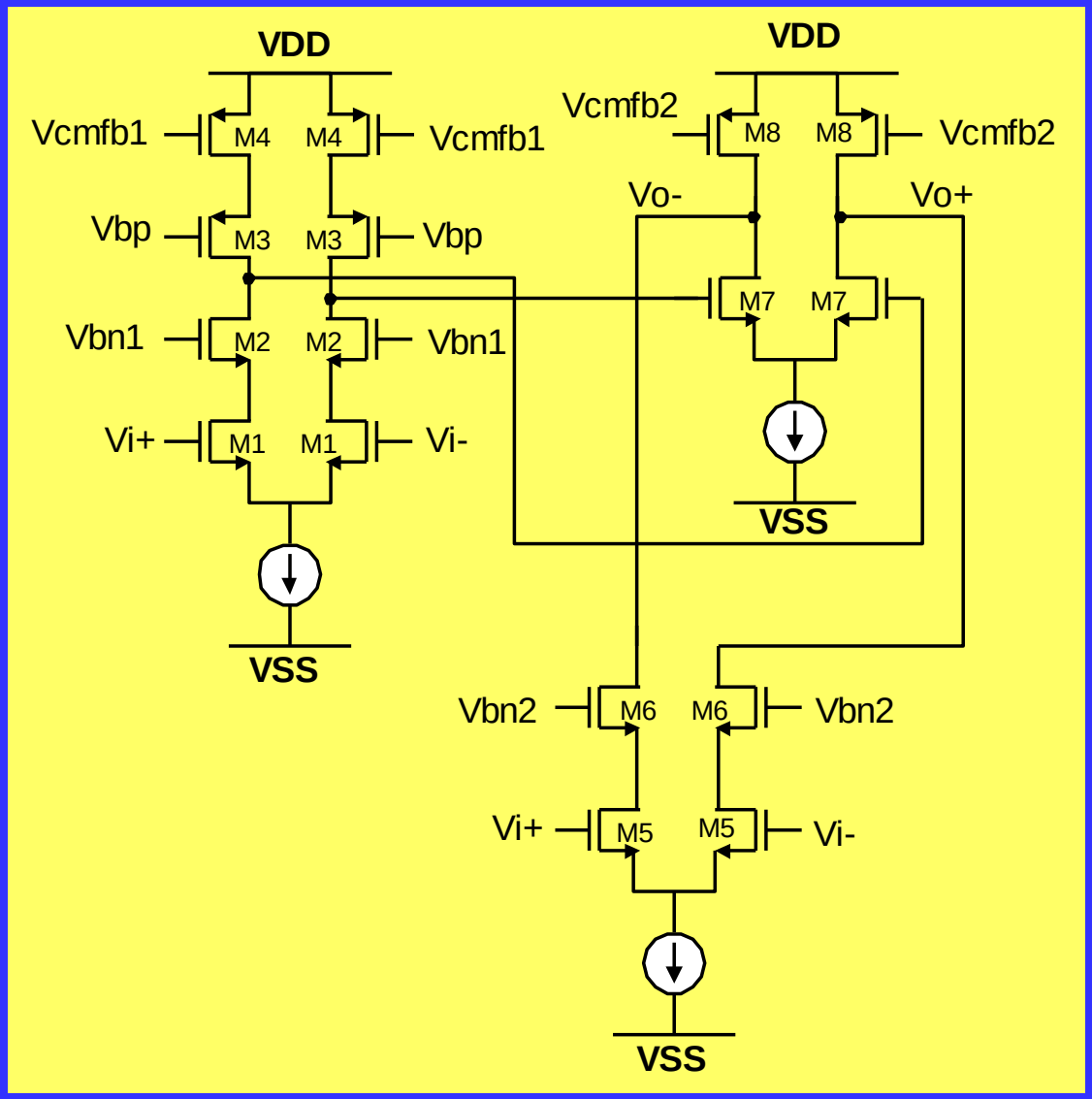
$$f_{GBW} > \frac{10 f_{clock}}{2\pi\beta}$$

- Amplifier non-idealities : Finite DC gain and GBW
- Gain > 70 dB and GBW > 1 GHz for fs =100 MHz and SNR > 85 dB

Amplifier design

- Two stage amplifier with NCFF compensation scheme
- First stage : High gain stage
- Second and Feedforward stage : Medium gain and high BW
- Pole-zero cancellation at high frequencies

Amplifier (final version)



- Use cascode in FF stage
- Conventional CMFB for both stages
- CMFB capacitors increase loading at output
- Bias network to fix Vg of M2,M3 and M6
- Currents

  First stage = 100 μA

  Second stage = 1.25 mA

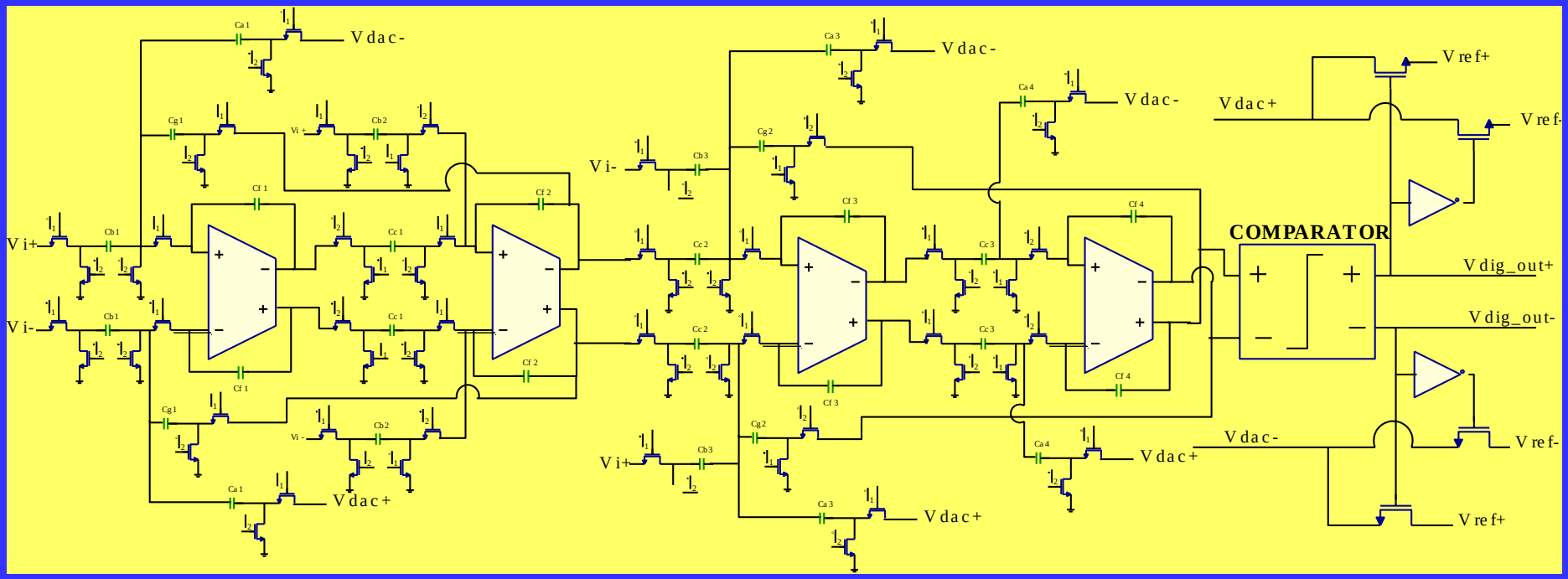
  FF stage = 3.25 mA

Amplifier performance

Parameter	CICC 2002 [*]	This design
DC gain	61 dB	80 dB
GBW	430 MHz	1.4 GHz
Phase margin	61°	62°
Current	9 mA	4.6 mA
Settling time (C_{LOAD})	N/A	2 ns (2pF)
Architecture	Single-stage folded cascode	Two-stage with NCFF scheme
Technology	0.35µm CMOS	0.35µm CMOS

[*] **T. *Salo et al,* "An 80 MHz 8th-order bandpass ΔΣ modulator with a 75 dB SNDR for IS-95 ", CICC, May 2002**

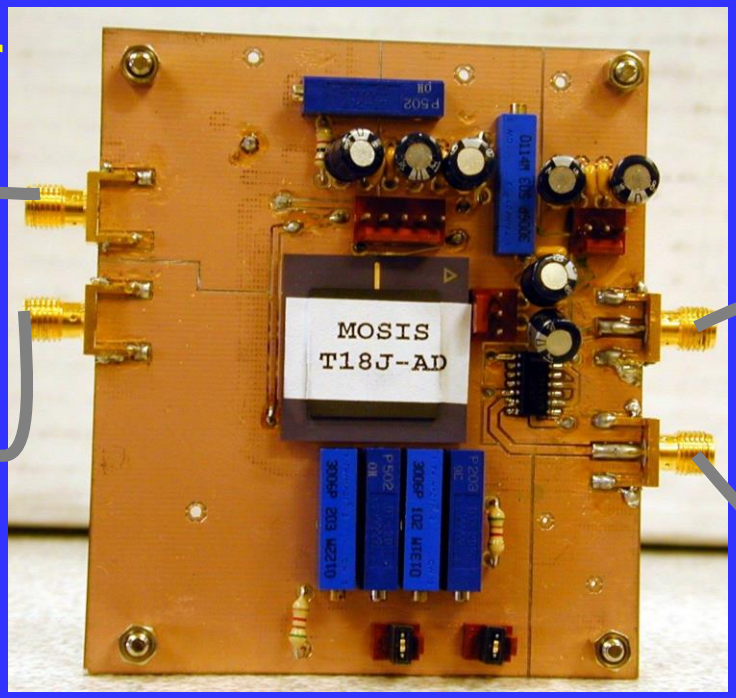
4th order Modulator



- Two-stage latched comparator
- Single-bit DAC – inherently linear
- NMOS switches with boosted clock voltage (2.5V)
- RC time constant of switches limit the speed of operation

Measurement setup

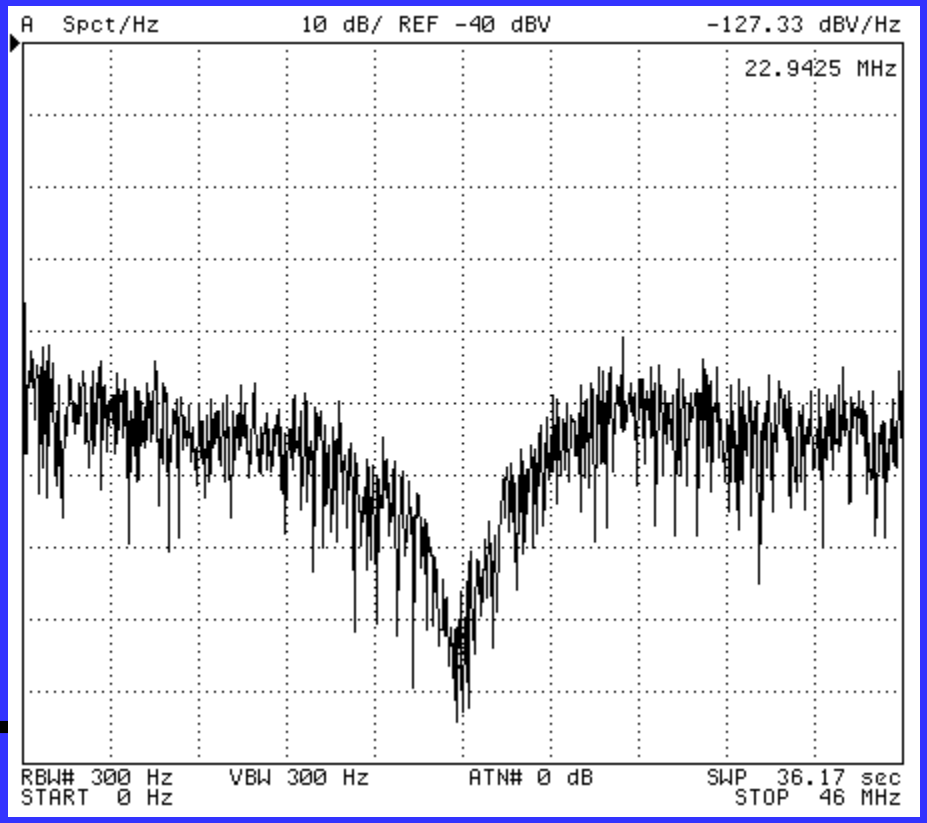
Signal generator



Spectrum analyzer

- Output bit stream is directly injected into spectrum analyzer
- SNR measurement is a conservative estimate as it includes noise in the bit stream
- Modulator works properly @110 MHz clock
- SNR degrades for fs > 92 MHz

Measurement results



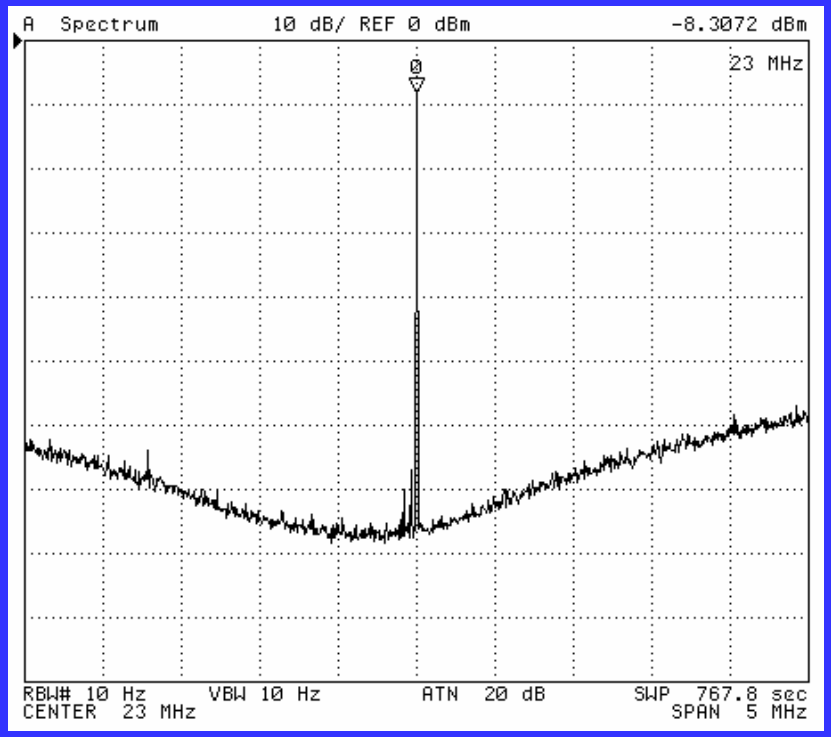
-127 dBV / Hz

0 Hz **23 MHz** **46 MHz**

- Noise floor is measured by grounding inputs
- Includes quantization and circuit (kT/C) noise
- Fs = 92 MHz

Output spectrum

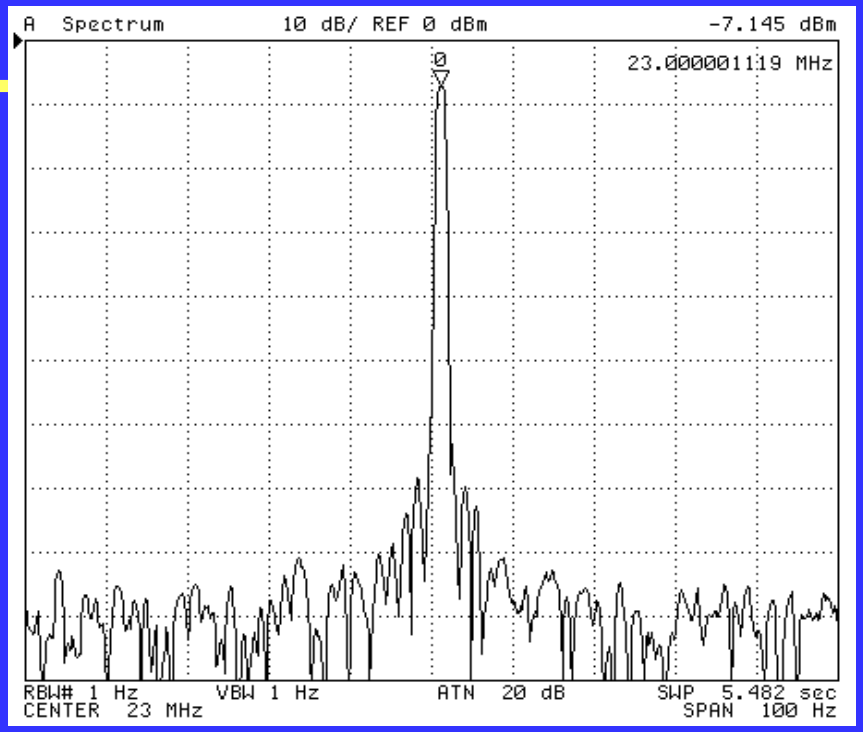
5 MHz span



23 MHz

-7.1 dBm

100 Hz span

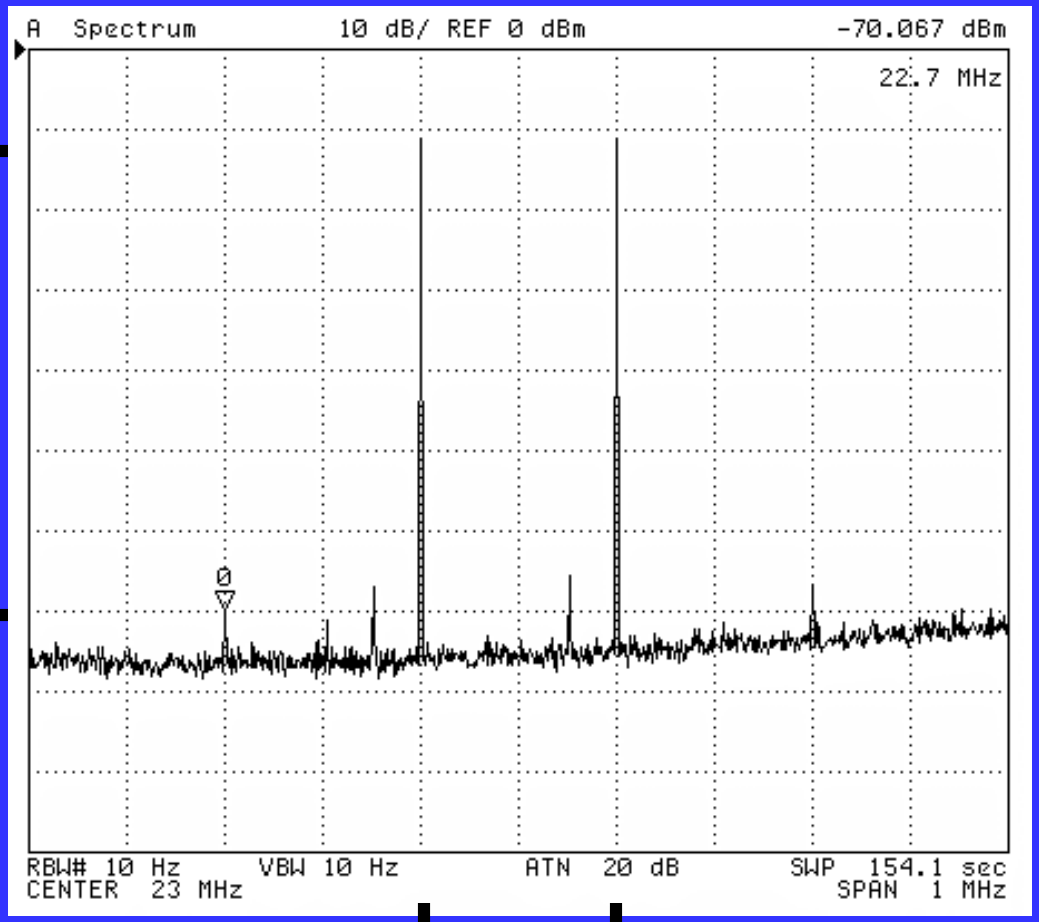


23 MHz

$$SNR = \frac{Signal\ \ power}{\int_{BW} Noise\ power}$$

SNR = 80 dB (270 kHz)
SNR = 54 dB (3.84 MHz)
Fs = 92 MHz

Two tone IMD test



-12 dBm

-70 dBm

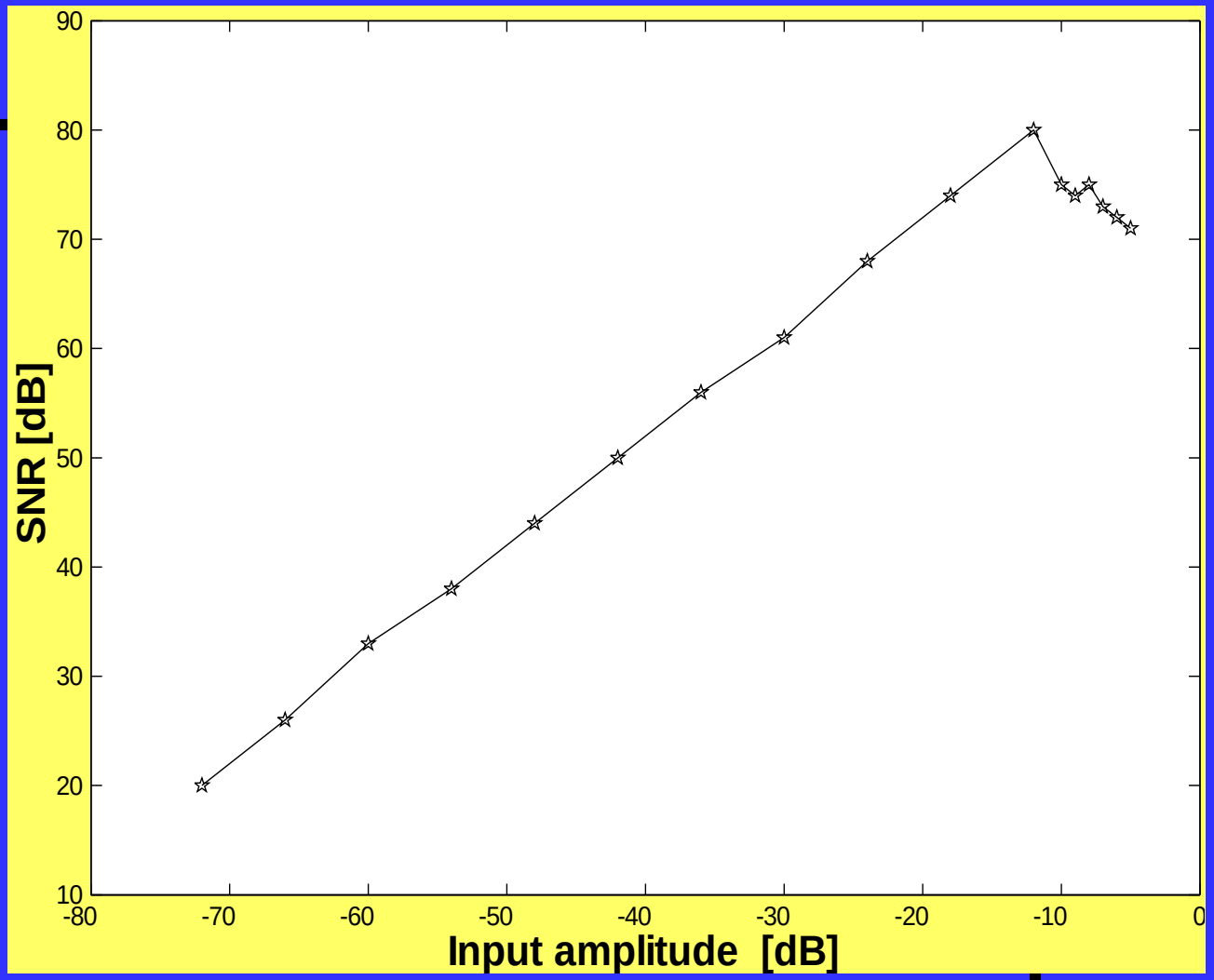
22.9 MHz

23.1 MHz

- Two tone input @ -11 dBr, 23.1 and 22.9 MHz
- Measured IMD3 = -58 dB

Plot of SNR vs input amplitude

80 dB



-12 dB

Performance summary of the modulator

Technology	TSMC 0.35μm CMOS
Peak SNR for 270 KHz BW	80 dB
Peak SNR for 3.84 MHz BW	54 dB
IMD3 @ -11dBr input	-58 dB
Supply voltage	±1.25V
Power consumption	47.5 mW
Sampling frequency	92 MHz
Core area	1.248 mm^2

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