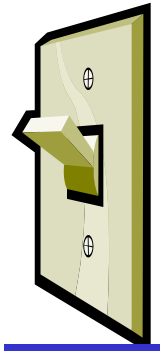
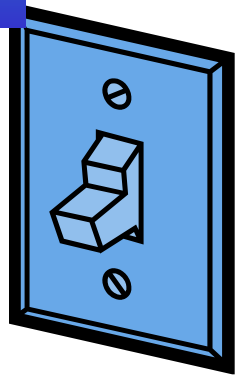


Switched-Capacitor Circuit Implementations

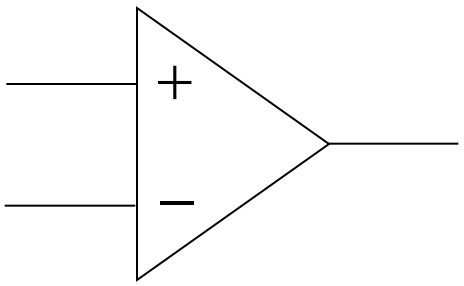
- SC Biquads: Block Diagram Representations and Implementations
- SC Techniques for reduced area and high Q-filters
- Other SC applications



PRACTICAL CONSIDERATIONS FOR OP AMPS

Key op amp specifications:

- Gain
- Speed (BW)
- Supply voltages
- Output swing
- Noise
- Power



NON-IDEAL EFFECTS OF OP AMPS

A. FINITE DC GAIN

For a two integrator biquadratic filter:

$$\omega_{o_A} = \frac{A_o}{1+A_o}\omega_o \qquad Q_a = \frac{1}{\frac{1}{Q}+\frac{2}{A_o}} \cong \left(1-\frac{2Q}{A_o}\right)Q$$

Therefore:

- **ω_o deviations are negligible**
- **Q deviations can be significant**

B. FINITE BANDWIDTH

- Bandwidth is very critical for high frequency applications

How to determine the GB of an Op Amp?

- The required GB is a function of the clock frequency and the feedback topology around the Op Amp.
- A rule of thumb to select GB requires to satisfy the following inequality:

$$a\,GB\,T/2 > 5 \quad \text{or}$$

$$GBT > 10/a$$

where T is the period of the clock frequency, a is the capacitor ratio between the sum of all the feedback capacitors divided by the sum of all the capacitors connected to the input terminal of the Op Amp. More details later

MULTI-STAGE OP AMP DESIGN

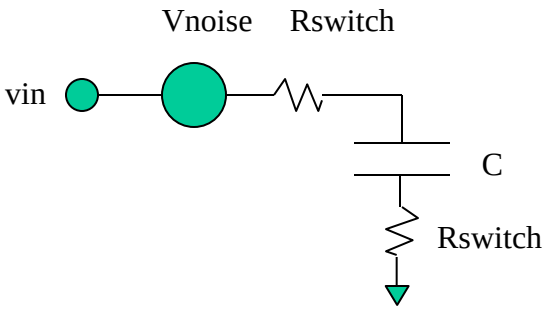
A. SINGLE-ENDED CONFIGURATION

- High gain
- CMRR = 0
- Nested compensation trades BW for stability

B. FULLY DIFFERENTIAL CONFIGURATION

- High gain
- Good CMRR
- Rail-to-rail output swing
- Higher bandwidth (less compensation)
- Requires and additional CMFB and dynamic reset

Noise due to the switches



- The switch noise density can be expressed as

$$v_{sw,noise}^{\ 2} = 4kTRswitch$$

- Because two switches are present

$$v_{sw,total}^{\ 2} = 8kTRswitch \int_{BW} df = \frac{4kTRswitch}{\pi RswitchC}$$

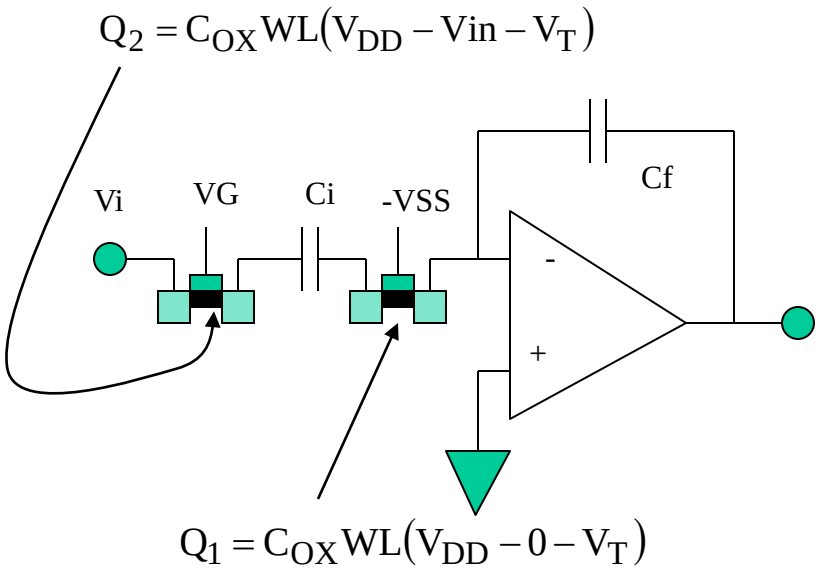
or

$$v_{sw,total} = \sqrt{\frac{4kT}{\pi C}}$$

$4kT=16x10^{-21}V^2C$

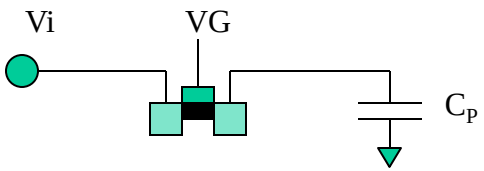
For C=1 pF the noise level is around 70 μV

C=10 pF ==> noise level is around 20 μV



Basic principle

It is a matter of parasitic capacitances



Clock Feedthrough

➧The charge in the channel is

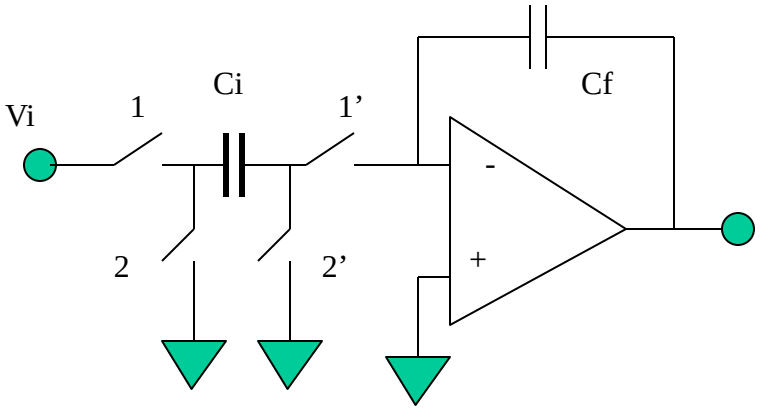
$$Q_{channel} = C_{OX}WL(V_{GS} - V_T)$$

When the switch is opened the channel charge, ideally, should be injected to v_{in}, otherwise an error proportional to Q-channel is induced.

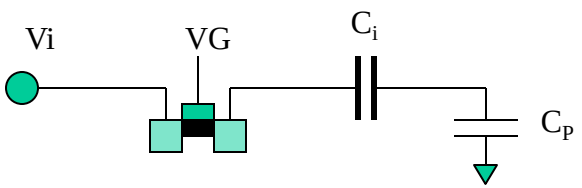
If CP is small, then few electrons charge the capacitor at lower voltage, then rejecting the electrons. Then most of the charge is absorbed by the previous stage.

IMPLEMENTATION

Minimization of Clock Feedthrough



The right hand side switches are opened before the others



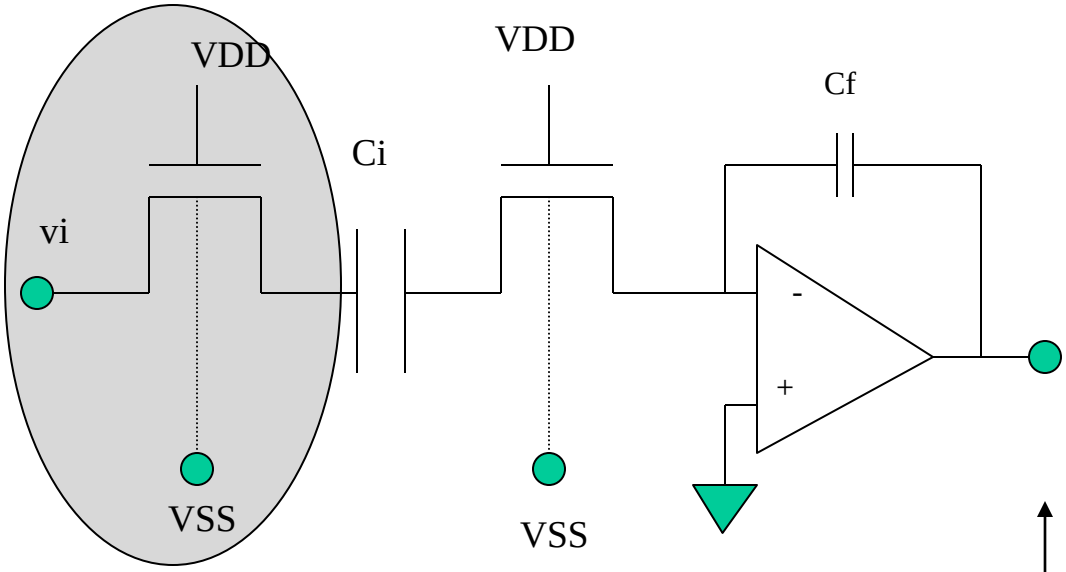
- switches 1' and 2' can be implemented with only n-channel and should be turn off before switches 1 and 2.

Error is minimized using these early clock phases

Reference.

D. A. Johns and K. Martin, " Analog Integrated Circuit Design" Chapter 10

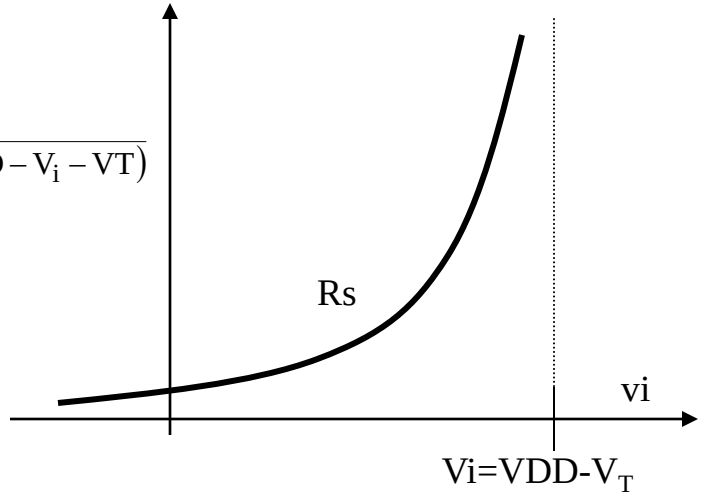
Switch Resistance



Body effect

$V_T = V_{T0} + \Delta V$

$$Rs = \frac{L}{\mu_n C_{OX} W (VDD - V_i - VT)}$$



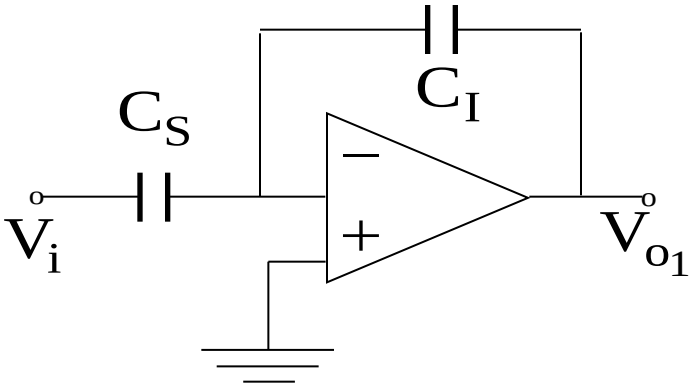
For VDD=1.5 V, and V_T=1 ==> Vi<0.5 V !!!

And for VDD=0.75 V ?

BASIC BUILDING BLOCKS

A. GAIN AMPLIFIERS

Basic Configuration:

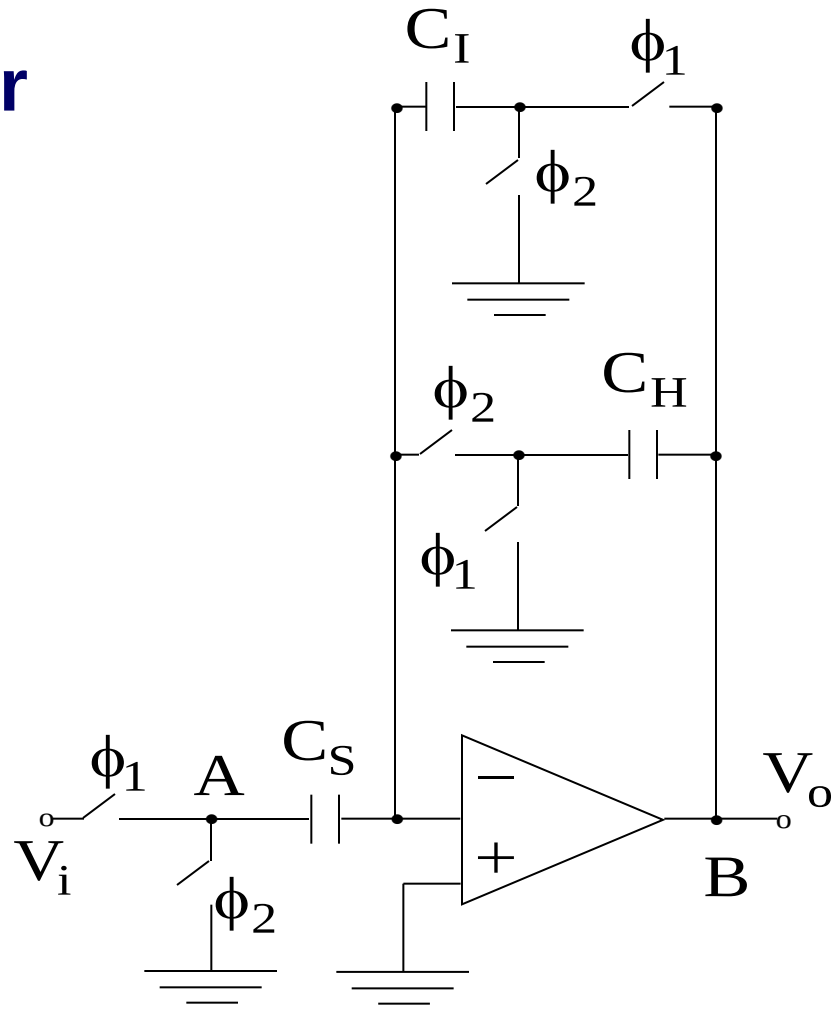


- Compact, versatile & time continuous
- Lacks dc feedback
  - Op amp is not stabilized
  - Leakage current saturates the circuit

$$\text{Gain} = -\frac{C_S}{C_I}$$

Improved Gain Amplifier

- Low sensitivity to the op amp offset voltage and open loop gain (due to charge cancellation
- Additional capacitor between nodes A and B eliminates the "spikes" during the non-overlapping clock phases

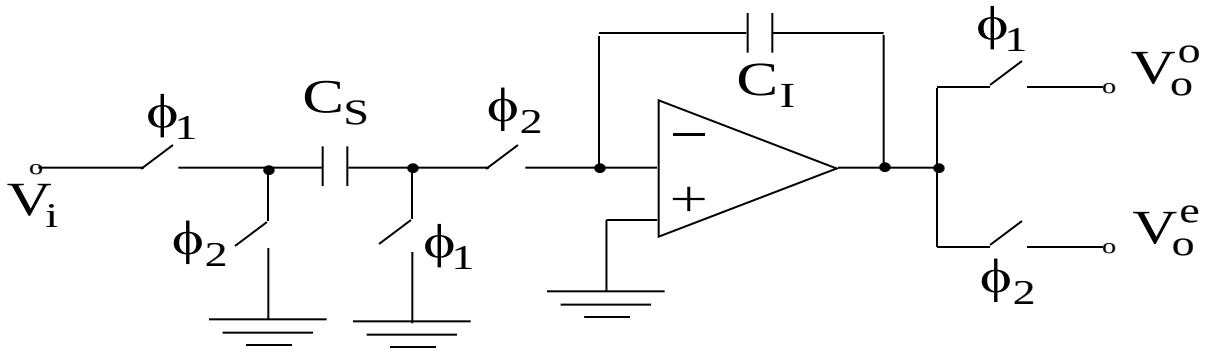


$$\text{gain} = -\frac{C_S}{C_I}$$

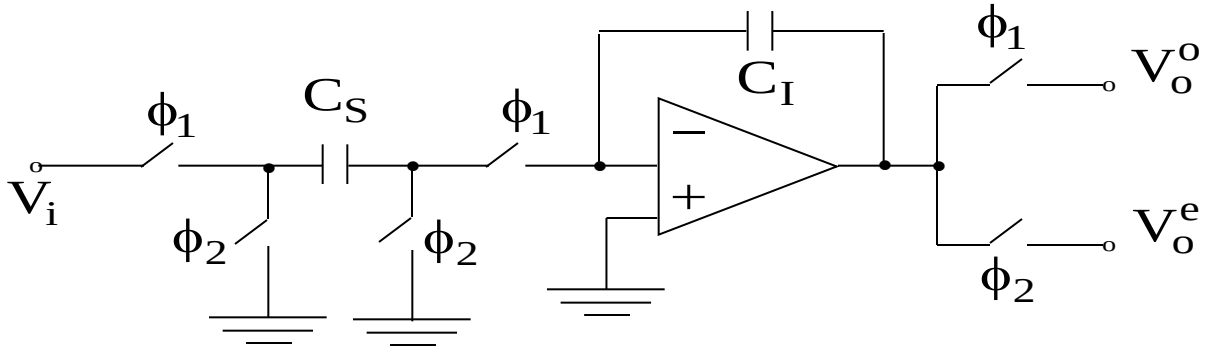
B. Integrators

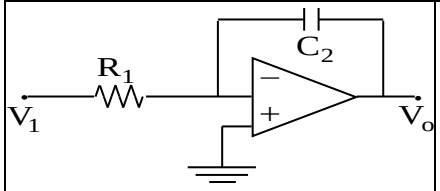
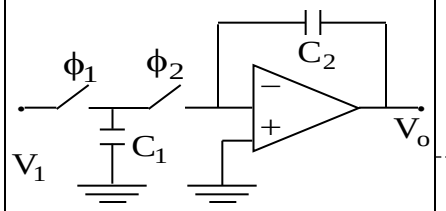
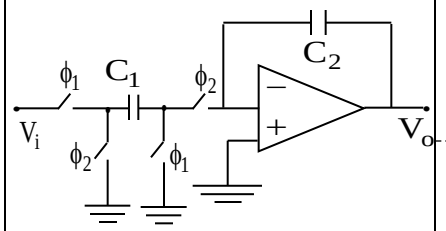
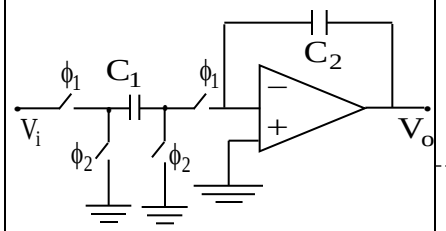
Conventional stray-insensitive integrators:

- Non-inverting:

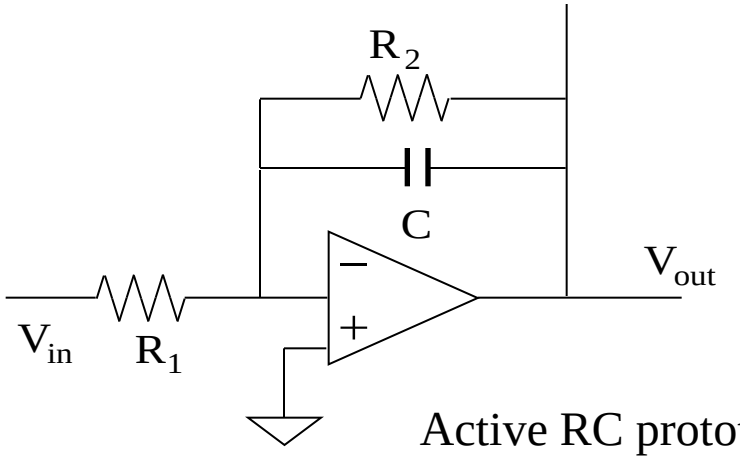


- Inverting:



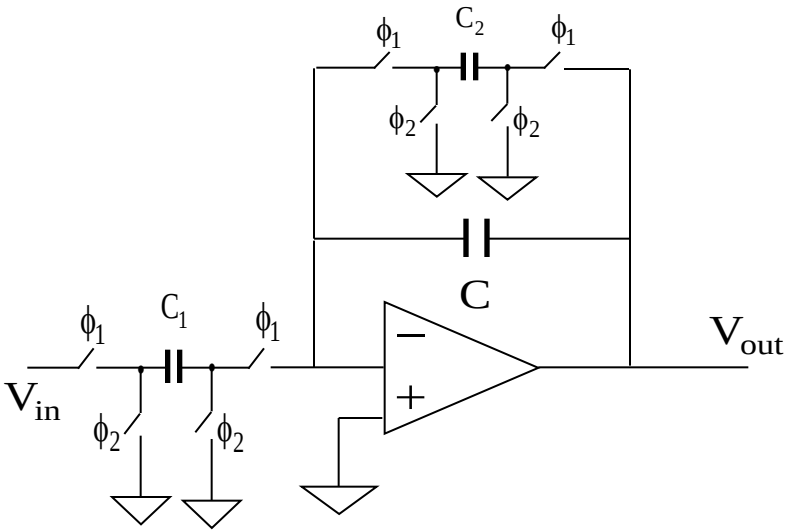
Type of Integrator	Magnitude, $\left\|H(e^{j\omega T})\right\|$	Phase, $A_{RG}H(e^{j\omega T})$	Mapping (Equivalent)	Transfer Function
	$\frac{\omega_o}{\omega}$	$\frac{\pi}{2}$	In the S-Plane	i.e. $H(S)=\frac{1}{SR_1C_2}=-\frac{\omega_o}{S}$
 Inverting (Forward)	For V_o at ϕ_2 $\frac{\omega_o}{\omega}\left(\frac{\omega T/2}{\sin(\omega T/2)}\right)$	$\frac{\pi}{2}$	LDI	$H(Z)=-\frac{C_1}{C_2}\left(\frac{Z^{-1/2}}{1-Z^{-1}}\right)$
	For V_o at ϕ_1 $\frac{\omega_o}{\omega}\left(\frac{\omega T/2}{\sin(\omega T/2)}\right)$	$\frac{\pi}{2}-\frac{\omega T}{2}$	Forward	$H(Z)=-\frac{C_1}{C_2}\left(\frac{Z^{-1}}{1-Z^{-1}}\right)$
 Non-Inverting	For V_o at ϕ_2 $\frac{\omega_o}{\omega}\left(\frac{\omega T/2}{\sin(\omega T/2)}\right)$	$-\frac{\pi}{2}$	LDI	$H(Z)=\frac{C_1}{C_2}\left(\frac{Z^{-1/2}}{1-Z^{-1}}\right)$
	For V_o at ϕ_1 $\frac{\omega_o}{\omega}\left(\frac{\omega T/2}{\sin(\omega T/2)}\right)$	$-\frac{\pi}{2}-\frac{\omega T}{2}$	Forward	$H(Z)=-\frac{C_1}{C_2}\left(\frac{Z^{-1}}{a-Z^{-1}}\right)$
 Inverting (Backward)	For V_o at ϕ_2 $\frac{\omega_o}{\omega}\left(\frac{\omega T/2}{\sin(\omega T/2)}\right)$	$\frac{\pi}{2}+\frac{\omega T}{2}$	Backward	$H(Z)=-\frac{C_1}{C_2}\left(\frac{1}{1-Z^{-1}}\right)$
	For V_o at ϕ_1 $\frac{\omega_o}{\omega}\left(\frac{\omega T/2}{\sin(\omega T/2)}\right)$	$\frac{\pi}{2}$	LDI	$H(Z)=-\frac{C_1}{C_2}\left(\frac{Z^{-1/2}}{1-Z^{-1}}\right)$

Basic SC first-order low-pass



Active RC prototype

$$H(s) = \frac{-R_2 / R_1}{1 + sCR_2}$$



$$R_{eq} = T / C_i = 1 / C_i f_S \ , \ i = 1,2$$

$$H(z) = \frac{-(C_1 / C)z}{z(1 + C_2 / C) - 1}$$

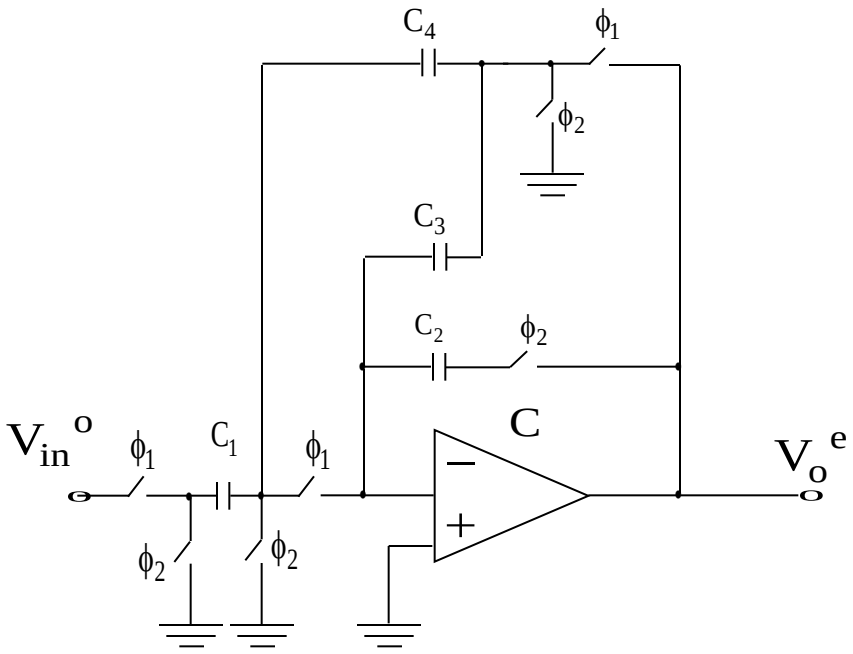
$$Z_{zero} = 0$$

$$Z_{pole} = 1/(1 + C_2 / C)$$

Improved Integrator with reduced capacitance spread

Problem: offset

Solution: use an offset & low dc gain compensated integrator as the 2nd stage (only valid for two-integrator loop applications)

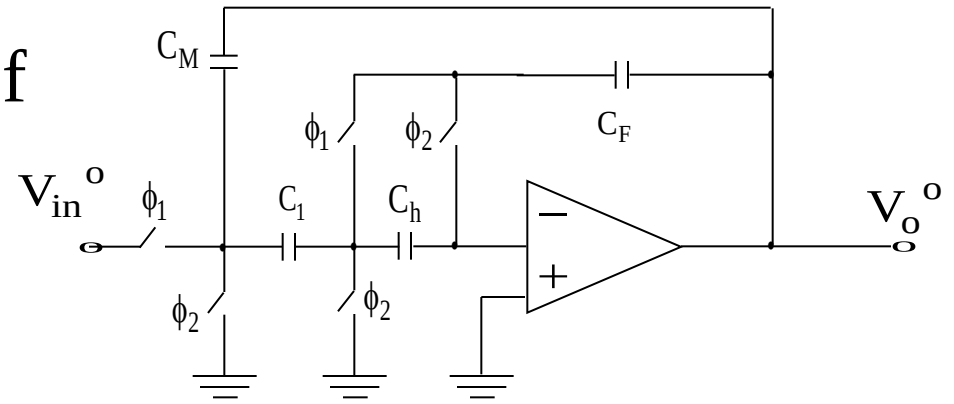


$$H^{oe}(z) = \frac{V_o^e(z)}{V_{in}^o(z)} = -\frac{C_1 C_3}{C_2 C_4^{'}} \frac{1}{1 - z^{-1}}$$

$$C_4^{'} = C_4 + C_3$$

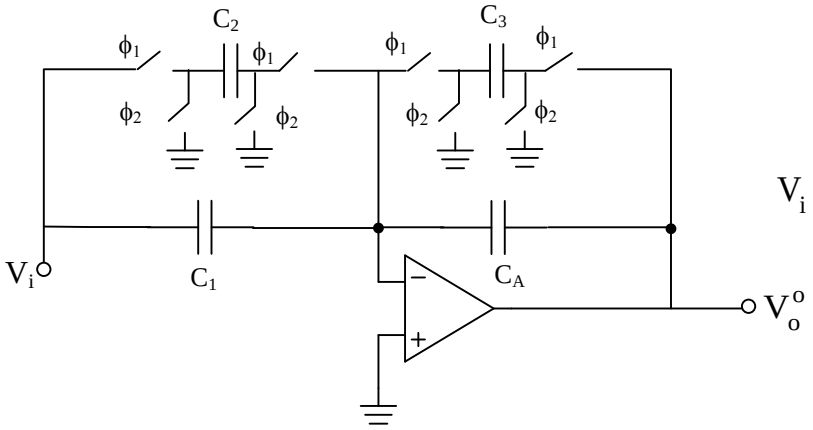
Offset and gain compensated Integrator

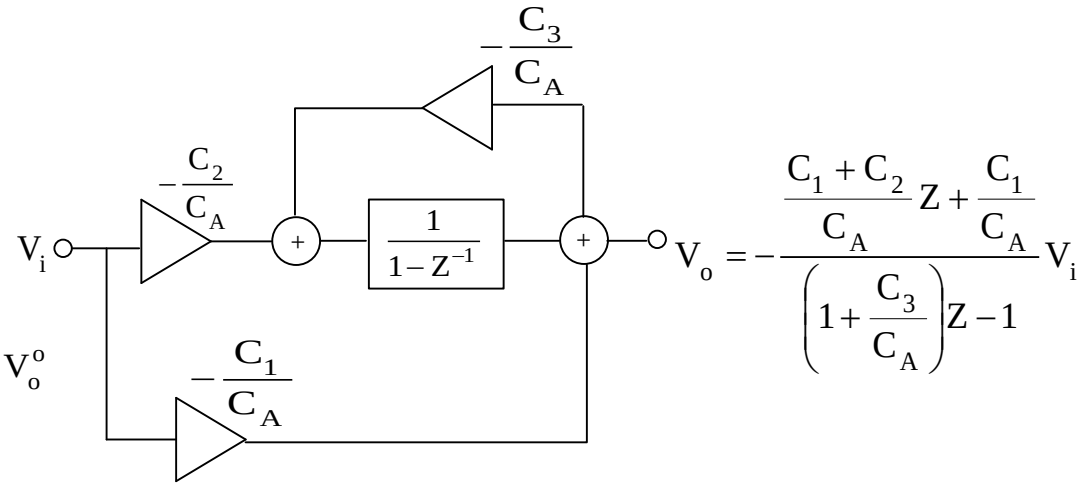
- C_h compensates the offset voltage and dc gain error of the op amp
- C_M eliminates spikes (providing continuous feedback to the op amp)

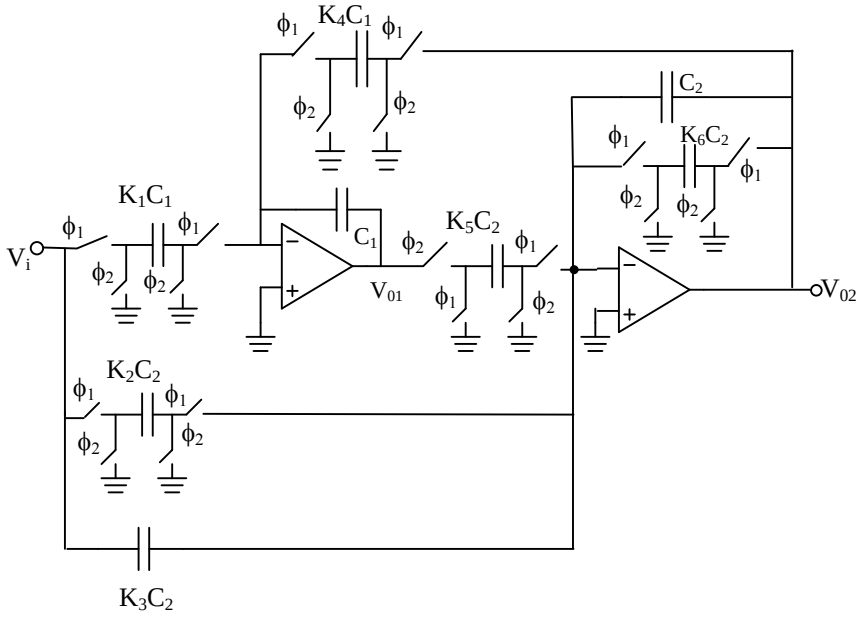


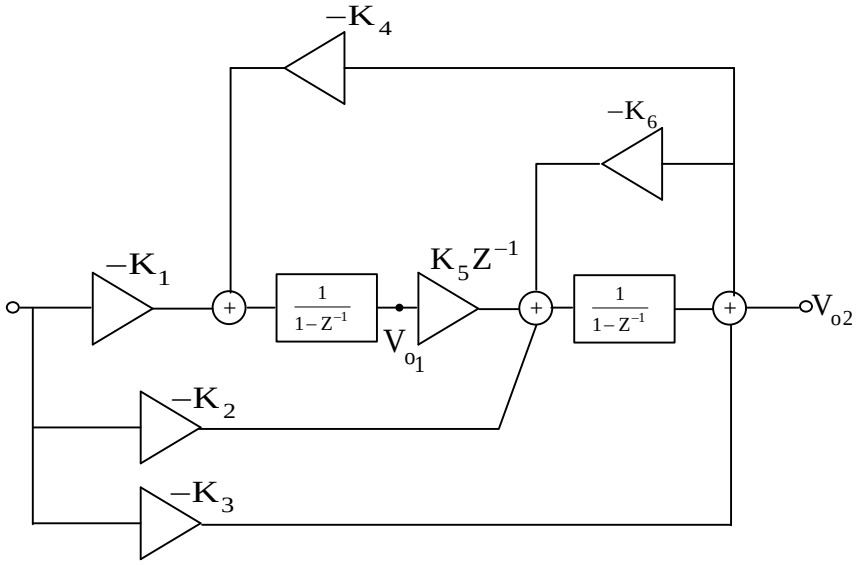
$$H^{oo}(z) = \frac{V_o^{\,o}(z)}{V_{in}^{o}(z)} = -\frac{C_1}{C_F}\frac{1}{1-z^{-1}}$$

SWITCHED-CAPACITOR FILTER IMPLEMENTATIONS



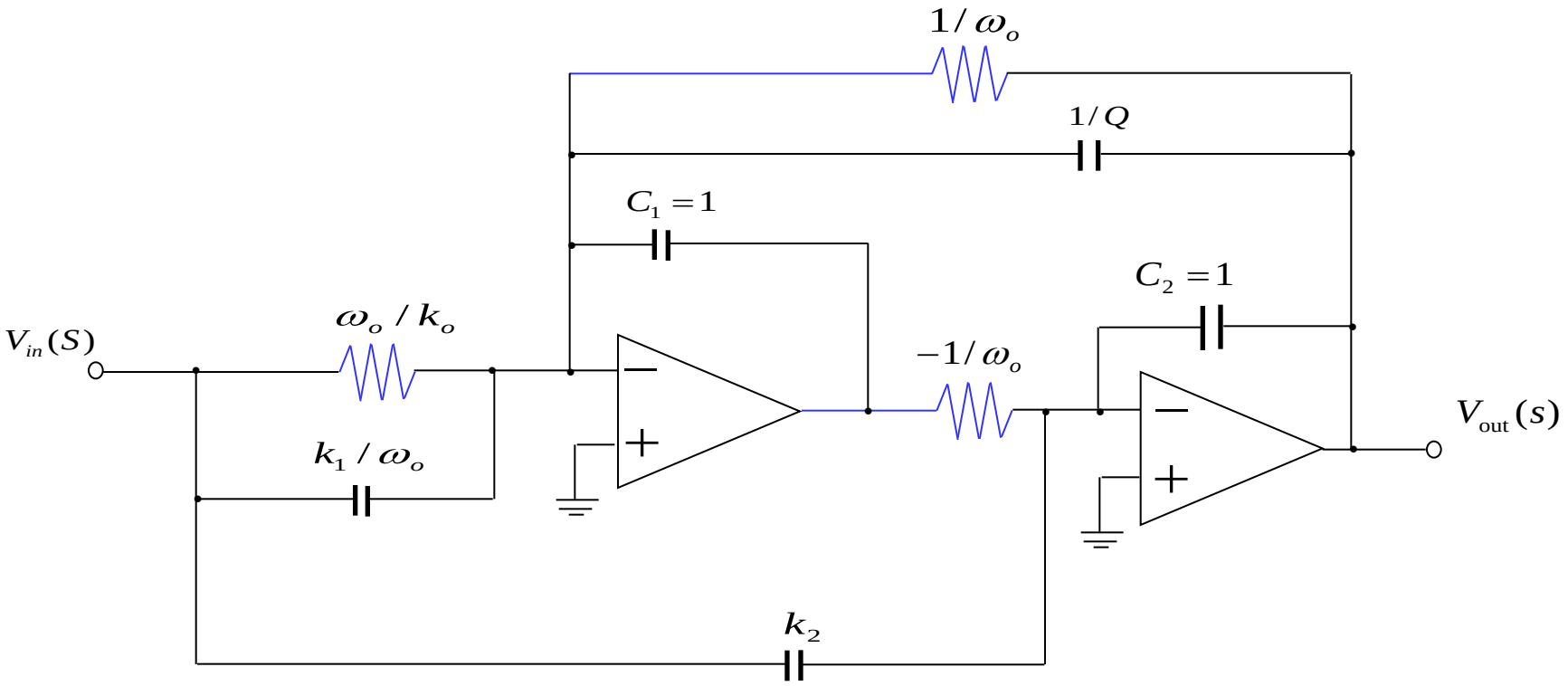




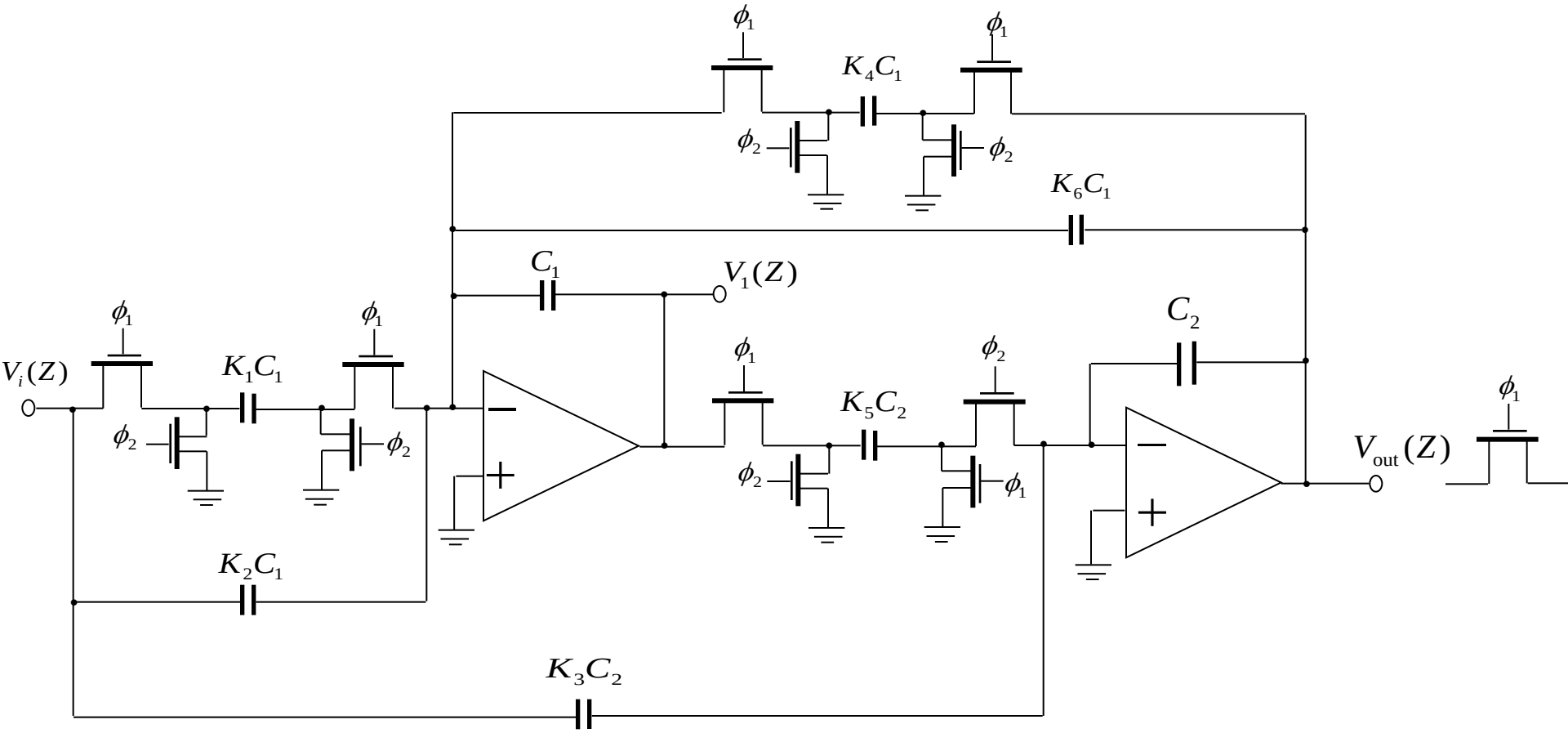


A direct mapping from an active-RC filter into a SC Filter.

Since negative (equivalent) resistances are easily implemented in SC,
a modified Active-RC prototype is next described

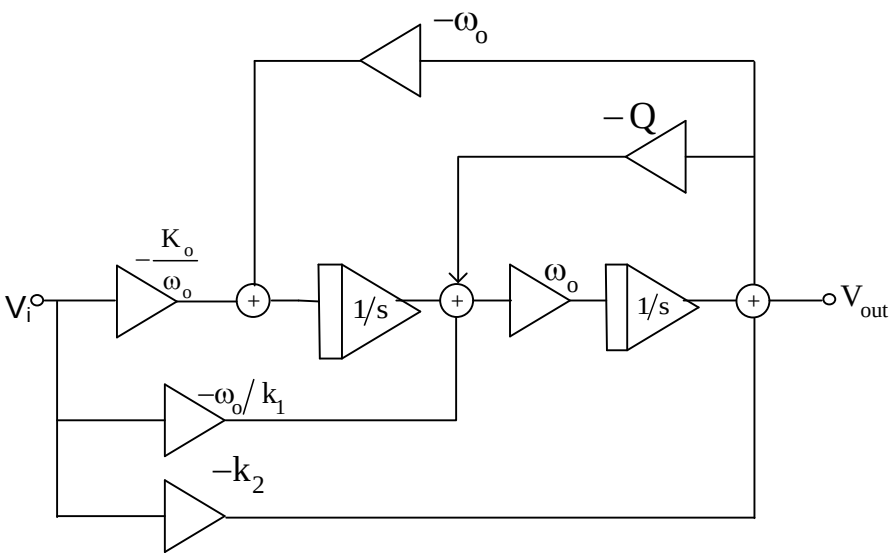


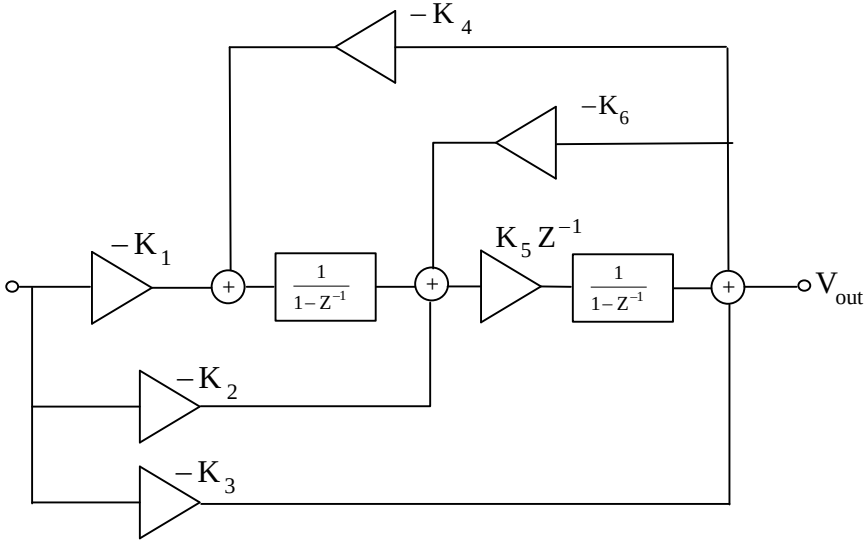
An alternate realization of a general active-RC biquad filter



A high-Q switched-capacitor biquad filter (without switch sharing).

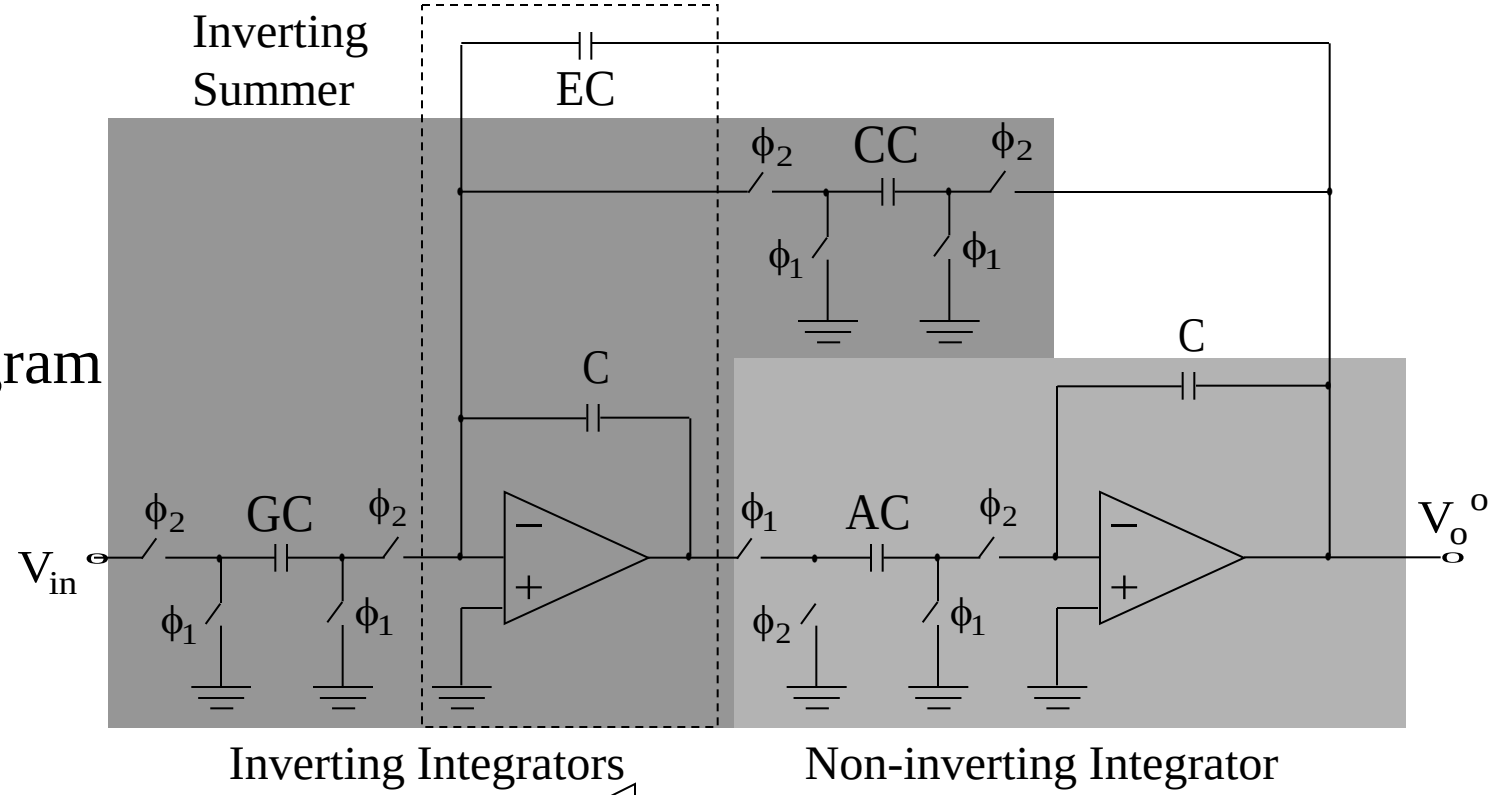
Building Block Diagrams of Figs. In p 18 and 19



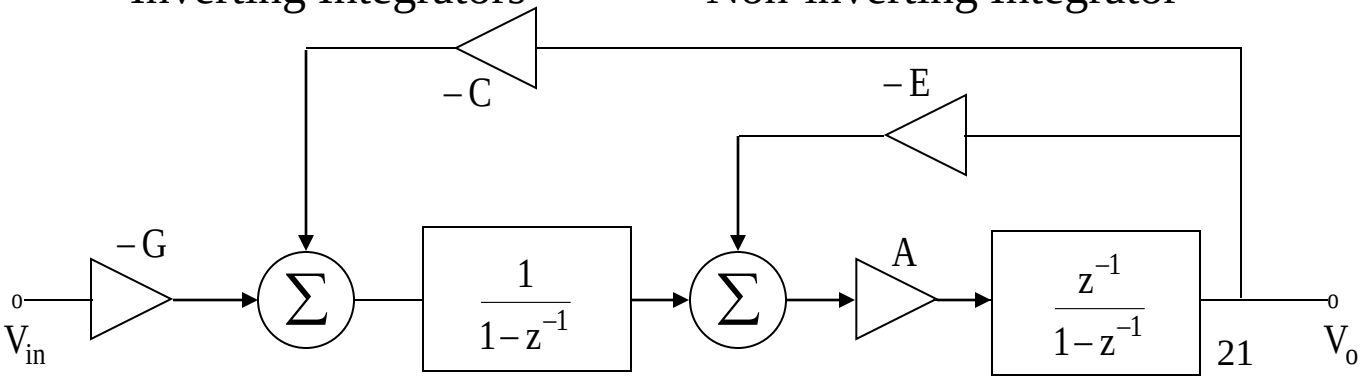


Biquad Circuit & Block Diagrams

Circuit Diagram

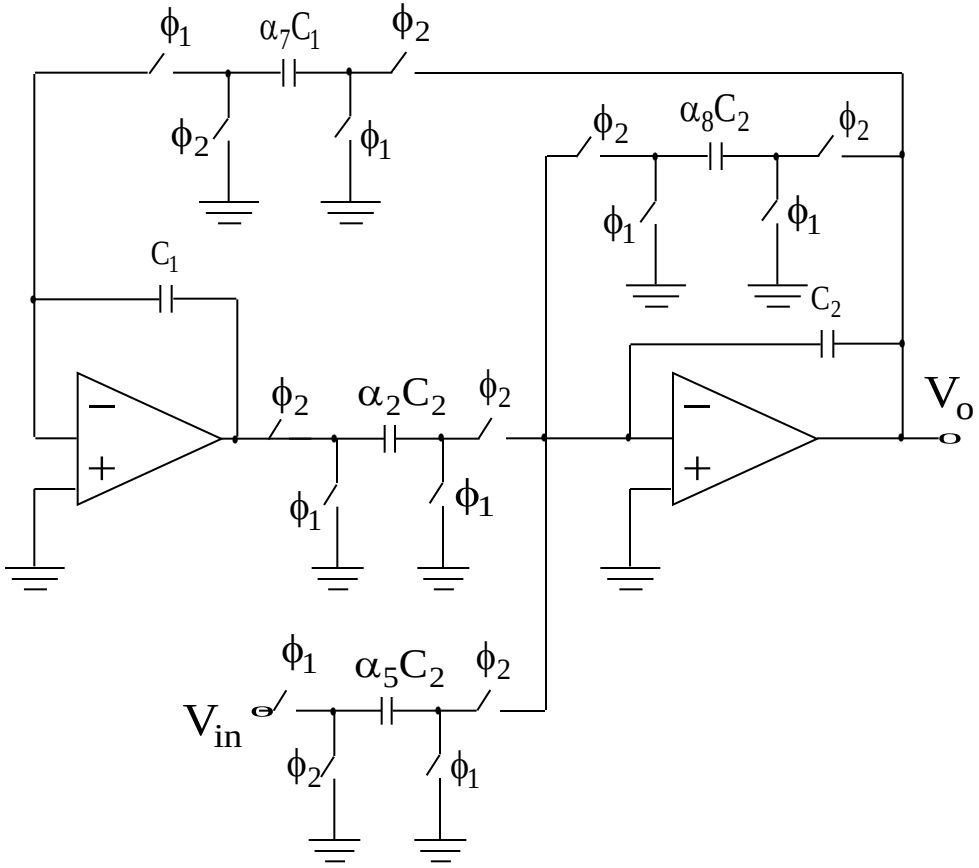


Block Diagram



Biquad Circuit 1

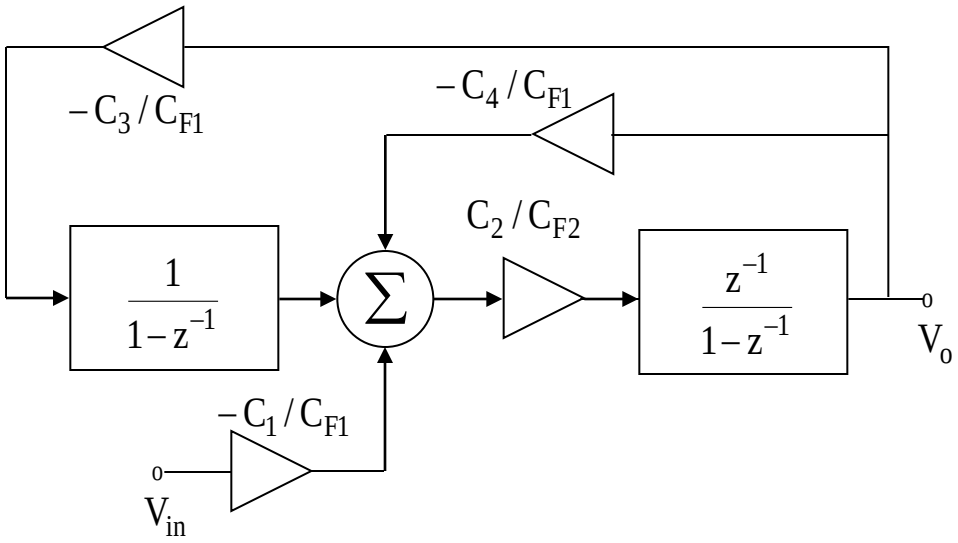
Circuit Diagram



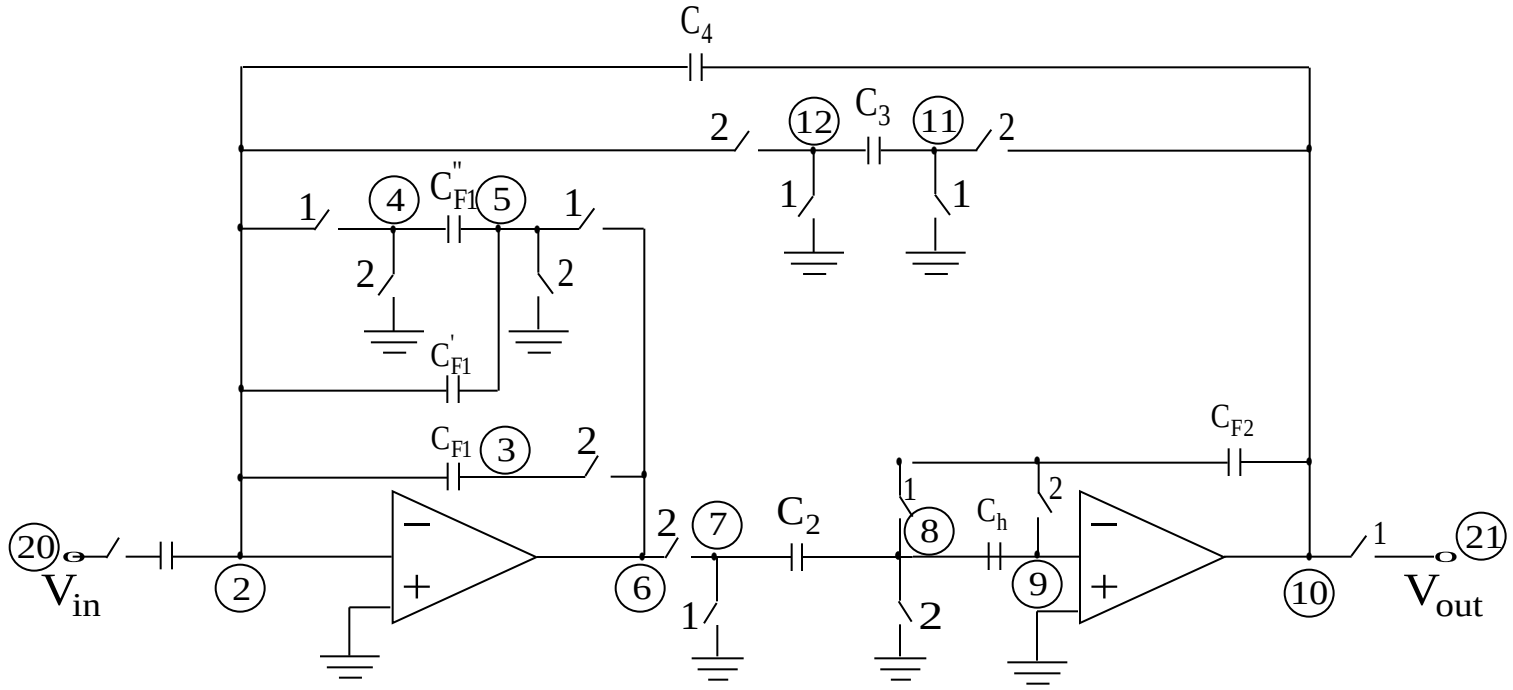
Block Diagram

Biquad Circuit 2

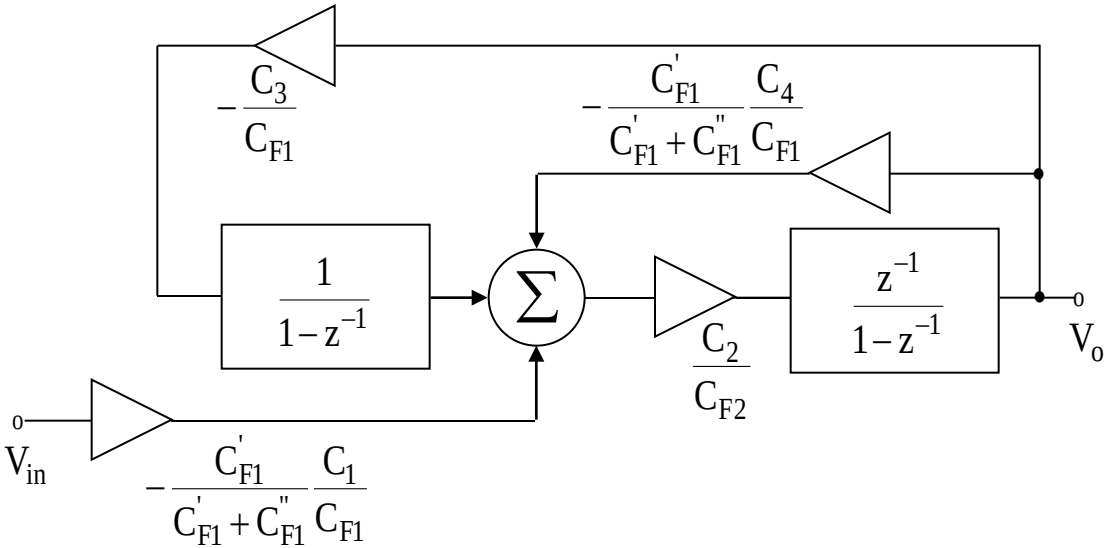
Block Diagram



Circuit Diagram



SC Bandpass C Diagram



SC Bandpass Filter Block Diagram

Capacitor Values for the SC Filter

Capacitor Values		
f_o (Hz)	C'_{F1} (Cu)	$C_{F1} = C_{F2}$ (Cu)
697	4	11.4
852	2.6	9.3
1209	1.5	6.6
1477	1.1	5.4
Where: $C_2 = C_3 = C_4 = C_h = 1\,\text{Cu}$, $C_1 = 2.2\,\text{Cu}$, $C''_{F1} = 3\,\text{Cu}$ and $f_c = 1/T = 50\,\text{kHz}$		

Specifications vs. Simulated Results for the SC Filter

Design Specifications			Simulated Results		
Gain (v/v)	f_o (Hz)	Q	Gain (v/v)	f_o (Hz)	Q
1	697	20	0.998	699.00	19.92
1	852	20	0.999	857.25	20.02
1	1209	20	1.000	1209.00	19.83
1	1477	20	1.002	1479.00	20.11

Design of 2nd-Order LP Notch Filter

Design a LP Notch Filter with f_z=1,800 Hz, f_p= 1,700 Hz, Q_p=30 and 0dB DC Gain.
The corresponding H(s) yields:

$$H(s) = \frac{0.89195s^2 + (1.140926 \times 10^8)}{s^2 + 356.0475s + (1.140926 \times 10^8)}$$

By using the bilinear mapping

$$s = K\frac{1 - z^{-1}}{1 + z^{-1}}$$

where $K = \omega a / \tan(\omega_d T / 2)$

The corresponding transfer function becomes:

$$H(z) = 0.89093\frac{1 + 1.99220z^{-1} + z^{-2}}{1 - 1.99029z^{-1} + 0.997232z^{-2}}$$

Next we will match the coefficients of H(z) with the ones of a SC Biquad Topology, i.e.,

$$H_{E_z}(\hat{z}) = -\frac{I + (I + G - J)\hat{z}^{-1} + (G - H)\hat{z}^{-2}}{1 + (E + C)\hat{z}^{-1} + C\hat{z}^{-2}}$$

where $\hat{z}^{-1} = \frac{z^{-1}}{1 - z^{-1}}$; $\quad \hat{z} = z - 1$

$$H(\hat{z}) = 0.89093\frac{1 + 0.0078\hat{z}^{-1} + 0.0078\hat{z}^{-2}}{1 + 0.0097\hat{z}^{-1} + 0.000694\hat{z}^{-2}}$$

CAPACITOR (PF)	E-CIRCUIT		
	INITIAL	DYNAMIC RANGE ADJUSTED	FINAL
A	1.0000	0.08308	1.0000
B	1.0000	1.0000	12.0365
C	0.00694	0.00694	2.5035
D	1.0000	0.08308	29.9613
E	0.00277	0.00277	1.0000
F	---	---	---
G	0.00694	0.00694	2.5035
H	---	---	---
I	---	---	---
J	---	---	---
K(I=J)	0.89093	0.89093	10.7238
$\sum$ C(pF)	---	---	59.7

$\hat{Z}$ - DOMAIN NOTATION : $\hat{Z} = Z - 1 ; Z = \hat{Z} + 1$

$$H(\hat{Z}) = \frac{\beta_o + \beta_1 \hat{Z}^{-1} + \beta_2 \hat{Z}^{-2}}{1 + \alpha_1 \hat{Z}^{-1}{}_1 + \alpha_2 \hat{Z}^{-2}} \, K = \frac{KN(\hat{Z})}{1 + (2 - 2r\cos\theta)\hat{Z}^{-1} + (1 + r^2 - 2r\cos\theta)\hat{Z}^{-2}}$$

$$H(Z) = \frac{b_2 Z^{-2} + b_1 Z^{-1} + b_o}{1 - a_1 Z^{-1} + a_2 Z^{-2}} \quad ; \quad a_1 = 2r\cos \quad , \quad a_2 = r^2$$

where

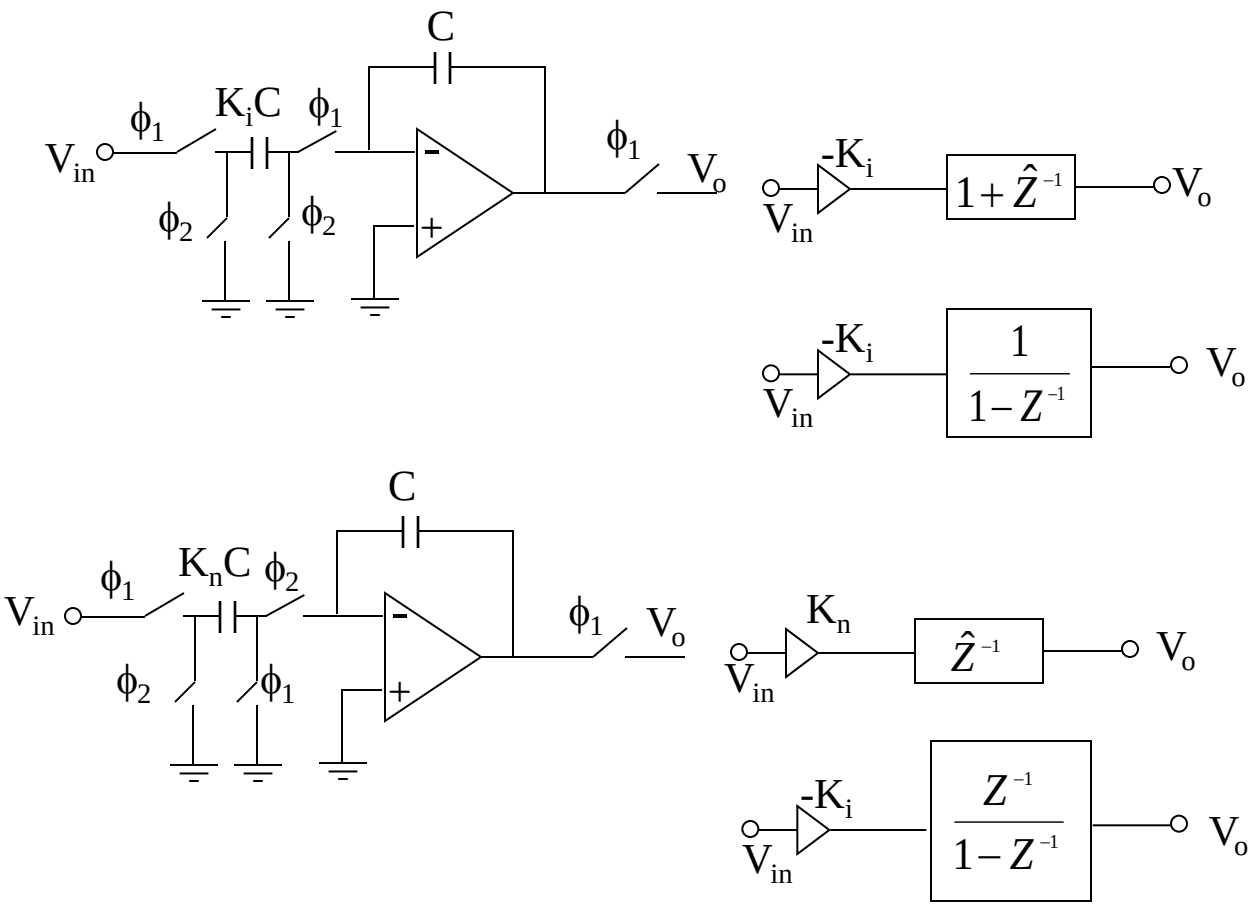
$$\beta_o = b_o \, , \beta_1 = 2b_o + b_1 \, , \beta_2 = b_1 + b_2 + b_o$$

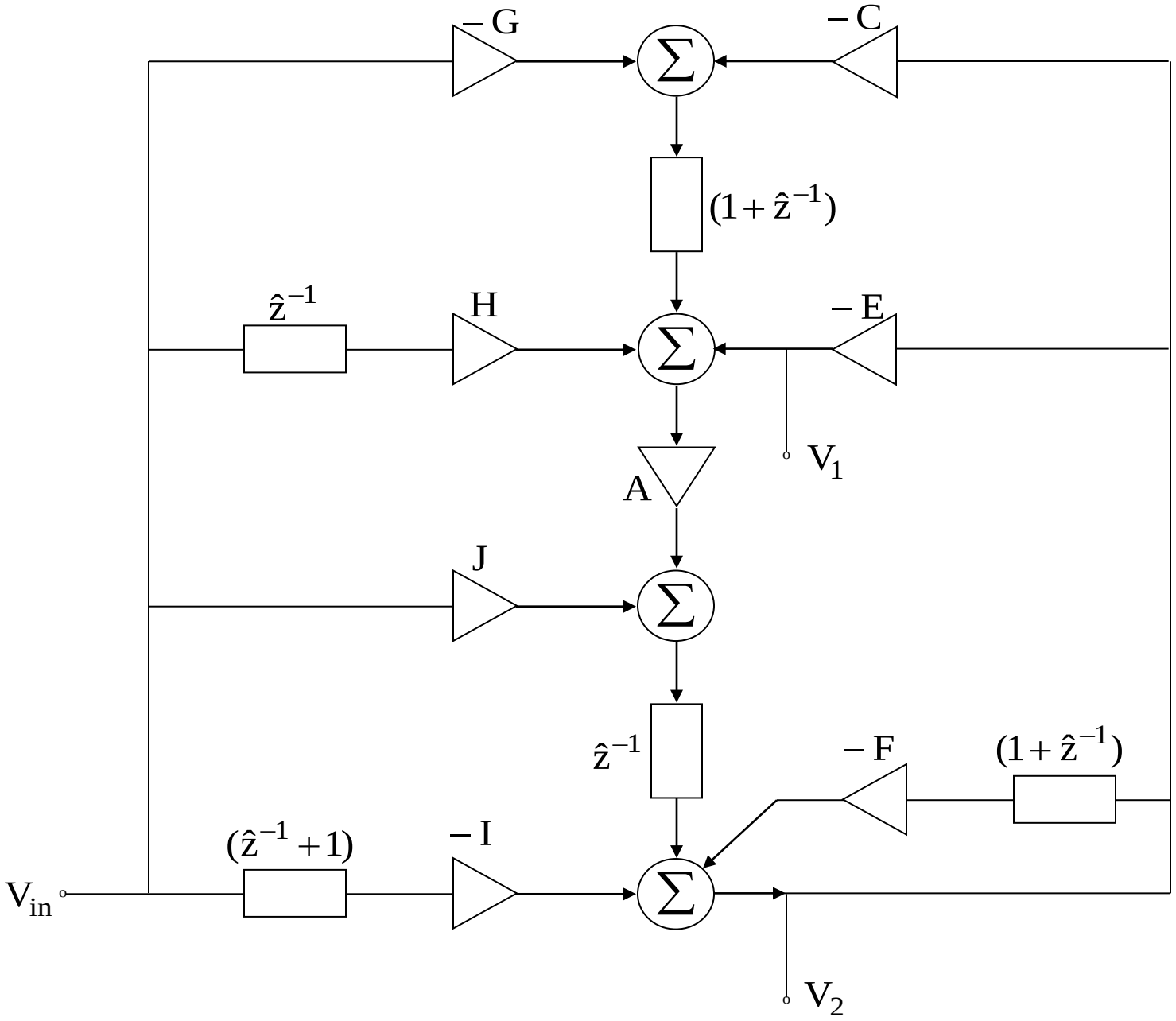
$$\alpha_1 = 2 - a_1 \quad , \quad \alpha_2 = 1 + a_2 - a_1$$

Generic Biquadratic Transfer Functions in the $\hat{z}-$domain, $\alpha = 2r\cos\theta$ and $\beta = r^2$

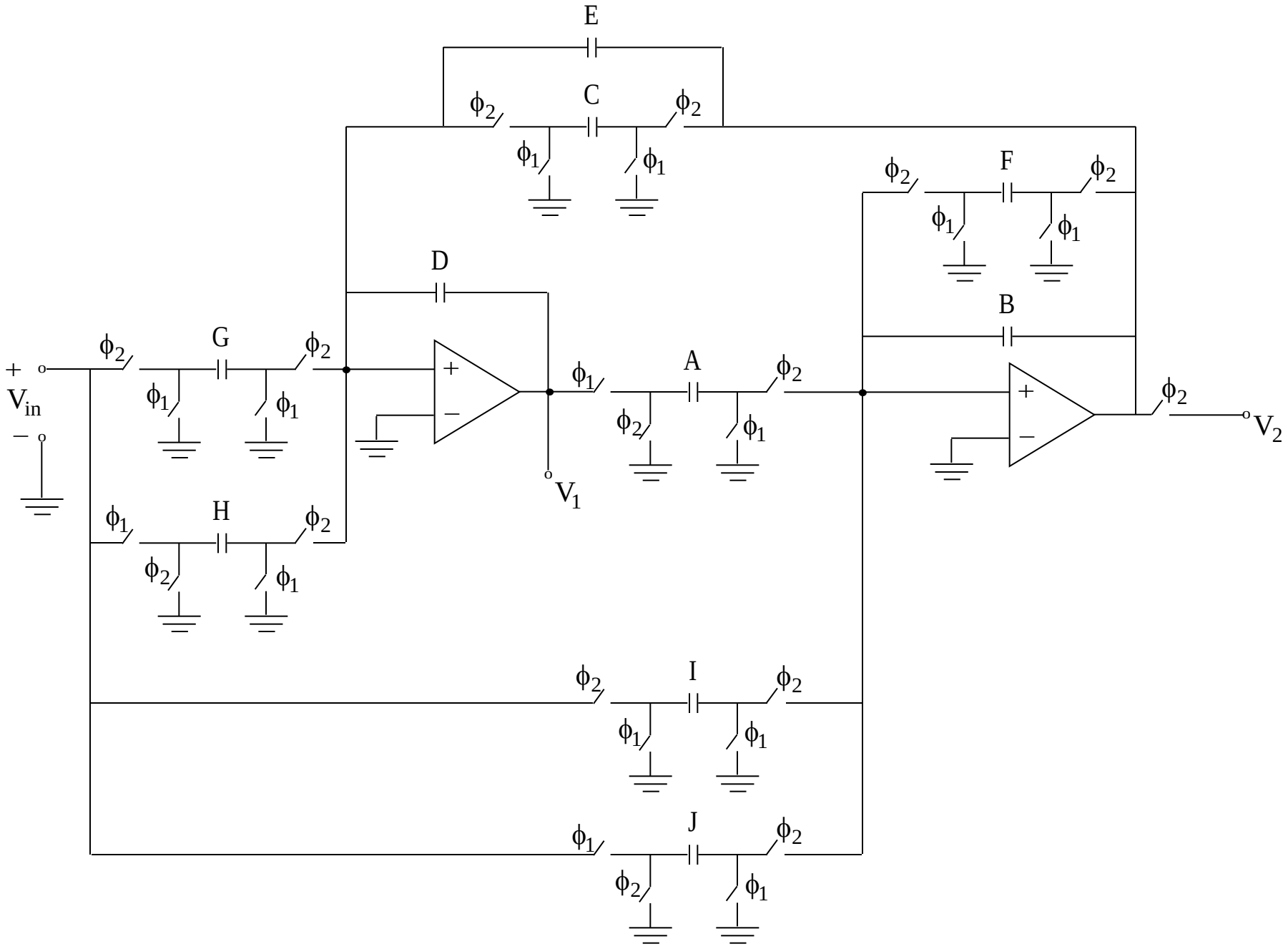
GENERIC FORM	NUMERATOR N(z)	NUMERATOR N($\hat{z}$)
LP 20 (bilinear transform)	$K(1+z^{-1})^2$	$K(1+4\hat{z}^{-1}+4z^{-2})$
LP 11	$Kz^{-1}(1+z^{-1})$	$K(2\hat{z}^{-1}+1)\hat{z}^{-1}$
LP 10	$K(1+z^{-1})$	$K(2\hat{z}^{-2}+3\hat{z}^{-1}3\hat{z}^{-1}+1)$
LP 02 (forward transform)	Kz^{-2}	Kz^{-2}
LP 01	Kz^{-1}	$K(1+\hat{z}^{-1})\hat{z}^{-1}$
LP 00 (backward transform)	K	$K(1+\hat{z}^{-1})^2$
BP 10 ((bilinear transform)	$K(1-z^{-1})(1+z^{-1})$	$K(1+2\hat{z}^{-1})$
BP 01 (forward)	$Kz^{-1}(1-z^{-1})$	$K\hat{z}^{-1}$
BP 00 (backward)	$K(1-z^{-1})$	$K(1+\hat{z}^{-1})$
HP	$K(1-z^{-1})^2$	K
LPN	$K(1+\varepsilon z^{-1}+z^{-2}),\ \varepsilon > \alpha/\sqrt{\beta},\ \beta > 0$	$K[1+\hat{z}^{-1}(2+\varepsilon)+(2+\varepsilon)\hat{z}^{-2}]$
HPN	$K(1+\varepsilon z^{-1}+z^{-2}),\ \varepsilon < \alpha/\sqrt{\beta},\ \beta > 0$	$K[1+\hat{z}^{-1}(2+\varepsilon)+[2+\varepsilon]\hat{z}^{-2}]$
AP	$K(\beta+\alpha z^{-1}+z^{-2})$	See Eq. (21), Sect. 5.1 $\alpha = -\alpha_1,\ \beta = \alpha_2$

Recall notation for $\hat{Z}$ and Z building blocks

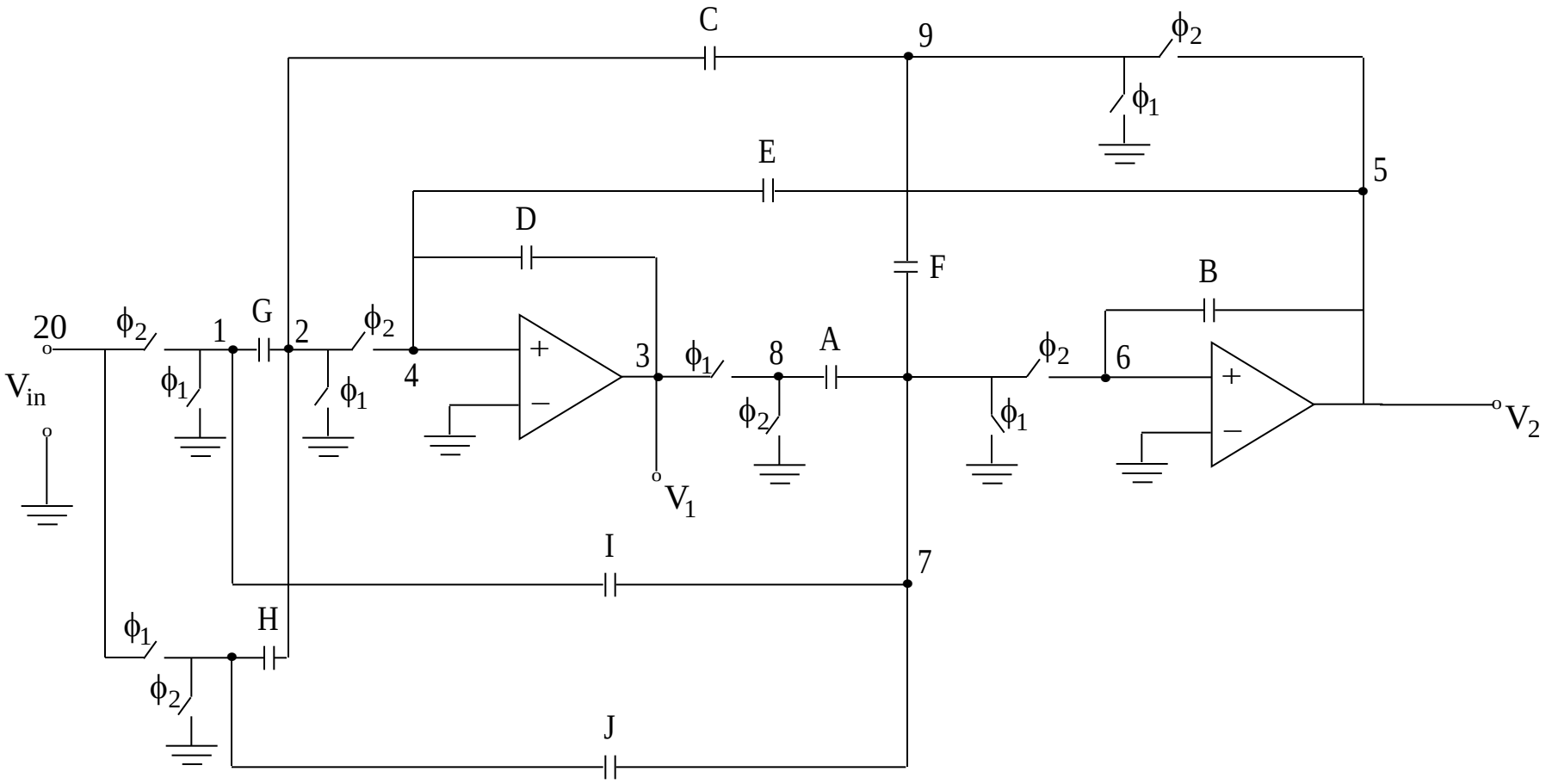




A general SC biquad flow diagram **type 1**.



SC implementation **type 1** with maximum number of switches.



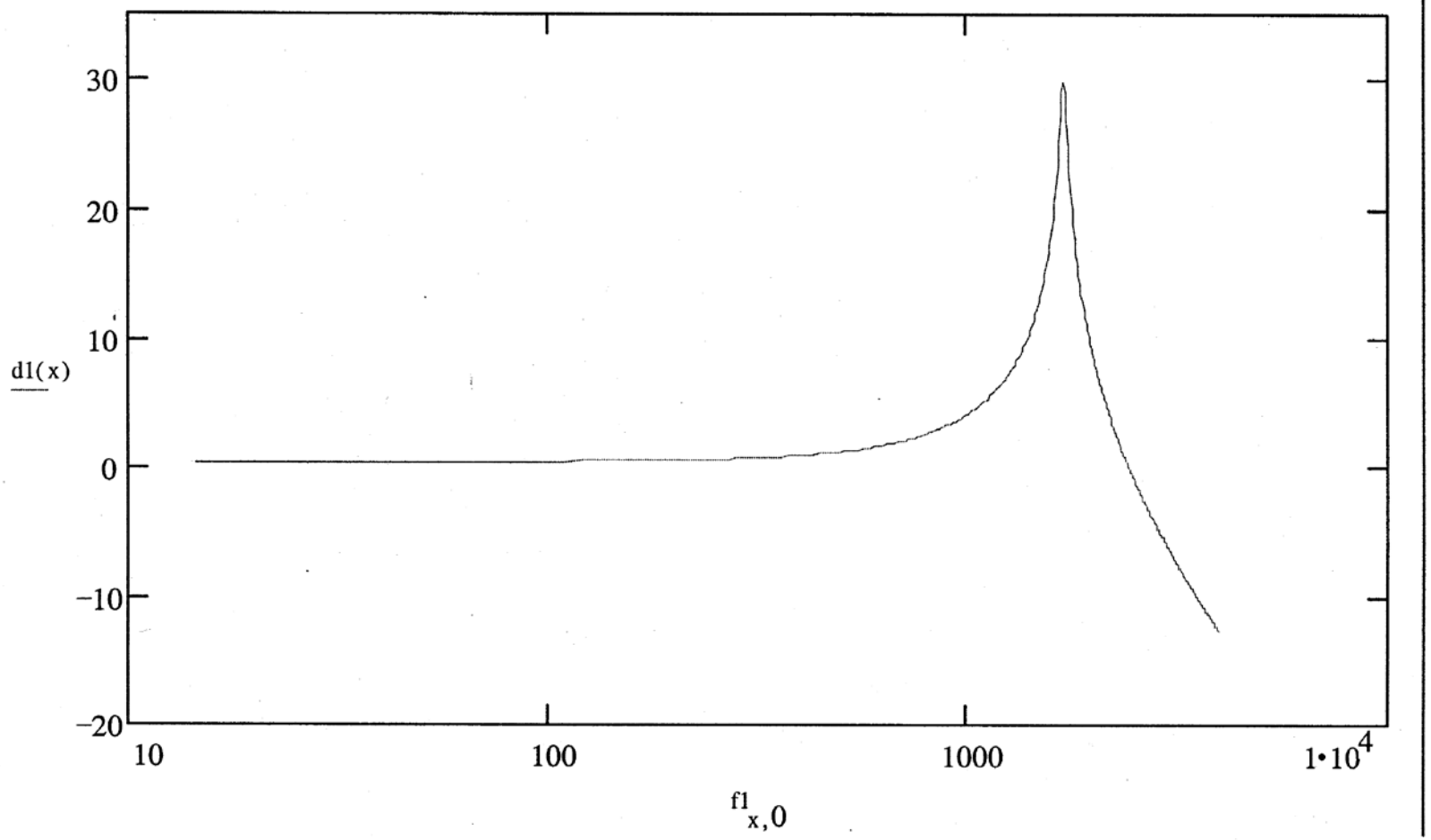
SC implementation **type 1** minimum switch configuration.

SWITCAP Input file

```
timing;
period 7.8125e-06;
clock clk 1 (0 1/2);
end;

circuit;
cg   (1 2) 2.5935;
ca   (8 7) 1.0000;
cd   (4 3) 29.9613;
cb   (6 5) 12.0365;
ce   (4 5) 1.00000;
cc   (2 9) 2.5035;
e1   (3 0 0 4) 28000;
e2   (5 0 0 6) 28000;
s1   (20 1) #clk;
s4   (2 4) #clk;
s5   (9 5) #clk;
s9   (8 0) #clk;
s10  (7 6) #clk;
s2   (1 0) clk;
s3   (2 0) clk;
s6   (9 0) clk;
s7   (3 8) clk;
s8   (7 0) clk;
v1   (20 0);
end;
analyze sss;
infreq 1 4000 lin 300;
set v1 ac 1.0 0.0;
print vm(5);
plot vm(5);
```

Low-pass notch SC



f_p = 1,700 Hz, f_z =1,800 Hz, Qp = 30, DC Gain = 0 dB

Periodic Non-Uniform Switched-Capacitor Technique

Francisco Duque-Carrillo & Edgar Sánchez-Sinencio

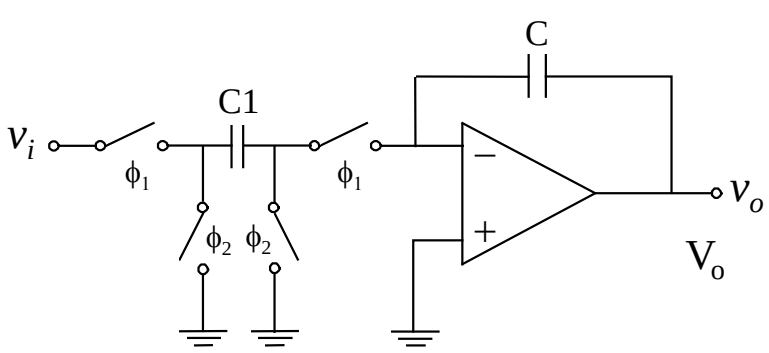
- Switched-capacitor techniques conventionally have only two degrees of freedom:
  - clock frequency
  - capacitor ratios

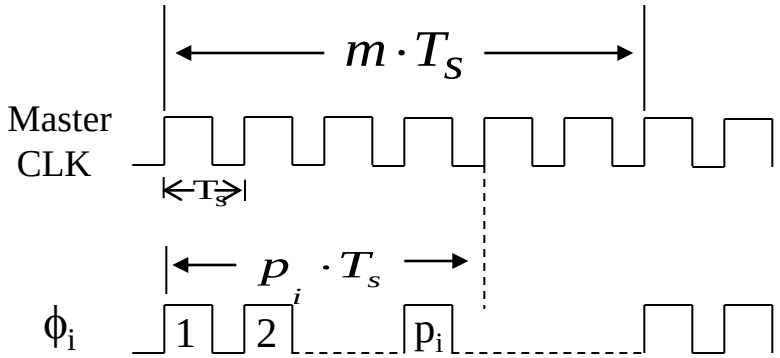
i.e.,

$$\tau = R_{eq}C = \frac{T_s \cdot C}{C_{eq}} = \frac{1}{f_s} \cdot \frac{C}{C_{eq}}$$

Periodic Non-Uniform Switched Capacitor Principle

- The number of active pulses (p_i) of a switched-capacitor branch controls the equivalent resistance value.



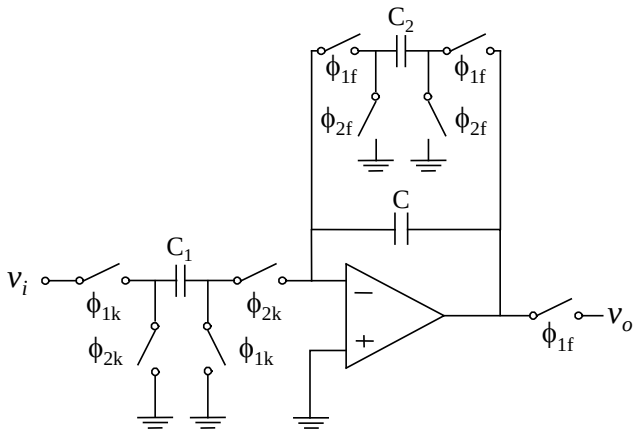


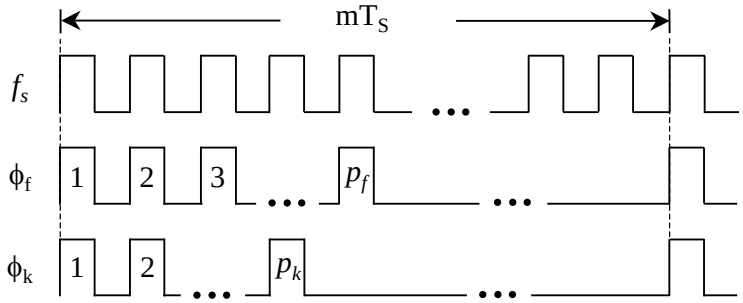
$$\tau = R_{eq} \cdot C = \frac{m}{p_i} \cdot \left(\frac{T_s \cdot C}{C_1} \right)$$

An additional degree of freedom (m/p_i) is provided by this approach

Periodic Non-Uniform Switched-Capacitor Example

- In more complex switched-capacitor networks, any response parameter can be fully-programmed by means of the number of active pulses of some switched-capacitor branches:





- DC gain:

$$H(0) = \frac{p_k}{p_f} \cdot \frac{C_1}{C_2}$$

- Cutoff frequency (ω_o):

$$z = e^{j\omega_o m T_s} = \left(\frac{C}{C + C_2} \right)^{p_f}$$

Periodic Non-Uniform Switched-Capacitor Remarks

Advantages:

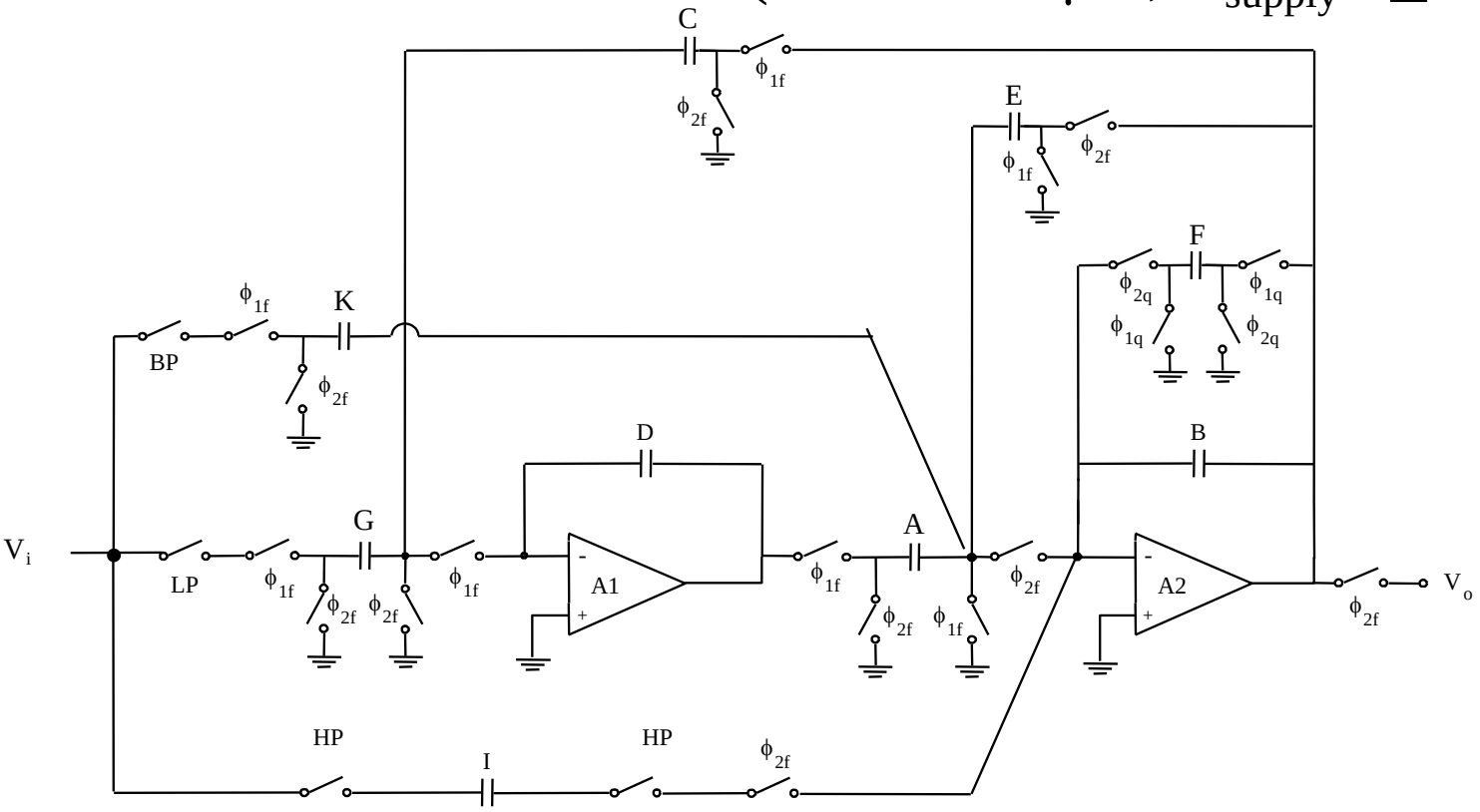
- Great flexibility and resolution for programming SC signal processors.
- The design is performed in the digital domain with a single logic programmable section (i.e., FPGA).
- Reduced cost (area) and high accuracy (no extra parasitic capacitances) respect to any other programming technique (i.e., capacitor arrays).
- Only one clock is used. One sub-clock (ϕ_i) is required for each output response parameter to be programmed.
- The programmability does not affect the circuit dynamic range.

Disadvantages:

- The master clock frequency must be *m* times the clock frequency of the traditional case (p_i=*m*). However, the amplifier requirements remain unchanged.

Example of the Proposed Technique

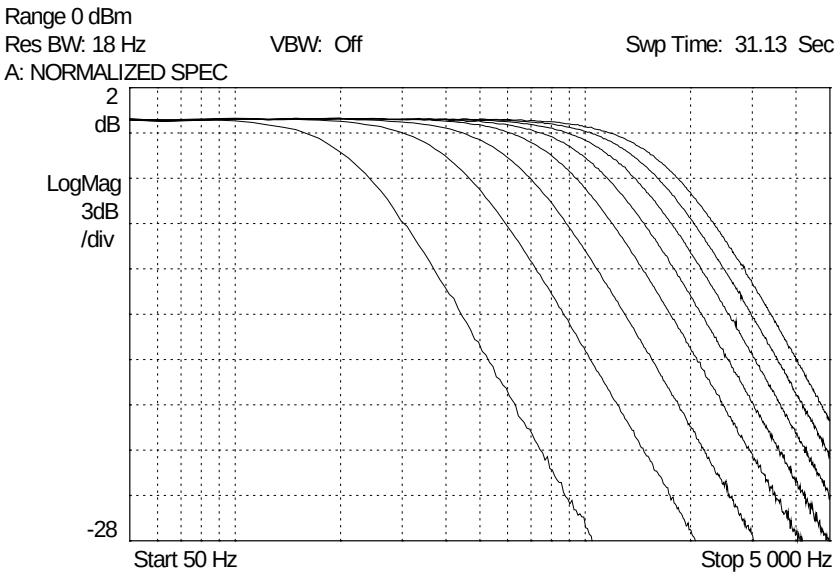
•Universal second-order SC filter (CMOS 1.2 μm, $V_{supply} = \pm 1.5$ V)



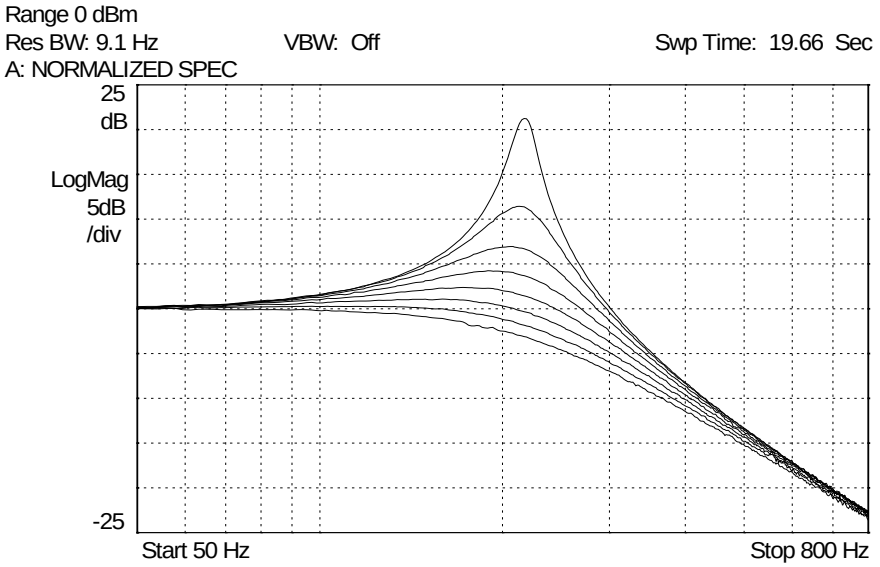
- Design specifications { f_o = 0.2 kHz, Q = 0.707, k = 0 dB } with f_s = 20 kHz
- The SC circuit was designed to operate with clock frequencies up to 1 MHz
- The digital programming signals were off-chip generated by a commercial FPGA

Experimental Results of Second-Order Non-Uniform SC

1. **Low-pass** response programmability ($m = 8$, $f_s = 160$ kHz)



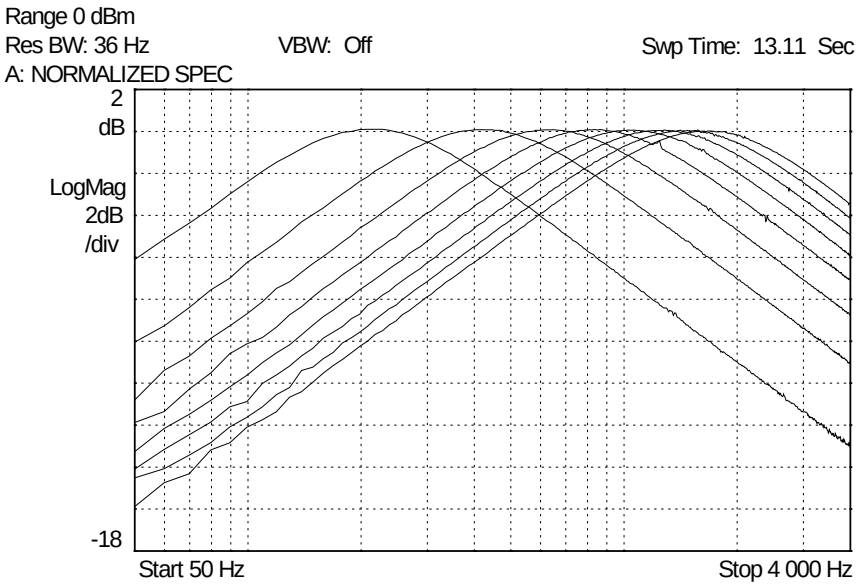
LP f_o-programmability
($1 \leq p_f \leq 8$)



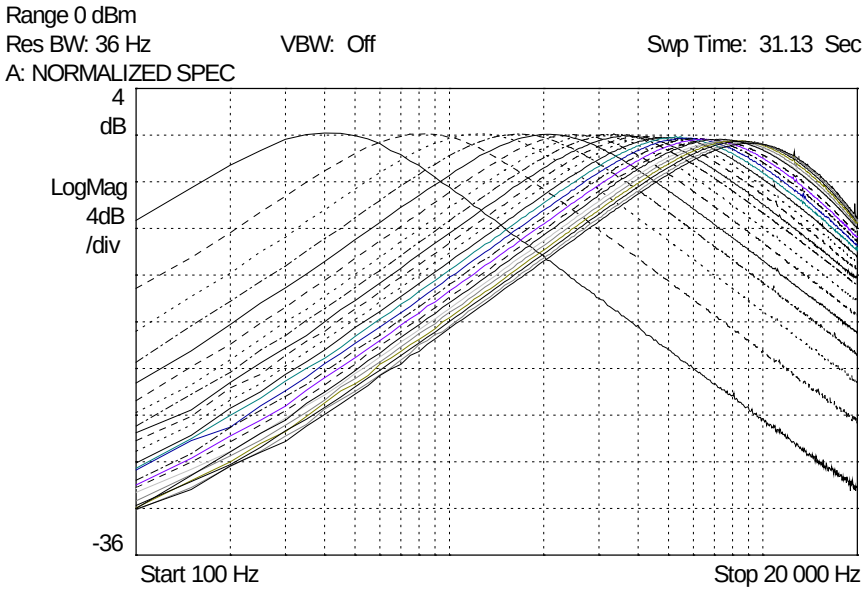
LP Q-factor programmability
($1 \leq p_q \leq 8$)

Experimental Results (continues)

2. f_o **Band-pass** response programmability



$m = 8$; $f_s = 160$ kHz
$(1 \leq p_f \leq 8)$

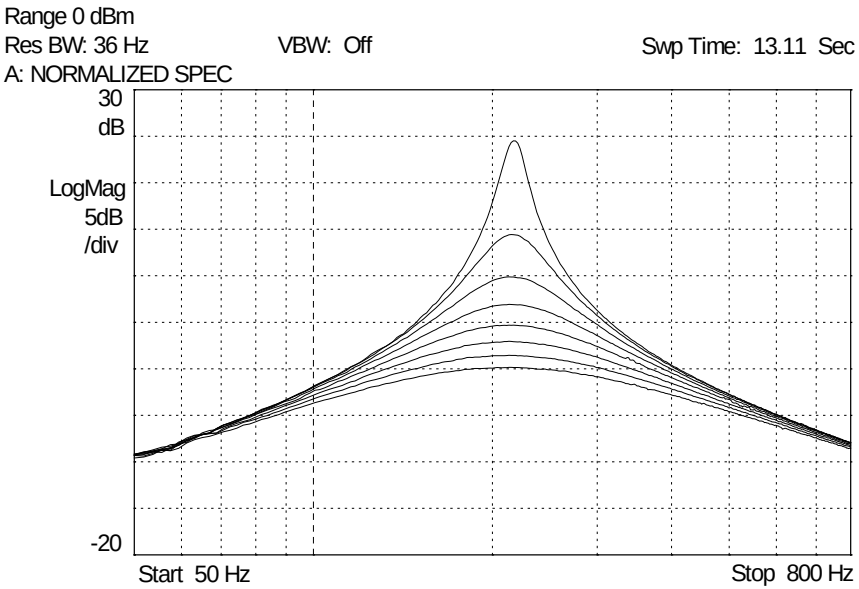


$m = 24$; $f_s = 960$ kHz
$(1 \leq p_f \leq 24)$

Note the increased resolution

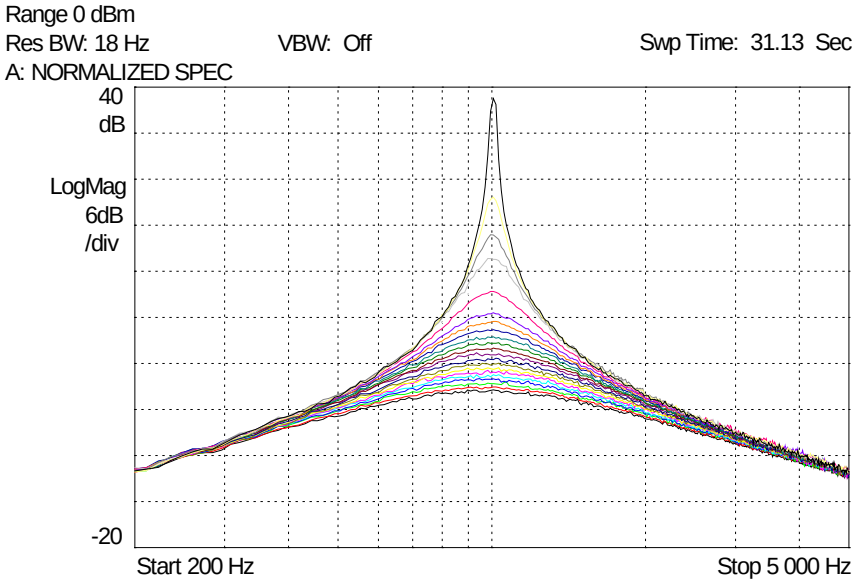
Experimental Results (continues)

3. *Q*-factor band-pass programmability



$m = 8$; $f_s = 160$ kHz

$(1 \leq p_q \leq 8)$



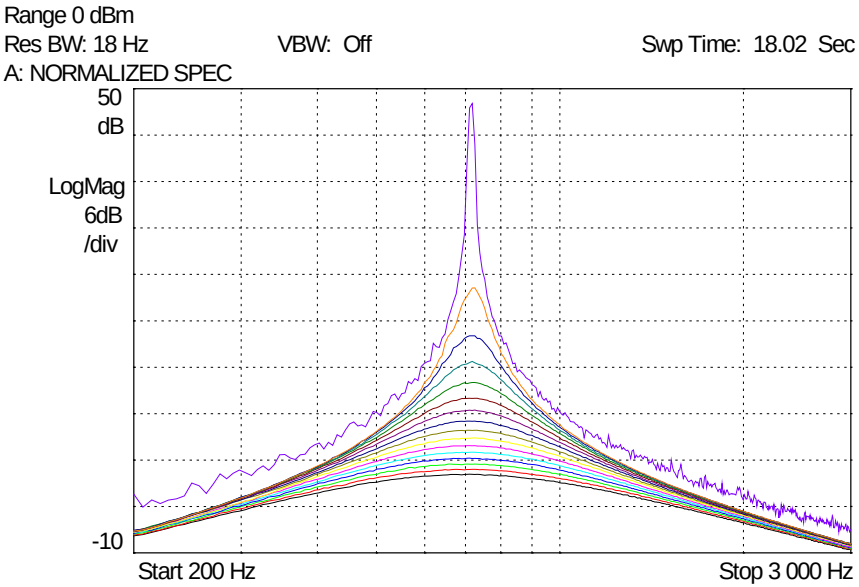
$m = 32$; $p_f = 3$; $f_s = 1$ MHz

$(1 \leq p_q \leq 25)$

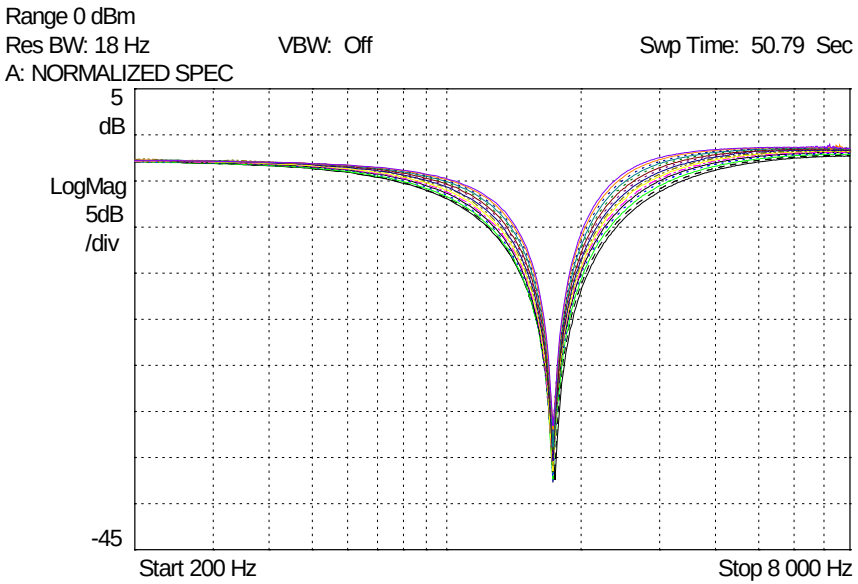
Enhanced Resolution

Experimental Results (continues)

4. *Q*-factor **Band-pass and Notch** programmability

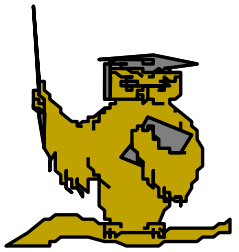


$m = 32$; $p_f = 2$; $f_s = 0.8$ MHz
$(1 \leq p_q \leq 16)$



$m = 24$; $f_s = 1$ MHz
$(1 \leq p_q \leq 16)$

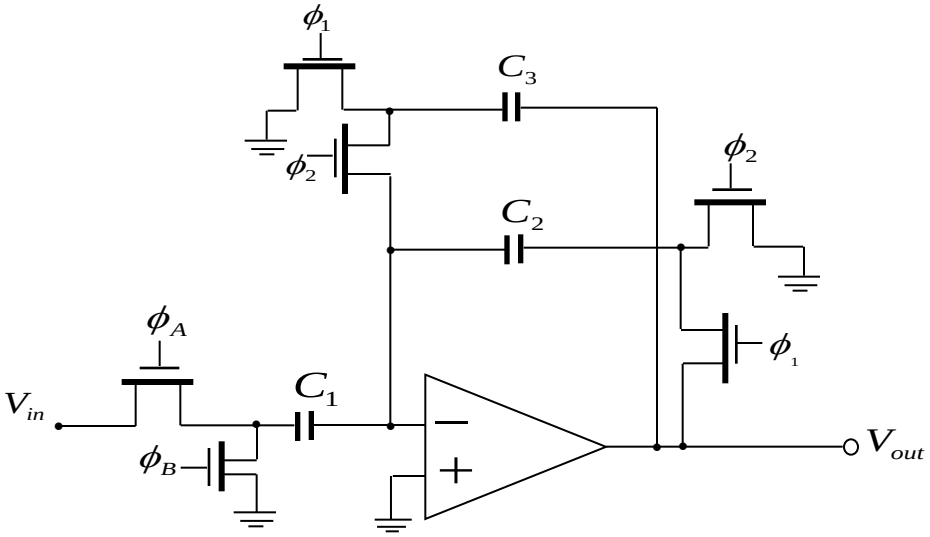
Conclusions



A SC technique with an additional degree of freedom is presented.

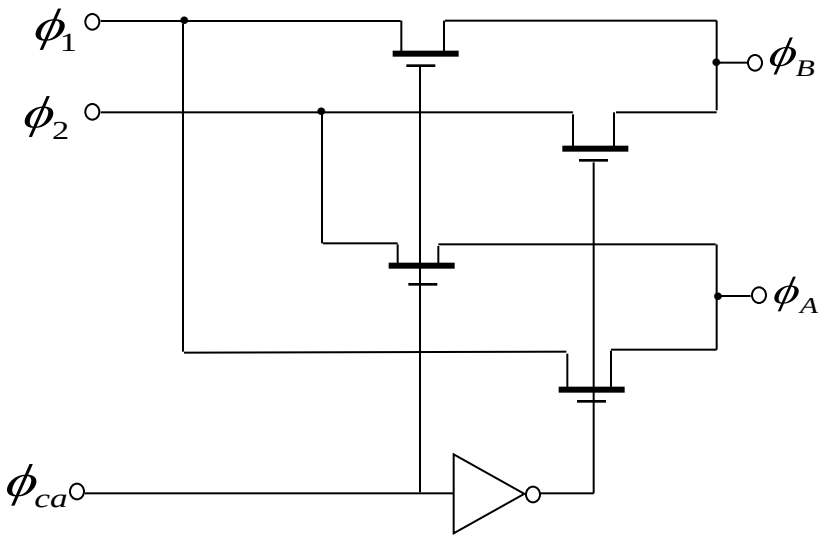
Potential applications are very wide and practical implications are very promising.

The ideal situation of analog processing and digital control are present in the proposed scheme.



$$\phi_A = (\phi_2 \bullet \phi_{ca}) + (\phi_1 \bullet \overline{\phi}_{ca})$$
$$\phi_B = (\phi_1 \bullet \phi_{ca}) + (\phi_2 \bullet \overline{\phi}_{ca})$$

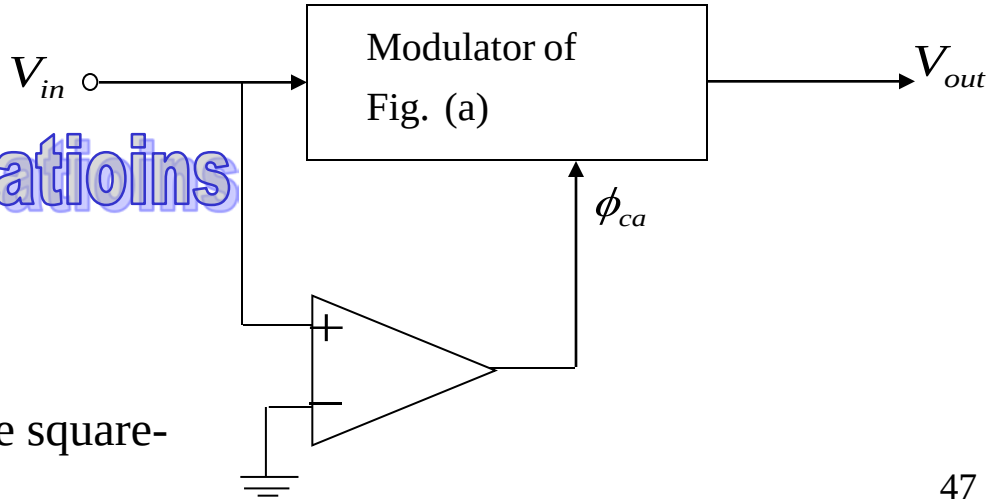
(a)



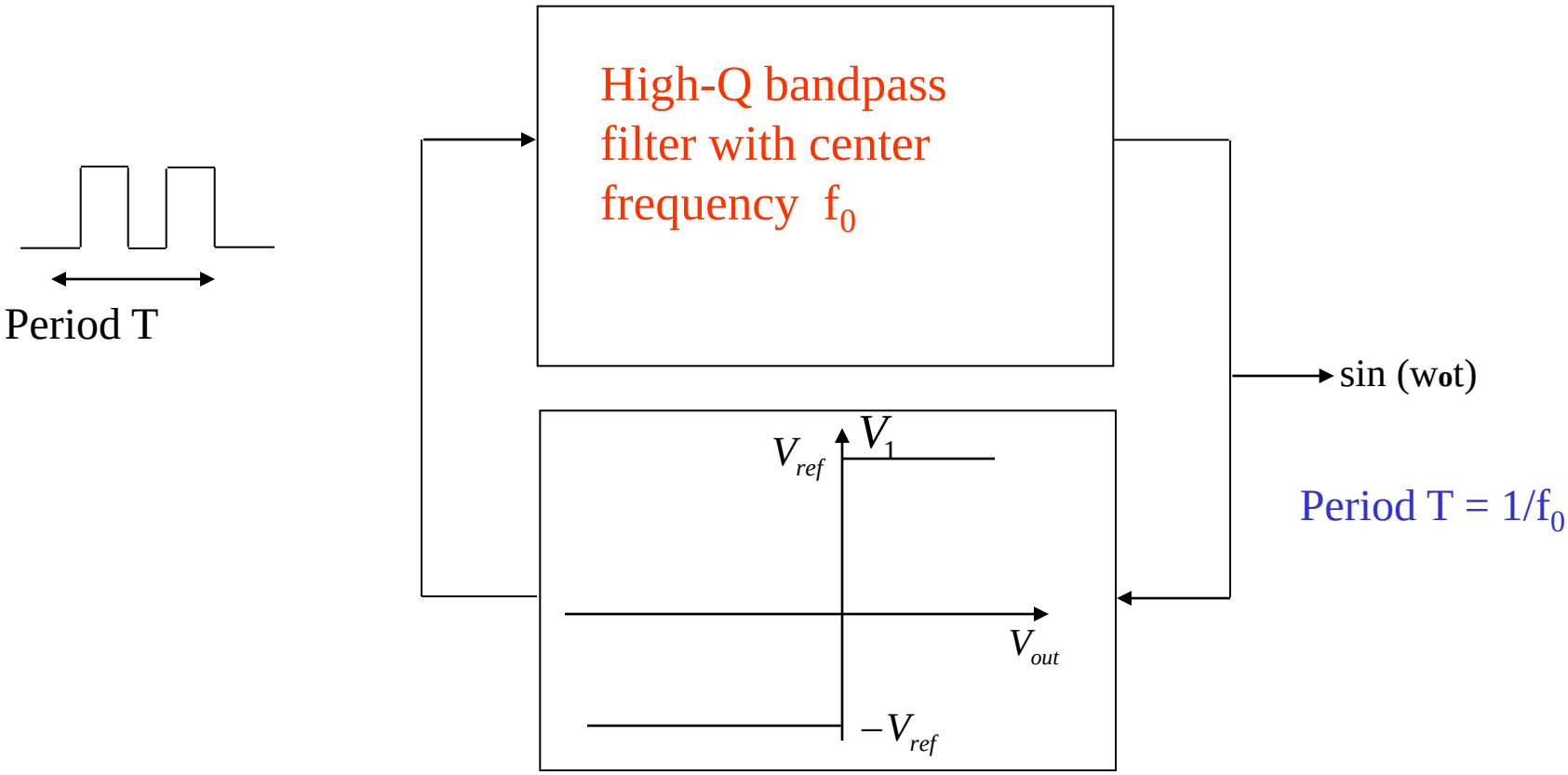
(b)

(a) A switched-capacitor square-wave modulator where the input clock phases are controlled by the modulating square wave ϕ_M. (b) A possible circuit realization for ϕ_A and ϕ_B.

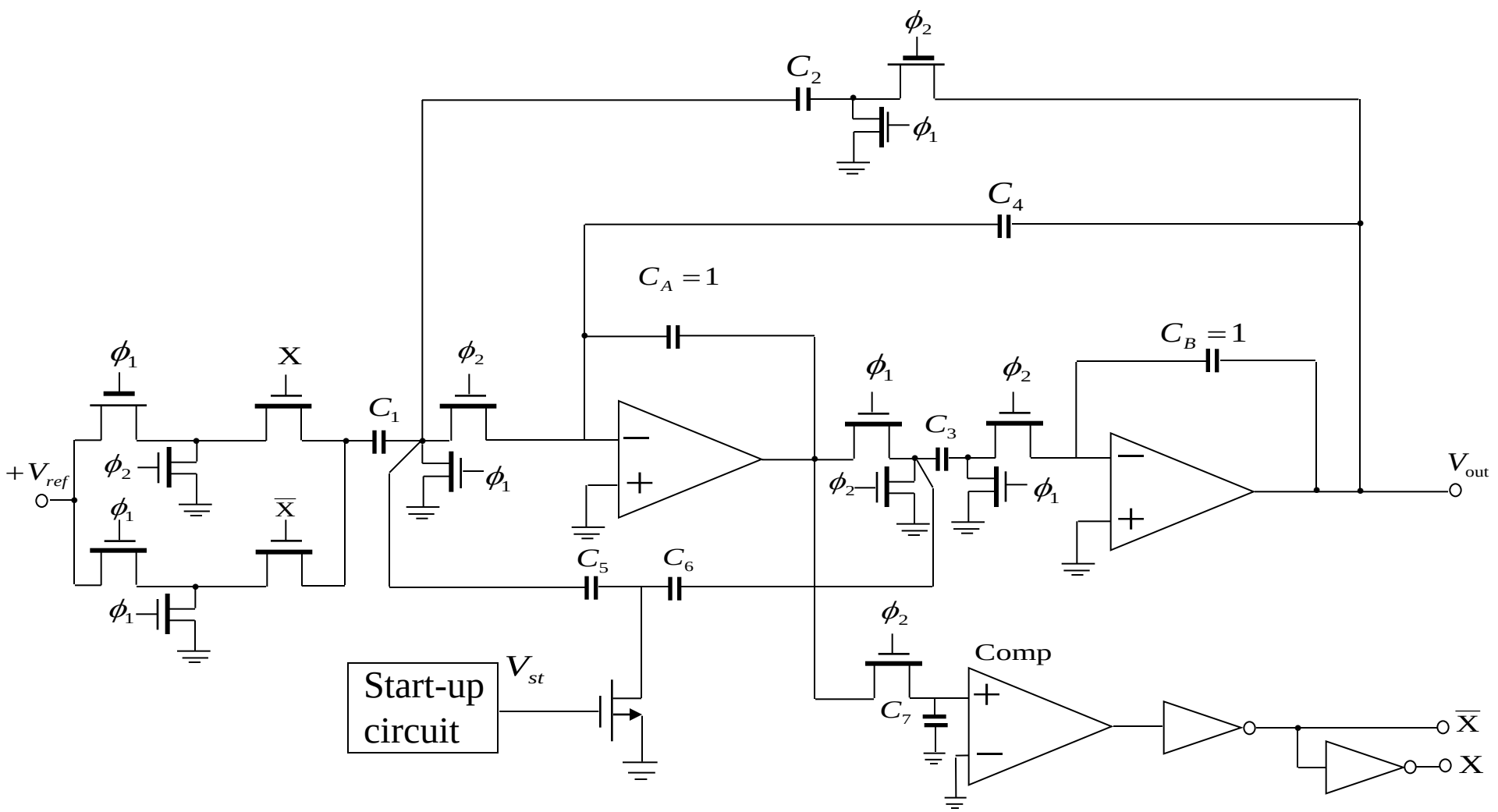
Non-Linear SC Applicatioins



A full-wave detector based on the square-modulator circuit of Fig. (a)



A BP Filter based sinusoidal oscillator.



A SC implementation of a BP based Oscillator

References

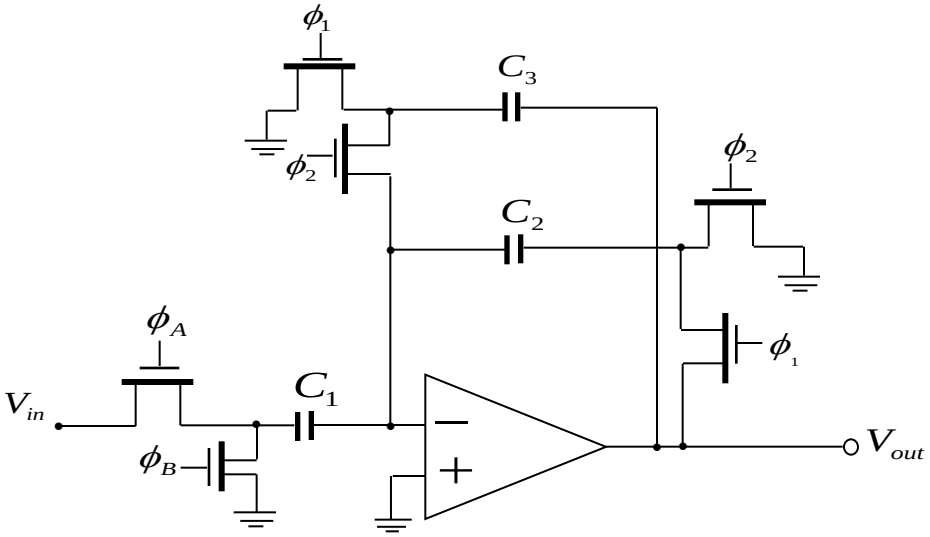
- E. Sánchez-Sinencio, J. Silva-Martínez, *The Circuits and Filters Handbook: Switched Capacitor Filters*, CRC Press Inc., section XV, pp. 2491-2520, 1995.

- E. Sánchez-Sinencio, R.L. Geiger and J. Silva-Martínez, "Tradeoffs between Passive Sensitivity, Output Voltage Swing and Total Capacitance in Biquadratic SC Filters," *IEEE Trans. Circuits and Systems*, Vol. CAS-31, No. 11, pp. 984-987, November 1984.

- E. Sánchez-Sinencio, J. Silva-Martínez, and R.L. Geiger, "Biquadratic SC Filters with Small GB Effects," *IEEE Trans. Circuits and Systems*, Vol. CAS-31, No. 10, pp.876-884, October 1984.

- R. Castello, F. Montecchi, F. Rezzi and A. Baschirotto, "Low-Voltage Analog Filters," *IEEE Trans. on Circuits and Systems I*, Vol. 42, No. 11, pp. 827-840, November 1995.

- A. Abo, "Low Voltage, High-Speed, High-Precision Switched-capacitor Circuits," *Qualifying Exam*, University Of California at Berkeley, May 1996.



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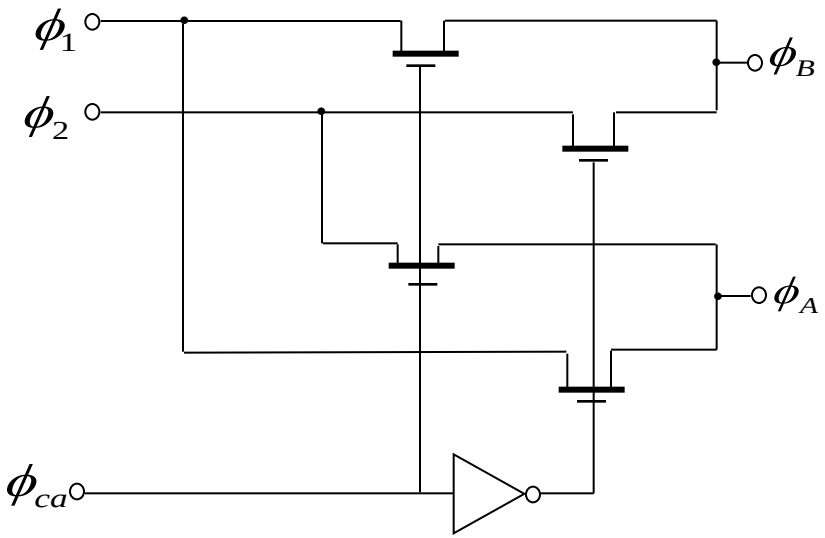
(a)



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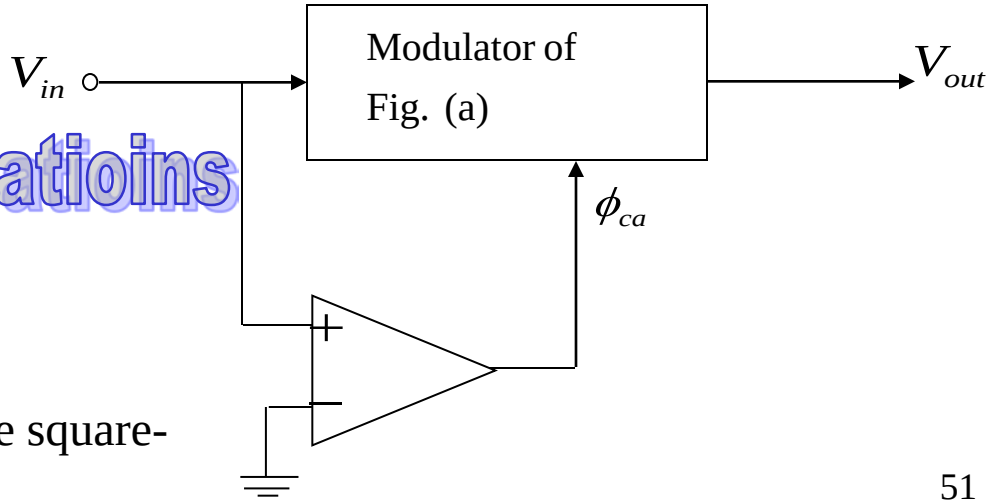

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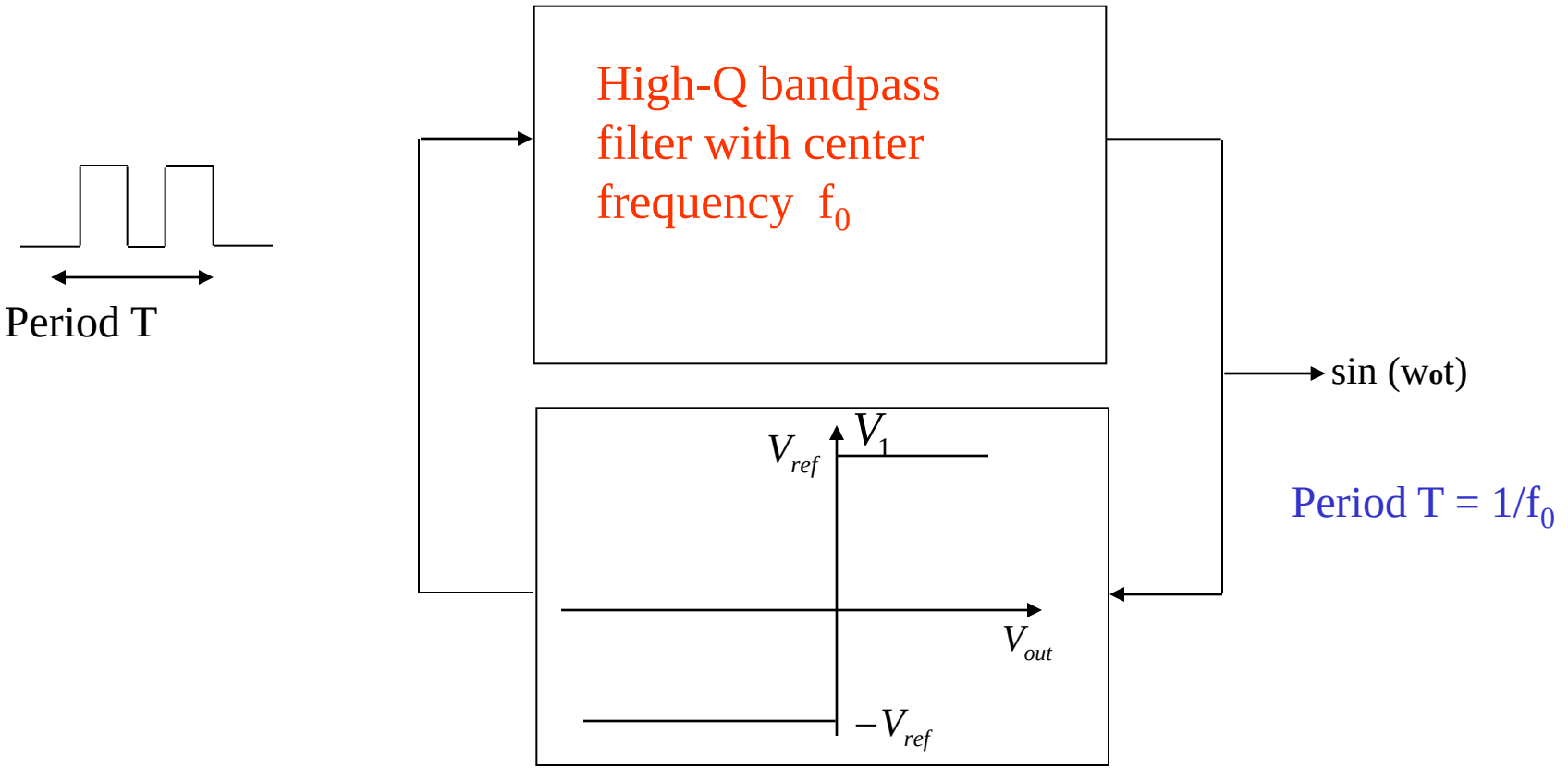

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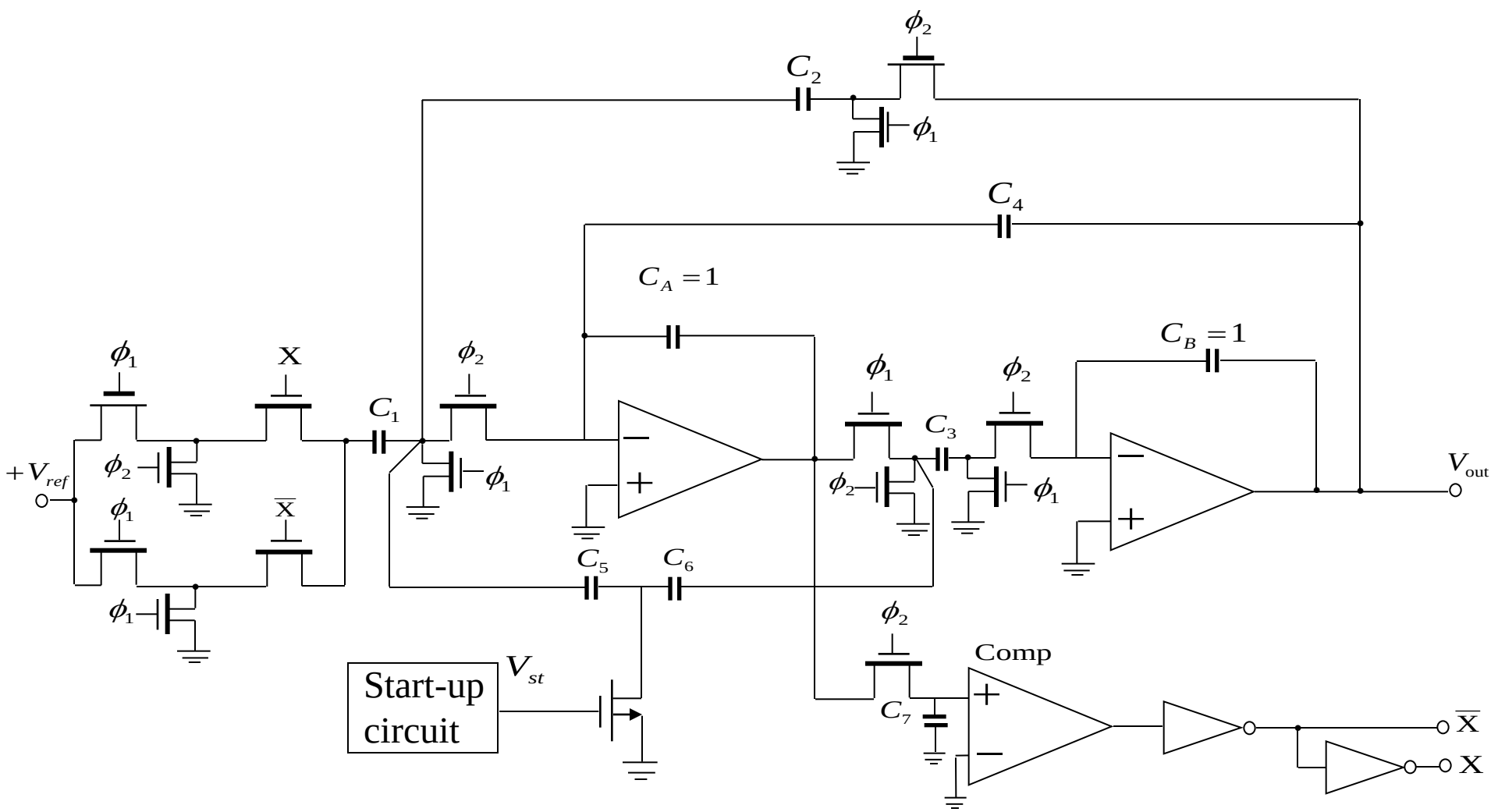

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