**HOMEWORK ASSIGNMENT #4**

Prob. 1. Design a multistage amplifier-frequency compensated (you can pick a topology different from NGCC that meets the specs of Problem 3, HW3, but uses at least 40% less power and/or reduces significantly the total compensation capacitance. You can ignore the SR requirement and use a suitable inversion level and/or different topology. Provide a detailed design procedure. Use one equation all region transistor model. Compare your results with the ones in Problem 3, HW3, include input capacitance.

Prob. 2 Using your results from Prob. 1, reduce further the power consumption by either reducing the high frequency poles and/o reducing the DC open loop gain. By doing this, your Op Amp might net be stable for a unity closed loop configuration. Thus, determine the maximum feedback ratio (less than 1) to yield a phase margin of 50 degrees. How much power was saved and what is the new GB? Provide comments and discussion

Prob. 3 Using your results of Prob. 1, design an inverter amplifier of gain = -3.
   i) Determine the ROC taking into account the input parasitic capacitance
   ii) Improve the ROC by using stray input capacitance compensation. Discuss your improvement and its tradeoffs

References:


