AMPLIFIERS

• Conventional Amplifiers
  - Two Stage Amplifier

• Amplifiers based on current buffers
  - Frequency compensation Techniques

• Feed Forward Compensation Technique

• Techniques for Wide Band Amplifiers
M1=M2; M3=M4

Ignoring zeros we can model this topology as:

\[
A_{V1}(0) \approx \frac{g_{m1}}{g_{o1} + g_{o3}} \quad \text{;} \quad A_{V2}(0) = \frac{-g_{m6}}{g_{o6} + g_{o7}} \quad \text{;} \quad \omega_p1 = g_{o2} + g_{o4} \quad \text{;} \quad \omega_p2 = \frac{g_{o6} + g_{o7}}{C_{p1}} \quad \text{;} \quad \omega_p3 \approx \frac{g_{m8}}{C_L} \\
A_{VT}(s) \approx \frac{A_{V1}(0)A_{V2}(0)A_{V3}(0)}{(1+s/\omega p1)(1+s/\omega p2)(1+s/\omega p3)} \quad \text{;} \quad \omega_p3 \approx \frac{g_{m8}}{C_L}
\]
• The low frequency voltage gain is high enough for a number of applications.

• The open loop poles are far from the origin, this can cause stability problems for closed loop applications.

• Closed loop poles might end very close to the jw axis and some in the RHP.

• How to tackle this stability problem will be discussed next.
Two-Stage Uncompensated Amplifier

Uncompensated Operational Amplifier

\[ AV = AV_1 AV_2 = \frac{g_{m2}}{g_{02} + g_{04}} \frac{g_{m6}}{g_{06} + g_{07}} \]

- Large voltage gain
- Poles are close to the jω axis causing stability problems
Employing a simple capacitor will split correctly the poles but will generate a Zero in the RHP.

Using an **RC compensation** can eliminate the zero and split poles. The resistor can be implemented with transistor in the ohmic region.

Improved internally compensated CMOS operational amplifier. Better bias for the output stage (M8 and M9)
A variation at the output stage with class–AB is shown below.

CMOS op-amp with class-AB output stage and RC pole splitting.
“Pole Splitting” can be carried out with a compensation capacitor feedback and a voltage buffer as shown below.

Two-Stage amplifier with source follower compensation scheme

- Without M12 and M11 a zero in the PRH
- With buffer (voltage follower), zero is eliminated and pole splitting (due to $C_C$) is kept.
Summary for Two Stage Op Amp Architecture Designs

• Roots close to the $j\omega$ axis for uncompensated

$$s_{p1}$$  $$s_{p2}$$

• Potentially unstable for some values of $C_L$

$$I_{bias} = C_L S_R * 2.5$$

• Improved output stage optimal bias of $Q_6$ and $Q_7$

• No significant change of pole locations.

$$A_v (0) -> +$$

$$A_v (\omega) -> -$$

Pole splitting $\Rightarrow$ one dominant pole

$$z_1$$ Phase deteriorates phase margin

The good and the bad news
Two possible solutions to cancel $z_1$ and keeping $s_{p2} > \omega_t = \text{GBW}$ and $s_{p1}$ small

Internally Compensated with $R_C C_C$

Internally Compensated with unity gain buffer $(Q_{10}, Q_{11})$

**Operational Amplifier (conventional) Architectures.**

*Reader.* See the internally Op Amp compensated with current gain buffer in previous pages
An Improved Frequency Compensation Technique for CMOS Operational Amplifiers using Current Buffers

ECEN 607 (ESS)

Courtesy of Hatem Osman
The first stage is a differential-input/single-ended output stage, and the second stage is a class A or class AB inverting output stage.

### DC Gain

\[ A_{v,0} = -A_v A_{v2} \]
\[ A_{v1} = g_{m1} r_{o1} \]
\[ A_{v2} = g_{m2} r_{o2} \]

### Transfer Function

\[ A_v = \frac{1 - C_c s}{g_{m2}} \]

### Pole/Zero locations

- **RHP zero**
  \[ s_{z} = \frac{g_{m2}}{C_c} \]

- **Dominant Pole**
  \[ s_{p1} = -\frac{1}{r_{o1} C_p + A_{v2} r_{o1} C_c + r_{o2} C_L} \approx -\frac{1}{A_{v2} r_{o1} C_c} \]

- **Non-dominant Pole**
  \[ s_{p2} = -\frac{r_{o1} C_p + A_{v2} r_{o1} C_c + r_{o2} C_L}{r_{o1} r_{o2} (C_p C_c + C_p C_L + C_c C_L)} \approx -\frac{g_{m2}}{C_L} \]
Two-Stage Op-amp with Miller compensation

- Pole Splitting

\[ V_{\text{IN},p} - g_{m1} - r_{o1} - C_p - r_{o2} - C_L - V_{\text{OUT}} \]

- Pole/zero locations

\[ s_z = \frac{g_{m2}}{C_c} \]

\[ s_{p1} = -\frac{1}{A_{\text{ro2}}r_{o2}C_C} \]

\[ s_{p2} = -\frac{g_{m2}}{C_L} \]

- Pole-zero position diagram

Increasing \( C_c \) achieves sufficient pole-splitting thus improving the PM. However, the larger \( C_c \) shifts the RHP zero to lower frequencies thus ruining the PM.
Introducing a small series resistance in series with $C_c$ may cancel the RHP zero or shift it to the LHP.

\[ R_c = \frac{1}{g_{m2}} \]

\[ R_c > \frac{1}{g_{m2}} \]

**Pole/zero locations**

\[ s_z = \frac{1}{\left(\frac{1}{g_{m2}} - R_c\right)C_c} \]

\[ s_{p1} = -\frac{A_{v2}r_{o1}C_c}{g_{m2}} \]

\[ s_{p2} = -\frac{g_{m2}}{C_L} \]

**Disadvantages:**

- To achieve a sufficient phase margin, second pole cross-over of the unity gain frequency should be avoided.

\[ f_{p2} \gg GBW \quad \Rightarrow \quad C_L \ll \frac{g_{m2}}{g_{m1}} C_c \]

Thus, the Op-amp stability is severely degraded for capacitive loads of the same order as compensation capacitor.
Improved compensation technique

- The RHP zero is a result of the feed-forward path through $C_c$.

- The RHP zero can be eliminated if we cut the feed-forward path and make the compensation capacitor unidirectional.

An Improved Frequency Compensation Technique for CMOS Operational Amplifiers

BHUPENDRA K. ARJUNA
Improved compensation technique

- The controlled current source injects AC current of $C_c \frac{dV_{out}}{dt}$ to the output of the first stage.

- DC Gain
  
  $A_{v,0} = -A_{v1}A_{v2}$
  
  $A_{v1} = g_{m1}r_{o1}$
  
  $A_{v2} = g_{m2}r_{o2}$

- Transfer Function
  
  $A_v = \frac{A_{v,0}}{1 + (r_{o1}C_p + A_{v2}r_{o1}C_c + r_{o2}(C_c + C_L))s + r_{o1}r_{o2}C_p(C_c + C_L)s^2}$

- Pole/zero locations
  
  $s_{p1} = \frac{-1}{r_{o1}C_p + A_{v2}r_{o1}C_c + r_{o2}(C_c + C_L)} \approx -\frac{1}{A_{v2}r_{o1}C_c}$

  $s_{p2} = -\frac{r_{o1}C_p + A_{v2}r_{o1}C_c + r_{o2}(C_c + C_L)}{r_{o1}r_{o2}C_p(C_c + C_L)} \approx -\frac{g_{m2}C_c}{C_p(C_c + C_L)}$

  Dominant Pole
  
  Non-dominant Pole

- To achieve sufficient PM
  
  $f_{p2} \gg GBW \rightarrow C_L \ll \frac{g_{m2}C_c^2}{g_{m1}C_p}$

- Virtual Ground
Improved compensation technique

- Numerical example

<table>
<thead>
<tr>
<th>Miller compensation with nulling resistance</th>
<th>Improved compensation technique</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dominant pole</td>
<td>Dominant pole</td>
</tr>
<tr>
<td>[ \omega_d = \frac{1}{g_{m2} r_{01} r_{02} C_c} ]</td>
<td>[ \omega_d = \frac{1}{g_{m2} r_{01} r_{02} C_c} ]</td>
</tr>
<tr>
<td>Non-dominant pole</td>
<td>Non-dominant pole</td>
</tr>
<tr>
<td>[ \omega_{nd} = \frac{g_{m2}}{C_L} ]</td>
<td>[ \omega_{nd} = \frac{g_{m2} C_c}{C_p (C_c + C_L)} ]</td>
</tr>
<tr>
<td>Gain-bandwidth product</td>
<td>Gain-bandwidth product</td>
</tr>
<tr>
<td>[ GBW = \frac{g_{m1}}{C_c} ]</td>
<td>[ GBW = \frac{g_{m1}}{C_c} ]</td>
</tr>
<tr>
<td>Phase margin</td>
<td>Phase margin</td>
</tr>
<tr>
<td>[ PM = 90 - \tan^{-1}\left(\frac{GBW}{\omega_{nd}}\right) ]</td>
<td>[ PM = 90 - \tan^{-1}\left(\frac{GBW}{\omega_{nd}}\right) ]</td>
</tr>
</tbody>
</table>

- If \( \frac{g_{m2}}{g_{m1}} = 10, C_c = 5 \text{ pF}, C_p = 0.5 \text{ pF}, \) and \( \frac{\omega_{nd}}{GBW} \geq 4 \) for \( PM > 75^\circ \)

\[ C_L \leq \frac{GBW}{\omega_{nd}} \frac{g_{m2}}{g_{m1}} C_c \rightarrow C_L \leq 12.5 \text{ pF} \]

\[ C_L \leq \frac{GBW}{\omega_{nd}} \frac{g_{m2} C_c^2}{g_{m1} C_p} \rightarrow C_L \leq 125 \text{ pF} \]

- The improved technique offers an order of magnitude improvement in capacitive load capability for the same performance.
Circuit Implementation

- Miller compensation with nulling resistance.

- Improved compensation technique.
Other performance parameters- PSR

- Miller compensation with nulling resistance.

\[ \frac{V_{OUT}}{V_{SS}} = \frac{1 + sA_{V,0}C_c C_R}{g_{m1}g_{m2}f \omega 1 + s} \]

- Improved compensation technique.

\[ \frac{V_{OUT}}{V_{SS}} = \frac{1 + sC_p f \omega 1}{g_{m1}g_{m2}f \omega 1 + s\left(1 + \frac{s}{GBW}\right)} \]

- Better PSR at high frequencies.
Design Example – Miller Compensation

- Design an OTA with GBW $> 5$MHz, $C_L = 10$pF, PM$> 70^\circ$, and SR$> 2$ V/µs.

  - Choose $C_c = C_L/2 = 5$ pF.
  - GBW $> 5$MHz
    \[
    GBW = \frac{g_{m1}}{C_c} \rightarrow g_{m1} \geq 157 \mu S
    \]
  - SR $> 2$ V/µS
    \[
    SR = \frac{l_{p,0}}{C_c} \rightarrow l_{p,0} \geq 20 \mu A
    \]
  - PM $> 70^\circ$
    \[
    PM = 90 - \tan^{-1}\left(\frac{GBW}{\omega_{nd}}\right) \rightarrow \omega_{nd} \geq 2.7GB
    \]

  Let
  \[
  \omega_{nd} = 3 \times GBW = \frac{g_{m2}}{C_L} \rightarrow \frac{g_{m2}}{g_{m1}} = 3 \frac{C_L}{C_c} = 6
  \]

  Then
  \[
  g_{m2} = 6g_{m1} \approx 1 \text{ mS} \rightarrow l_{p,2} = 3l_{p,0}
  \]

  - Choose $R_c > 1/g_{m2}$
    \[
    R_c \geq 1 \text{ KΩ}
    \]
Design Example – Miller Compensation

- Simulation results
  - OL Transfer function
  - Negative supply rejection
  - Positive supply rejection
  - Transient step response
Design Example – Miller Compensation

- Capacitive load driving capability

- PM $> 70^\circ$ for $C_L < 15$ pF.
Design Example – Improved Compensation

• Design an OTA with $\text{GBW} > 5\text{MHz}$, $C_L = 10\text{pF}$, $PM > 70$, and $SR > 2\text{V/µs}$.

  • Choose $C_c = C_L/2 = 5\text{ pF}$.
  • $\text{GBW} > 5\text{MHz}$
  
  \[
  \text{GBW} = \frac{g_m}{C_c} \rightarrow g_m \geq 157\ \mu S
  \]

  • $SR > 2\text{V/µs}$

  \[
  SR = \frac{I_{p0}}{I_{p0}} \rightarrow I_{p0} \geq 20\ \mu A
  \]

  In order to make the current transformer biased during slewing interval

  \[
  I_{p3} > I_{p0} \rightarrow I_{p3} = 30\ \mu A
  \]

  • $PM > 70^\circ$

  \[
  PM = 90 - \tan^{-1}\left(\frac{GBW}{\omega_{nd}}\right) \rightarrow \omega_{nd} \geq 2.7\text{GBW}
  \]

  Let

  \[
  \omega_{nd} = 3 \times GBW = \frac{g_m^2 C_c}{C_p (C_c + C_L)} \rightarrow \frac{g_{m2}}{g_{m1}} = 0.3
  \]

  Then

  \[
  \frac{g_{m2}}{g_{m1}} = 0.3 \geq 52\ \mu S \rightarrow I_{p,2} = 0.3 I_{p,0}
  \]

  ✓ Let’s use $g_{m2} = 6g_{m1}$ like the Miller Op-amp to make a comparison between the capacitive driving capability.

  ✓ For the same capacitive load driving capability, the second stage will consume less current making it suitable for low power applications.
Design Example – Improved Compensation

- Simulation results

[Graphs showing OL Transfer function, Negative supply rejection, Positive supply rejection, Transient step response]
Design Example – Improved Compensation

• Capacitive load driving capability

• PM > 70° for $C_L < 100 \text{ pF}$. 
## Design Example – Improved Compensation

### Summary of Simulation results

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Spec</th>
<th>Miller Compensation</th>
<th>Improved Compensation</th>
</tr>
</thead>
<tbody>
<tr>
<td>GBW</td>
<td>&gt; 5MHz</td>
<td>5.5 MHz</td>
<td>6 MHz</td>
</tr>
<tr>
<td>PM</td>
<td>&gt; 70°</td>
<td>75°</td>
<td>87.6°</td>
</tr>
<tr>
<td>SR⁺</td>
<td>&gt; 2 V/µs</td>
<td>2.75 V/µs</td>
<td>3 V/µs</td>
</tr>
<tr>
<td>SR⁻</td>
<td>&gt; 2 V/µs</td>
<td>3 V/µs</td>
<td>3.15 V/µs</td>
</tr>
<tr>
<td>PSR⁻</td>
<td>-</td>
<td>-65.6 dB At (0-3.1 kHz)</td>
<td>-51.9 dB At (0-245.4 kHz)</td>
</tr>
<tr>
<td>PSR⁺</td>
<td>-</td>
<td>-97.2 dB At (0-44 kHz)</td>
<td>-37.2 dB At (0-538.9 kHz)</td>
</tr>
<tr>
<td>DC gain</td>
<td>-</td>
<td>64.5 dB</td>
<td>51.3 dB</td>
</tr>
<tr>
<td>Current consumption</td>
<td>-</td>
<td>80 µA</td>
<td>110 µA</td>
</tr>
<tr>
<td>Capacitive load driving capability</td>
<td>-</td>
<td>PM &gt; 70° for $C_l &lt; 15$ pF</td>
<td>PM &gt; 70° for $C_l &lt; 100$ pF</td>
</tr>
</tbody>
</table>

- **GBW**: Gain Bandwidth
- **PM**: Phase Margin
- **SR⁺**: Rise Time
- **SR⁻**: Fall Time
- **PSR⁺**: Positive PSR
- **PSR⁻**: Negative PSR
- **DC gain**: DC Gain
- **Current consumption**: Current Consumption
- **Capacitive load driving capability**: Capacitive load driving capability
Using another **current buffer Op Amp topology**.

Two-Stage amplifier with Current Buffer compensation scheme.

- Improve SR at the expense of power consumption.
Differential Output Two Stage Amp with a capacitor compensation with a current Buffer (Common Gate)

\[ p_1 \approx -\frac{1}{g_{m5}R_LR_{\alpha A}C_c} \cdot \]

\[ p_2 \approx -\frac{g_{m5}}{(C_L + C_c) C_A} \frac{C_c}{C_B + C_c} \cdot \]

\[ z \approx \frac{g_{m7}}{C_B + C_c} \cdot \]

\[ g_{m7} \to \infty \text{ then } p_3 \to \infty \]
Differential mode half circuit of previous topology

![Circuit Diagram]

<table>
<thead>
<tr>
<th>Element</th>
<th>Fig. 1(a)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{oA}$</td>
<td>$r_{o1}</td>
</tr>
<tr>
<td>$C_A$</td>
<td>$C_{gs5} + C_{db1} + C_{db3} + C_{db7}$</td>
</tr>
<tr>
<td>$R_{oB}$</td>
<td>$\infty$ *</td>
</tr>
<tr>
<td>$C_B$</td>
<td>$C_{gs7} + C_{sb7}$ **</td>
</tr>
<tr>
<td>$R_I$</td>
<td>$r_{o5}$</td>
</tr>
<tr>
<td>$C_L$</td>
<td>$C_{db5}$</td>
</tr>
</tbody>
</table>
Note that this and previous structure are fully differential but this approach could be used for single output topologies.

Compensation using a current buffer (current gain)

Note that the current-mirror introduces an extra inversion which must be taken into consideration for the single ended version.

P.J. Hurst, Lewis, S.H.; Keane, J.P.; Aram, F.; Dyer, K.C.

<table>
<thead>
<tr>
<th>Element</th>
<th>Description</th>
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<tbody>
<tr>
<td>$R_{oA}$</td>
<td>$r_{o1}</td>
</tr>
<tr>
<td>$C_A$</td>
<td>$C_{gs0} + C_{db1} + C_{dbs} + C_{dz1}$</td>
</tr>
<tr>
<td>$R_{oB}$</td>
<td>$r_{eg}$</td>
</tr>
<tr>
<td>$C_B$</td>
<td>$C_{gs9} + C_{gs11} + C_{dbs}$ **</td>
</tr>
<tr>
<td>$R_L$ ***</td>
<td>$r_{o5}$</td>
</tr>
<tr>
<td>$C_L$ ****</td>
<td>$C_{db5}$</td>
</tr>
</tbody>
</table>

$z \approx -\frac{g_{m11}}{C_B + C_C}$.

Besides the above zero the amp has three poles.

**Elements of Current-Mirror Cc compensated**

*Note that the common-gate and current mirror topologies under ideal case are almost identical, however in practice the one using current-mirrors is more power hungry and has a larger parasitic capacitance $C_B$*
Folded Cascode, Two stage and Class A/AB two stage Amplifiers

Fig. 3. (a) Folded cascode amplifier, (b) two-stage class A amplifier, and (c) two-stage class A/AB amplifier.
Techniques for Wideband Amplifiers
Focus the improvement in the load of the differential pair

Conventional

Current Mirror at the output load

Wideband Alternative

Frequency Dependent Current Mirror (FDCM)

\[ R \]

\[ C_F \]

\[ I_b \]

\[ C_F \]

Low Frequency Behavior

High Frequency Behavior

\[ C_F >> C_{gs} \]

\[ 0.1K < R < 1K \]

An example of its use:

Wideband Amplifier with Feedforward Technique

- What is the optimal value of $R_1$ as a function of $G_{mp3}$?
- $C_{F1}$ bypasses two current mirrors.
- $C_{F2}$ is fed forward to the input of another FDCM and signal is amplified.
Next, we discuss different families of wideband reported in the literature.


An alternative is to connect $C_F$ instead to nodes B to nodes A.
Folded-Cascode Wideband Amplifier

- Conventional Folded-Cascode (FC)
- FC with Capacitive Feedforward

Differential Wideband Amplifier

Fig. 1 Transconductance Amp
Basic Structure based on current-mode

\[ i_R = \frac{\text{Vin}}{R} \]
\[ i_X = -i_R \]
\[ I_B > i_R \]

Fig. 2
Pseudo Differential Op Amp

Fig 3 VCVS Amplifier:  Op Amp


Very low-voltage analog signal processing based quasi-floating gate transistors, J

Low threshold CMOS circuits with low standby current

A dynamic threshold voltage MOSFET (DTMOS) for ultra low voltage operation Assaderaghi, F.; Sinitsky, D.; Parke, S.; Bokor, J.; Ko, P.K.; Chenming Hu;

Resizing rules for MOS analog-design reuse
Galup-Montoro, C.; Schneider, M.C.; Coitinho, R.M.;
Design & Test of Computers, IEEE , Volume: 19 , Issue: 2 , March-April 2002 Pages:50 - 58


Series-parallel association of FET's for high gain and high frequency applications


This reference discusses three different Op Amp topologies:
