A 6b 10GS/s TI-SAR ADC with Embedded 2-Tap FFE/1-Tap DFE in 65nm CMOS

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Abstract

A 64-way time-interleaved successive approximation based ADC front-end efficiently incorporates a 2-tap embedded FFE and a 1-tap embedded DFE, while achieving 4.56-bits peak ENOB at a 10GS/s sampling rate. Fabricated in 1.1V 65nm CMOS, the ADC with embedded equalization achieves 0.48 pJ/conv.-step FOM, while consuming 79.1mW and occupying 0.33mm^2 core ADC area.

Keywords: ADC, ADC-based receiver, DFE, embedded equalization, FFE, SAR, time interleaving.

Introduction

ADC-based receivers for wireline applications allow for implementing flexible, complex, and robust equalization in the digital domain [1], as well as easily supporting bandwidth-efficient modulation schemes, such as PAM4 and duobinary. However, front-end baud-rate ADCs can consume a significant percentage of the system power. Embedded analog equalization can reduce ADC resolution requirements [2] and allow for overall lower receiver power consumption, provided a low-overhead implementation. A recent example of this is the work of [1], where a pre-ADC continuous-time high-pass filter (HPF) is used in combination with a sampled feed-forward equalizer (FFE) that follows the flash ADC track-and-holds (T/H). However, this approach requires additional CML input stages which add to the ADC power. This work presents a 10GS/s 6b ADC which efficiently incorporates both a 2-tap embedded FFE and a 1-tap embedded decision feedback equalizer (DFE) directly into the capacitive DAC (CDAC) of a time-interleaved successive approximation register (SAR) ADC which further optimizes power through the use of dual voltage supplies.

ADC Architecture with Embedded FFE and DFE

Fig. 1 shows the 64-way time-interleaved SAR ADC block diagram with embedded equalization. The 10GS/s converter consists of eight parallel sub-ADCs, where each sub-ADC is formed by a front-end T/H clocked at 1.25GHz and followed by eight unit SAR ADCs. A differential divide-by-four circuit is used with a 5GHz input clock to generate eight clock phases spaced at 100ps. Digitally controlled capacitor banks, with a 0.5ps resolution and 36ps range, are employed to calibrate timing mismatches in the clock distribution to the T/H blocks. A source-follower based T/H with PMOS inputs and bootstrapped front-end sampling switches is used.

The conceptual implementation of the proposed embedded 2-tap FFE and 1-tap DFE is depicted in Fig. 2 during each SAR cycle. A two-tap discrete-time FFE [3] is realized with the cursor tap having a gain of unity for the current ADC input sample, while the post-cursor tap coefficient β for the previous sample is set with the SAR CDAC weighting during the sampling phase. In order to efficiently embed the 1-tap DFE, a redundant cycle approach [4] is used where the MSB is calculated for both +α and −α as the DFE tap coefficient during two consecutive cycles. At the end of second MSB cycle the correct coefficient is decided based on the previous ADC channel MSB using a MUX, and five cycles follow to compute the remaining bits. Compared to a loop-unrolled DFE approach, this redundant cycle approach utilizes roughly half the CDAC and comparator circuitry, while only increasing the total 6-bit conversion time by a factor of 8/7.

Fig. 3 shows the implementation of each unit SAR ADC with embedded FFE and DFE. A 4-input comparator is used, with one input connected to sample capacitors, C_S, and the other input connected to the CDAC. Utilizing the C_S capacitor, the current input sample from the main T/H$_{(n)}$ forms the FFE first tap with unity gain, while DFE ISI subtraction is performed by connecting the other C_S terminal to a shifted common-mode voltage during subsequent cycles. The other input from the binary CDAC forms the FFE post-cursor tap and the SAR reference voltage levels. During the sampling phase the previous signal held at the output of T/H$_{(n-1)}$ is sampled on part of the binary CDAC, with the weighting determining the FFE post-cursor coefficient β, while the rest of the DAC capacitors that are used to set the SAR reference levels are discharged to zero. When the sampling phase of the previous unit ADC channel ends, charge sharing in the CDAC combines the post-cursor FFE tap and the SAR reference levels. Small custom-designed unit 0.45fF metal flux capacitors are utilized for a relatively low area implementation and to reduce the CDAC switching power and the power of common-mode and reference voltage buffers. A 4-input modified StrongArm comparator with 6-bit current-steering offset calibration DACs [4] is used to calibrate the unit-ADC offset at a resolution of 4mV. Also, comparator metastability issues are addressed with a metastability detector and correction circuit [5]. While the T/Hs, CDAC switches, and voltage buffers operate with a 1.1V supply, the total power consumption is decreased by reducing the supply voltage of comparators and SAR logic to LV_{DD}=0.9V in the core time-interleaved ADC.

Experimental Results

The GP 65nm CMOS die micrograph, where the unit ADCs order is optimized in the floorplan to reduce the 1-tap DFE critical delay path, is shown in Fig. 4. Setting the embedded FFE post-cursor and DFE coefficients to zero, the measured post-calibration SNDR and SFDR of the 10GS/s 6b ADC are shown in Fig. 5. A low input frequency maximum SNDR of 29.19dB is achieved, which translates to 4.56 bits ENOB, and the effective resolution bandwidth (ERBW) is 4.5GHz.

Fig. 6 shows post-ADC quantized eye diagrams for 10Gb/s 2^{10}-1 PRBS data passed through a 10-inch FR4 channel. Due to ISI, disabling the ADC embedded equalization results in a closed eye and all 64 codes being present. Independently activating the 1-tap DFE and 2-tap FFE results in a timing margin of 0.23UI and 0.41UI, respectively. Enabling both embedded FFE and DFE improves the timing margin to 0.5UI and the quantized eye opening to 19 LSB, which verifies the effectiveness of the proposed implementation.

Table I summarizes the performance of the 6-bit 10GS/s ADC with a 2-tap embedded FFE and a 1-tap embedded DFE and compares this work against similar previous systems in the 10GS/s range. The ADC, including the front-end T/Hs, clock generation, voltage buffers, and calibration circuitry, consumes 79.1mW total power, achieving a 0.48 pJ/conv.-step FOM. Overall, the proposed design performance is comparable to the state-of-the-art design of [6], which does not include embedded equalization, and includes an increased amount of embedded equalization options relative to [1]. The total ADC area, including clock phase generation, front-end T/H array, and voltage buffers is 0.52mm^2, with the core ADC occupying 0.33mm^2.

Acknowledgments

The authors would like to thank the SRC for supporting this research under grant 1836.040 and TI for chip fabrication.

References

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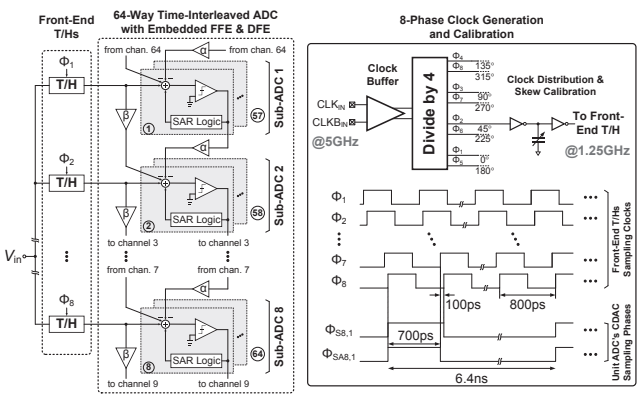


Fig. 1. Time-interleaved ADC with embedded FFE and DFE.

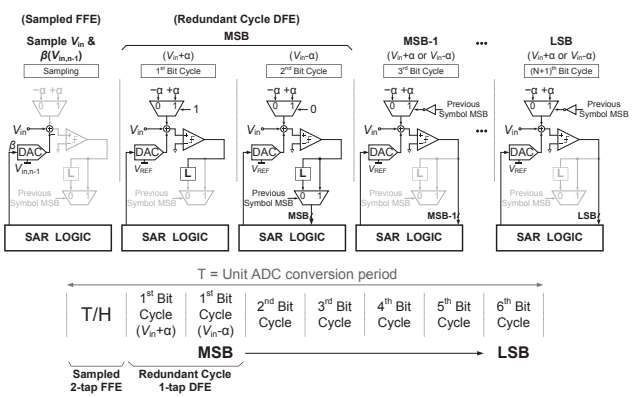


Fig. 2. Conceptual embedded FFE/DFE phases of operation.

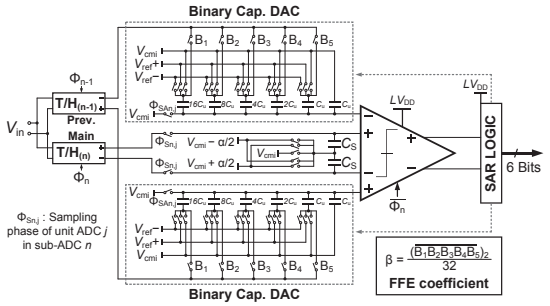


Fig. 3. Unit ADC implementation with embedded FFE and DFE.

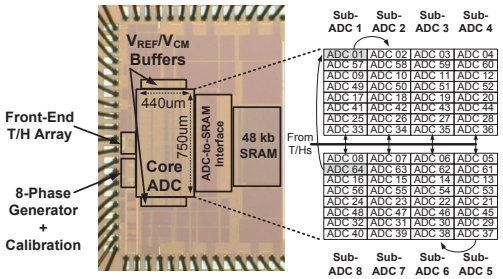


Fig. 4. Micrograph of the ADC with embedded FFE/DFE.

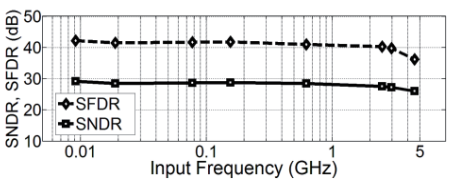
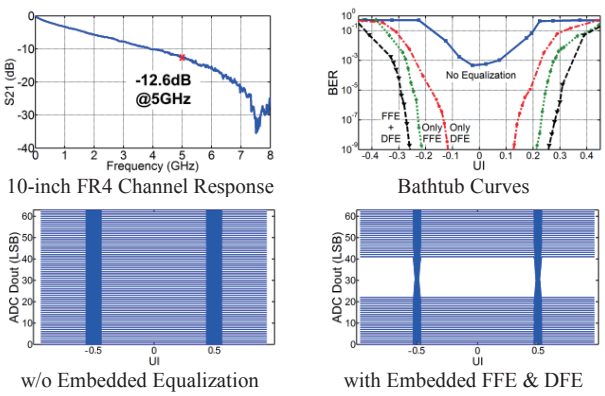


Fig. 5. ADC dynamic performance at f_s = 10GHz.



10-inch FR4 Channel Response | Bathtub Curves

w/o Embedded Equalization | with Embedded FFE & DFE

Fig. 6. Channel response and measured functionality of embedded FFE/DFE for a 10Gb/s 2^{10}-1 PRBS input through a 10-inch FR4 channel.

TABLE I: PERFORMANCE SUMMARY

Specification	[6]	[1]	This Work
Technology	65nm	65nm	65nm
Power Supply	1.1V	1.1V	1.1V/0.9V
ADC Structure	TI-Flash	TI-Flash	TI-SAR
Equalization	No	HPF + FFE	Embedded FFE + DFE
Sampling Rate	12 GS/s	10 GS/s	10 GS/s
Resolution	5 bits	4 bits	6 bits
ENOB @ ERBW	3.88 bits	N/A	4.03 bits
Input Range	590 mV_{pp}	600 mV_{pp}	500 mV_{pp}
FOM ($P/2^{ENOB}.f_s$)	0.46 pJ/c.-s.	N/A	0.48 pJ/c.-s.
Area	0.44 mm^2	0.29 mm^2	0.52 mm^2
Power	81 mW	93 mW*	79.1 mW

* This value includes the clock and analog front-end power consumption.