A 10 Gb/s 2-IIR-Tap DFE Receiver with 35 dB Loss Compensation in 65-nm CMOS

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Abstract

A serial I/O receiver efficiently implements a decision feedback equalizer (DFE) employing 2 IIR taps for improved long-tail ISI cancellation. The use of a modified multi-input two-stage slicer allows for both DFE summation to be performed directly at the slicer and optimization of the first-tap IIR filter/mux feedback path to allow for cancellation of the critical first post-cursor. Fabricated in GP 65-nm CMOS, the receiver occupies 0.0304 mm^2 area and consumes 9.9 mW while operating at a BER<10^{-12} for 10 Gb/s data passed over a 40-inch FR4 channel with 35 dB loss at 5 GHz.

Keywords: serial link, receiver, decision feedback equalizer, infinite impulse response (IIR) DFE.

Introduction

Increasing serial I/O data rates over high-loss channels necessitate efficient approaches to ISI cancellation at the receiver. While receivers with DFEs are now in wide use, architectures which employ a common FIR feedback filter require an ever-growing number of taps to cancel the long-tail ISI found in typical backplane channels. In order to address this, DFEs with IIR feedback filters have been implemented and shown to improve equalization efficiency for RC-limited and backplane channels [1-3]. A key challenge associated with these architectures involves optimizing the critical IIR feedback path to allow for ISI cancellation beginning at the first post-cursor. Also, while the use of multiple IIR taps can provide for further ISI cancellation [4], the IIR tap number should be carefully chosen in order to avoid excessive area and power consumption. This work presents a decision feedback equalizer (DFE) employing 2 IIR taps that allows for improved long-tail ISI cancellation. First post-cursor ISI cancellation is efficiently achieved through the use of a modified multi-input two-stage slicer that allows for both DFE summation to be performed directly at the slicer and optimization of the IIR filter/mux feedback path.

System Architecture

The 10 Gb/s pulse response of a 20 inch backplane channel [5], Fig. 1(a), shows that the postcursor ISI can be approximated by two decaying exponential functions; a fast-decaying short-tail term with time constant τ_1 and a slow-decaying long-tail term with time constant τ_2. IIR feedback filters which generate this long-tail behavior are very efficient in cancelling this ISI when used in a DFE, as shown in the peak distortion analysis of Fig. 1(b) where two IIR taps provide the same amount of ISI cancellation as 15 FIR feedback taps. However, adding extra IIR taps doesn't yield significant improvements in ISI cancellation. Eye diagram simulations, shown in Fig. 1(c) and (d), confirm that increasing from one to two IIR taps offers improvements in both eye height and width due to the additional degree of freedom provided to better match the pulse response.

Fig. 2 shows the proposed half-rate DFE receiver with two IIR taps. Here the first IIR tap is placed at the first post-cursor location to cancel the initial high-amplitude fast-decaying ISI tail. As this IIR tap only must cancel this fast-decaying ISI, this allows a short IIR filter time constant and a reduction in the required tap current. Rather than placing the second IIR tap also at the first post-cursor location, as was done in [4], it begins cancelling the slow-decaying long-tail ISI at the third post-cursor. This eliminates an additional 1 UI critical feedback path and also reduces the required current in the second IIR filter tap.

Circuit Implementation

A detailed schematic of the slicer and optimized first IIR tap filter/mux is shown in Fig. 3. Here a double-tail comparator [6] is modified to perform both the DFE summation and slicing operations. Current summation is performed in the first stage by utilizing three differential pairs controlled by the main input signal and the two IIR feedback taps. The use of a two-stage comparator provides two critical benefits for optimizing the critical first IIR tap feedback path: 1) Smaller input transistors, relative to a single-stage comparator, allow for reduced loading on the feedback IIR filter and improves the DFE critical path delay. 2) As both signals which comprise the comparator's differential output are low during the pre-charge phase, this allows for the mux function to be more efficiently combined with the IIR filter. Here the half-rate (I and Q) slicer outputs are multiplexed to full-rate in the optimized first-tap IIR filter/mux by the alternating pre-charge states of the I and Q slicers. Relative to the IIR filter/mux design of [2], this allows for the removal of the CLK transistor from the stack-up, resulting in reduced critical path delay and increased summation time and reduced current levels for the first IIR feedback tap. While the IIR filter/mux implementation ensures that the output common mode is fixed and independent of both the tap weight and feedback data, any static mismatch in the comparator's three common-mode input voltages can result in a static gain error. Thus, sufficient tap current range is provided to compensate for this. The first IIR tap time constant can be adjusted by changing C_d and R_d, with tuning range between 0.5 T_b and 2 T_b at 10 Gb/s, while the second IIR tap has a tuning range between 0.5 T_b and 5 T_b. Note that the second IIR filter/mux includes a clocked transistor in the circuit stack-up, as the driving flip-flop does not have a pre-charge state.

Experimental Results

Fig. 4(a) shows the chip micrograph of the 2-IIR-Tap DFE receiver, which was fabricated in a GP 65nm CMOS process and occupies an area of 0.0304 mm^2. The channels used to evaluate the receiver performance are shown in Fig. 4(b), with the 20, 30, 35, and 40 inch FR-4 PCB traces having loss of 18 dB, 24 dB, 28 dB and 33 dB at 5 GHz, respectively. Not shown is the additional ~2 dB loss at 5 GHz due to the chip package and additional short test-board traces. 700 mV_{ppd} 10 Gb/s data is transmitted over these channels and BER bathtub curves are obtained for two cases; with only the first IIR tap enabled and with both the IIR taps enabled. Testing with a PRBS31 pattern, there is not much performance difference for the lowest-loss

20 inch channel, with the two IIR case achieving 0.09 UI additional eye width. However, repeating this with the 30 inch channel shows an improvement of 0.18UI. While the receiver was not able to support PRBS31 for the 35 inch channel, PRBS10 data was successfully received, with the two IIR tap case improving the eye width by 0.24 UI. For the longest 40 inch channel the receiver could only support PRBS7 data, and a 0.07UI improvement is achieved with the second IIR tap. Table I summarizes the receiver performance and compares this work against other DFE-IIR designs. The presented receiver consumes 9.9mW at 10Gb/s and is able to support a BER<10^{-12} for the highest loss channel among these designs.

Acknowledgments

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References

[1] E. Mensink, et al., "A 0.28pJ/b 2Gb/s/ch transceiver in 90 nm CMOS for 10 mm on-chip interconnects," *ISSCC* 2007.

[2] B. Kim, et al., "A 10-Gb/s compact low-power serial I/O with DFE-IIR equalization in 65-nm CMOS," *JSSC,* vol. 44, no. 12, Dec. 2009.

[3] Y.-C. Huang and S.-I. Liu, "A 6 Gb/s receiver with 32.7 dB adaptive DFE-IIR equalization," *ISSCC* 2011.

[4] S. Shahramian, et al., "Decision Feedback Equalizer Architectures With Multiple Continuous-Time Infinite Impulse Response Filters," *TCAS II*, vol.59, no.6, June 2012.

[5] IEEE P802.3ap Task Force Channel Model Material, http://www.ieee802.org/3/ap/public/channel_model.

[6] D. Schinkel, et al., "A Double-Tail Latch-Type Voltage Sense Amplifier with 18ps Setup+Hold Time," *ISSCC 2007.*

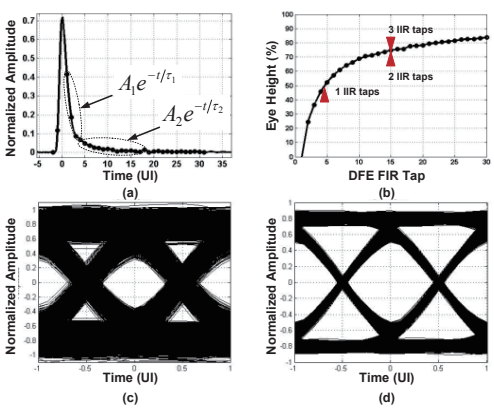

Fig. 1. (a) Simulated 10Gb/s pulse response of a 20" backplane channel [5]. (b) Eye height from peak distortion analysis versus DFE FIR feedback tap number. Simulated equalized 10Gb/s eye diagrams using: (c) one IIR tap, (d) two IIR taps.

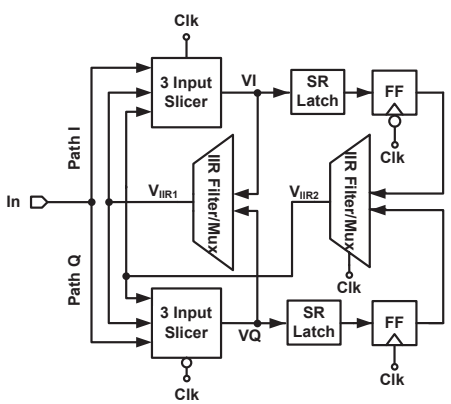

Fig. 2. Proposed 2-IIR-tap DFE receiver architecture.

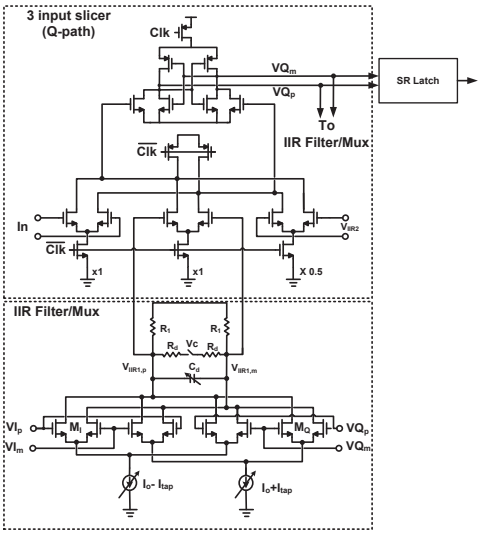

Fig. 3. Circuit realization of the DFE first IIR tap feedback path.

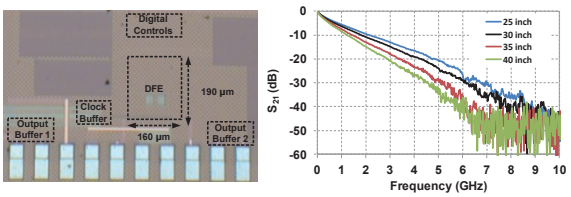

Fig. 4. (a) DFE receiver micrograph. (b) Channels' S_{21} responses.

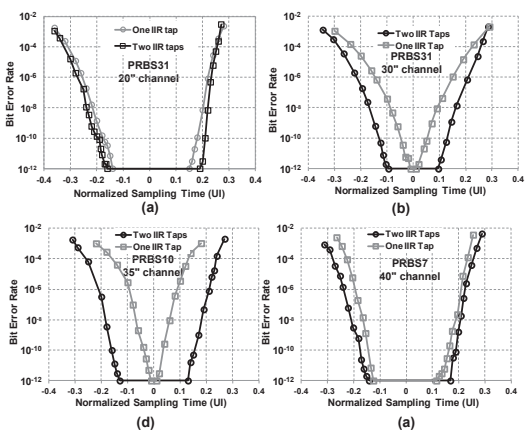

Fig. 5. Equalized BER bathtub curves using one IIR tap and two IIR taps for: (a) 20" and (b) 30" channels with PRBS31, (c) 35" channel with PRBS10, and (d) 40" channel with PRBS7.

TABLE I: PERFORMANCE SUMMARY

Specification	This Work	[2]	[3]	[4]
Data Rate	10 Gb/s	10 Gb/s	6 Gb/s	3.7 Gb/s
Architecture	2-IIR tap	1-IIR tap	1-IIR tap	3-IIR tap
Channel Loss @ Nyquist	35* dB	27* dB	32.7 dB	8 dB
Eye width BER PRBS Code	31 % 10^{-12} PRBS7	28 % 10^{-9} PRBS7	NA 10^{-12} PRBS7	6 % 10^{-12} PRBS7
Supply (V)	1	1	NA	1.2
Power (mW)	9.9	7	4	17.3
Area (mm^2)	0.0304	0.0175	0.089**	0.0535
Technology	65-nm	65-nm	90-nm	130-nm

* Including ~2 dB of setup loss.
** Include the area of a whole receiver.