Sequential Correlated Level Shifting: A Switched-Capacitor Approach for High-Accuracy Systems

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***Abstract*—Analog circuit accuracy is severely limited by finite and nonlinear opamp gain. For switched-capacitor circuits, correlated level shifting (CLS) is an effective technique to improve system accuracy with negligible additive noise. A modification of this method, called sequential CLS, is introduced in this brief, which provides dramatic increases in the effective accuracy of a switched-capacitor structure. Measurements of prototype sample-and-hold structures utilizing simple single-stage opamps in an LP 90-nm CMOS technology show that at the same power and area consumption, the proposed modification can improve the settling accuracy of simple CLS from 5.8 to 8.8 bits with two additional sequential steps.**

***Index Terms*—Correlated level shifting (CLS), sample-and-hold (S/H) circuits, sequential CLS (SCLS).**

I. Introduction

FINITE and nonlinear swing-dependent opamp gain can severely limit performance in high-precision analog circuits. These shortcomings become more apparent in newer CMOS technologies, mainly due to reduced supply voltages and reduced metal–oxide–semiconductor field-effect transistor (MOSFET) intrinsic gain.

Fig. 1 shows the schematic of a conventional flip-around switched-capacitor sample-and-hold (S/H). The input–output characteristic of this block is

$$V_{\text{out}} = V_{\text{in}} - \left(1 + \frac{C_{\text{ip}}}{C_F}\right)\frac{V_{\text{out}}}{A} \tag{1}$$

where C_{ip} is the parasitic capacitance at the opamp input, and A is the opamp low-frequency gain, which is, in practice, dependent on the voltage swing.

Various approaches have been developed to address the error term in (1) due to the finite opamp gain. The work in [1] proposes techniques to subtract the gain error in each pipeline stage of a pipeline analog-to-digital converter (ADC) either in the analog or digital domain. In [2]–[4], correlated double sampling (CDS)-based methods are presented for pipelined ADCs. While these methods can reduce this error term, they neglect the error due to nonlinear dependence of gain on the output swing. Correlated level shifting (CLS) techniques alleviate the nonlinear gain issue by decreasing the opamp output swing during the final amplification phase [5], [6].

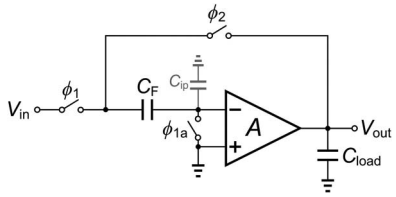

Fig. 1. Flip-around switched-capacitor S/H.

In spite of the advantages of this CLS method, achieving medium-to-high accuracies in nanometer CMOS technologies remains difficult with simple and robust opamp topologies. Some CLS modifications have been proposed in [7] and [8]. The split-CLS technique [7] uses two amplifiers, i.e., one with large swing and bandwidth for the estimation phase and one with large gain for the level shifting phase. However, the improved accuracy is still limited to one level shifting phase. In [8], a modified CLS method with two level shifting capacitors in series is proposed. Although this technique increases the effective gain of the switched-capacitor structure, similar to the proposed method in this brief, expanding [8] to more than two series capacitors is not practical due to the parasitics.

This brief presents a sequential CLS (SCLS) technique that allows for the use of simple single-stage opamps and significantly improves circuit accuracy relative to conventional CLS methods at the same power and area consumption. The conventional CLS technique is reviewed and analyzed with a simplified, but accurate, low-speed feedback analysis approach in Section II. Section III details the proposed SCLS approach, which nests additional level shifting capacitor operations for improved accuracy. Two different flip-around switched-capacitor S/H circuits are designed using CLS and 3xCLS configurations, with experimental results from an LP 90-nm CMOS prototype presented in Section IV. Finally, Section V concludes this brief.

II. CLS

A. Basic Structure

Fig. 2 shows a flip-around switched-capacitor S/H that includes CLS [5]. The S/H requires three phases of operation,

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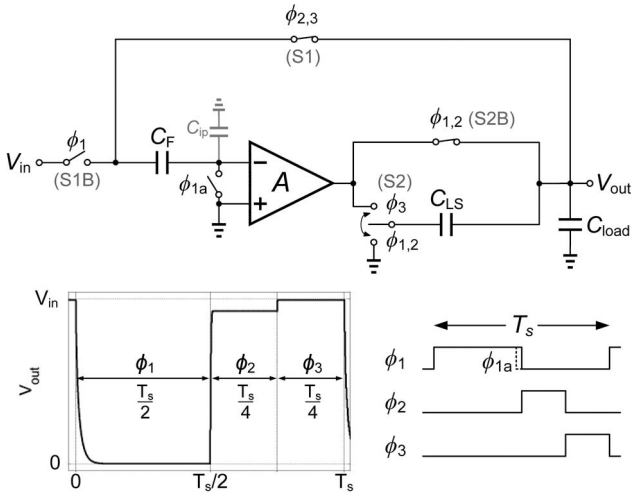

Fig. 2. Flip-around switched-capacitor S/H with conventional CLS and its step response during the three operating phases.

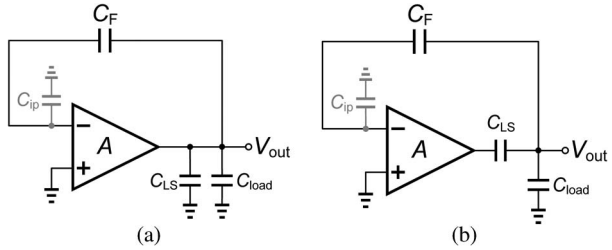

Fig. 3. Equivalent schematics of the closed-loop CLS-S/H during (a) estimation phase (ϕ_2) and (b) level shifting phase (ϕ_3).

i.e., ϕ_1 for sampling, ϕ_2 for estimated output generation, and ϕ_3 for final level shifting. Note that ϕ_1 and ϕ_2 are identical to the operation of a standard S/H (see Fig. 1), with the error in the estimated output during ϕ_2 mainly stemming from the finite opamp gain, assuming low-speed operation. The estimated output sampled onto $C_{\rm LS}$ during ϕ_2 is used to shift the output level toward the ideal value during the final phase ϕ_3 for level shifting.

While this method requires an extra phase, the improved accuracy allows for a reduced number of time constants to settle for an absolute error, minimizing any speed penalty for a fixed output swing. Moreover, as this technique allows for increased output swing, it is possible to use smaller capacitors for the same SNR, improving the circuit's accuracy–speed tradeoff. As discussed in [5], CLS offers advantages over another approach, i.e., CDS, by reducing gain sensitivity to swing, adding negligible kT/C noise, and improving the SNR by increasing output swing. The major CLS tradeoffs include no offset or flicker noise cancellation and the ability to drive only capacitive loads.

B. CLS-S/H Steady-State Error Analysis

With the conventional CLS approach, the final settling error depends on the transient behavior during the two consecutive phases, i.e., ϕ_2 and ϕ_3, which perform the holding function. Fig. 3(a) shows the equivalent circuit during ϕ_2, which is similar to the standard S/H circuit in the hold phase except that the level shifting capacitor is now included at the opamp output in addition to the main load capacitor. While this circuit can be analyzed with a charge-redistribution method [5], a simpler feedback analysis approach is applicable given sufficient settling time.

Assuming the duration of ϕ_2 is long enough for sufficient opamp transient settling, the output voltage at the end of ϕ_2 is

$$V_{\rm out} = V_{\rm in}\left(1 - \frac{1}{1 + C_F A/(C_F + C_{\rm ip})}\right). \tag{2}$$

Hence, at the end of ϕ_2, the normalized error due to the finite opamp gain is

$$e_{S,\phi 2} = \frac{1}{1 + \beta_{\phi 2} A_{\phi 2}} \tag{3}$$

where $\beta_{\phi 2} = C_F/(C_{\rm ip} + C_F)$ is the feedback factor, and $A_{\phi 2}$ is the low-frequency open-loop opamp gain during ϕ_2.

Fig. 3(b) shows the equivalent circuit during the level shifting phase ϕ_3 when $C_{\rm LS}$ is placed between the opamp output and $V_{\rm out}$. Since the external output load is only capacitive, the capacitive path between the opamp output and input can be considered as the feedback network. Hence, this results in the normalized settling error during ϕ_3 to be

$$e_{S,\phi 3} = \frac{1}{1 + \beta_{\phi 3} A_{\phi 3}} \tag{4}$$

where the equivalent feedback factor during ϕ_3 is

$$\beta_{\phi 3} = \left(\frac{C_{\rm LS}}{C_{\rm LS} + C_{\rm load} + \beta_{\phi 2} C_{\rm ip}}\right)\left(\frac{C_F}{C_F + C_{\rm ip}}\right) = \gamma \beta_{\phi 2}. \tag{5}$$

Note that the γ coefficient in (5) is basically the voltage gain from the opamp output node to $V_{\rm out}$, and $\beta_{\phi 2}$ is the voltage gain from $V_{\rm out}$ back to the opamp input. Since the error at the end of ϕ_2, i.e., $e_{S,\phi 2}$, is the maximum desired swing during ϕ_3, the total normalized error at the end of ϕ_3, i.e., $e_{S,\rm total}$, can be derived by multiplying the normalized errors in each phase. Thus

$$e_{S,\rm total} = e_{S,\phi 2} e_{S,\phi 3} = \left(\frac{1}{1 + \beta_{\phi 2} A_{\phi 2}}\right)\left(\frac{1}{1 + \beta_{\phi 3} A_{\phi 3}}\right). \tag{6}$$

Assuming that $A_{\phi 2} = A_{\phi 3} = A$, and $\beta_{\phi 2,3}\ A \gg 1$ in all hold phases, (6) can be simplified to

$$e_{S,\rm total} \approx \frac{1}{\beta_{\phi 2}\beta_{\phi 3} A^2} = \frac{1}{\gamma \beta_{\phi 2}^2 A^2} \tag{7}$$

which shows a relative improvement in gain error proportional to $\beta_{\phi 3} A$ compared with the simple S/H without CLS.

III. SCLS

With the conventional CLS approach, two-stage opamps with 10-bit accuracy and rail-to-rail output swing have been implemented in submicrometer technology [5]. However, while the $\beta_{\phi 2,3} A$ term from (7) is generally greater than unity, $\beta_{\phi 2,3} A \gg 1$ is not always a good assumption, particularly if it is desired to use single-stage opamps for design simplicity and also considering the reduced opamp gain in nanometer CMOS technologies. This motivated the proposed SCLS technique,

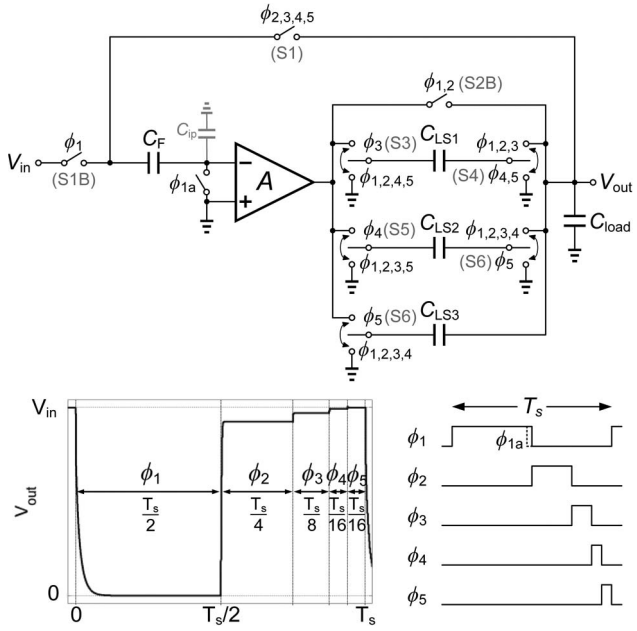

Fig. 4. Flip-around switched-capacitor S/H with 3xCLS and its step response during the five operating phases.

which shifts the output toward its ideal value during multiple consecutive steps in order to further improve circuit accuracy.

A. Proposed Structure

Fig. 4 shows a flip-around switched-capacitor S/H that has been modified to include the proposed SCLS method with three level shifting steps. Here, three level shifting capacitors, i.e., $C_{\mathrm{LS}1-3}$, and two extra operating phases, i.e., ϕ_4 and ϕ_5, are employed. The first three operation phases are the same as the conventional CLS technique, with $C_{\mathrm{LS}1}$ acting as the level shifting capacitor. During ϕ_4, $C_{\mathrm{LS}1}$ is separated from the opamp output node and discharged to zero voltage, and $C_{\mathrm{LS}2}$, which holds the corrected voltage of the previous phase, is connected between the opamp output and the S/H output in order to generate a more accurate value. The same process is repeated a third time using $C_{\mathrm{LS}3}$ during the ϕ_5 phase.

Due to the single-stage opamps used in this SCLS implementation, the opamp unity-gain bandwidth (UGBW) will vary in the different level shifting phases with SCLS, with the lowest UGBW occurring at the first level shifting phase due to level shifting capacitors being in parallel with the load, and the highest UGBW occurring at the last level shifting phase due to the opamp only seeing the main load capacitor. The total amount of time allocated for ϕ_{3-5} can be made equal to the time allocated for ϕ_3 in the conventional CLS implementation. Phase ϕ_3 occupies half of this time, and ϕ_4 and ϕ_5 equally occupy one quarter of this time, due to the higher UGBW during the final two phases.

Theoretically, this technique can be repeated to increase the S/H accuracy further. However, the generation of the extra operating phases and the area consumed by the extra level shifting capacitors place practical limitations. Other secondary issues, such as charge injection and clock feedthrough of the extra switches at the output, can also limit the maximum achievable accuracy and number of level shifting steps.

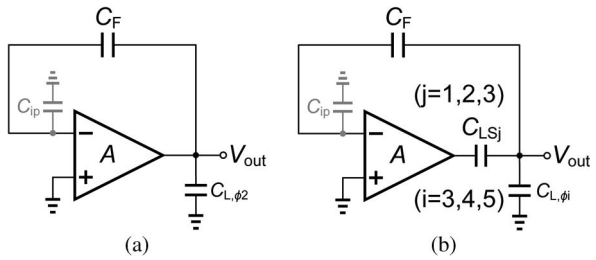

Fig. 5. Equivalent schematics of the closed-loop 3xCLS-S/H during (a) estimation phase (ϕ_2) and (b) first (ϕ_3), second (ϕ_4), and third (ϕ_5) level shifting phases.

B. SCLS-S/H Steady-State Error and Noise Analysis

With the proposed SCLS approach with three CLS steps, the final settling error depends on the transient behavior during the four consecutive phases, i.e., ϕ_{2-5}, which perform the holding function. Fig. 5 shows the equivalent S/H circuit during ϕ_{2-5}. Here, the equivalent load capacitor during ϕ_2, i.e., $\mathrm{C}_{\mathrm{L},\phi 2}$, is equal to the total of the main $\mathrm{C}_{\mathrm{load}}$ and the three level shifting capacitors, and during each subsequent phase, a level shifting capacitor is removed.

Again assuming that the opamp has sufficient settling time during the phases, the simple feedback analysis approach in Section II can be applied, and the final normalized output voltage error for ϕ_2 is given by (3). For ϕ_{3-5}, the normalized settling error at the end of ϕ_i is

$$e_{S,\phi i} = \frac{1}{1+\beta_{\phi i} A_{\phi i}}, \quad i = 3,4,5 \tag{8}$$

where the equivalent feedback factor during ϕ_i is

$$\beta_{\phi i} = \left(\frac{C_{LSj}}{C_{LSj}+C_{L,\phi i}+\beta_{\phi 2} C_{\mathrm{ip}}}\right)\left(\frac{C_F}{C_F+C_{\mathrm{ip}}}\right) = \gamma_j \beta_{\phi 2} \qquad j = 1,2,3, \quad i = 3,4,5 \tag{9}$$

and $C_{L,\phi 3} = C_{\mathrm{load}} + C_{LS2} + C_{LS3}$, $C_{L,\phi 4} = C_{\mathrm{load}} + C_{LS3}$, and $C_{L,\phi 5} = C_{\mathrm{load}}$. The final total settling error of the system is

$$e_{S,\mathrm{total}} = e_{S,\phi 2} e_{S,\phi 3} e_{S,\phi 4} e_{S,\phi 5}. \tag{10}$$

Assuming that $A_{\phi 2} = A_{\phi 3} = A_{\phi 4} = A_{\phi 5} = A$, and $\beta_{\phi 2,3,4,5} A \gg 1$ in all hold phases, (10) can be simplified to

$$e_{S,\mathrm{total}} \approx \frac{1}{\beta_{\phi 2}\beta_{\phi 3}\beta_{\phi 4}\beta_{\phi 5} A^4} = \frac{1}{\gamma_1\gamma_2\gamma_3\beta_{\phi 2}^4 A^4}. \tag{11}$$

In comparison to the conventional CLS approach, the 3xCLS technique provides a relative improvement in gain error proportional to $\beta_{\phi 4}\beta_{\phi 5} A^2$.

While at low sampling frequencies the transient settling error is negligible, this can impact performance at increased sample frequencies. The Appendix provides settling error analysis that includes finite opamp bandwidth and slew rate.

For a 3xCLS design, the single-ended additive noise is

$$v_{no,3\times CLS}^2 \approx \frac{v_{no,\phi 2}^2 + \alpha(kT/C_{LS1})}{(\beta_{\phi 2}A_{\phi 3})^2(\beta_{\phi 2}A_{\phi 4})^2(\beta_{\phi 2}A_{\phi 5})^2} + \frac{v_{no,\phi 2}^2 + \alpha(kT/C_{LS2})}{(\beta_{\phi 2}A_{\phi 3})^2(\beta_{\phi 2}A_{\phi 4})^2} + \frac{v_{no,\phi 2}^2 + \alpha(kT/C_{LS3})}{(\beta_{\phi 2}A_{\phi 5})^2} \tag{12}$$

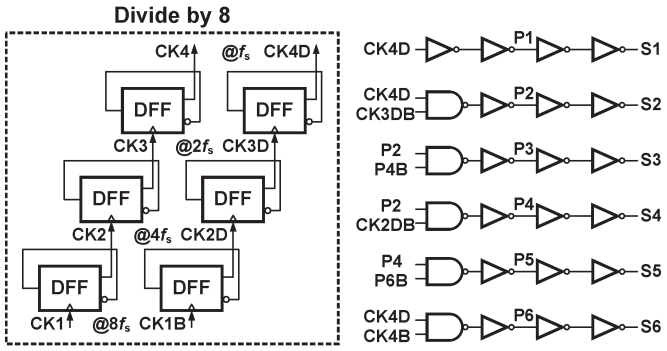

Fig. 6. Simplified schematic of the 3xCLS phase generator and its output phases.

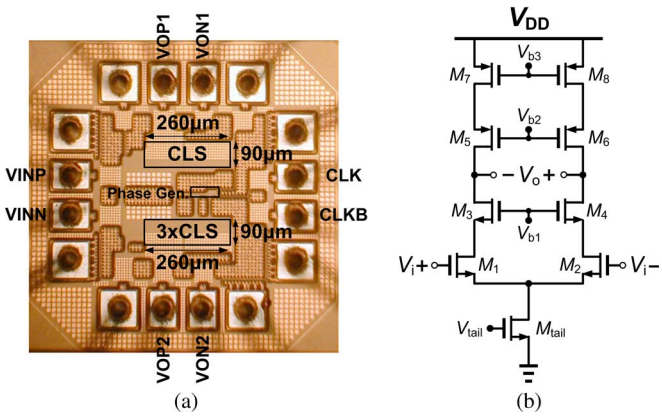

Fig. 7. (a) Die photograph of the CLS and 3xCLS flip-around S/Hs. (b) Opamp topology used in the S/Hs under study.

where $\alpha \approx R_{\mathrm{on,SW}}/(R_{\mathrm{on,SW}} + 1/\beta_{\phi 2} g_{\mathrm{mi}})$. Note that the term $v^2_{no,\phi 2}$ is the total output noise power by the end of ϕ_2, and the other terms are the added output noise power due to C_{LS1}, C_{LS2}, and C_{LS3}. Assuming $\beta_{\phi 2} A_{\phi 3,4,5} \gg 1$, (12) simplifies to

$$v^2_{no,3\times CLS} \approx \frac{v^2_{no,\phi 2} + \alpha(kT/C_{LS3})}{(\beta_{\phi 2} A_{\phi 5})^2}. \tag{13}$$

Assuming $A_{\phi 3} = A_{\phi 4} = A_{\phi 5} = A$ and that $C_{LS3} = C_{LS}/3$, as in the presented 90-nm CMOS prototype, the extra noise power in 3xCLS is $2\alpha kT/[(\beta_{\phi 2} A)^2 C_{LS}]$ relative to conventional CLS. Note that this extra noise is negligible compared with the sampling noise on C_{F}.

C. Phase Generator

A circuit for generating all phases required for 3xCLS is shown in Fig. 6. In order to generate ϕ_4 and ϕ_5 with $T_{\mathrm{s}}/16$ duration (see Fig. 4), a differential input clock with eight times the sampling frequency (CK1/CK1B) serves as the input of the phase generator. Using three cascaded DFF-based divide-by-two stages and simple CMOS gates, the sampling clock and all other switch controls in Figs. 2 and 4 are generated.

IV. Experimental Results

A prototype chip containing S/H circuits utilizing the conventional CLS and the proposed 3xCLS approach was fabricated in an LP 90-nm CMOS process. In order to provide a fair comparison, the sum of the three level shifting capacitors in the 3xCLS design is set to 700 fF (233 fF each), which is equal to the one 700-fF level shifting capacitor used in the CLS structure. As shown in the die photograph in Fig. 7(a), the area of the CLS and 3xCLS designs are both equal to 0.023 mm^2.

The transient responses of the S/Hs, implemented with a single-stage telescopic cascode opamp shown in Fig. 7(b), to a 500-mV step input with 200-ns width are shown in Fig. 8. Both S/Hs have settled to 452 mV by the end of ϕ_2, which implies a 3.4-bit settling accuracy at this signal level for a simple non-level shifting flip-around S/H using the same opamp. The conventional CLS design has settled to 491 mV at the end of ϕ_3, for a 5.8-bit settling accuracy. While the proposed SCLS design does not reach this level during ϕ_{3-4} due to the smaller individual level shifting capacitors, the output settles to 498.9 mV at the end of ϕ_5, yielding an 8.8-bit settling accuracy. Note that in this implementation, the achievable accuracy was limited

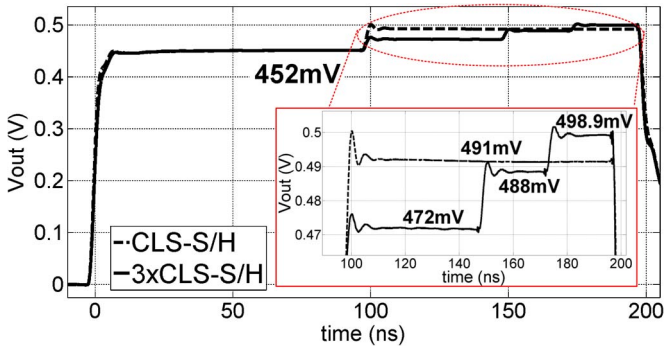

Fig. 8. Measured responses of flip-around S/Hs to a 2.5-MHz pulse with 500-mV amplitude (1 V_{pp}) using CLS and 3xCLS.

TABLE I
Performance Comparison

SPECIFICATION		Simple	CLS	3xCLS [This Work]
Technology		LP 90nm CMOS		
Supply Voltage (V)		1.2	1.2	1.2
Sampling Rate (MHz)		2.5	2.5	2.5
Sampling Capacitance (pF)		0.5	0.5	0.5
Load Capacitance (pF)		1.8	1.8	1.8
Opamp DC Gain (dB)		26	26	26
Level Shifting Cap. (fF)		0	700	700 (total) 233 (each)
Output Steady-State Error (%)	@ 0.2V_{pp} Input	3.8	0.83	0.13
	@ 0.5V_{pp} Input	4.95	0.95	0.15
	@ 1.0V_{pp} Input	9.6	1.8	0.22
Accuracy (bit)†	@ 0.2V_{pp} Input	4.7	6.9	9.6
	@ 0.5V_{pp} Input	4.3	6.7	9.4
	@ 1.0V_{pp} Input	3.4	5.8	8.8
Power (mW)		1.91*	1.92	1.92
Area (mm^2)		0.016**	0.023	0.023

† Accuracy is calculated as $\log_2(1/\text{output error})$.
* The power difference is due to the phase generator block.
** The area difference is due to level shifting capacitors.

to less than 9 bits by a relatively large load capacitance, i.e., $C_{\mathrm{load}} = 1.8$ pF, induced by the off-chip measurement setup. With a small total level shifting capacitance, i.e., $C_{\mathrm{LS,tot}} = 0.7$ pF, relative to the load capacitance, the feedback factors during the level shifting phases are reduced for both CLS and 3xCLS structures, as suggested by (5) and (9). However, the

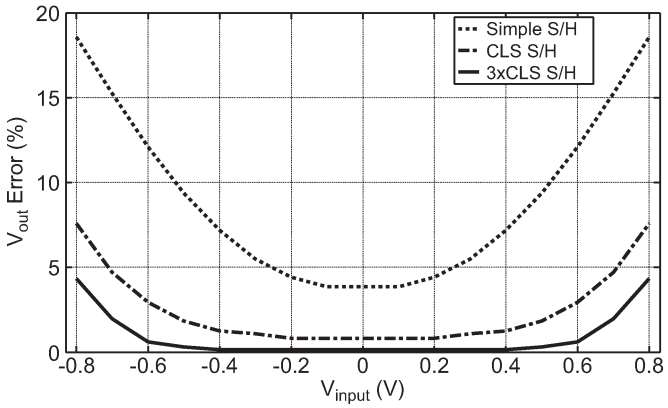

Fig. 9. Measured output voltage error versus input pulse amplitude for the three different S/H structures under study.

proposed technique can achieve improved accuracy in more controlled loading environments.

Table I compares the proposed SCLS S/H with both the CLS S/H and the implied simple design without level shifting capacitors. The measured steady-state errors decrease with smaller output swings due to increased opamp gain. For a small input swing, the maximum opamp gain is equal to its 26-dB small-signal value. According to (3), (6), and (10), the final settling errors of the conventional, CLS, and 3xCLS S/Hs are 5%, 0.8%, and 0.19%, respectively, which are in good agreement with the measurement results.

Fig. 9 shows the three S/H structures' steady-state errors with a low-frequency pulse input. The 3xCLS method achieves superior linear dynamic range, allowing for a 1% gain error for amplitudes less than or equal to 600 mV, relative to the conventional CLS, which requires amplitudes less than or equal to 200 mV, and the simple S/H that cannot achieve this.

V. Conclusion

This brief has presented an SCLS technique that addresses a limiting factor in many analog circuits, finite and nonlinear swing-dependent opamp gain. While a conventional single level shifting capacitor CLS approach can yield accuracy improvements proportional to the opamp gain, this may be insufficient for systems that use simple single-stage opamps and for designs in reduced-gain nanometer CMOS technologies. The proposed SCLS method adds additional level shifting capacitor operations for improved accuracy, with each sequential operation reducing the gain error by a factor proportional to the opamp gain.

Appendix
SCLS Output Settling Error Including Finite Opamp Bandwidth and Slew Rate

Here, a single-stage opamp with one dominant pole is assumed. During ϕ_2, the output swing may be large enough to make the opamp output slew. The total settling error is

$$e_{S,\phi 2} = \exp(-\beta_{\phi 2}\mathrm{UGBW}_{\phi 2}t_{\phi 2}) \times [\exp(\beta_{\phi 2}\mathrm{UGBW}_{\phi 2}t_{LS,\phi 2}) - \beta_{\phi 2}\mathrm{UGBW}_{\phi 2}t_{LS,\phi 2}] + \frac{1}{1+\beta_{\phi 2}A_{\phi 2}} \tag{14}$$

where $\mathrm{UGBW}_{\phi 2} = g_{\mathrm{mi}}/C_{L,\phi 2}$ is the unity gain bandwidth

$$t_{LS,\phi 2} = \frac{(V_{S,pp}/V_{\mathrm{effi}} - 1/\beta_{\phi 2})}{\mathrm{UGBW}_{\phi 2}} \tag{15}$$

V_{effi} is the opamp input transistors' overdrive voltage, and $V_{S,pp}$ is the input voltage swing.

Assuming that the duration of ϕ_2 allows the opamp to enter into small-signal settling, it is a reasonable assumption that the opamp does not slew during the level shifting phases. Hence, the total settling error during ϕ_3 to ϕ_5 is

$$e_{S,\phi i} = \exp(-\beta_{\phi i}\mathrm{UGBW}_{\phi i}t_{\phi i}) + \frac{1}{1+\beta_{\phi i}A_{\phi i}}, \quad i = 3,4,5 \tag{16}$$

where $t_{\phi i}$ is the duration of ϕ_{i}, and $\beta_{\phi i}$ is the feedback factor as derived in (9). As mentioned previously in Section III-A, the UGBW will vary in the different level shifting phases, as opposed to conventional CLS, which has the maximum UGBW during the single level shifting phase. The total opamp settling error is calculated by multiplying normalized error terms in all hold phases.

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