A 6 bit 10 GS/s TI-SAR ADC With Low-Overhead Embedded FFE/DFE Equalization for Wireline Receiver Applications

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***Abstract*—High-speed ADC front-ends in wireline receivers allow for implementing flexible, complex, and robust equalization in the digital domain, as well as easily supporting bandwidth-efficient modulation schemes, such as PAM4 and duobinary. However, the power consumption of these ADC front-ends and subsequent digital signal processing is a major issue. This paper presents a 64-way 6 bit 10 GS/s time-interleaved successive-approximation-based ADC front-end that efficiently incorporates a two-tap embedded FFE and a one-tap embedded DFE, providing the potential for a lower complexity back-end DSP and/or decreased ADC resolution. Fabricated in a 1.1V GP 65nm CMOS process, the ADC with embedded equalization achieves 0.48 pJ/conv.-step FOM, while consuming 79.1mW and occupying 0.33 mm^2 core ADC area. The effectiveness of the embedded FFE and DFE is demonstrated with significant timing margin improvement observed for 10 Gb/s operation over several FR4 channels.**

***Index Terms*—ADC-based receiver, analog to digital converter (ADC), decision feedback equalizer (DFE), embedded equalization, feed-forward equalizer (FFE), successive approximation register (SAR), time interleaving.**

I. Introduction

As THE DATA RATES of wireline communication links increases, channel impairments such as skin effect, dielectric loss, fiber dispersion, reflections and cross-talk become more pronounced. This warrants more interest in analog-to-digital converter (ADC)-based serial link receivers (Fig. 1), as they allow for more complex and flexible back-end digital signal processing (DSP) relative to binary or mixed-signal receivers [1]–[4]. Utilizing this back-end DSP allows for complex digital equalization and more bandwidth-efficient modulation schemes, while also displaying reduced process/voltage/temperature (PVT) sensitivity. Furthermore, these architectures offer straightforward design translation and can directly leverage the area and power scaling offered by new CMOS technology nodes.

One key issue with ADC-based receivers is the significant power consumption of both the front-end ADC and the subsequent digital equalization and symbol detection at high data rates. Previous works, such as [4], [5], and [6], present techniques to reduce the front-end ADC power by using optimal positioning of threshold voltages, configurable resolution based on the channel characteristics, and mixed-mode pre-equalization. Embedding analog equalization in the ADC is another promising approach to both reduce ADC resolution and digital equalization complexity [7], allowing for improvements in overall receiver power consumption with low-overhead implementations of the common feed-forward equalizer (FFE) and decision-feedback equalizer (DFE) topologies used in wireline receivers [8]–[11].

Feed-forward equalizers are effective in canceling a large amount of inter-symbol interference (ISI) with a relatively small number of taps. A 2-tap version of this equalizer topology has been implemented in a time-interleaved (TI) flash ADC with additional CML input stages that follow the input track-and-holds (T/H) to realize the extra FFE tap [4]. While this approach is effective, significant linearity, speed, and power consumption trade-offs exist with this current-mode approach. FFEs have also been embedded in successive approximation register (SAR) ADCs [12], [13], with charge-sharing in a capacitive digital-to-analog converter (CDAC) performing the signal scaling and summation of multiple input samples, followed by ADC conversion. However, a drawback of this single-CDAC approach is that the main cursor signal is attenuated such that the FFE tap sum is always fixed, similar to transmitter de-emphasis equalization [11].

Decision-feedback equalizers offer the ability to cancel post-cursor inter-symbol interference (ISI) without amplifying noise or cross-talk. Embedded multi-level decision-feedback equalization (DFE) has been previously proposed for pipeline ADCs [14]. As satisfying the DFE feedback critical timing path is not trivial at high data rates, [14] employs loop unrolling or speculative-summing [15] with additional comparators, resulting in significant hardware overhead. A more efficient implementation in a SAR ADC involves the use of a redundant conversion cycle [16], [17] rather than redundant comparators and DACs, to

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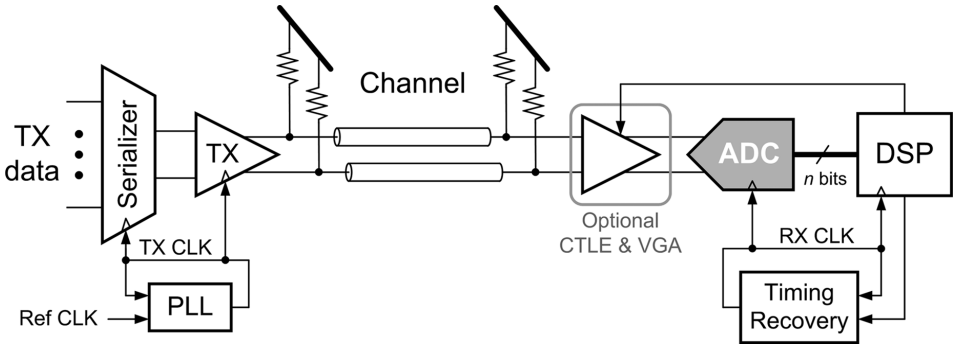


Fig. 1. A high-speed electrical link system with an ADC-based receiver.

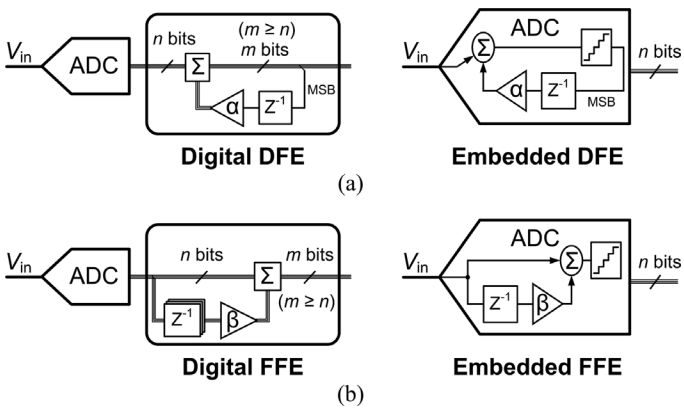


Fig. 2. Block diagrams of (a) digital versus embedded DFE, and (b) digital versus embedded FFE.

perform the loop unrolling operation. While this does increase the number of required conversion cycles, the overhead is only (8/7)X for a conventional 6 bit SAR converter.

This work presents a 10GS/s 6 bit ADC which efficiently incorporates both a novel 2-tap embedded FFE and a 1-tap embedded DFE directly into the capacitive DAC of a time-interleaved SAR ADC [17]. A key goal of this design was to demonstrate the viability of the embedded equalizer approach for wireline receiver ADCs through the implementation of a 10GS/s concept prototype. Section II presents statistical bit error rate (BER) modeling results of ADC-based receivers that quantify the performance advantages of embedded equalization. The proposed embedded equalization techniques, which allow for flexibility in equalizer tap weighting at minimal hardware and power overhead, are analyzed in Section III. Section IV details the ADC architecture and the main circuit blocks, where power is further optimized through the use of dual voltage supplies. Experimental results from a general purpose (GP) 65 nm CMOS prototype are presented in Section V. Finally, Section VI concludes the paper.

II. Embedded Equalization Modeling

Statistical link modeling [18] allows for both system voltage and timing margins to be efficiently estimated. This section first highlights the differences between a conventional architecture, consisting of an ADC and subsequent digital equalization, and a system with an ADC with embedded DFE and FFE. Results from an ADC-based serial link statistical modeling tool [7] are then presented that show the system performance impact of embedded DFE and FFE equalization for 10 Gb/s operation over four different FR4 channels.

A conventional architecture, consisting of an ADC and subsequent digital equalization, and a system with an ADC with embedded DFE and FFE are shown in Fig. 2. In order to implement a 1-tap DFE with NRZ signaling (Fig. 2(a)), the MSB of either the digital equalizer output or the ADC with embedded DFE is fed back, weighted by the DFE coefficient, and subtracted. Quantization noise is reduced in the system with an ADC with embedded DFE, as the equalization tap is subtracted from the un-quantized analog input. In order to implement a 2-tap FFE (Fig. 2(b)), the input signal is delayed, weighted by the FFE coefficient, and then summed. Again, quantization noise is reduced in the system with an ADC with embedded FFE, as the full analog resolution is preserved for the input, delayed signal, and the final summation value. Previous statistical modeling studies [7], [16] have shown that the quantization noise reduction offered by both the embedded DFE and FFE equalization allows for both a lower ADC resolution and reduced digital equalization complexity at a target BER.

In order to quantify the relative performance impact of embedded DFE and FFE equalization, the four FR4 channels of Fig. 3 are utilized. As shown in Fig. 3(a), the loss at the 5 GHz Nyquist frequency increases with channel length, with the longest 30” channel having 23.8 dB attenuation. This is reflected in the time domain 10 Gb/s pulse responses (Fig. 3(b)), where the ratio of the main cursor to the ISI cursor values degrades with channel length. 10 Gb/s operation is modeled with the statistical link tool, assuming a 500 $\mathrm{mV_{ppd}}$ transmit swing, 1 $\mathrm{mV_{rms}}$ receiver input-referred thermal noise, 5 mV uniform supply noise, and receiver sampling jitter with a 0.02 unit interval (UI) deterministic component (DJ) in the form of duty cycle distortion and a 0.02 $\mathrm{UI_{rms}}$ random component (RJ).

Fig. 4 shows the advantage of embedded equalization over its digital counterpart for channels 1–3, with the receiver voltage margin (BER = 10^{-12}) obtained versus front-end ADC resolution for both digital and embedded implementations of a 2-tap

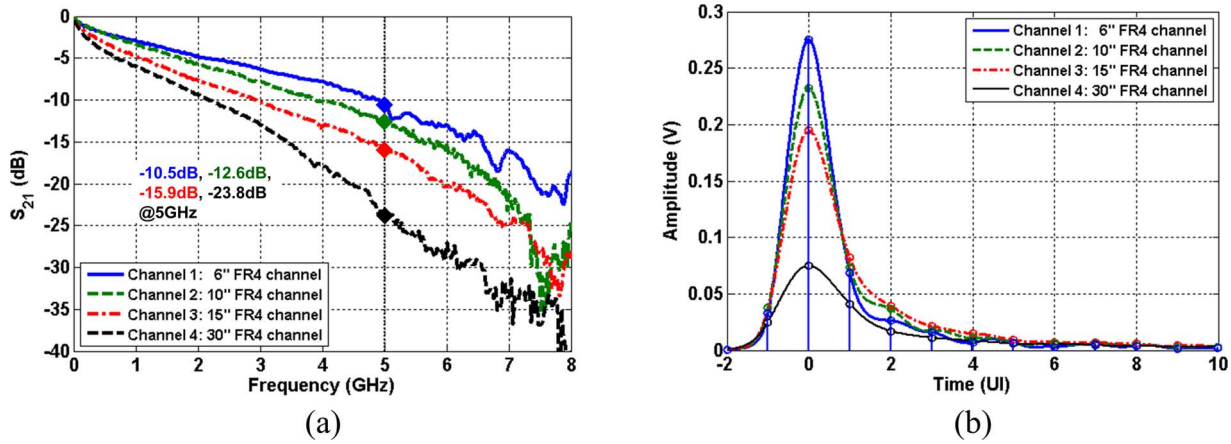


Fig. 3. (a) Magnitude and (b) 10 Gb/s pulse responses of four FR4 channels.

FFE plus 1-tap DFE equalization structure. Similar to the prototype discussed later, here the embedded 2-tap FFE consists of an un-attenuated main cursor and an adjustable second FFE tap with $V_{LSB}/4$ maximum coefficient resolution, while the embedded DFE has an un-quantized analog resolution. Due to the quantization error, the digital equalization implementation requires more than 6 bits effective ADC resolution to achieve a similar performance as the embedded equalization architecture. The impact of the various embedded equalization schemes is shown in the 10 Gb/s voltage and timing margins of Fig. 5(a) and (b), respectively. For the case when no equalization is embedded in the ADC, only the relatively low-loss 6" channel displays an open eye. Including a 1-tap DFE allows cancellation of the first post-cursor ISI term, which improves the 6" channel margins and opens the previously closed eye for the 10" channel. However, operation is still not possible for the 15" channel due to excessive residual ISI. As a 2-tap FFE can cancel significant long-tail ISI, better margins are obtained relative to the DFE-only scenario, with all three channels displaying open eyes. Combining both the 2-tap FFE and 1-tap DFE yields the best margins, with the 15" channel having the largest 6X increase in voltage margin relative to the FFE-only case. Finally, it is interesting to consider the potential impact adding a front-end continuous-time linear equalizer (CTLE) can have, particularly with the highest-loss 30" channel. As shown in the Fig. 5(c) voltage and timing margins, combining embedded equalization with a front-end CTLE allows for opening a previously closed eye, with the embedded DFE providing a higher relative improvement versus embedded FFE.

These modeling results show that embedded equalization can be useful for both reducing the required ADC resolution and providing a better input signal for subsequent digital equalization, translating into a simpler digital back-end. Although it is beyond the scope of the presented work, the embedded DFE can also be used to enable a hybrid receiver mode [3]. For low ISI channels, only the embedded equalization is used with a reduced reconfigurable ADC resolution, while for high ISI channels where the embedded equalization alone does not provide the target BER, the embedded DFE can be disabled to avoid potential error propagation and the front-end ADC with embedded FFE allows for a reduced complexity digital equalizer relative to a separate dual-path front-end implementation [3].

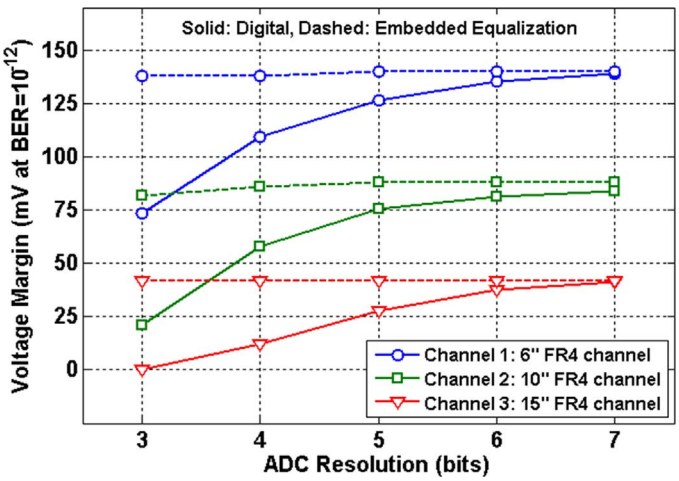


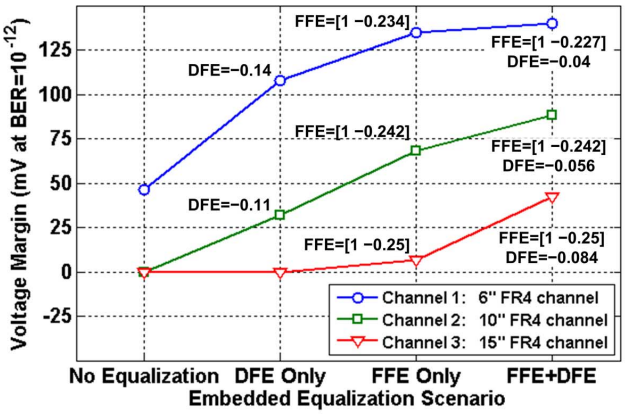
Fig. 4. Simulated voltage margin versus ADC resolution with both digital and embedded implementations of a 2-tap FFE + 1-tap DFE equalization structure for channels 1–3 in Fig. 3.

III. SAR ADC With Low-Overhead Embedded FFE and DFE

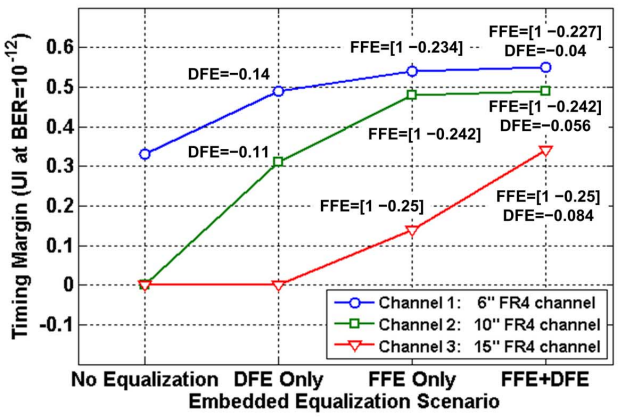
In order to leverage the potential performance improvements predicted by the modeling results of the previous section, low-overhead implementations of embedded FFE and DFE are necessary. This section describes a novel approach to efficiently embed both a 2-tap FFE and 1-tap DFE into a time-interleaved SAR ADC, with the conceptual operation first explained, followed by the switched-capacitor implementation details.

A. Unit ADC With Embedded 2-Tap FFE and 1-Tap DFE

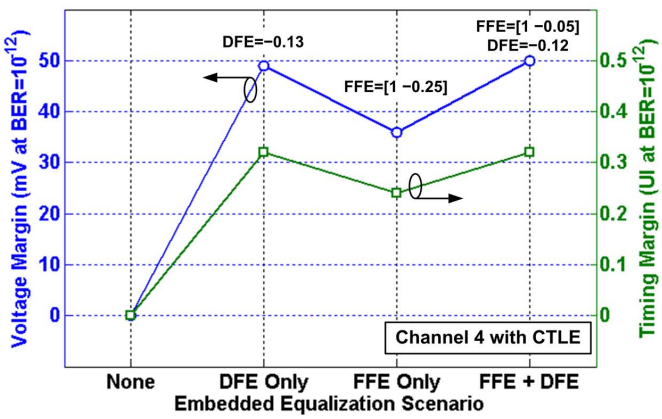
A sequential block diagram detailing the different operation phases of the proposed unit SAR ADC with embedded 2-tap FFE and 1-tap DFE is shown in Fig. 6. In order to realize



(a)



(b)



(c)

Fig. 5. Impact of including embedded DFE and FFE equalization on (a) voltage margin and (b) timing margin for channels 1–3 in Fig. 3, with tap coefficients shown for the embedded equalization. (c) Impact of including embedded DFE and FFE equalization on voltage margin and timing margin in the presence of a front-end CTLE for channel 4 in Fig. 3.

the 2-tap FFE, this implementation uses the output of two consecutive track-and-holds (T/Hs) found in a time-interleaved (TI) architecture. Both the current input voltage $V_{\mathrm{in,n}}$ and the previous input voltage $V_{\mathrm{in,n-1}}$ are sampled during the first cycle, with a weighting factor of β applied to $V_{\mathrm{in,n-1}}$ via charge sharing in a CDAC. These two voltages are subtracted at the input of the comparator during the subsequent conversion periods to create the transfer function of a 2-tap FFE. The redundant cycle 1-tap DFE is realized in the second and third cycle, with the MSB value first computed with a $+\alpha$ DFE coefficient value and latched, followed by the MSB computation with a $-\alpha$ value in the next cycle [16]. This allows the use of only one comparator and DAC, as in a conventional SAR ADC. At the end of the second MSB cycle the previous symbol MSB is used to select the correct computation and α polarity to use in all the remaining SAR conversion cycles. While the redundant cycle 1-tap embedded DFE adds some latency to the data conversion process, the critical delay path is similar to that of a loop-unrolled 1-tap DFE, as detailed in [16]. Overall, eight equal cycles are used for each sample conversion in a 6 bit ADC, including the sampling cycle and the redundant cycle for the embedded 1-tap DFE. For a given total ADC sample rate, the proposed redundant cycle method results in an (8/7)X increase in time-interleaving factor and conversion latency, and almost the same increase in the core ADC area.

B. Switched-Capacitor Implementation

Fig. 7(a) shows a simplified single-ended unit ADC schematic to illustrate the switched-capacitor implementation of the 2-tap FFE and 1-tap DFE during the first three phases of the SAR conversion, the sampling phase and the two redundant-cycle MSB computations. An efficient implementation of the redundant cycle 1-tap embedded DFE MUX is realized with the current input sampling capacitor C_{S} and switches between $+\alpha$, $-\alpha$, and GND. The sampled input on C_{S} also acts as the un-attenuated main cursor tap for the embedded FFE. Embedding the second FFE tap inside the negative-input capacitive DAC structure is achieved with the $\mathrm{B_1}-\mathrm{B_5}$ switches that select between the previous input or GND to provide the β coefficient weighting without impacting the main cursor value.

During the sampling cycle $V_{\mathrm{in,n}}$ is sampled on the C_{S} capacitor using top-plate sampling, while $V_{\mathrm{in,n-1}}$ is sampled on a portion of the negative-input DAC capacitors using bottom-plate sampling, as shown in Fig. 7(b). The FFE coefficient β is defined by a 5 bit word $\mathrm{B_1B_2B_3B_4B_5}$, set to 10001 in this example to charge only 16 C_{u} and C_{u} capacitors with $V_{\mathrm{in,n-1}}$ and discharge the other DAC capacitors. In the next cycle (Fig. 7(c)) the Φ_{S} switches are OFF and the bottom-plate of all the negative-input DAC capacitors are connected to ground. The resultant charge sharing induces a $\beta V_{\mathrm{in,n-1}}$ value at the comparator negative input. By having the main cursor value $V_{\mathrm{in,n}}$ at the comparator positive input, assuming the DFE coefficient $\alpha = 0$ for now, the voltage $V_{\mathrm{in,n}} - \beta V_{\mathrm{in,n-1}}$ appears at the comparator differential input to emulate the 2-tap FFE, where only the post-cursor tap coefficient is adjustable. Note that while a negative version of the previous input voltage $-V_{\mathrm{in,n-1}}$ is required in this technique, this is easily available in a fully differential architecture. Considering a non-zero DFE coefficient for this first MSB cycle, the comparator differential input voltage is $V_{\mathrm{in,n}} - \beta V_{\mathrm{in,n-1}} + \alpha$ due to the top side of C_{S} being connected to $+\alpha$. The MSB value for this DFE tap polarity is then stored in a latch. In the next phase (Fig. 7(d)), the MSB is re-evaluated for the opposite DFE tap polarity, as the top side of C_{S} is now connected to $-\alpha$, resulting in a differential voltage at the comparator input of

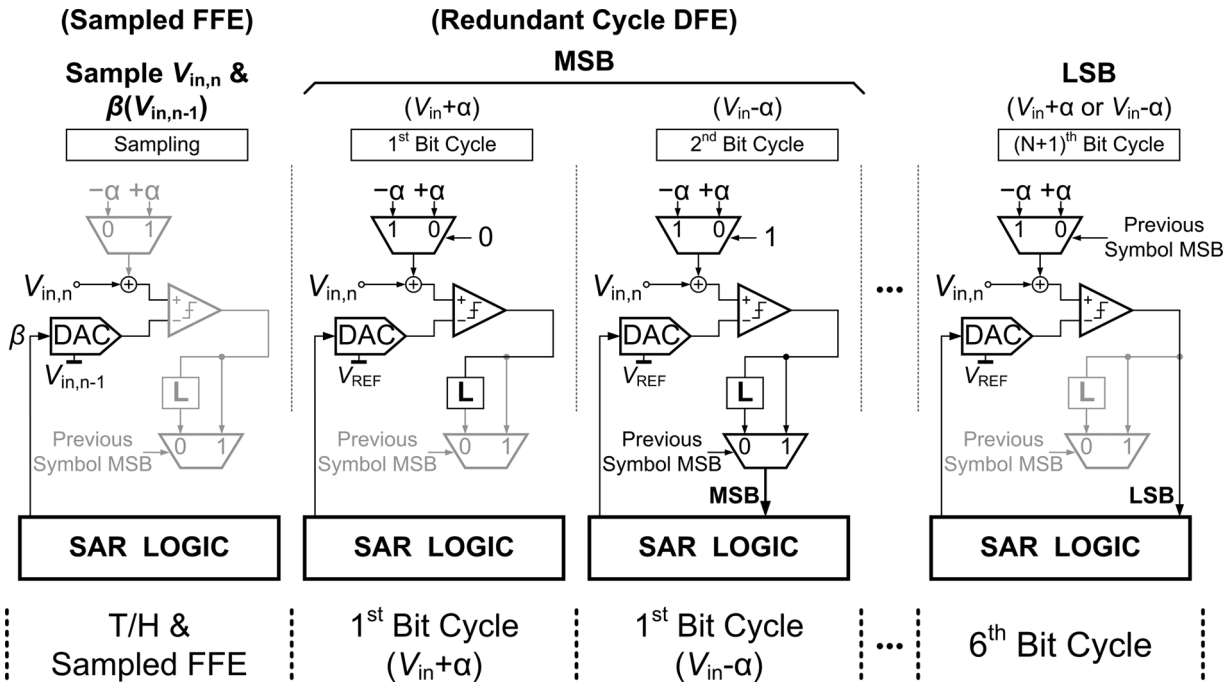


Fig. 6. Conceptual schematic of a unit SAR ADC with the proposed sampled 2-tap embedded FFE and redundant cycle 1-tap embedded DFE.

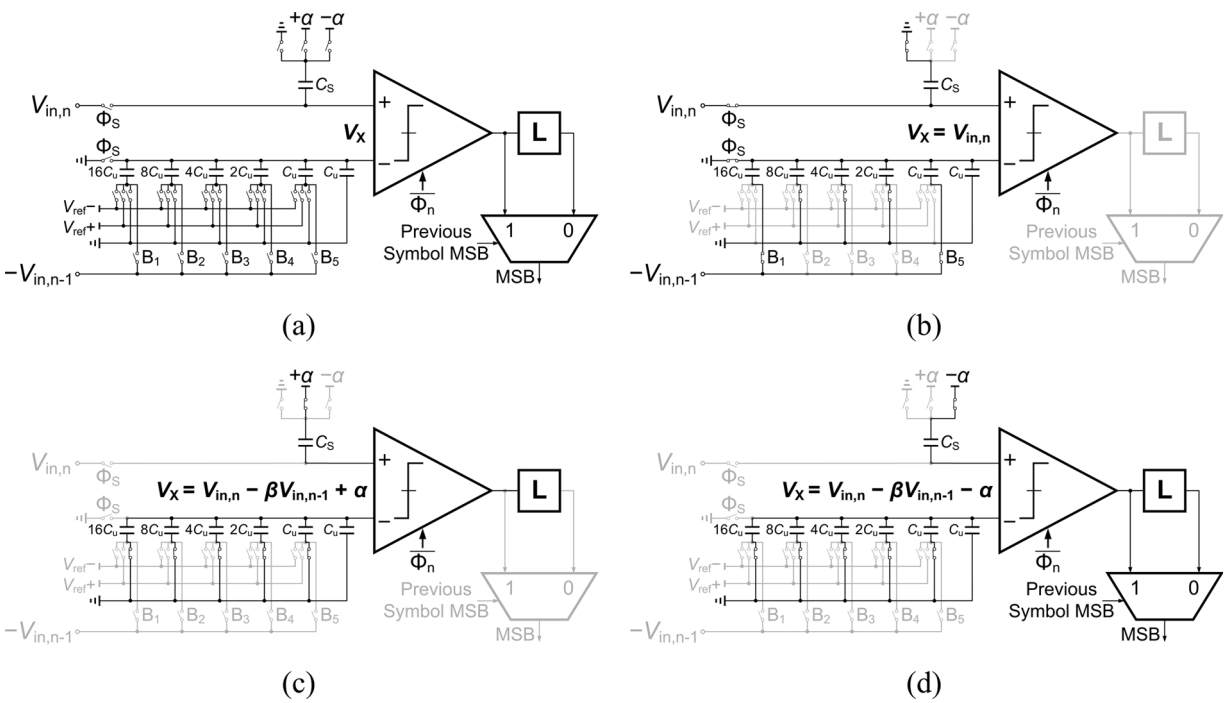


Fig. 7. Simplified unit SAR ADC with embedded 2-tap FFE and 1-tap DFE: (a) single-ended schematic, and operation during the (b) sampling phase, (c) first MSB evaluation, and (d) second MSB evaluation assuming $\mathrm{B_1B_2B_3B_4B_5} = 10001$ for the FFE.

$V_{\mathrm{in,n}} - \beta V_{\mathrm{in,n-1}} - \alpha$. The correct MSB decision is then made based on the MSB of the previous ADC channel, and for the remaining ADC bit cycles the corresponding switch for selecting $+\alpha$ or $-\alpha$ is fixed till the end of the SAR conversion period.

According to Fig. 7, the FFE second tap coefficient β normalized to the main cursor tap is ideally equal to $(\mathrm{B_1B_2B_3B_4B_5})_2/32$, where $(.)_2$ represents the binary-to-decimal conversion operator. However, since the main cursor is sampled directly on the top-plate of C_{S}, while bottom-plate sampling is employed for the second tap, some attenuation is introduced at the DAC output due to capacitive division between the DAC capacitors and the comparator input capacitance. In practice β can be calculated as

$$\beta = \frac{(B_1B_2B_3B_4B_5)_2}{32} \times \frac{C_{\mathrm{DAC}}}{C_{\mathrm{DAC}} + C_{ip}} \tag{1}$$

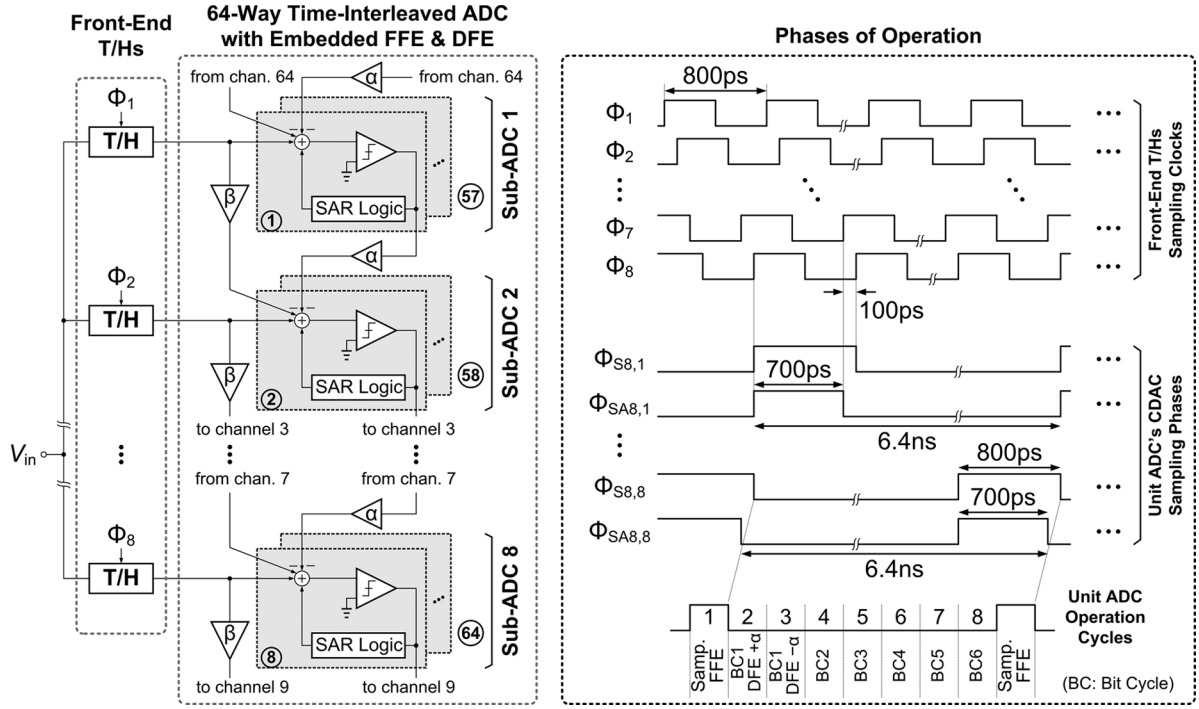


Fig. 8. Block diagram of the 64-way time-interleaved SAR ADC with embedded FFE and DFE.

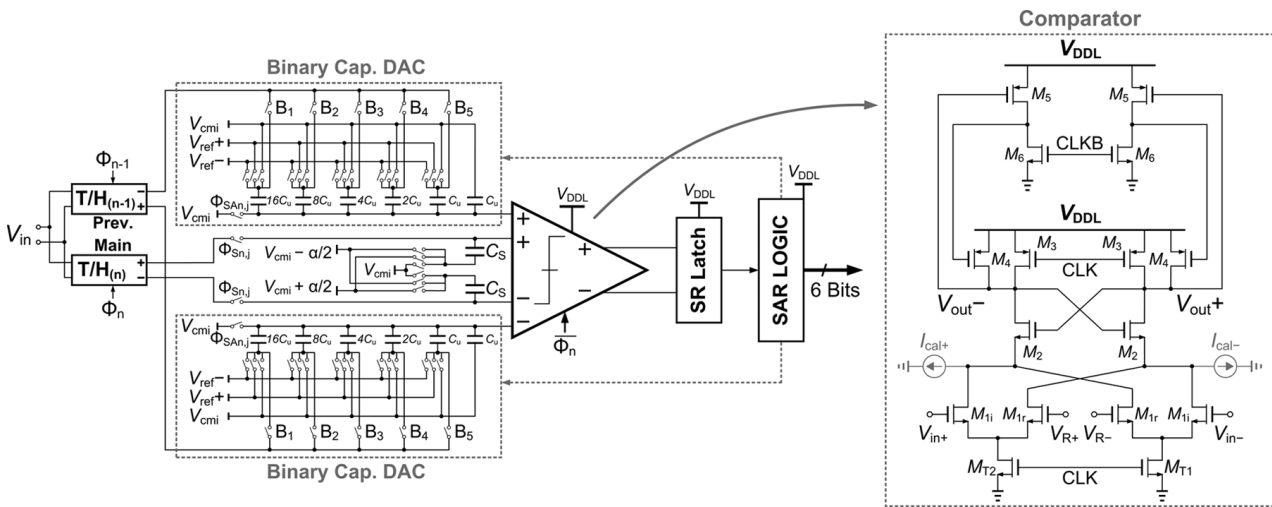


Fig. 9. Fully differential schematic of the unit ADC with sampled 2-tap embedded FFE and redundant cycle 1-tap embedded DFE.

where C_{DAC} is the total CDAC capacitance, and C_{ip} is the comparator input capacitance. Although not included in the current prototype, extra digitally controlled capacitors can be added to the capacitive DAC in order to control the FFE tap coefficient with one more degree of freedom.

IV. ADC Design

A. Time-Interleaved Architecture

Fig. 8 shows the implementation of the SAR ADC with embedded FFE and DFE in a 10 GS/s 6 bit converter with 64 time-interleaved unit ADCs. The entire 64-way time-interleaved structure consists of eight time-interleaved sub-ADCs, where each sub-ADC operates at $f_s/8 = 1.25$ GS/s and is formed by eight parallel unit ADCs. Each unit ADC has eight operation cycles: one for input/2-tap FFE sampling, six for bit conversions, and one extra cycle for the embedded 1-tap DFE. Eight front-end track-and-holds, one per sub-ADC, are employed to allow for the use of only eight critical sampling phases at 1.25 GHz. Calibration DACs are included for both comparator offset correction in all 64 unit SAR ADCs and sampling clock skew correction for the eight front-end T/H sampling phases.

B. Unit ADC With Embedded 2-Tap FFE and 1-Tap DFE

The fully differential schematic of the 6 bit unit SAR ADC with embedded 2-tap sampled FFE and redundant cycle 1-tap embedded DFE is shown in Fig. 9. A modified StrongArm comparator with two differential input pairs is used. One input pair is connected to the sampling capacitor, which samples the main

cursor and implements the embedded 1-tap DFE functionality. The other input pair is connected to the DAC output, which also implements the FFE second-tap. Since part of the DAC capacitors are connected to the $\mathrm{T/H_{(n-1)}}$ output whose hold phase ends 1 UI = 100 ps sooner than $\mathrm{T/H_{(n)}}$, a modified version of the sampling phase $\Phi_{\mathrm{SAn,j}}$, which falls to zero 100ps in advance of normal sampling phase $\Phi_{\mathrm{Sn,j}}$ (Fig. 8), is used for connecting the top-plate of the DAC capacitors to the input common-mode voltage $\mathrm{V_{cmi}}$ during the sampling phase.

A merged capacitor switching (MCS) scheme [19], which allows for very low switching energy and reduced area through removing the MSB capacitor, is employed in the DAC of each 6 bit unit SAR ADC. To further reduce DAC area, a custom layout with a 0.45 fF metal-oxide-metal (MOM) unit capacitor (C_{u}) is employed, as shown in Fig. 10(a). Minimum width metal 4 (MET4) and metal 5 (MET5) layers with minimum spacing are used, resulting in the optimum desired capacitance value with respect to the bottom-plate parasitic capacitance to the substrate. Both matching and noise performance are considered in the selection of the unit capacitor value. Monte Carlo simulations of the worst-case DNL error due to DAC capacitive mismatch, which happens in the transition from 01111 to 10000 in the utilized 5 bit CDAC, are shown in Fig. 10(b). These results consider both process and local mismatch variations, with the Monte Carlo parameters extrapolated beyond the 4 fF minimum MOM capacitor offered by the design kit [20]. Since the spacing of the metal fingers in the MOM capacitor is always equal to the minimum 100nm, the unit capacitor mismatch $\sigma_{C_{\mathrm{u}}}$ is approximately scaled by the square root of the capacitor area controlled by the finger length and number of fingers. The 0.45 fF unit capacitor value results in this maximum DNL error having 3σ<0.5 LSB at 6 bit resolution. This value is also larger than the 0.136 fF capacitor size required for an additive noise voltage less than 0.5 $\mathrm{V_{LSB}}$ with a 500 $\mathrm{mV_{pp}}$ maximum swing.

As the two-stage dynamic comparator allows for high performance at low supply voltages [21], a lower $V_{\mathrm{DDL}} = 0.9$ V is used for the comparator and SAR logic to reduce the core ADC power, while the nominal $V_{\mathrm{DD}} = 1.1$ V is used for the DAC switches. A foreground technique [16] is employed to control the pseudo-differential 6 bit current-steering DACs that perform offset calibration of the 64 comparators in the time-interleaved ADC. By injecting this calibration current into the internal comparator nodes, an offset correction < 3 mV is achieved. Fig. 11 shows the simplified setup for foreground offset calibration. The ADC differential input is set to zero by connecting both positive and negative inputs to the 300-mV input common-mode voltage. A 64-to-1 MUX is then used to choose the MSB of the unit ADC under calibration. The optimum calibration code, applied using the serial scan chain, is determined when the MSB of the unit ADC under test toggles between 0 and 1 with near 50% probability. Simulations show that the temperature variation impact on the unit ADC residual offset after initial foreground calibration is +62 μV/°C for the worst calibration code, which is tolerable for the 6 bit ADC with 500 $\mathrm{mV_{pp}}$ input range. Furthermore, the comparator input pairs sharing the same source

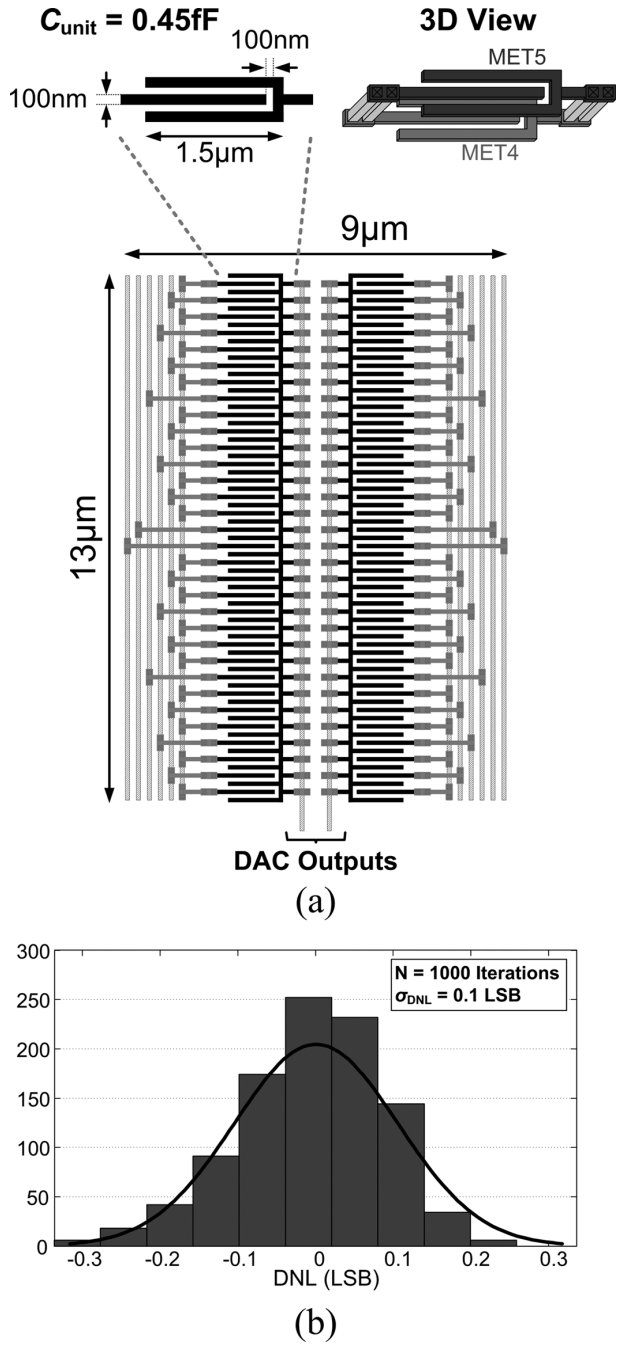


Fig. 10. (a) Custom layout of the capacitive DAC with 0.45 fF MOM unit capacitors. (b) CDAC worst-case 01111 to 10000 transition DNL simulation results using 1000 Monte Carlo iterations.

connection are swapped as $\mathrm{V_{in+}/V_{R+}}$ and $\mathrm{V_{in-}/V_{R-}}$ (Fig. 9) in order to decrease the sensitivity to common-mode variations between the differential input and reference terminals. This configuration also helps with the comparator sensitivity near a large DAC differential output.

In order to relax the comparator device sizing constraints and also maintain low metastability error impact, the metastability detection and correction algorithm detailed in Fig. 12 is utilized. Metastability is detected by sampling the XOR of the comparator differential outputs using a version of the comparator

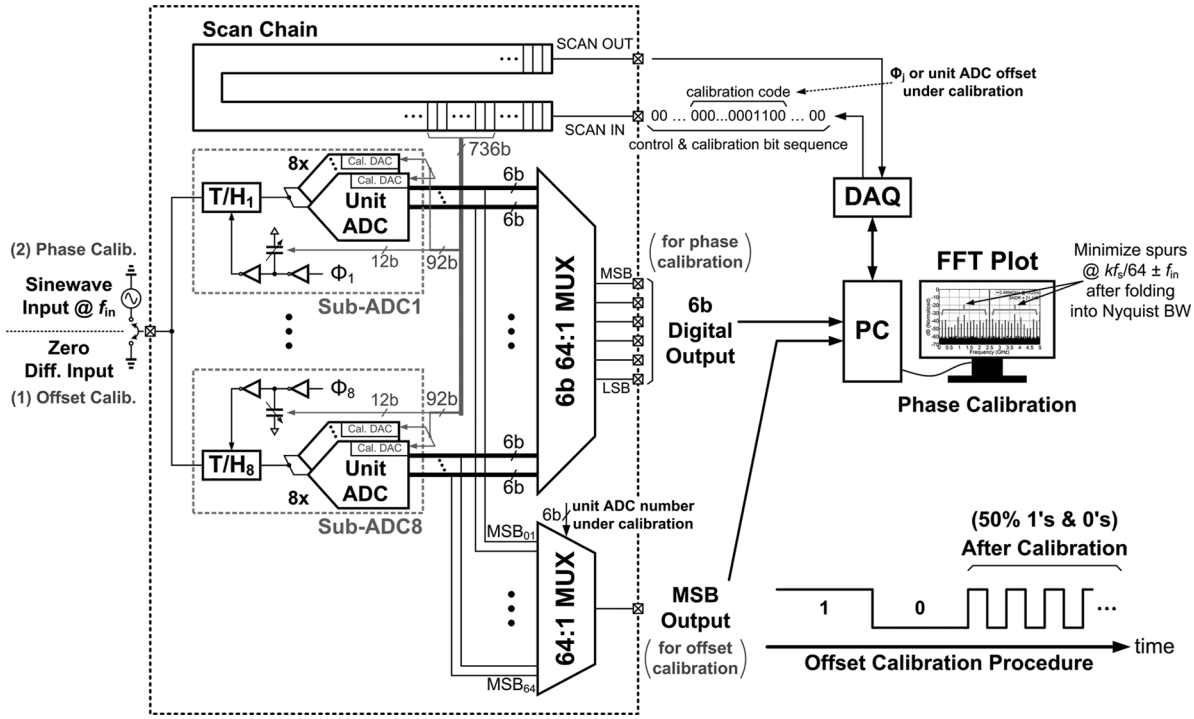


Fig. 11. Simplified diagram of the foreground offset and clock skew calibrations setup.

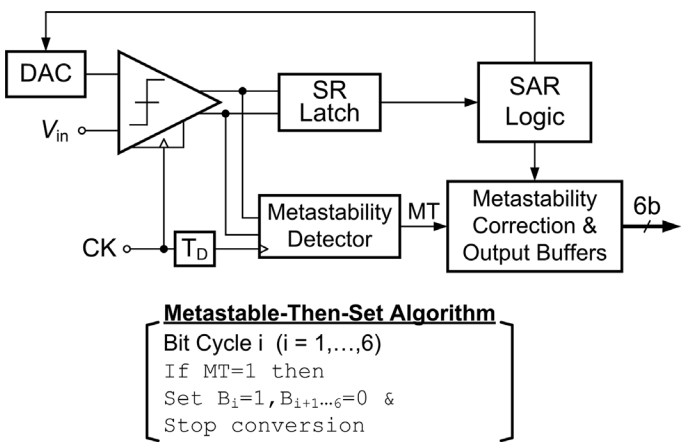


Fig. 12. Metastability detection and correction algorithm.

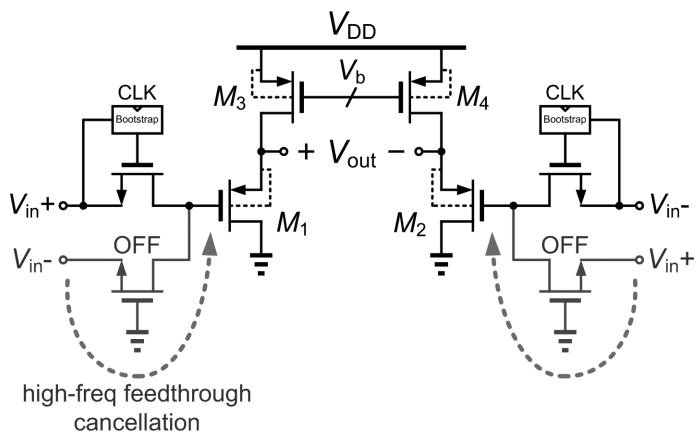


Fig. 13. Front-end T/H schematic with dummy OFF switches for high-frequency input feed-through cancellation.

clock delayed by half a bit cycle period (400ps). If the sampled XOR output is ZERO, the comparator input is not large enough to force the outputs into distinguishable logic levels after half a clock cycle and metastability has occurred. The MT signal is then set to ONE and a metastable-then-set (MTS) algorithm [22] is used to assign the current bit to ONE and the remaining bits to ZERO. Utilizing the MTS algorithm, now the comparator sizing is not dictated by a very low metastability error specification; instead, it can be relaxed in a manner to just resolve digital output levels for a 0.5 V_{LSB} input in less than half a bit cycle period. This way metastability only happens for inputs less than 0.5 V_{LSB} away from the assigned digital output by the MTS algorithm, and the maximum output error due to metastability is only one LSB. In order to reduce the probability of the XOR detector going into a metastable state, it should be verified that the combination of comparator and XOR achieve the target metastability error rate. However, since these two stages are cascaded, this error is exponentially reduced, and it is usually not critical.

C. Front-End T/H

Fig. 13 shows the front-end T/H in each sub-ADC, consisting of a switched capacitor sampling network using a bootstrapped switch [23] followed by an active source-follower based buffer. Based on simulation results, the bootstrapped switch structure proves necessary for not limiting the linearity of the 500 mV_{pp} swing 6 bit core ADC over the entire 5 GHz input frequency range. Extra cross-coupled OFF dummy transistors are used at the input pair, with the same size as the main bootstrapped NMOS switches, to partially cancel the feed-through path between source and drain of the sampling switch. These dummy

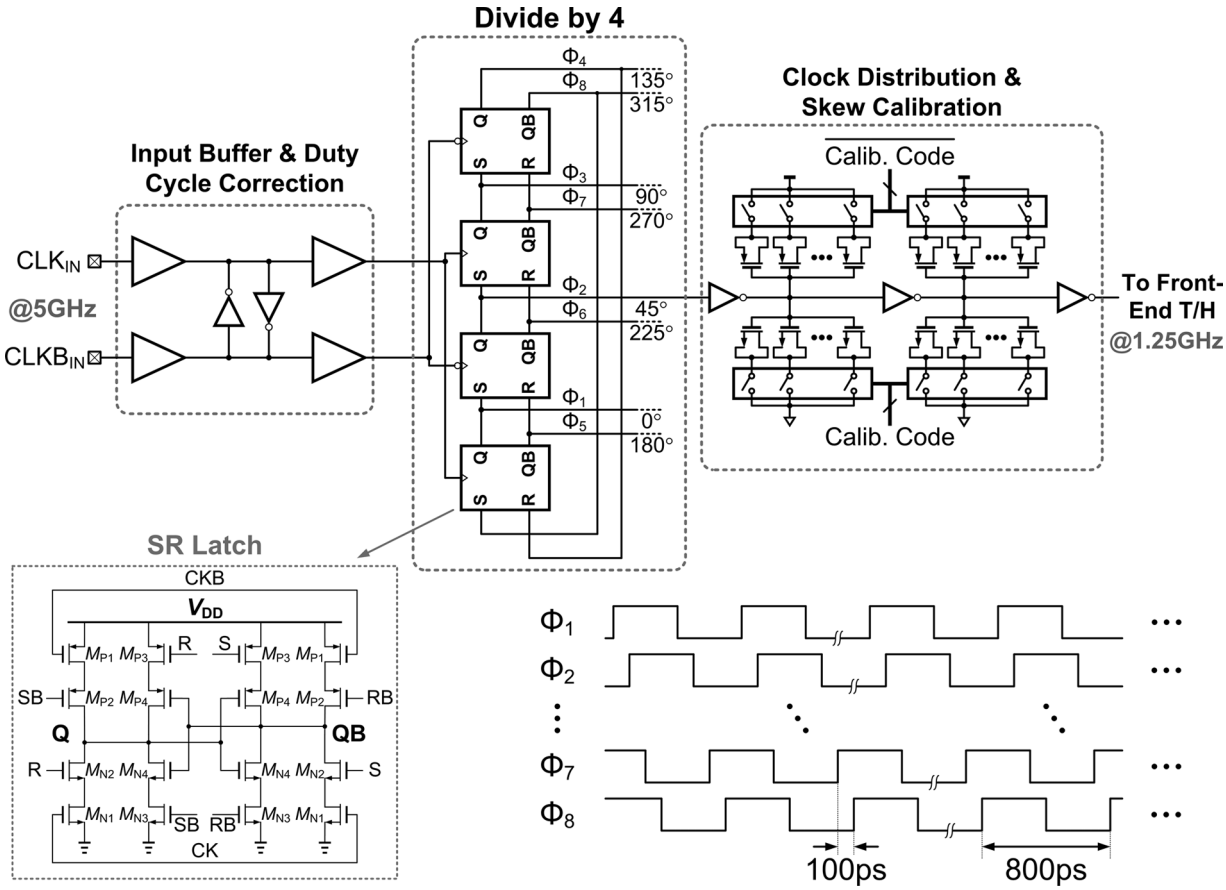


Fig. 14. Front-end T/Hs sampling clocks generation, distribution, and calibration network.

transistors improve the front-end T/H linearity, specifically at high input frequencies.

The front-end T/H architecture allows for a large input sampling bandwidth, as the sampling capacitor is just the input capacitance of the pseudo-differential PMOS source-follower buffer stage. This buffer drives the core ADC input capacitance and provides isolation from kick-back noise. Simulation results show a low-frequency gain of -1.9 dB and a 5 GHz -3 dB bandwidth for the buffers. Transient simulations also verify that with a 300 mV input common-mode voltage and a 500 $\mathrm{mV_{pp}}$ input swing, a linearity better than 6 bits is achieved up to a 5 GHz input bandwidth with a 1.25 GHz sample clock. On-chip buffering of the reference and common-mode voltages, generated off-chip, is also performed with similar PMOS source follower stages.

D. Multi-Phase Sampling Clock Generation and Calibration

Eight equally spaced sampling phases for the front-end T/Hs are generated from an input 5 GHz differential clock, as shown in Fig. 14. A pseudo-differential self-biased input stage buffers the 5 GHz differential clock to drive a divide-by-4 stage. Utilizing four symmetric clocked SR latches [24] in a loop creates eight 1.25 GHz clock phases spaced at 100 ps.

A sinewave-input FFT-based foreground method [16] is used to digitally control MOS capacitor arrays in the per-phase distribution network to calibrate the phase mismatches between the eight critical sampling phases. Fig. 11 shows the clock skew calibration setup, where the optimum calibration code for each sampling phase is obtained using a successive approximation algorithm. Measurement results verify that the clock skew calibration has a resolution of about 0.4 ps and allows for a maximum tuning range of 39 ps per phase. This is sufficient to compensate for the mismatch $\sigma\sim$6 ps between consecutive sampling phases observed in Monte Carlo simulations of the clock input buffer, divider, and distribution network.

V. Experimental Results

A chip microphotograph of the prototype 6 bit ADC, which was fabricated in a GP 65 nm CMOS process and occupies a total active area of 0.52 $\mathrm{mm^2}$, is shown in Fig. 15. The core time-interleaved ADC, consisting of eight sub-ADCs that each have eight parallel unit SAR ADCs, occupies 0.33 $\mathrm{mm^2}$. In order to minimize the critical MSB delay path for DFE operation at 10 Gb/s, the order of the unit ADCs in each sub-ADC is optimized to decrease the maximum distance between consecutive ADCs. This maximum distance is about 400 μm length, which adds a $\sim$70 fF capacitive load due to routing. An inverter chain drives this load, while meeting the 100 ps critical delay path including the 1-tap DFE MUX. Routing from the sampling clocks phase generator and the parasitic capacitance on the input lines is minimized by placing the eight front-end T/Hs close together in the vicinity of the differential input pads. Also, splitting the

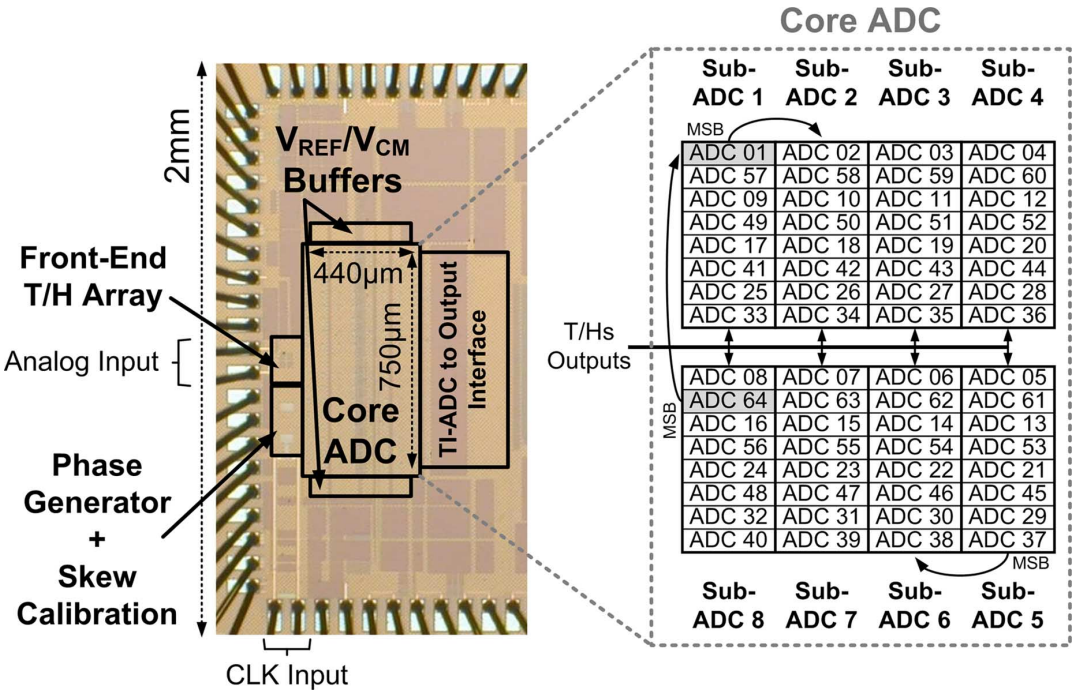


Fig. 15. Prototype ADC chip microphotograph and core ADC floorplan.

global reference and common-mode voltage buffers equally on the top and bottom of the core ADC layout improves the symmetry among the unit ADCs. Local decoupling capacitors in each unit ADC reduce the impact of kickback noise on the reference and common-mode voltages, routed from the two sets of on-die global source-follower based buffers, to an acceptable level for a 6 bit ADC.

A. Core ADC Characterization

In characterizing the general performance of the 6 bit ADC, both the DFE coefficient α and FFE coefficient β are set to zero. After calibrating the offset errors among the 64 time-interleaved unit ADCs and the phase errors of the eight sampling clocks, the dynamic performance of the full time-interleaved ADC at 10 GHz sampling frequency is shown in Fig. 16. A low input frequency maximum SNDR of 29.19 dB is achieved, primarily limited by nonlinearity in the unit ADCs, which translates to an effective number of bits (ENOB) of 4.56 bits. The ADC achieves an effective resolution bandwidth (ERBW) of 4.53 GHz, with a 4.03 bits ENOB at this ERBW. Fig. 17 shows the frequency spectrum of the 10 GS/s ADC output using an $\sim$2.4994 GHz input frequency for three cases, before calibration, after only offset calibration, and after both offset and clock skew calibrations. Before calibration, both the distortion harmonics due to offset mismatch, located at $kf_s/64$, and phase mismatch, located at $kf_s/64 \pm f_{in}$ $(k = 1, 2, \ldots, 32)$, limit the performance. Performing only offset calibration provides a marginal 1.9 dB improvement in SNDR. However, after calibrating for both offset and sampling clock skew, the distortion harmonics due to offset and phase mismatches are non-dominant, and the ADC performance is limited by the nonlinearity

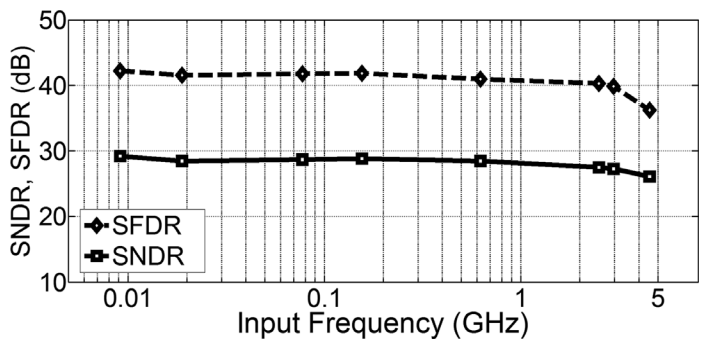


Fig. 16. ADC SNDR and SFDR vs. input frequency at $f_s = 10$ GHz.

of the core ADC and the raised uniform noise floor due to the equipment-limited sampling clock jitter.

A sinewave histogram technique [25] is utilized for static characterization. Fig. 18 shows that, with a 9.746 MHz input at 10 GS/s, the maximum DNL and INL values for the 6 bit ADC are $+0.19/-0.15$ LSB and $+0.65/-0.23$ LSB, respectively.

B. Embedded Equalization Characterization

The range and resolution of the embedded FFE are extracted by averaging the ADC output variation as a function of the 5 bit FFE second tap coefficient $\gamma = B_1B_2B_3B_4B_5$ with a maximum DC input voltage $V_{in} = 0.25$ V for the 500 mV_{pp} input range. As shown in Fig. 19(a), since the second FFE tap is hardwired to subtract from the main cursor as a high-pass filter, the ADC output variation starts from 0 for $\gamma = (00000)_2 = 0$ and linearly decreases to more negative values as the coefficient reaches its maximum $\gamma = (11111)_2 = 31$. The maximum ADC output variation is about 8 LSB, for a maximum 25% range for the

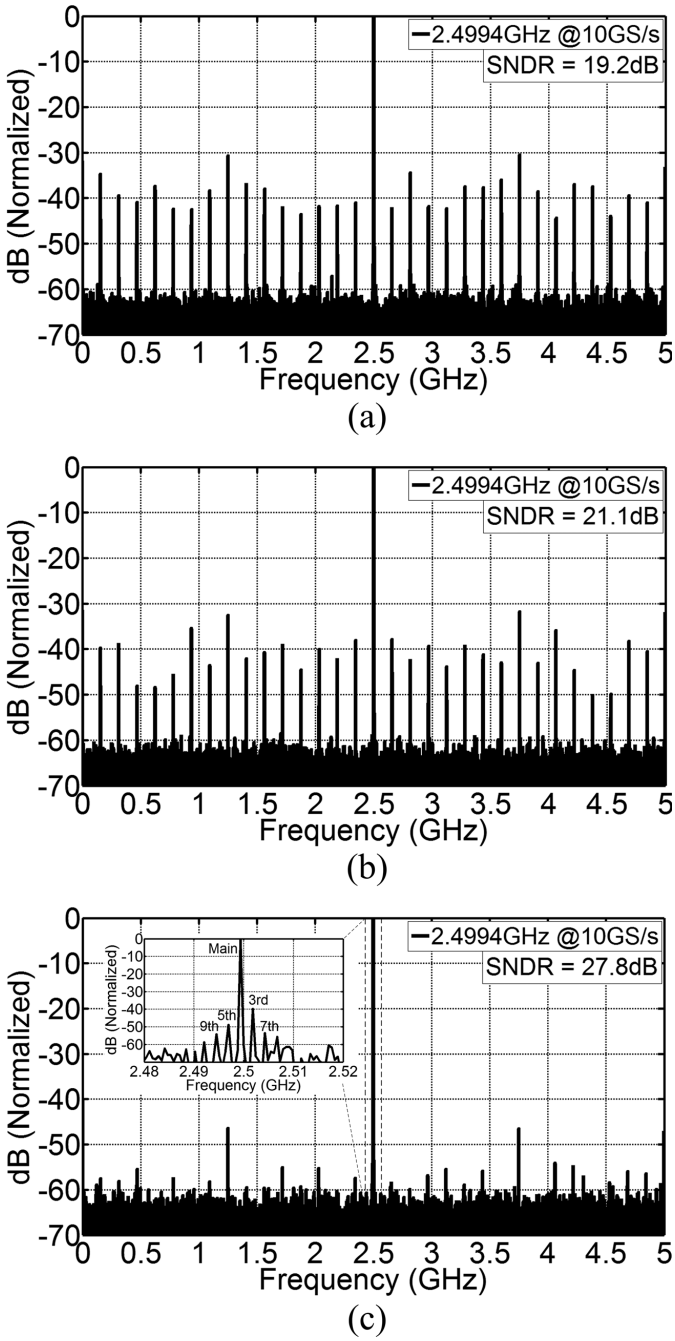


Fig. 17. 10 GS/s ADC normalized output spectrum for $f_{\rm in} = 2.4994$ GHz using a 16k-point FFT: (a) before calibration, (b) after only offset calibration, and (c) after offset and clock skew calibration.

second FFE tap relative to the main cursor. While the coefficient maximum range is limited by the ~ 40 fF $C_{\rm ip}$, consisting of the comparator input devices, DAC capacitance to substrate, and wire capacitance, the linear transfer characteristic allows the 5 bit FFE tap coefficient to achieve a resolution about four times smaller than the core 6 bit ADC.

A similar procedure is utilized to extract the range and resolution of the embedded 1-tap DFE, but with two DC input cases of $V_{\rm in} = 0.25$ V and $V_{\rm in} = -0.25$ V, i.e., the extremes of the 500 $\rm mV_{pp}$ input range. As shown in the right-half of Fig. 19(b), for $V_{\rm in} = 0.25$ V, the MSB should resolve to one and the DFE

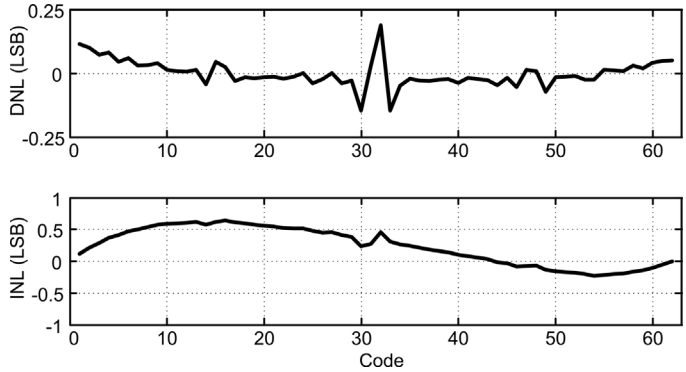


Fig. 18. DNL/INL plots with $f_{\rm in} = 9.746$ MHz at $f_{\rm s} = 10$ GHz.

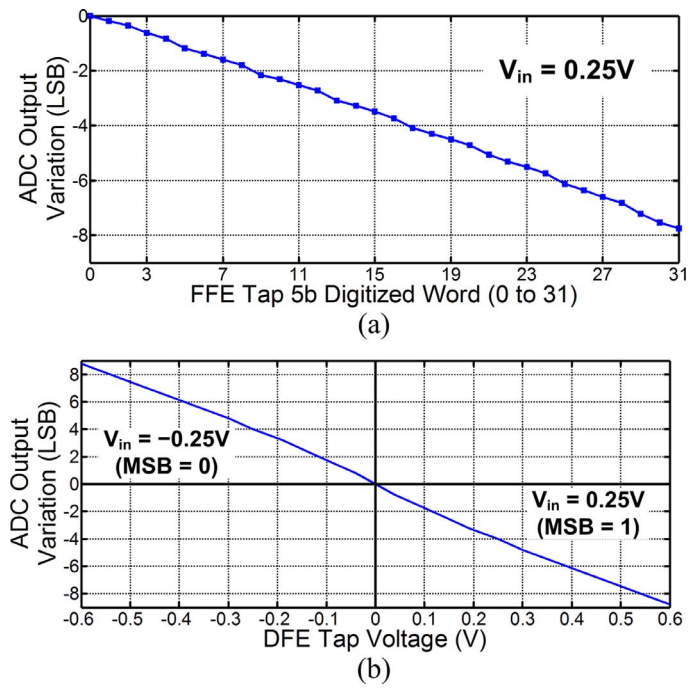


Fig. 19. Measured tap coefficient range and resolution using DC input voltages for embedded (a) FFE 2nd tap, and (b) 1-tap DFE.

coefficient should subtract from the input voltage, resulting in the averaged ADC output code linearly decreasing as the DFE coefficient is increased. With $V_{\rm in} = -0.25$ V the DFE coefficient should effectively add to the input voltage, and in the left half of Fig. 19(b) the averaged ADC output code linearly increases as the absolute value of the DFE coefficient is increased. A similar range of $\sim$25% of the ADC maximum input range is observed for the embedded DFE coefficient, with the linear transfer characteristic also displaying a resolution better than the 6 bit ADC.

In order to verify the functionality of the embedded equalization schemes, a 10 Gb/s $2^{10}-1$ PRBS input is passed through a 10" FR4 channel (channel 2 from Fig. 3) from a Centellax PCB12500 transmit module and the output of the prototype 6 bit ADC is measured using the test setup shown in Fig. 20. The mid-point digitized eye diagram at the ADC output after reconstruction of the digital 6 bit output word is shown in Fig. 21 without and with embedded equalization enabled. Due to ISI,

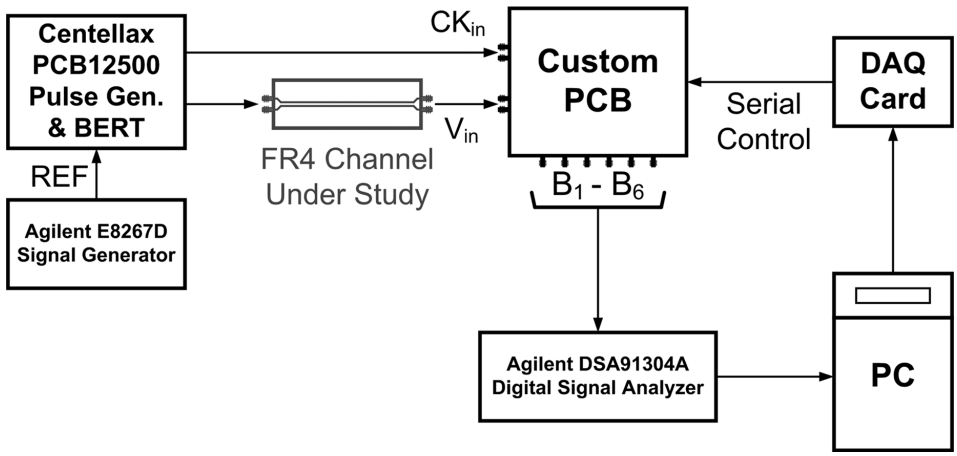


Fig. 20. Embedded equalization characterization test setup.

TABLE I
ADC PERFORMANCE COMPARISON

Specification	Nazemi'08 [27]	Verma'13 [28]	Chung'09 [29]	El-Chammas'11 [30]	Yang'13 [31]	Zhang'13 [3]	Chen'12 [4]	This Work
CMOS Technology	90-nm	40-nm	65-nm	65-nm	65-nm	40-nm	65-nm	65-nm
Supply Voltage (V)	N/A	0.9	1.1	1.1	1.2	N/A	1.1	1.1/0.9
ADC Structure	TI-Pipelined	TI-Flash	Flash	TI-Flash	TI PA-Flash	TI-Flash	TI-Flash	TI-SAR
Equalization	No	No	No	No	No	No	HPF+FFE	Embedded FFE/DFE
Input Range (mV_{pp})	N/A	N/A	800	590	N/A	N/A	600	500
Resolution (bit)	6	6	4.5	5	6	6	4	6
Sampling Rate (GS/s)	10.3	10.3	7.5	12	10	8.5 – 11.5	10	10
ERBW (GHz)	4	>6	>6	6.5	5	5	N/A	4.53
ENOB @ERBW (bit)	5.1	5.1	3.8	3.88	5	4.56	N/A	4.03
Power (mW)	1600	240	52	81*	83	195	93**	79
FOM (pJ/conv.-step)	4.52	0.68	0.497	0.46	0.26	0.59	N/A	0.48
Active Area (mm^2)	N/A	0.27	0.01	0.44	0.2	0.82***	0.29	0.52

* Excluding input clock buffers.
** This value includes the analog front-end power.
*** This is the whole dual-path receiver area including the front-end CTLE and slicer for the second path.

disabling the ADC embedded equalization results in a closed eye and all 64 codes being present. Independently activating the 1-tap DFE and 2-tap FFE results in an eye opening of 9 LSB and 15 LSB, respectively. Enabling both embedded FFE and DFE improves the eye opening to 19 LSB, which verifies the effectiveness of the proposed implementation.

BER measurements are also performed on the three 6", 10" and 15" FR4 channels from Fig. 3 in order to further verify the embedded equalization operation. The BER bathtub curves of Fig. 22 are produced with a 500 mV_{ppd} $2^{10}-1$ PRBS input without any transmit equalization applied to the channel and the MSB output of the ADC fed back to the Centellax PCB12500. For the case when no equalization is embedded in the ADC, only the relatively low-loss 6" channel displays an open eye with ~0.3 UI timing margin at a BER $<10^{-9}$. Activating only the 1-tap DFE improves the 6" channel margins and opens the previously closed eye for the 10" channel. However, operation is still not possible for the 15" channel due to excessive residual ISI. Activating only the 2-tap FFE allows a more significant improvement, with all three channels displaying open eyes. Enabling both the 2-tap FFE and 1-tap DFE yields the best margins, with a 0.37 UI timing margin achieved with the highest-loss 15" channel.

Note that the 25% maximum range of the embedded equalization tap coefficients limits the stand-alone system operation for channels with less than 20 dB Nyquist attenuation, where

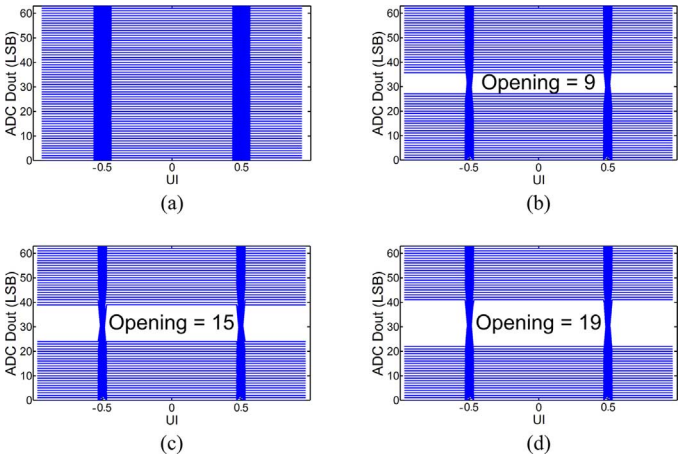


Fig. 21. Measured digitized 6b ADC output (a) without equalization, (b) with only 1-tap embedded DFE, (c) with only 2-tap embedded FFE, and (d) with both embedded FFE and DFE, for a 10 Gb/s $2^{10}-1$ PRBS input over a 10-inch FR4 channel.

mixed-signal receivers, such as a CTLE followed by a DFE, are generally more energy efficient. While utilizing a subsequent digital equalizer with the presented front-end ADC with embedded FFE should allow for the support of higher loss channels, this was beyond the scope of the presented work. In order to allow the stand-alone ADC with embedded equalization to support higher-loss channels, a solution to increase the equalization taps' range relative to the main cursor is to sample the main cursor on the bottom plate of the switched-capacitor sampling network in each unit ADC. Due to the parasitic capacitance at the comparator input, this attenuates the main cursor in a similar manner as the DFE tap and second FFE tap, which can ideally increase the maximum achievable tap coefficient range to near 100% of the main cursor. The authors are currently implementing this solution in a future ADC-based receiver prototype.

C. Performance Summary

The 10 GS/s ADC with embedded equalization consumes 79.1 mW, with the power breakdown shown in Fig. 23. The core TI-ADC consumes the majority of the power, followed by the front-end T/Hs and reference/common-mode buffers, and the phase generator power of the input clock buffer, phase generator block, and distribution network.

Table I summarizes the main specifications and compares this work with previously reported CMOS ADCs with sampling rates around 10 GHz. To the best of our knowledge, this is the first 10 GS/s ADC with combined embedded FFE and DFE functionality. The figure of merit (FOM) for the prototype ADC (also known as Walden's FOM [26]) results in a 0.48 pJ/conv.-step, considering the ENOB at ERBW. Performance comparable to the ADCs in [27]–[31], which do not include any equalization functionality, is obtained. While the advanced flash-ADC architecture of [31] achieves a better FOM, the presented dual-supply design offers the potential for lower-voltage operation. Compared to the designs in [3] and [4], which are examples of state-of-the-art ADC-based

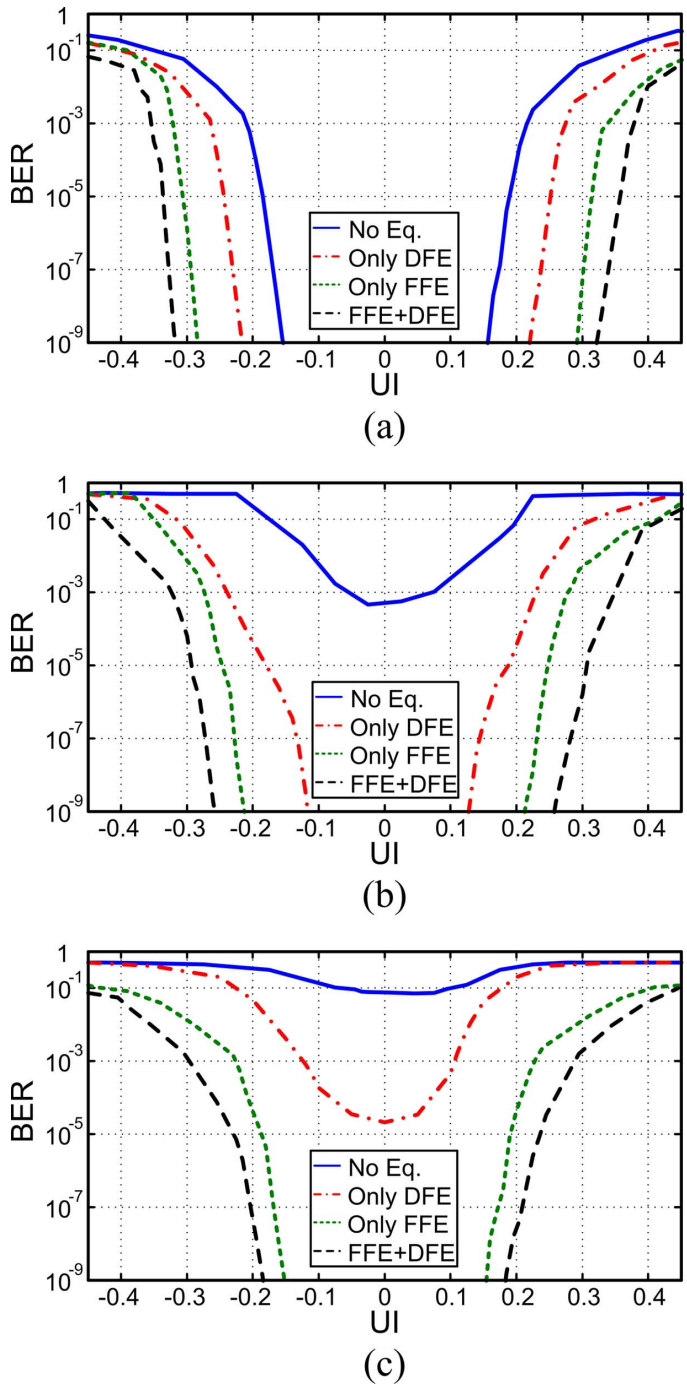


Fig. 22. Measured bathtub curves without and with embedded equalization for a 10 Gb/s $2^{10}-1$ PRBS input over (a) 6-inch FR4, (b) 10-inch FR4, and (c) 15-inch FR4 channels, with channel frequency responses shown in Fig. 3(a).

receivers, the proposed ADC with embedded 2-tap FFE and 1-tap DFE achieves a better ADC FOM while also including the low-overhead embedded equalization schemes.

VI. Conclusion

This paper presented a 10 GS/s 6 bit ADC which efficiently incorporates both a novel 2-tap embedded FFE and a 1-tap embedded DFE. Statistical BER modeling results of ADC-based receivers show that an ADC with embedded equalization can provide both voltage and timing margin improvements for FR4

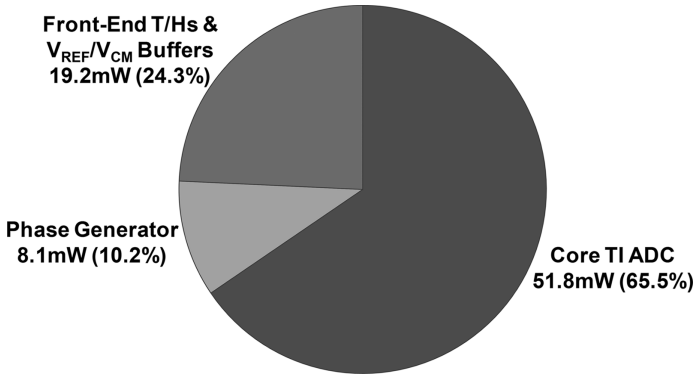


Fig. 23. ADC power breakdown.

channels. These equalization functions are embedded in the capacitive DAC of a time-interleaved SAR ADC, with the FFE post-cursor tap efficiently implemented in the reference DAC, and a redundant cycle technique employed to relax the DFE critical feedback timing path. Measurements verify that the embedded equalization circuitry provides improved timing margins over several FR4 channels. While the maximum embedded equalization coefficient range limits system operation to channels with less than 20 dB Nyquist attenuation, the authors are currently investigating alternative unit ADC sampling schemes for support of 30+ dB attenuation channels. Leveraging the proposed ADC with embedded equalization design techniques in wireline receivers has the potential to allow for reductions in ADC resolution and digital equalization complexity.

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REFERENCES

[1] M. Harwood *et al.*, "A 12.5Gb/s SerDes in 65nm CMOS using a baud-rate ADC with digital receiver equalization and clock recovery," in *IEEE ISSCC Dig. Tech. Papers*, 2007, pp. 436–437.

[2] D. E. Crivelli *et al.*, "Architecture of a single-chip 50 Gb/s DP-QPSK/BPSK transceiver with electronic dispersion compensation for coherent optical channels," *IEEE Trans. Circuits Syst. I: Reg. Papers*, vol. 61, no. 4, pp. 1012–1025, Apr. 2014.

[3] B. Zhang *et al.*, "A 195 mW/55 mW dual-path receiver AFE for multi-standard 8.5-to-11.5 Gb/s serial links in 40nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, 2013, pp. 34–35.

[4] E.-H. Chen, R. Yousry, and C.-K. K. Yang, "Power optimized ADC-based serial link receiver," *IEEE J. Solid-State Circuits*, vol. 47, no. 4, pp. 938–951, Apr. 2012.

[5] J. Kim *et al.*, "Equalizer design and performance trade-offs in ADC-based serial links," *IEEE Trans. Circuits Syst. I: Reg. Papers*, vol. 58, no. 9, pp. 2096–2107, Sep. 2011.

[6] R. Narasimha, M. Lu, N. R. Shanbhag, and A. C. Singer, "BER-optimal analog-to-digital converters for communication links," *IEEE Trans. Signal Process.*, vol. 60, no. 7, pp. 3683–3691, Jul. 2012.

[7] A. Shafik, K. Lee, E. Zhian Tabasy, and S. Palermo, "Embedded equalization for ADC-based serial I/O receivers," in *Proc. IEEE Elect. Performance of Electron. Packaging and Syst.*, Oct. 2011, pp. 139–142.

[8] T.-C. Lee and B. Razavi, "A 125-MHz CMOS mixed-signal equalizer for Gigabit ethernet on copper wire," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, 2001, pp. 131–134.

[9] J. Liu and X. Lin, "Equalization in high-speed communication Systems," *IEEE Circuits Syst. Mag.*, vol. 4, no. 2, pp. 4–17, Sep. 2004.

[10] S. Hoyos, J. A. Garcia, and G. R. Arce, "Mixed-signal equalization architectures for printed circuit board channels," *IEEE Trans. Circuits Syst. I: Reg. Papers*, vol. 51, no. 2, pp. 264–274, Feb. 2004.

[11] R. Payne *et al.*, "A 6.25-Gb/s binary transceiver in 0.13-μm CMOS for serial data transmission across high loss legacy backplane channels," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2646–2657, Dec. 2005.

[12] J. Kang, D. T. Lin, L. Li, and M. P. Flynn, "A reconfigurable FIR filter embedded in a 9b successive approximation ADC," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, 2008, pp. 711–714.

[13] D. T. Lin, L. Li, and S. F. P. Flynn, "A flexible 500 MHz to 3.6 GHz wireless receiver with configurable DT FIR and IIR filter embedded in a 7b 21 MS/s SAR ADC," *IEEE Trans. Circuits Syst. I: Reg. Papers*, vol. 59, no. 12, pp. 2846–2857, Dec. 2012.

[14] A. Varzaghani and C.-K. K. Yang, "A 4.8 GS/s 5-bit ADC-based receiver with embedded DFE for signal equalization," *IEEE J. Solid-State Circuits*, vol. 44, no. 3, pp. 901–915, Mar. 2009.

[15] S. Kasturia and J. H. Winters, "Techniques for high-speed implementation of nonlinear cancellation," *IEEE J. Sel. Areas Commun.*, vol. 9, no. 5, pp. 711–717, Jun. 1991.

[16] E. Zhian Tabasy, A. Shafik, S. Huang, N. H.-W. Yang, S. Hoyos, and S. Palermo, "A 6-b 1.6-GS/s ADC with redundant cycle one-tap embedded DFE in 90-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 48, no. 8, pp. 1885–1897, Aug. 2013.

[17] E. Z. Tabasy, A. Shafik, K. Lee, S. Hoyos, and S. Palermo, "A 6b 10GS/s TI-SAR ADC with embedded 2-tap FFE/1-tap DFE in 65nm CMOS," in *Proc. IEEE Symp. VLSI Circuits*, 2013, pp. C274–C275.

[18] G. Balamurugan, B. Casper, J. E. Jaussi, M. Mansuri, F. O'Mahony, and J. Kennedy, "Modeling and analysis of high-speed I/O links," *IEEE Trans. Adv. Packag.*, vol. 32, no. 2, pp. 237–247, May 2009.

[19] V. Hariprasath, J. Guerber, S.-H. Lee, and U. Moon, "Merged capacitor switching based SAR ADC with highest switching energy-efficiency," *Electron. Lett.*, vol. 46, no. 9, pp. 620–621, Apr. 2010.

[20] P. Harpe *et al.*, "A 26 μW 8 bit 10 MS/s asynchronous SAR ADC for low energy radios," *IEEE J. Solid-State Circuits*, vol. 46, no. 7, pp. 1585–1595, Jul. 2011.

[21] B. Goll and H. Zimmermann, "A comparator with reduced delay time in 65-nm CMOS for supply voltages down to 0.65 V," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 56, no. 11, pp. 810–814, Nov. 2009.

[22] S.-H. Cho, C.-K. Lee, S.-G. Lee, and S.-T. Ryu, "A two-channel asynchronous SAR ADC with metastable-then-set algorithm," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 20, no. 4, pp. 765–769, Apr. 2012.

[23] M. Dessouky and A. Kaiser, "Very low-voltage digital-audio $\Delta\Sigma$ modulator with 88-dB dynamic range using local switch bootstrapping," *IEEE J. Solid-State Circuits*, vol. 36, no. 3, pp. 349–355, Mar. 2001.

[24] B. Nikolic, V. G. Oklobdzija, V. Stojanovic, W. Jia, J. K.-S. Chiu, and M. M.-T. Leung, "Improved sense-amplifier-based flip-flop: design and measurements," *IEEE J. Solid-State Circuits*, vol. 35, no. 6, pp. 876–884, Jun. 2000.

[25] W. Kester, *The Data Conversion Handbook*. Burlington, MA, USA: Newnes, 2005.

[26] R. H. Walden, "Analog-to-digital converter survey and analysis," *IEEE J. Sel. Areas Commun.*, vol. 17, no. 4, pp. 539–550, Apr. 1999.

[27] A. Nazemi *et al.*, "A 10.3GS/s 6bit (5.1 ENOB at Nyquist) time-interleaved/pipelined ADC using open-loop amplifiers and digital calibration in 90nm CMOS," in *Proc. IEEE Symp. VLSI Circuits*, Jun. 2008, pp. 18–19.

[28] S. Verma *et al.*, "A 10.3GS/s 6b flash ADC for 10G ethernet applications," in *IEEE ISSCC Dig. Tech. Papers*, 2013, pp. 462–463.

[29] H. Chung, A. Rylyakov, Z. T. Deniz, J. Bulzacchelli, G.-Y. Wei, and D. Friedman, "A 7.5-GS/s 3.8-ENOB 52-mW flash ADC with clock duty cycle control in 65nm CMOS," in *Proc. IEEE Symp. VLSI Circuits*, 2009, pp. 268–269.

[30] M. El-Chammas and B. Murmann, "A 12-GS/s 81-mW 5-bit time-interleaved flash ADC with background timing skew calibration," *IEEE J. Solid-State Circuits*, vol. 46, no. 4, pp. 838–847, Apr. 2011.

[31] X. Yang, R. Payne, and J. Liu, "A 10GS/s 6b time-interleaved ADC with partially active flash sub-ADCs," in *Proc. IEEE Custom Integr. Circuits Conf.*, Sep. 2013.

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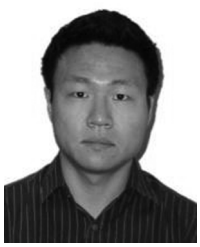

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