A 0.8V, 560fJ/bit, 14Gb/s Injection-Locked Receiver with Input Duty-Cycle Distortion Tolerable Edge-Rotating 5/4X Sub-Rate CDR in 65nm CMOS

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Abstract

A quarter-rate forwarded-clock receiver utilizes an edge-rotating 5/4X sub-rate CDR for improved jitter tolerance with low power overhead relative to conventional 2X oversampling CDR systems. Low-voltage operation is achieved with efficient quarter-rate clock generation from an injection-locked oscillator (ILO) and through automatic independent phase rotator control that optimizes timing margin of each input quantizer in the presence of receive-side clock static phase errors and transmitter duty-cycle distortion (DCD). Fabricated in GP 65nm CMOS, the receiver operates up to 16Gb/s with a BER<10^{-12}, achieves a 1MHz phase tracking bandwidth, tolerates ±50%UI_{pp} DCD on input data, and has 14Gb/s energy efficiency of 560fJ/bit at V_{DD}=0.8V.

Keywords: forwarded-clock receiver, injection-locking.

Introduction

The power consumed by high-speed multi-channel serial link systems is a critical design metric for next-generation computing systems. Improvements in energy-efficiency are possible with forwarded-clocking architectures which allow the potential for high-frequency jitter tolerance and low-complexity periodically-trained de-skew. Furthermore, operating the high-speed transceiver at a lower supply voltage can dramatically improve the energy efficiently due to the quadratic dependency on V_{DD}, at the cost of degraded transistor speed and increased timing uncertainty. While speed limitations can be overcome with increased receiver input de-multiplexing ratios [1], timing uncertainties caused by low-V_{DD} operation (static phase mismatches and temperature/low-frequency power-supply induced jitter) remain significant challenges to the widespread adoption of low-V_{DD} serial links. This work presents a low-voltage quarter-rate forwarded-clock receiver that utilizes a low overhead edge-rotating 5/4X sub-rate CDR that improves jitter tolerance and enables automatic independent phase rotator control to optimize timing margin of each input quantizer in the presence of receive-side clock static phase errors and transmitter duty-cycle distortion (DCD).

Receiver Implementation

Fig. 1 shows the receiver block diagram, with the data path consisting of an inductor-peaked continuous-time linear equalizer (CTLE) driving four de-multiplexing quantizers. The forwarded clock path consists of an input CML clock buffer followed by an AC-coupled ILO that generates four quarter-rate clock phases. I-Q mismatches caused by injection-locking are minimized by adding dummy loads to the ILO internal nodes and delay-tuning buffers that proceed the ILO. Four phase rotators are incorporated that provide independent phase tuning ability for each of the demultiplexing data eyes, enabling the RX to compensate for static phase mismatches and tolerate duty cycle distortion (DCD) in the transmitted data caused by a TX's multiplexing skew. An inverter-based phase interpolator array follows the phase rotators, generating the data and edge clocks used by the 5/4X CDR. Additional statically-tuned delay-adjustable buffers are implemented in each clock path to compensate phase mismatch at startup.

Relative to a conventional 2X oversampling system which doubles the input quantizers, the proposed edge-rotating 5/4X sub-rate CDR shown in Fig. 2 only requires one edge sampling quantizer that rotationally detects early/late information for each sampling clock of the 1:4 demultipexing RX. The bang-bang phase detector output is sub-sampled by a digital accumulator with programmable depth. Adjustment of the phase tracking loop bandwidth is achieved by changing the clock divider ratio from 4 to 1024. The CDR logic updates a bidirectional 128-bit shift register for each phase rotator, preventing the switching glitch typically observed with a conventional binary-to-thermometer decoder.

Experimental Results

Fig. 3 shows the chip micrograph of the proposed quarter-rate receiver, which was fabricated in a GP 65nm CMOS process and occupies an area of 0.36mm^2. A BertScope BSA175C is used for input PRBS data generation, real-time BER testing and sinusoidal jitter (SJ) tolerance testing. Receiver BER bathtub curve at different data rates with a 200mV PRBS31 pattern passing through a 10cm FR4 PCB trace with SMA cables and connectors is shown in Fig. 4. A 0.35UI eye width (BER<10^{-12}) is achieved at 14Gb/s, with the 3.5GHz clock displaying 1.99ps rms jitter and the 3.5Gb/s demuxed data output having healthy margins. Fig. 5(a) shows that the jitter tolerance (BER<10^{-11}) improves dramatically when the 5/4X CDR is activated and a phase tracking bandwidth near 1MHz is achieved at 12Gb/s operation. Fig. 5(b)(c) also shows an oscilloscope capture of the CDR loop operating correctly when a low frequency clock dither is added by digitally toggling the ILO current. In order to demonstrate input DCD tolerance, an 8Gb/s PRBS7 pattern is generated by Tektronix AWG7122B with 0%UI and ±50%UI deterministic DCD, respectively. As shown in Fig. 6, after the CDR is enabled the edge clock is aligned correctly to 4 different edges of the input data with less than 9% UI phase error. Fig. 7 shows the measured receiver jitter tolerance and jitter transfer of the ILO after adding source

synchronous SJ on both the input data and clock. The receiver jitter tolerance corner frequency is ~100MHz, matching the measured ILO jitter transfer bandwidth (JTB). Table I summarizes the system performance and compares this work against recent low-power receivers. The low-voltage operation enabled by the proposed quarter-rate receiver allows for a dramatic improvement in 14Gb/s FOM.

Acknowledgements

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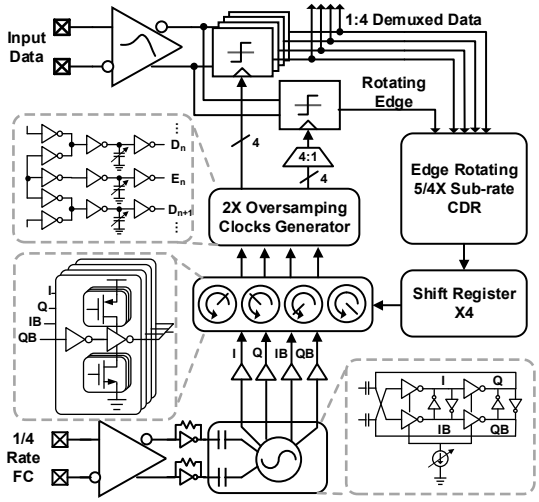

Figure 1. Receiver architecture.

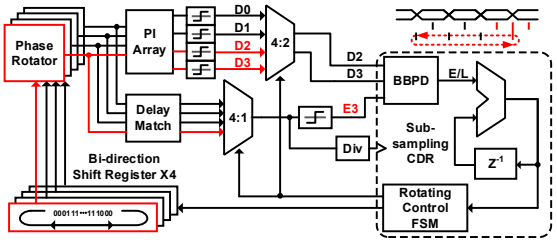

Figure 2. Block diagram of the edge-rotating 5/4X sub-rate CDR.

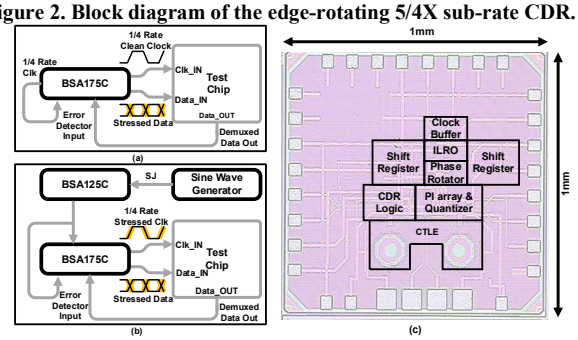

Figure 3. (a) CDR sinusoidal-jitter (SJ) tolerance test setup; (b) Receiver jitter tolerance test setup; (c) Die photo.

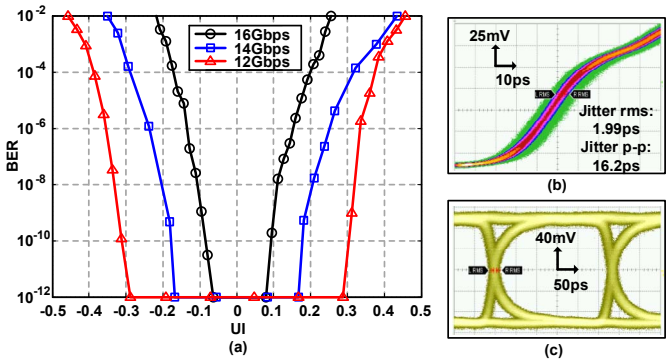

Figure 4. (a) Measured BER bathtub curve; (b) 3.5GHz clock output; (c) 3.5Gbps demuxed data output.

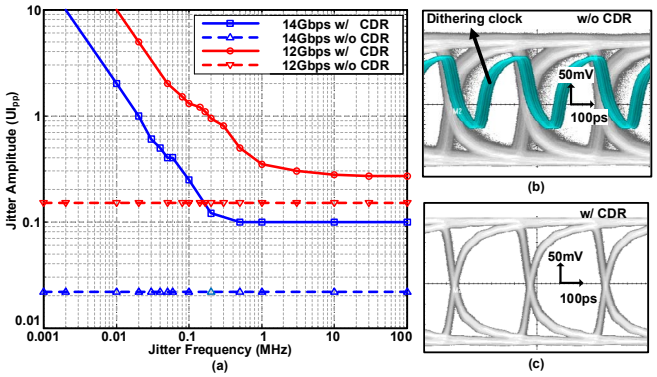

Figure 5. (a) CDR sinusoidal-jitter (SJ) tolerance; (b)(c) 3Gb/s demuxed data with dithering clock when CDR is disabled and enabled.

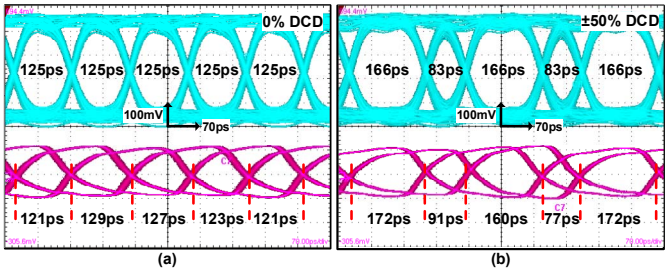

Figure 6. (a)(b) Edge clock rotationally aligned different edges of 8Gb/s data with 0%UI and ±50%UI DCD.

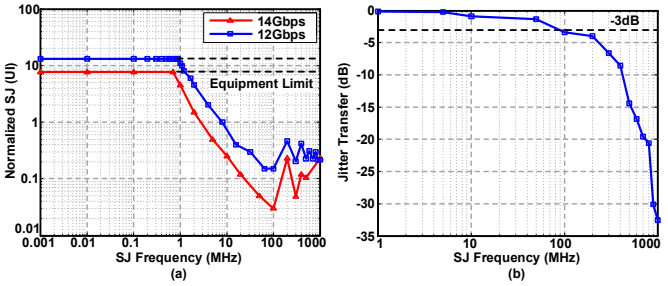

Figure 7. (a) Measured RX jitter tolerance at 12Gb/s and 14Gb/s; (b) Measured jitter transfer bandwidth (JTB) of receiver.

TABLE I: RX PERFORMANCE COMPARISONS

	[2]	[3]	[4]	This Work
V_{DD}, Process	1.0V/65nm	1.25V/90nm	1.08V/32nm	0.8V/65nm
Data Rate	6.4Gb/s	8Gb/s	16Gb/s	14Gb/s
Clock Rate	3.2GHz	2GHz	4GHz	3.5GHz
Clock Arch.	FC	Embedded	FC	FC
Multi-phase Gen.	PLL/PI	DLL	ILO/PI	ILO/PI
RX FOM *(Excludes PLL)	**3.9pJ/bit***	**1.59pJ/bit***	**1.02pJ/bit**	**0.56pJ/bit**