A 15b, Sub-10ps Resolution, Low Dead Time, Wide Range Two-Stage TDC

Noble Narku-Tetteh, Alex Titriku, and Samuel Palermo
Department of Electrical and Computer Engineering
Texas A&M University
College Station, TX, USA 77843
noble.ntetteh@tamu.edu, akntitriku@tamu.edu, spalermo@ece.tamu.edu

***Abstract*—Advancements in imaging and ranging system performance creates the need for increased resolution, range, and speed of time-to-digital converters, a core part of the main data acquisition interface between the analog world and the ranging or imaging system's signal processing or computing core. In this paper, a coarse-fine hierarchical time-to-digital converter (TDC) utilizes two looped structures to achieve a wide dynamic range with high resolution and minimal dead time. The coarse stage consists of a looped TDC, a counter, and a novel counter clock control scheme which allows for indefinite range extension, while the fine stage employs a Vernier delay loop with a new edge-sensitive pulse-generator-based delay element that reduces loop non-linearity associated with mismatched rise/fall times. Also in order to achieve a high sampling rate and low dead-time during conversion, a control algorithm is devised and implemented at circuit level. Fabricated in 1.8V 0.18µm CMOS, the TDC achieves an input range of 204.8ns, 8.125ps resolution, and 7.5ns dead-time, while utilizing 35mW at 100MS/s and 0.23mm^2 in core area.**

Keywords—coarse-fine architecture, time-of-flight (ToF), TDC, Vernier delay loop, positron-emission tomography (PET), laser/light detection and ranging (LIDAR).

I. Introduction

High performance imaging applications, such as PET /MRI (Magnetic-Resonance Imaging), and ranging systems, such as LIDAR, require TDCs with time resolution on the order of picoseconds. For example, increased frame rates and higher resolution of pixels translates to higher resolution of the time-data conversion performed by the TDC. Achieving the required precision level over a wide dynamic range and with minimal system dead time is challenging. Also the push for lower cost system design solutions emphasizes the need for optimization of the TDC architecture.

Some existing TDCs employ time amplification [1-3] to relax the trade-off between dynamic range (DR) and resolution, at the cost of degraded linearity. While a counter-based successive approximation design [4] enables improved DR and resolution performance, this approach suffers from larger area and dead time and is highly non-linear. Also, another digitally intensive approach [5] exploits the latent time quantizing properties of a delay-locked loop (DLL) in an array fashion, coupled with a time interpolation scheme, to achieve fine resolution and dynamic range. While this scheme enhances performance, the tradeoff is additional power and area. Hierarchical architectures [6] with both coarse and fine time quantizer stages offer the potential to maintain high linearity while efficiently scaling to high resolutions. However, the control of this two-stage topology can result in excessive dead time between measurements.

This work presents a two-stage hierarchical TDC which utilizes a coarse looped TDC and a fine Vernier delay loop to achieve a wide dynamic range with high resolution and minimal dead time. A novel counter clock control scheme allows for indefinite range extension in a robust manner, while the fine stage Vernier delay loop employs a new edge-sensitive pulse-generator-based delay element that reduces loop non-linearity associated with mismatched rise/fall times. This mismatch, if unresolved, leads to pulse growth and shrinking in the loop which causes the loop to latch to a digital 1 or 0 permanently until a possible reset action is performed to reset the loop into the open or initial position. The aforementioned event causes instabilities in the quantization process and corrupts the time information.

II. System Architecture

A. Top-Level Structure and Overview

The proposed architecture breaks down the time quantization into two distinct steps: A coarse quantization characterized by wide dynamic range and low resolution with optimized power consumption and small area, followed by a fine quantization. This step is characterized by high resolution and limited dynamic range while maintaining linearity and minimizing area consumption. A control scheme is implemented to stream-line and to synchronize these two stages seamlessly while keeping to a minimum, the latency and conversion time involved. This leads to the small dead-time performance and relatively high sampling rate reported in this work.

Fig. 1 shows the two-stage TDC which utilizes a first-stage 10b coarse quantizer followed by a 5b fine quantizer. A global 1.25GHz delay-locked loop (DLL) with a replica delay line provides an analog control voltage V_{CTRL} to the delay lines employed in both the coarse-stage TDC (CTDC) and fine-stage TDC (FTDC), allowing for resolution tunability and providing improved tracking of PVT variations and errors from correlated jitter sources. A final output buffer stage and clock distribution H-tree enables synchronization of the digital output bits from the two main stages of quantization onto a clock edge generated from the STOP signal.

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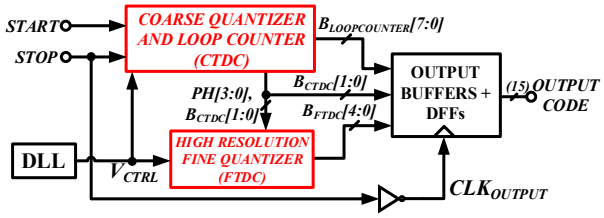

Fig. 1. Two-stage TDC top-level block diagram.

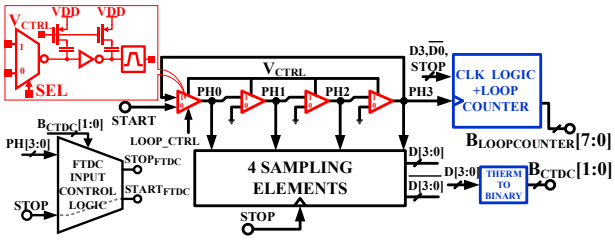

Fig. 2. Coarse stage TDC.

B. *Coarse Quantization Stage TDC*

The coarse quantization stage is designed to achieve large dynamic range with relaxed resolution while utilizing a small area. Also, the decision to utilize as few delay elements as possible is made to allow for better symmetry and matching in order to minimize non-linearity associated with mismatches between delay elements. Hence the CTDC, shown in Fig. 2, utilizes a four-element looped delay line triggered by the START pulse to clock an 8b MSB loop counter. Two additional bits are resolved by sampling the delay cell outputs with the STOP signal. Upon arrival of the STOP signal the loop is reset into the initial open-loop position, awaiting the next START pulse to trigger a pulse recycling event.

The capacitively-tuned delay cells used in the CTDC are symmetric, with all cells having mux input stages for improved matching. As mismatches in the delay cell rise/fall times can accumulate and distort the pulse signal circulating in the delay line, resulting in increased non-linearity for long time measurements, a novel rising-edge triggered pulse generator is used in each delay cell. This pulse generator ensures that the recycled signal is preserved after every delay element without altering the pulse width. The CTDC is designed to have a count resolution of 800ps/step of the 8b counter, and a 204.8ns DR. Robust clocking of the CTDC counter is achieved with the logic shown in Fig. 3. By using the information in the 1st and 4th sampling elements, the position of PH3 relative to the STOP signal can be accurately determined, avoiding any overclocking of the CTDC counter due to residual pulses that may be cycling through the delay line during the reset process. Unresolved, this incorrect clocking would result in MSB errors. However, the aforementioned control scheme addresses this challenge, allowing for indefinite range extension with a larger counter.

C. *FTDC STOP Input Signal Control Block*

In order to allow for optimization of power and also synchronization between the two stages of quantization, the

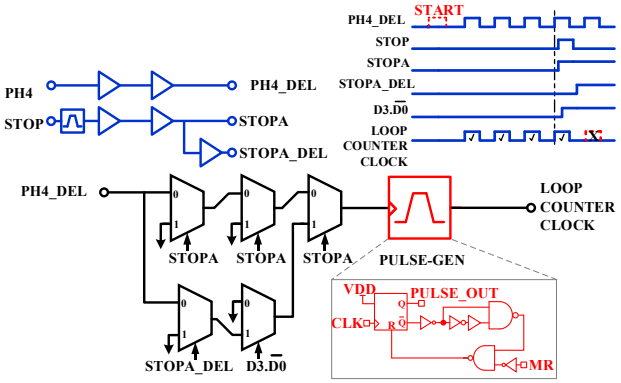

Fig. 3. CTDC counter clock control logic.

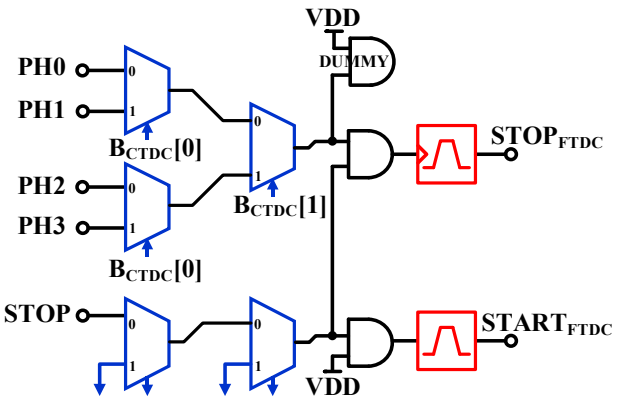

Fig.4. FTDC $START_{FTDC}$ and $STOP_{FTDC}$ signal generation control logic.

FTDC inputs are generated with the goal of limiting the FTDC maximum possible input only to the delay of a single CTDC delay element. This allows for tailoring the design of the CTDC towards high resolution.

The circuit implementation of the control logic to generate the FTDC start and stop signals is shown in Fig. 4. This block takes all four phases from the CTDC delay elements as inputs, and in the absence of STOP passes no signal to the output. At the arrival of the main STOP signal, the computed CTDC phase code determines which of the four phases (PH3-0) to pass as the $STOP_{FTDC}$ signal. $START_{FTDC}$ is generated by passing the main STOP signal through a replica signal path seen by any of the four phases from input of the control logic to the $STOP_{FTDC}$ signal output, preserving the relative delay. Overall, this allows for a simple design with low latency and an identical signal path for all signals.

D. *Fine Quantization Stage TDC*

The FTDC stage (Fig. 5) is a Vernier loop with inputs $START_{FTDC}$ and $STOP_{FTDC}$. These are generated by passing the top-level STOP signal through delay-matching logic, yielding $START_{FTDC}$, and by selecting the appropriate PH[3:0] signals from the CTDC as $STOP_{FTDC}$, described previously. These inputs cycle through their respective delay loops, with the relative delay difference reduced by

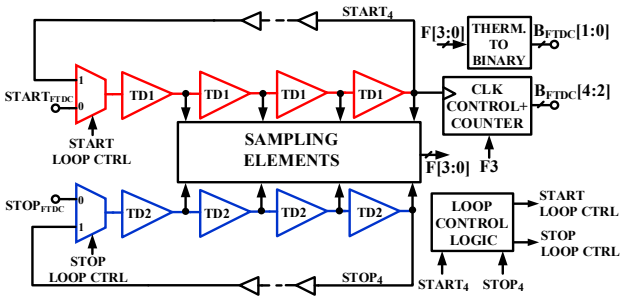

Fig. 5. Fine stage TDC.

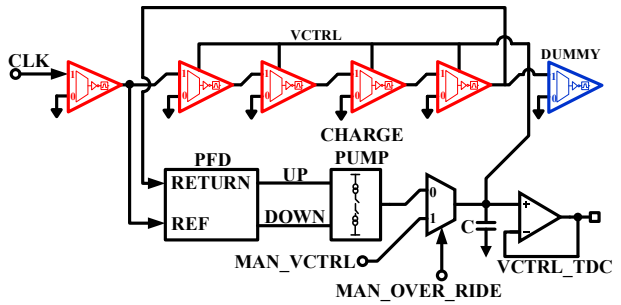

Fig.6. DLL used to generate V_{CTRL} for CTDC and FTDC.

(T_{RES}=T_{D2}-T_{D1}) for every passed delay element, until the $STOP_{FTDC}$ leads the $START_{FTDC}$ signal, signifying the end of the quantization. The Vernier structure makes achieving sub-gate delay resolution possible, however effects of delay mismatch becomes more prevalent with increasing time resolution and this also worsens for increasing delay element count. The open loop version of the Vernier delay line alone would require doubling the number of delay elements per bit increment. This obviously leads to heavy area penalties while making the issue of non-linearity even worse. These challenges are hence addressed by adapting a looped version of the Vernier delay line and maintain only four delay elements per delay line. This looped structure reduces area and non-linearity associated with mismatches in delay element due to reduced element count, while utilizing the pulse-generator delay cells allows for indefinite pulse circulation and a large DR at no area cost.

E. Delay-Locked Loop (DLL)

In order to reduce non-linearity in the TDC operation, due to variations in the delay of the delay elements resulting from PVT variations and correlated noise, a DLL (Fig. 6) is used to provide an analog control voltage for tuning the delay elements. In this work a replica of the CTDC delay path, located close to the CTDC, is used as the delay line for the DLL. The DLL is used to set and track the delays along this line and the control voltage is provided to the actual CTDC delay elements by use of a unity-gain buffer, allowing for some decoupling between the DLL and the CTDC. The nature of the input signals START and STOP is non-periodic and asynchronous to the DLL clock; hence a direct DLL approach with the CTDC would be unsuitable. Using this replica delay line proved suitable in this work.

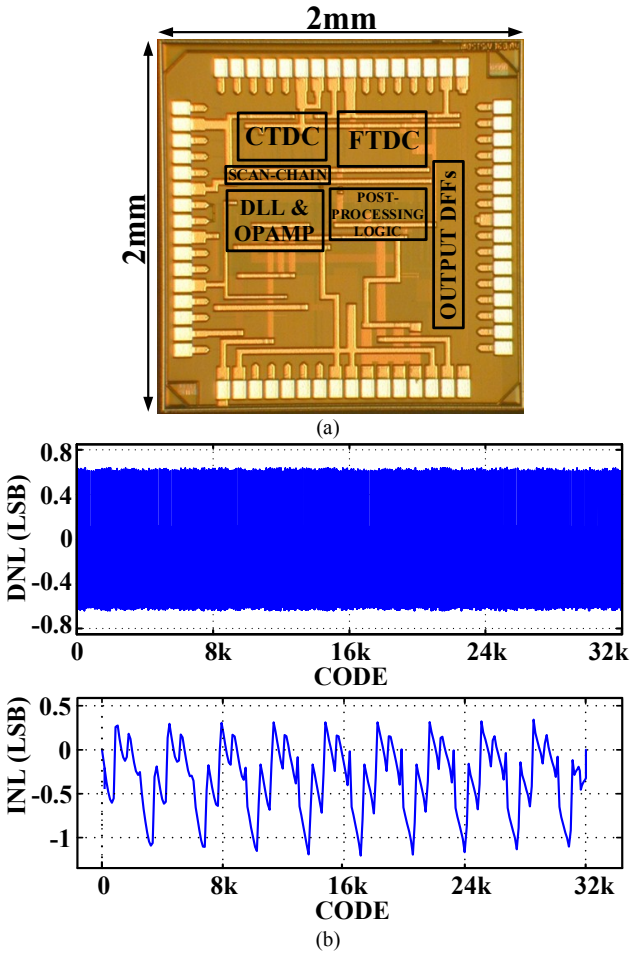

Fig. 7: (a) Chip Micrograph. (b) DNL and INL over the 15b code range.

III. Experimental Results

Fig. 7(a) shows the chip micrograph of the two-stage TDC, which was fabricated in a 0.18µm CMOS process and occupies a core area of 0.23mm^2. DNL and INL performance with 5MHz and (5MHz+10Hz) clock signals used to generate a ramp input is also shown in Fig. 7(b). The maximum DNL and INL values are +0.64/-0.64 LSB and +0.37/-1.21 LSB, respectively, with the periodic behavior due to the looped structures' inherent re-use of delay elements. Fig. 8 shows the TDC code distribution for single-shot experiments taken near the measurement range extremes and the measurement standard deviation versus input time difference. The single-shot precision (SSP) degrades slightly with increasing input time due to accumulated jitter primarily in the CTDC, and has a peak value across the input range that is < 1.5*LSB. In Fig. 9 the supply voltage is varied from 1.5V to 2.2V and the SSP is determined as a function of this variation, for a constant input of 3.022ns. The SSP is seen to improve with increasing supply. This is due to sharper transition edges and improved time resolution. Table I summarizes the performance of the proposed TDC and compares this work against recent hierarchical and successive approximation TDCs. Overall, the TDC achieves

a 204.8ns DR, 8.125ps resolution, and the shortest 7.5ns dead time, while consuming 35mW, and supporting a dramatically higher 100MS/s sampling rate.

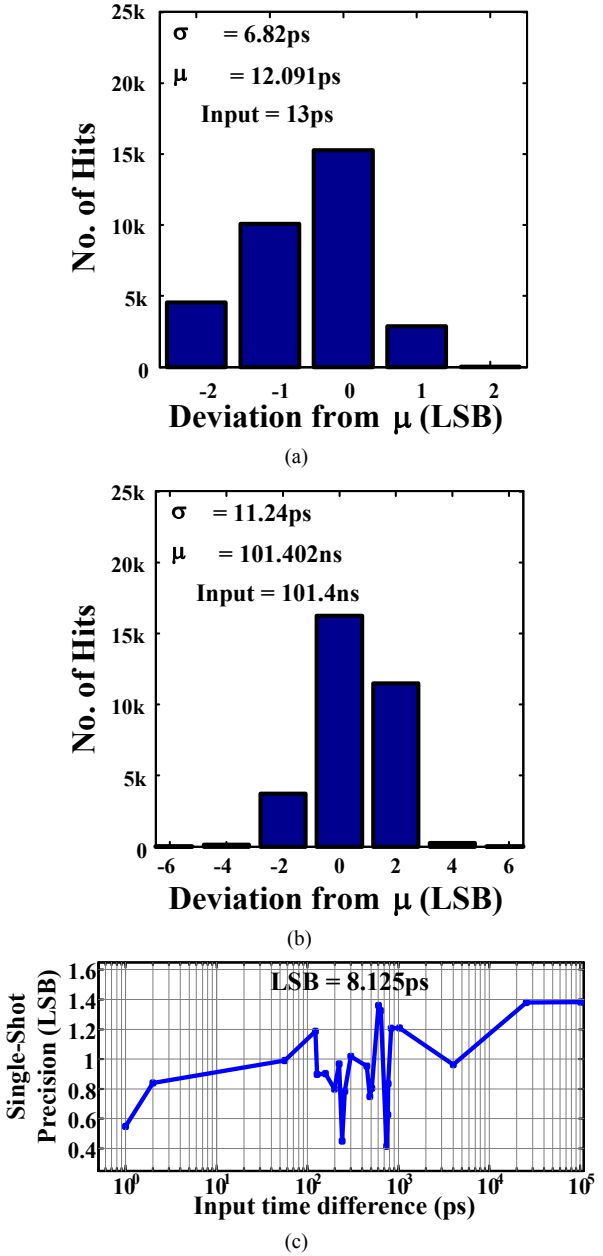

Fig. 8: Single-shot experiment code distribution for (a) 13ps and (b) 101.4ns input times. (c) Single-shot precision versus input time.

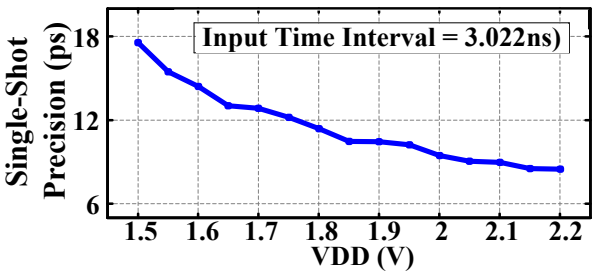

Fig. 9. Single-shot precision versus power supply voltage

IV. Conclusion

A two-stage hierarchical TDC has been demonstrated in a 0.18µm technology which allows for both a wide dynamic range with high resolution and minimal dead time. The proposed novel counter clock control scheme allows for indefinite range extension, while the fine stage employs a Vernier delay loop with a new edge-sensitive pulse-generator-based delay element that reduces loop non-linearity associated with mismatched rise/fall times. These techniques allow for a wide dynamic range with minimal area overhead, providing an efficient TDC architecture for potential high-performance imaging and ranging applications.

Acknowledgements

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V. References

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TABLE I. Performance Summary

Specification	[6]	[4]	This work
Technique	*Hierarchical*	*Successive Approximation*	*Hierarchical*
Technology	0.35µm	0.35µm	0.18µm
Max. Sampling Rate	3MS/s	5MS/s	100MS/s
No. of Bits	15	29	15
Resolution (ps)	10	1.22	8.125
DR (ns)	160	327680	204.8
DNL_{PEAK}/INL_{PEAK}(LSB)	0.04/1.5	14.7/22.1*	0.64/1.21
Dead-time (ns)	150	200	7.5
Power (mW)	<80	33	35
Core Area (mm^2)	0.3	0.79*	0.23

*Estimated – from material and figures in Section E of reference paper. Area is estimated from Fig. 11 and the data provided in Table I of reference paper.