A 0.18-µm CMOS Fully Integrated 0.7-6 GHz PLL-Based Complex Dielectric Spectroscopy System

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***Abstract* — A fully-integrated sensing system utilizes a ring oscillator-based phase locked loop (PLL) for wideband complex dielectric spectroscopy of materials under test (MUT). Characterization of both real and imaginary MUT permittivity is achieved with frequency-shift measurements between a sensing oscillator, with a frequency that varies with MUT-induced changes in capacitance and conductance of a delay-cell load, and an amplitude-locked loop (ALL)-controlled MUT-insensitive reference oscillator. Fabricated in 0.18-µm CMOS, the 0.7-6 GHz spectroscopy system occupies 6.25 mm^2 area and achieves 3.7% maximum permittivity error.**

I. Introduction

Broadband dielectric spectroscopy (BDS) is the study of the frequency profile of a material's complex relative permittivity $\varepsilon_r^* \triangleq \varepsilon_r' - j\varepsilon_r''$ [1]. The use of BDS for biosensing applications at radio and microwave frequencies has been demonstrated, e.g. [2] uses a time domain reflectometry variant of the BDS technique to probe biological samples on cellular and molecular length scales. BDS is also a valuable technique for industrial applications in material characterization at radio and microwave frequencies, e.g. detection of concentration, bulk density, structure, moisture content, etc. [3]. However, the instruments used in the mentioned biomedical and industrial applications are bulky and expensive, while also requiring large sample sizes. The potential system cost and size reduction motivates the development of fully integrated BDS systems in CMOS for point-of-care medical diagnosis platforms and for lab-on-chip industrial sensors.

Previously, CMOS BDS systems based on *LC* voltage-controlled oscillators (VCO) [4], [5] have enabled efficient embedding of lumped sensing capacitor elements within the excitation VCO/synthesizer to allow for self-sustained measurement of the MUT-induced frequency shift with simple and highly precise readout circuits. Unfortunately, due to the *LC*-oscillator implementation these systems can only characterize the real part of permittivity (ε_r') over a limited frequency range. Recent advances in dielectric spectroscopy systems have enabled complex permittivity detection over extended frequency ranges. The work of [6] measures MUT-induced changes in insertion loss of off-chip coupled transmission lines using parallel low- and high-bandwidth RF modules to extend ε_r' detection over a MHz to GHz range. Integration of on-chip sensors and RF receiver front-ends is achieved in [7], [8] to enable both real and imaginary ($\varepsilon_r', \varepsilon_r''$) permittivity detection over wide bands. However, these CMOS implementations lack the integration of critical components, such as the sensor [6], frequency synthesizer (excitation source) and read-out ADC [6]-[8], necessitating the use of expensive, bulky equipment (e.g. RF signal generator) for system operation.

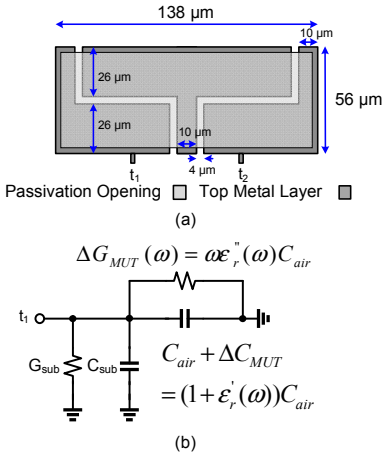

Fig. 1. (a) Sensing capacitor layout, and (b) its single-ended model.

This work presents a self-sustained, fully-integrated PLL-based BDS system which utilizes two ring oscillators, one loaded with an on-chip sensing capacitor and the other serving as a reference, for precise permittivity measurement over a broad frequency range. A measurement procedure is proposed with a parallel amplitude locked loop (ALL) that equalizes the sensor and reference oscillators' delay cell conductance to enable quantitative detection of *both* real and imaginary permittivity components over 0.7-6 GHz with only a simple digital counter for frequency shift measurements.

II. VCO-Based Complex Permittivity Sensor

Fig. 1 shows the sensing capacitor, implemented in the

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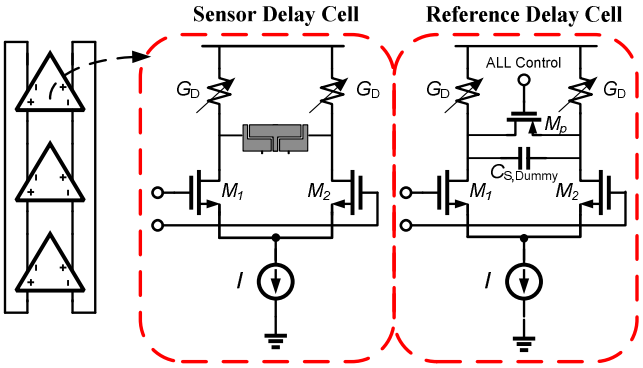

Fig. 2. 3-stage sensing and reference ring oscillators' delay cells.

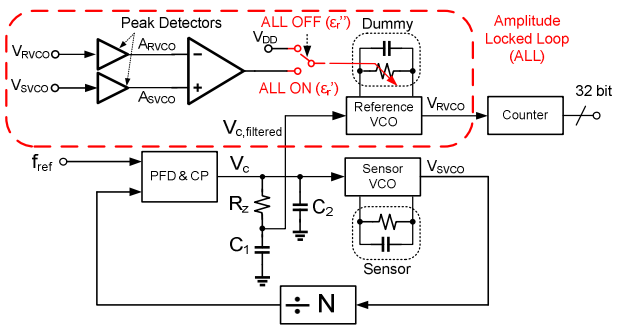

Fig. 3. Broadband PLL-based complex dielectric spectroscopy system.

top metal layer of a 0.18-μm CMOS process. Exposing the capacitor to a MUT changes its capacitance ($\Delta C_{\mathrm{MUT}}(\omega)$) and conductance ($\Delta G_{\mathrm{MUT}}(\omega)$) proportional to ε_r' and ε_r'', respectively.

Unlike LC oscillators, the frequency of a ring oscillator (Fig. 2) is a function of the total load conductance G and capacitance C of the delay cell ($f \propto G/C$) and the oscillation amplitude is a function of its tail current I and load conductance ($A \propto I/G$). Using the MUT-induced shifts in oscillation frequency and output amplitude of a sensor ring oscillator (SVCO) loaded with the sensing capacitor and MUT, $\Delta C_{\mathrm{MUT}}(\omega)$ and $\Delta G_{\mathrm{MUT}}(\omega)$ can potentially be determined, and thus ε_r' and ε_r'' subsequently calculated to fully characterize the MUT complex permittivity.

In order to avoid precisely measuring the ring oscillator amplitude to extract distinct capacitance and conductance shifts, this work proposes a novel two-step procedure that utilizes an unexposed, MUT-insensitive reference oscillator and an ALL. Consider first the open-loop case shown in Fig. 2, with the sensor load substituted with a dummy capacitor and PMOS resistor M_p in the delay cell of the reference oscillator (RVCO). After MUT application the first step is ε_r' measurement mode, where the ALL is activated to set the reference oscillator amplitude equal to that of the sensor oscillator by adjusting the M_p gate voltage such that the two delay cells' conductance are matched. Then the measured frequency shift between the two oscillators ($\Delta f_{\mathrm{ALL,ON}} = f_{\mathrm{RVCO,ALL,ON}} - f_{\mathrm{SVCO}}$) can be formulated as

$$\frac{\Delta f_{\mathrm{ALL,ON}}}{f_{\mathrm{SVCO}}} = \frac{\Delta C_{\mathrm{MUT}}}{C}, \qquad (1)$$

which shows that $\Delta f_{\mathrm{ALL,ON}}$ is a function of $\Delta C_{\mathrm{MUT}}(\omega)$ only, regardless of MUT loss, and can be used to determine ε_r'. In the second step, ε_r'' measurement mode, while the MUT is still on top of the sensor the ALL is deactivated and the frequency shift between the two oscillators ($\Delta f_{\mathrm{ALL,OFF}} = f_{\mathrm{RVCO,ALL,OFF}} - f_{\mathrm{SVCO}}$) can be formulated as

$$\frac{\Delta f_{\mathrm{ALL,OFF}}}{f_{\mathrm{SVCO}}} = \frac{\Delta C_{\mathrm{MUT}}/C - \Delta G_{\mathrm{MUT}}/G}{1 + \Delta G_{\mathrm{MUT}}/G}, \qquad (2)$$

which shows that $\Delta f_{\mathrm{ALL,OFF}}$ is a function of both the sensor's capacitance $\Delta C_{\mathrm{MUT}}(\omega)$ and conductance $\Delta G_{\mathrm{MUT}}(\omega)$. As $\Delta C_{\mathrm{MUT}}(\omega)$ has been previously determined in ε_r' mode, it is possible to isolate $\Delta G_{\mathrm{MUT}}(\omega)$ and determine ε_r''. In summary, the proposed system only needs two straightforward frequency shift measurements to completely and precisely characterize the MUT complex permittivity.

III. System Implementation

Placing the sensing VCO inside an integer-N PLL allows precise control of the sensing frequency [5], as shown in the proposed BDS system block diagram (Fig. 3). In parallel, the open-loop reference VCO is controlled by an RC-filtered version of the PLL control voltage, $V_{c,\mathrm{filtered}}$ to enable cancellation of frequency drift due to temperature variations and correlated low frequency noise.

The SVCO and RVCO frequency-vs-voltage curves of Fig. 4 illustrate the closed-loop system operation. Placing the MUT on top of SVCO shifts its free running frequency down by a value that varies with both MUT ε_r' and ε_r''. The PLL then maintains an SVCO frequency equal to Nf_{ref} by adjusting the control voltage from $V_{c,Air}$ to $V_{c,MUT}$, setting G_D to compensate for $\Delta C_{\mathrm{MUT}}(\omega)$ and $\Delta G_{\mathrm{MUT}}(\omega)$. In ε_r' mode the ALL is enabled to match/increase the RVCO delay cell conductance to the SVCO value, such that the frequency shifts upwards relative to SVCO by

$$\frac{\Delta f_{\mathrm{ALL,ON}}}{f_{\mathrm{SVCO}}} = \frac{f_{RVCO} - Nf_{ref}}{Nf_{ref}} = \frac{\Delta C_{MUT}}{C}. \qquad (3)$$

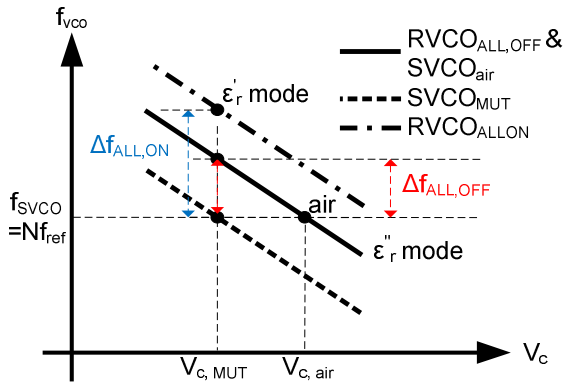

Fig. 4. Sensor and reference VCO frequency versus control voltage during the MUT characterization procedure.

In ε_r'' mode the ALL is disabled and the RVCO frequency returns to its original $V_{c,MUT}$ value, with a frequency difference of

$$\frac{\Delta f_{ALL,OFF}}{f_{SVCO}} = \frac{f_{RVCO} - Nf_{ref}}{Nf_{ref}} = \frac{\Delta C_{MUT}}{C} - \frac{\Delta G_{MUT}}{G}. \quad (4)$$

Thus, precise frequency shift measurements allow for computation of $\Delta C_{\mathrm{MUT}}(\omega)$ and $\Delta G_{\mathrm{MUT}}(\omega)$ with Equations (3) and (4). Given that the sensing oscillator frequency is always Nf_{ref}, the frequency shifts $\Delta f_{\mathrm{ALL,ON}}$ and $\Delta f_{\mathrm{ALL,OFF}}$ can be determined by simply measuring the oscillating frequency of the reference VCO. This is achieved using an on-chip 32-bit counter to allow for noise filtering by averaging over a long time interval. This method enables the same frequency detection precision as in [9], while also accurately controlling the sample excitation frequency as in [4], [5].

Aside from the sensor and replica loads, the two ring oscillators are identical. A three-stage CML topology is employed to allow for wide-band operation and low harmonic distortion, with the CML delay cell gain designed higher than 2 to guarantee oscillation for worst-case MUT loss. Frequency tuning is performed by varying G_D, which consists of a 2-bit discrete resistor bank and a PMOS transistor in triode for continuous tuning. To make the oscillation amplitude independent of the PLL control voltage, the VCO bias current is set via a common mode feedback circuit that utilizes a replica delay cell and a pre-defined reference voltage.

In order to form the ALL, two peak detectors are connected to the reference and sensing VCOs to monitor the amplitude difference between the two oscillators. These peak detector outputs feed a high gain opamp to control M_p in the reference VCO. The maximum conductance of M_p is designed to match the maximum value of ΔG_{MUT}, with additional margin to account for process variations. Disabling the ALL for ε_r'' measurement mode is achieved by connecting the gate of M_p to V_{DD} to maximize its resistance.

IV. Experimental Results

Fig. 5 shows the chip micrograph of the BDS system, which is fabricated in a 0.18-μm CMOS process. The system occupies 6.25 mm^2, and consumes 69-140 mW from a 1.8V supply. Utilizing a 28.5 MHz reference frequency, the PLL operates between 0.7-6 GHz for MUTs with ε_r' in the range between 1 and 30 and ε_r'' in the range between 0 and 30, corresponding to organic chemical values.

For all the reported results a 300 ms counting time is used for frequency shift measurements, with each measurement repeated 10 times and averaged. Measuring the counter output with the sensor exposed to air allows for characterization of the system noise, resulting in a normalized standard deviation of 0.01% with the ALL OFF and 0.08% with the ALL ON.

System performance over frequency is verified by exposing the sensor to several binary mixtures of ethanol and methanol with mixing ratios of methanol q = {0, 20, 50, 80, 100}% and measuring the frequency shifts due to each mixture with the ALL ON and OFF across 0.7-6GHz. The mixtures with q = {0, 50, 100}% are utilized for calibration, as described in [4], [5]. From (3) and (4), the relative frequency shifts $\Delta f_{ALL,ON}/(Nf_{ref})$ and $(\Delta f_{ALL,ON} - \Delta f_{ALL,OFF})/(Nf_{ref})$ are functions of $\Delta C_{\mathrm{MUT}}(\omega)/C$ and $\Delta G_{\mathrm{MUT}}(\omega)/G$, and so they are also functions of ε_r' and ε_r'', respectively. System calibration is performed with a quadratic equation to fit $\Delta f_{ALL,ON}/(Nf_{ref})$ and $(\Delta f_{ALL,ON} - \Delta f_{ALL,OFF})/(Nf_{ref})$ as a function of reported ε_r' and ε_r'' of the reference mixtures (q = {0, 50, 100}%). For mixtures with q = {20, 80}, ε_r' and ε_r'' are determined by substituting frequency shift measurements in the calibrated equations, with the

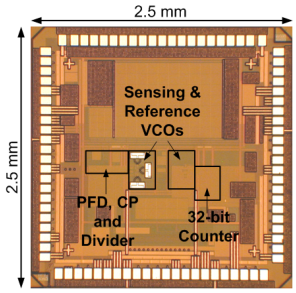

Fig. 5. Micrograph of the PLL-based dielectric spectroscopy chip.

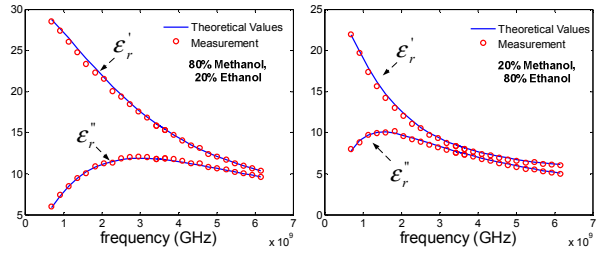

Fig. 6. Measured and theoretical ε_r' and ε_r'' of ethanol-methanol mixtures versus frequency.

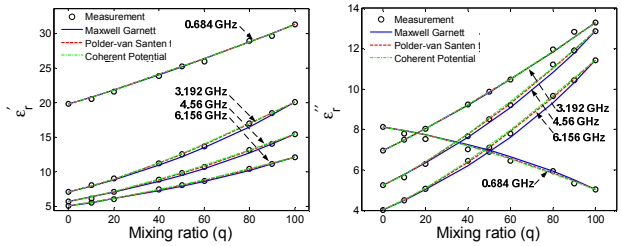

Fig. 7. Measured and theoretical ε_r' and ε_r'' of ethanol-methanol mixtures versus mixing ratio, q, at different frequencies.

measured and reported values of ε_r' and ε_r'' shown in Fig. 6. These measurements show that the maximum error between the measured and theoretical values over the entire frequency range is less than 3.7% for both ε_r' and ε_r''.

System performance over mixing ratio is verified using more binary mixtures of ethanol and methanol with mixing ratios of methanol q = {0, 10, 20, 40, 50, 60, 80, 100}% for frequencies 0.684, 3.192, 4.56 and 6.156 GHz. Similar to the previous experiment, mixtures with q = {0, 50, 100}% are utilized for calibration. Fig. 7 shows measured and theoretical ε_r' and ε_r'' versus mixing ratio, q, with the measurements following the theoretical values with a maximum error of 3.5%.

Table I summarizes the system performance and compares this work against other reported CMOS BDS designs. To the best of our knowledge, this work presents the first fully integrated system that could characterize both MUT ε_r' and ε_r''. Compared to [6], [7], which require external frequency synthesizers and voltage-mode ADCs, the proposed system integrates the sensor inside the on-chip VCO/PLL and uses a simple counter for frequency shift measurements that yield comparable accuracy. Relative to the LC-VCO system of [4], this work achieves a much wider 0.7-6 GHz range and is capable of characterizing both ε_r' and ε_r''.

V. Conclusion

This work presented a fully integrated BDS system utilizing a ring oscillator-based PLL for wide band operation. A novel procedure is proposed for extracting MUT ε_r' and ε_r'' using two frequency shift measurements, which is considerably simpler than voltage measurement approaches. The proposed system achieves the highest CMOS integration level and could accurately characterize ε_r' and ε_r'' of methanol and ethanol mixtures over a wide frequency range.

TABLE I: Performance Summary

Specification	This Work	[7]	[6]	[4]
Technology	180 nm	65 nm	350 nm	90 nm
Functionality	ε_r', ε_r''	ε_r', ε_r''	ε_r'	ε_r'
Sensing Frequency (GHz)	0.7– 6	1-50	0.05-2.5	7-9
Max Error	3.7 %	NA	1% (2GHz) 8.7%(2.5GHz)	3.7 %
Power (mW)	69-140	114**	4-9**	16.5
Area (mm^2)	6.25	1.2	1.44***	6.25

* Calculated for |ε|= 4.45 @ 20 GHz
**Does not include frequency synthesizer and ADC.
*** Sensor is not integrated

Acknowledgement

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