Statistical Modeling of Metastability in ADC-Based Serial I/O Receivers

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***Abstract*— This paper develops metastability error models for flash and asynchronous SAR ADCs and describes a novel ADC-based receiver statistical modeling methodology to analyze the BER performance impact of metastability error propagation through digital FFE equalization.**

Keywords—ADC-based receiver; metastability; statistical BER

I. Introduction

For operation at high data rates over high-loss channels, ADC-based serial link receivers (Fig. 1) are being proposed due to their ability to perform equalization in the digital domain and support bandwidth efficient modulation schemes, such as PAM4 and duobinary [1]. However, ADC-based receivers generally consume higher power than binary receivers because of the multi-GS/s ADC implementations. Therefore, power-efficient ADC structures employing binary search algorithms, such as SAR ADCs, are being considered in favor of flash ADCs which use a brute-force search algorithm. Despite potential power efficiency advantages, the binary search algorithm is inherently prone to comparator metastability, which can cause large conversion errors at the ADC output and degrade BER performance in ADC-based receivers. While time-domain simulations can show the impact of metastability error on BER performance, the number of bits required to validate typical BER targets ($<10^{-12}$) becomes prohibitive and makes time domain simulation impractical. Thus, efficient simulation approaches are desirable to guide system designers in ADC architecture choice and allow circuit designers to see the receiver-level impact of comparator performance.

This paper presents an ADC-based statistical modeling methodology to analyze the BER impact of ADC metastability errors. Metastability models are developed in Section II for two popular high-speed ADC structures: flash and asynchronous SAR (aSAR) ADCs. Section III presents different methods to model metastability error propagation through a digital feed-forward equalizer (FFE), with a detailed discussion on the proposed partial-bit mapping approach that generates the error probability density function (PDF) at the FFE output. This error PDF is inserted into a statistical link model to evaluate BER degradation due to metastability error, with simulations comparing the proposed statistical model and transient results shown in Section IV. Finally, Section V concludes the paper.

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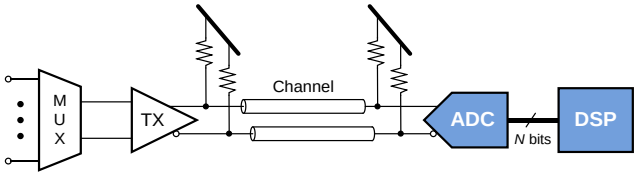

Fig.1. High-speed serial I/O link with an ADC-based receiver.

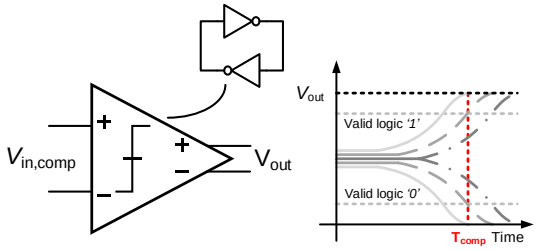

Fig. 2. Comparator evaluation behavior.

II. ADC Metastability Model

ADC metastability happens when a small input makes a comparator's regeneration time longer than the time assigned by design. This excessive regeneration time will cause uncertainty at the comparator output and potential metastability errors at the ADC output. In the proposed model, a metastability event is characterized by an input metastability window (MW) and a metastability error magnitude (ME). The ME is defined as the difference between the ideal and metastable ADC output when the input falls in the corresponding MW.

A. Comparator Model

Dynamic comparator evaluation (Fig. 2) can be modeled as

$$T_{comp} = \tau \ln \frac{V_{FS}}{V_{in}}, \tag{1}$$

where τ is the regeneration time constant, often determined by the gain of an effective cross-coupled inverter stage and the total capacitance, and T_{comp} is the time required to regenerate the input V_{in} to a full logic swing V_{FS}. In order to investigate the impact of metastability in different ADC structures, the following assumptions are made in the ADC models:

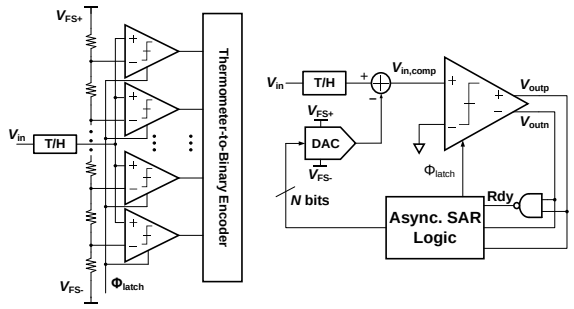

Fig.3. Block diagrams of flash and asynchronous SAR ADCs.

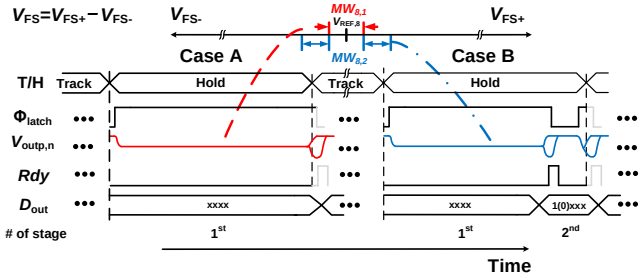

Fig. 4. Two cases for MW characterization in a 4-bit aSAR ADC.

1) Comparators have zero offset.

2) The ADC full scale reference is equal in magnitude to the full logic swing for simplification.

3) Metastable comparator outputs are perceived as either 0's or 1's with 50% probability by the encoder circuit.

B. Flash ADC Model

Flash ADCs (Fig. 3) compare the input simultaneously against every reference level to enable parallel conversion. Assuming the ADC is designed such that only one comparator has the potential for metastability with a given input, this metastable comparator has a 50% chance to give correct output and a 50% chance of a worst-case ±1 LSB ME. The MW is derived from Eq. 1 assuming that all comparators have the entire hold phase, T_{hold}, for regeneration.

$$V_{in,meta} = V_{FS} / \exp\left(\frac{T_{hold}}{\tau}\right)$$
$$ME_i = \begin{cases} 1LSB,\ 50\% \\ 0LSB,\ 50\% \end{cases} \text{or} \begin{cases} -1LSB,\ 50\% \\ 0LSB,\ 50\% \end{cases} \quad (2)$$
$$MW_i = \left(V_{REF,i} - V_{in,meta},\ V_{REF,i} + V_{in,meta}\right)$$

Here the two ME_i subsets correspond to the possible metastability error when V_{in} falls on the negative/positive side of MW_i, the metastability window centered on reference i ($V_{REF,i}$). Both MW_i and ME_i are the same for every reference.

C. Asynchronous SAR ADC Model

Compared with its synchronous counterpart, asynchronous SAR (aSAR) ADCs eliminate the need for a high-speed internal clock and achieve better Figure-of-Merit [2]. However, similar to synchronous SAR ADCs [3], aSAR ADC performance is sensitive to comparator metastability. Fig. 3 shows the block diagram of an N-bit aSAR ADC, with the comparison in the current cycle not triggered until the previous cycle comparison finishes. Thus, a metastable event can cause multiple uncertain bits and a large ME at the ADC output.

In the aSAR model, the hold phase consists of comparator regeneration and DAC settling times, with the comparator reset during DAC settling. The DAC settling time is the same for each stage and assumed to be equal to the comparator regeneration time with 0.5 LSB input. This results in a hold phase time for an N-bit aSAR ADC of

$$T_{hold} \geq T_{total} = \sum_{i=1}^{N} \tau \ln \frac{V_{FS}}{V_{res}[i]} + \sum_{i=1}^{N-1} T_{DAC} \quad (3)$$
$$T_{DAC} = \tau \ln \frac{V_{FS}}{0.5LSB} = \tau \ln 2^{N+1},$$

where T_{total} is the total time an N-stage comparison takes and $V_{res}[i]$ is the residue voltage at comparator input during the i-th comparison stage. Here only N-1 T_{DAC} is included because the first stage DAC settling happens during the track phase. Overall, T_{hold} should be larger than the worst case T_{total}, which is input-dependent. A reasonable estimate for the worst-case input, neglecting metastability, is $V_{FS}/3$ or $2V_{FS}/3$ [2], which yields $T_{hold}=21.72\tau$ for an example 4-bit aSAR ADC. Using this example value to set the ADC speed, metastability windows can be characterized stage by stage throughout all the reference levels.

Fig. 4 shows two cases for first stage metastability characterization. Case A shows when the ADC input is very close to reference 8, such that the first stage comparison is still incomplete at the end of T_{hold}. This metastable event causes an unreliable MSB decision with a 50% error probability and results in no additional bit comparisons. In the proposed model it is assumed that all the unresolved bits following a metastable event are assigned 1 values, corresponding to all of the bit storage elements being reset to 1 at the beginning of each conversion cycle. This assumption leads to some input-polarity dependent asymmetry in the resultant ME.

$$ME_{8,1} = \begin{cases} 8LSB,\ 50\% \\ 0LSB,\ 50\% \end{cases} \text{or} \begin{cases} -1LSB,\ 50\% \\ 7LSB,\ 50\% \end{cases}, \quad (4)$$

where $ME_{8,1}$ denotes the metastability error when metastability occurs around reference level 8 and at the first stage comparison. The MW for this case is

$$V_{in,meta} = V_{FS} / \exp\left(\frac{T_{hold}}{\tau}\right) = 2^4 LSB / \exp\left(\frac{21.72\tau}{\tau}\right) \approx 5.9\times10^{-9} LSB \quad (5)$$
$$MW_{8,1} = \left(V_{REF,8} - 5.9\times10^{-9} LSB,\ V_{REF,8} + 5.9\times10^{-9} LSB\right)$$

Case B is when the first stage comparison finishes before T_{hold} and the MSB is reliable, but the insufficient conversion time left for the second stage comparison results in a metastable event. Following the same method, the ME is

$$ME_{8,2} = \begin{cases} -4LSB,\ 50\% \\ 0LSB,\ 50\% \end{cases} \text{or} \begin{cases} 7LSB,\ 50\% \\ 3LSB,\ 50\% \end{cases}. \quad (6)$$

In order to calculate this MW, the second stage comparison time is calculated and subtracted from T_{total}.

$$t_{2nd} = \tau \ln \frac{V_{FS}}{V_{res}[2]} = \tau \ln \frac{V_{FS}}{V_{FS}/4} = \tau \ln 4 \quad (7)$$

$$V_{in,meta} = V_{FS} / \exp\left(\frac{T_{hold} - T_{DAC} - t_{2nd}}{\tau}\right) = 2^4 / \exp\left(\frac{16.87\tau}{\tau}\right) \approx 7.5\times10^{-7}\,LSB$$
$$MW_{8,2} = \left(V_{REF,8} - 7.5\times10^{-7}\,LSB,\ V_{REF,8} - 5.9\times10^{-9}\,LSB\right) \cup \left(V_{REF,8} + 5.9\times10^{-9}\,LSB,\ V_{REF,8} + 7.5\times10^{-7}\,LSB\right) \quad (8)$$

Note that $MW_{8,1}$ should be excluded from $MW_{8,2}$ in this case because the input inside $MW_{8,1}$ yields a different ME.

All of the MW and ME sets can be characterized following the method introduced above, with Table I showing the characterization of a 4-bit aSAR ADC with T_{hold}=21.72τ. Here the numbers correspond to (MW_i amplitude, negative-side ME_i, positive-side ME_i). Note that the actual MW_i width for a given stage should exclude any sub-MW_i's in previous stages.

TABLE I.
4-BIT ASAR ADC METASTABILITY WINDOW AND ERROR SETS

Ref./Stage	1st	2nd	3rd	4th
1	0	0	0	(3.7E-02, 1/0, -1/0)
2	0	0	(1.3E-04, 2/0, -1/1)	(6.6E-02, -1/0, 1/0)
3	0	0	0	(1.6E-01, 1/0, -1/0)
4	0	(7.5E-07, 4/0, -1/3)	(1.9E-04, -2/0, 3/1)	(9.9E-02, -1/0, 1/0)
5	0	0	0	(2.6E-01, 1/0, -1/0)
6	0	0	(3.9E-04, 2/0, -1/1)	(2.0E-01, -1/0, 1/0)
7	0	0	0	(2.6E-01, 1/0, -1/0)
8	(5.9E-09, 8/0, -1/7)	(7.5E-07, -4/0, 7/3)	(1.9E-04, -2/0, 3/1)	(9.9E-02, -1/0, 1/0)
9	0	0	0	(2.6E-01, 1/0, -1/0)
10	0	0	(3.9E-04, 2/0, -1/1)	(2.0E-01, -1/0, 1/0)
11	0	0	0	(2.6E-01, 1/0, -1/0)
12	0	(7.5E-07, 4/0, -1/3)	(1.9E-04, -2/0, 3/1)	(9.9E-02, -1/0, 1/0)
13	0	0	0	(1.6E-01, 1/0, -1/0)
14	0	0	(1.3E-04, 2/0, -1/1)	(6.6E-02, -1/0, 1/0)
15	0	0	0	(3.7E-02, 1/0, -1/0)

III. METASTABILITY ERROR PROPAGATION IN DIGITAL FFE

Utilizing the MW and ME from the ADC models, the propagation of metastability errors through a digital FFE equalizer is now considered. The ADC metastability table is inserted into a statistical modeling framework [4], where ADC quantization noise is treated as a uniform PDF scaled by the FFE coefficient and convolved with the equalized ISI PDF to obtain the ISI PDF at the FFE output and the final BER curves.

Decomposing the actual ADC output into ME and ADC output without metastability terms results in the following FFE output.

$$\begin{aligned} FFE_{out} &= ADC_{out} * \alpha = \left(ADC_{out,ideal} + ME\right) * \alpha \\ &= ADC_{out,ideal} * \alpha + ME * \alpha \\ &= FFE_{out,ideal} + ME' \end{aligned}, \quad (9)$$

where α is the FFE coefficient matrix. Because the probability of two metastability errors appearing in the FFE chain is extremely low, the presented model assumes that ME contains only 1 non-zero *me* term.

While utilizing the ADC input PDF (Fig. 5) and the MW values allows determination of $ADC_{out,ideal}$ and ME, obtaining an accurate FFE output PDF requires mapping the ADC inputs inside MWs to FFE outputs in order to determine the appropriate starting position for the scaled ME addition. Three different mapping methods are introduced which tradeoff accuracy and computational complexity.

A. Full-bit Mapping

One straight-forward way to map the ADC inputs to FFE outputs is to keep track of the exact bit sequence combinations that makes the ADC inputs fall inside a MW, as shown in Fig. 5. Fundamentally, this method is the same as time-domain simulation. Although it gives an accurate FFE output PDF, the computational expense is extremely high and makes this method impractical.

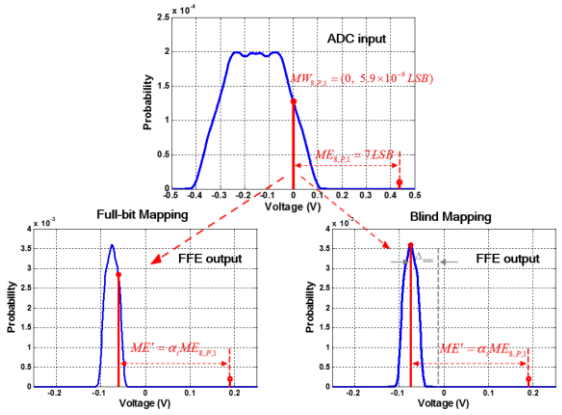

Fig. 5. Model of metastability error propagation from the ADC input, which is 10Gb/s transmission over the Fig. 7 backplane channel, to the digital FFE output: full-bit and blind mapping.

B. Blind Mapping

Another simple method is to map every ADC input inside MWs blindly to the center of the FFE output PDF, such that no bit tracking is required. However, since some ADC inputs should be mapped to the edge instead of the center, this leads to a maximum error of

$$\Delta_{\max} = \sum_{\substack{k=-a \\ k\neq 0}}^{b} \left|ISI_{EQ}(k)\right| \ , \quad (10)$$

where a and b are the relevant pre- and post-cursor ISI tap values of the equalized channel pulse response, ISI_{EQ}.

C. Partial-bit Mapping

A good trade-off between the two aforementioned mapping schemes is to employ partial bit tracking, such that both the error and computation cost is acceptable. In order to reduce the maximum error, the bits that corresponds to the most significant ISI terms in the equalized channel response are tracked.

Fig. 6 gives an example of 2-bit mapping, where the two most significant ISI terms from the equalized channel pulse response are the 1st pre-cursor and the 4th post-cursor. These two bits are tracked and the remaining untracked bits are convolved together to create the partial PDF profiles centered on the four ISI combinations of these two bits. Each MW is checked on the four partial PDFs at the ADC input. In Fig. 6, the positive side of $MW_{8,1}$ is examined at the ADC input and mapped to the [1 -1] ISI combination at the FFE output. The FFE output with metastability can be obtained by shifting the corresponding scaled error ME' from the [1 -1] spike. This results in the following maximum error.

$$\Delta_{\max} = \sum_{\substack{k=-a \\ k\neq 0,B}}^{b} \left|ISI_{EQ}(k)\right|,\ B = \{-1,\ 4\} \quad (11)$$

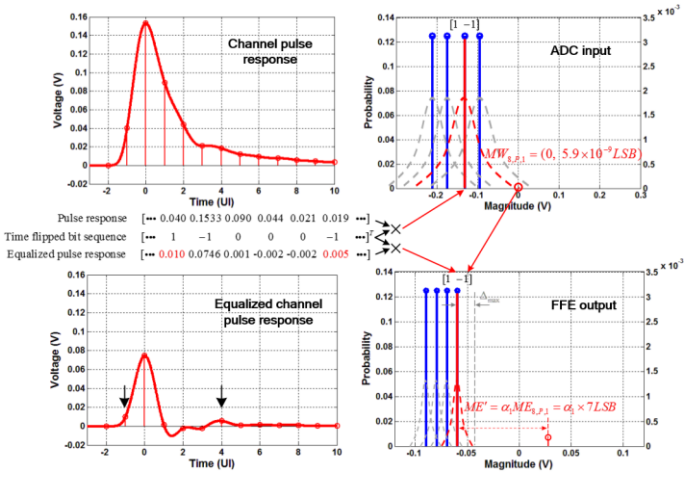

Fig. 6. Partial-bit mapping with two bits tracked.

Note that in the proposed model, only a metastability error occurring at the main FFE tap is considered due to the main tap coefficient α_1 in FFE having the largest value. Verification against transient simulations show that this simplification does not have a major impact when metastability error is limiting the BER performance.

The relationship between maximum error and number of bits tracked is shown in Fig. 7 for 10Gb/s NRZ signaling over a 32" backplane channel and a receiver that consists of a 6-bit ADC and a 3-tap digital FFE. In order to keep the maximum error below 1 LSB, tracking of the six most significant ISI terms is required.

IV. Simulation Results

BER degradation due to metastability is evaluated with the proposed statistical model for 10Gb/s NRZ signaling over a 32" backplane channel (Fig. 7) and receivers that consists of a 6-bit ADC followed by a 3-tap digital FFE. For the 10GS/s aggregate sampling rate ADCs, both a 2-channel time-interleaved (TI) flash and a 32-channel TI aSAR architecture are compared for τ values of 13.2ps and 16.5ps. A 50% duty cycle T/H phase for the flash ADC is assumed, resulting in T_{hold} times of 7.57τ/6.06τ, while for the higher-TI aSAR ADC a 25% duty cycle T/H phase is employed, resulting in T_{hold} times of 45.4τ/36.3τ. Transient simulation models are produced with these assumptions in order to validate the statistical model performance. However, the transient simulations are limited to 10^8 input bits due to the excessive simulation time and lack of computer memory resources.

Fig. 8 compares the relative performance of the two ADC architectures with and without metastability. There is no difference in the ADC models if metastability is not included, and they both yield an 57.4mV eye height for a BER=10-12. For this scenario, the matching of the transient simulation results validates the handling of quantization noise in the statistical modeling framework. Minimal eye height impact is observed with the flash ADC architecture when metastability is included due to the maximum 1LSB ME. However due to the larger ME in the aSAR architecture, the eye is just barely closed at a BER=10^{-12} with τ=13.2ps, with the transient simulations matching the statistical results down to a simulation-limited 10^{-5} BER. Metastability severely limits the

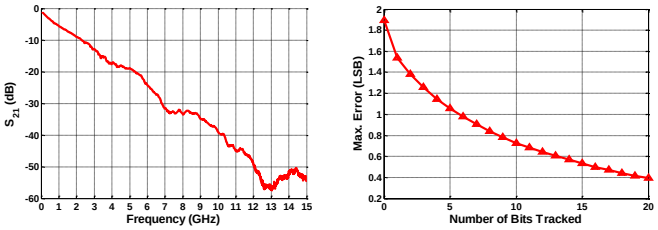

Fig. 7. (a) 32" backplane channels used for model verification. (b) Maximum mapping error v.s. number of bits tracked.

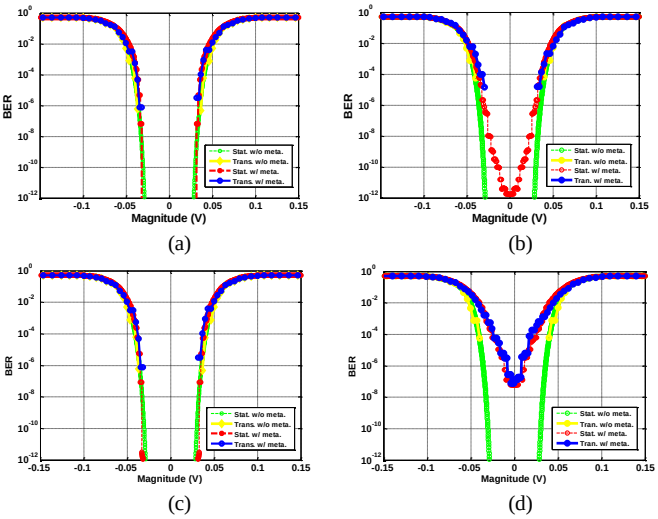

Fig. 8. Transient and statistical simulation BER bathtub curves with τ=13.2ps for (a) flash, (b) aSAR, and τ=16.3ps for (c) flash, (d) aSAR.

aSAR architecture to a BER=10^{-7} when τ is increased to 16.3ps, with good matching between transient and statistical simulations throughout the entire voltage range.

V. Conclusion

This paper presented ADC metastability models for both flash and aSAR ADCs and proposed a partial-bit mapping method to statistically model metastability error propagation through a digital FFE. Simulation results show that the model has good accuracy, with significantly less computational expenses than transient simulation. Overall, the proposed model can serve to guide high-speed link system designers in ADC architecture choice and allow circuit designers to see the receiver-level impact of comparator performance.

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