µA741 General-Purpose Operational Amplifiers

1 Features

- Short-Circuit Protection
- Offset-Voltage Null Capability
- Large Common-Mode and Differential Voltage Ranges
- No Frequency Compensation Required
- No Latch-Up

2 Applications

- DVD Recorders and Players
- Pro Audio Mixers

3 Description

The µA741 device is a general-purpose operational amplifier featuring offset-voltage null capability.

The high common-mode input voltage range and the absence of latch-up make the amplifier ideal for voltage-follower applications. The device is short-circuit protected and the internal frequency compensation ensures stability without external components. A low-value potentiometer may be connected between the offset null inputs to null out the offset voltage as shown in Figure 12.

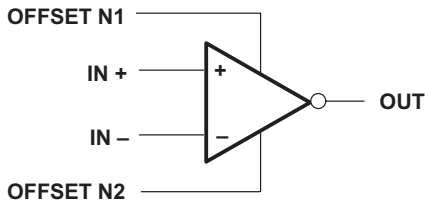
The µA741C device is characterized for operation from 0°C to 70°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
µA741CD	SOIC (8)	4.90 mm × 3.91 mm
µA741CP	PDIP (8)	9.81 mm × 6.35 mm
µA741CPS	SO (8)	6.20 mm × 5.30 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

4 Revision History

Changes from Revision F (May 2017) to Revision G **Page**

- Changed supply voltage unit from "°C" to "V" in *Absolute Maximum Ratings* table ... 5

Changes from Revision E (January 2015) to Revision F **Page**

- Updated data sheet text to the latest documentation and translation standards ... 1
- Deleted text regarding µA741M device (obsolete package) from *Description* section ... 1
- Added µA741CD, µA741CP, and µA741CPS devices to *Device Information* table ... 1
- Deleted µA741x device from *Device Information* table ... 1
- Updated pinout diagrams and *Pin Functions* tables in the *Pin Configurations and Functions* section ... 4
- Deleted µA741M pinout drawings information from *Pin Configurations and Functions* section ... 4
- Deleted Electrical Characteristics: µA741M table from *Specifications* section ... 5
- Added operating junction temperature (T_J) and values to *Absolute Maximum Ratings* table ... 5
- Deleted text regarding µA741M from *Absolute Maximum Ratings* table ... 5
- Deleted text regarding µA741M device from *Recommended Operating Conditions* table ... 5
- Deleted *Dissipation Ratings* table ... 5
- Added *Thermal Information* table and values ... 5
- Deleted µA741M in *Switching Characteristics* table ... 7
- Correct typo in Figure 1 ... 8
- Deleted text regarding µA741M device from *Detailed Description* section ... 10
- Updated text in *Overview* section ... 10
- Added 2017 copyright to *Functional Block Diagram* ... 10
- Added caption to Figure 11 in *Device Functional Modes* section ... 11
- Changed pins 1 and 5 from "NC" to "Offset N1" and "Offset N2" in Figure 18 ... 15

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Changes from Revision D (February 2014) to Revision E **Page**

- Added *Applications*, *Device Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. 1
- Moved *Typical Characteristics* into *Specifications* section. 8

Changes from Revision C (January 2014) to Revision D **Page**

- Fixed *Typical Characteristics* graphs to remove extra lines. 8

Changes from Revision B (September 2000) to Revision C **Page**

- Updated document to new TI data sheet format - no specification changes. 1
- Deleted *Ordering Information* table. 1

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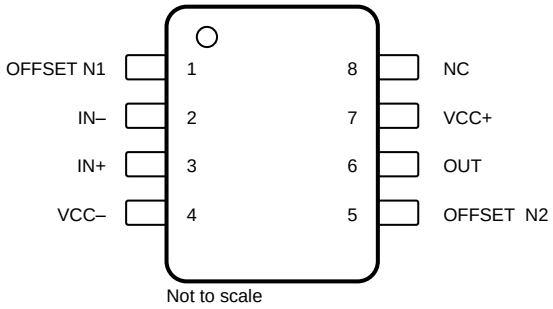
5 Pin Configurations and Functions

uA741C D, P, or PS Package
8-Pin SOIC, PDIP, SO
Top View



Not to scale

NC- no internal connection

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
IN+	3	I	Noninverting input
IN–	2	I	Inverting input
NC	8	—	No internal connection
OFFSET N1	1	I	External input offset voltage adjustment
OFFSET N2	5	I	External input offset voltage adjustment
OUT	6	O	Output
VCC+	7	—	Positive supply
VCC–	4	—	Negative supply

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6 Specifications

6.1 Absolute Maximum Ratings

over virtual junction temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
Supply voltage, V_{CC} (2)	µA741C		–18	18	V
Differential input voltage, V_{ID} (3)	µA741C		–15	15	V
Input voltage, V_I (any input) (2)(4)	µA741C		–15	15	V
Voltage between offset null (either OFFSET N1 or OFFSET N2) and $V_{CC–}$	µA741C		–15	15	V
Duration of output short circuit(5)			Unlimited		
Continuous total power dissipation			See *Thermal Information*		
Case temperature for 60 seconds		µA741C	N/A	N/A	°C
Lead temperature 1.6 mm (1/16 inch) from case for 60 seconds		µA741C	N/A	N/A	°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds	D, P, or PS package	µA741C		260	°C
Operating junction temperature, T_J				150	°C
Storage temperature range, T_{stg}		µA741C	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and $V_{CC–}$.
(3) Differential voltages are at IN+ with respect to IN –.
(4) The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
(5) The output may be shorted to ground or either power supply.

6.2 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC+}	Supply voltage		5	15	V
$V_{CC–}$			–5	–15	
T_A	Operating free-air temperature	µA741C	0	70	°C

6.3 Thermal Information

THERMAL METRIC(1)		µA741			UNIT
		D (SOIC)	P (PDIP)	PS (SO)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	129.2	87.4	119.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	73.6	89.3	66	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	72.4	64.4	70	°C/W
ψ_{JT}	Junction-to-top characterization parameter	25.9	49.8	27.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	71.7	64.1	69	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.4 Electrical Characteristics: µA741C

at specified virtual junction temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_O = 0	25°C		1	6	mV
			Full range			7.5	
$\Delta V_{IO(adj)}$	Offset voltage adjust range	V_O = 0	25°C		±15		mV
I_{IO}	Input offset current	V_O = 0	25°C		20	200	nA
			Full range			300	
I_{IB}	Input bias current	V_O = 0	25°C		80	500	nA
			Full range			800	
V_{ICR}	Common-mode input voltage range	25°C		±12	±13		V
		Full range		±12			
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ	25°C	±12	±14		V
		R_L ≥ 10 kΩ	Full range	±12			
		R_L = 2 kΩ	25°C	±10			
		R_L ≥ 2 kΩ	Full range	±10			
A_{VD}	Large-signal differential voltage amplification	R_L ≥ 2 kΩ	25°C	20	200		V/mV
		V_O = ±10 V	Full range	15			
r_i	Input resistance	25°C		0.3	2		MΩ
r_o	Output resistance	V_O = 0; see[2]	25°C		75		Ω
C_i	Input capacitance	25°C			1.4		pF
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICRmin}	25°C	70	90		dB
			Full range	70			
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	V_{CC} = ±9 V to ±15 V	25°C		30	150	µV/V
			Full range			150	
I_{OS}	Short-circuit output current	25°C			±25	±40	mA
I_{CC}	Supply current	V_O = 0; no load	25°C		1.7	2.8	mA
			Full range			3.3	
P_D	Total power dissipation	V_O = 0; no load	25°C		50	85	mW
			Full range			100	

(1) All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range for the µA741C is 0°C to 70°C.
(2) This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

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6.5 Electrical Characteristics: µA741Y

at specified virtual junction temperature, $V_{CC\pm}$ = ±15 V, T_A = 25°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS (2)	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_O = 0		1	5	mV
$\Delta V_{IO(adj)}$	Offset voltage adjust range	V_O = 0		±15		mV
I_{IO}	Input offset current	V_O = 0		20	200	nA
I_{IB}	Input bias current	V_O = 0		80	500	nA
V_{ICR}	Common-mode input voltage range		±12	±13		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ	±12	±14		V
		R_L = 2 kΩ	±10	±13		
A_{VD}	Large-signal differential voltage amplification	R_L ≥ 2 kΩ	20	200		V/mV
r_i	Input resistance		0.3	2		MΩ
r_o	Output resistance	V_O = 0; see(1)		75		Ω
C_i	Input capacitance			1.4		pF
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICRmin}	70	90		dB
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	V_{CC} = ±9 V to ±15 V		30	150	µV/V
I_{OS}	Short-circuit output current			±25	±40	mA
I_{CC}	Supply current	V_O = 0; no load		1.7	2.8	mA
P_D	Total power dissipation	V_O = 0; no load		50	85	mW

(1) This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.
(2) All characteristics are measured under open-loop conditions with zero common-mode voltage unless otherwise specified.

6.6 Switching Characteristics: µA741C

over operating free-air temperature range, $V_{CC\pm}$ = ±15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Rise time	V_I = 20 mV, R_L = 2 kΩ C_L = 100 pF; see Figure 1		0.3		µs
	Overshoot factor			5%		
SR	Slew rate at unity gain	V_I = 10 V, R_L = 2 kΩ C_L = 100 pF; see Figure 1		0.5		V/µs

6.7 Switching Characteristics: µA741Y

over operating free-air temperature range, $V_{CC\pm}$ = ±15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Rise time	V_I = 20 mV, R_L = 2 kΩ C_L = 100 pF; see Figure 1		0.3		µs
	Overshoot factor			5%		
SR	Slew rate at unity gain	V_I = 10 V, R_L = 2 kΩ C_L = 100 pF; see Figure 1		0.5		V/µs

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6.8 Typical Characteristics

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

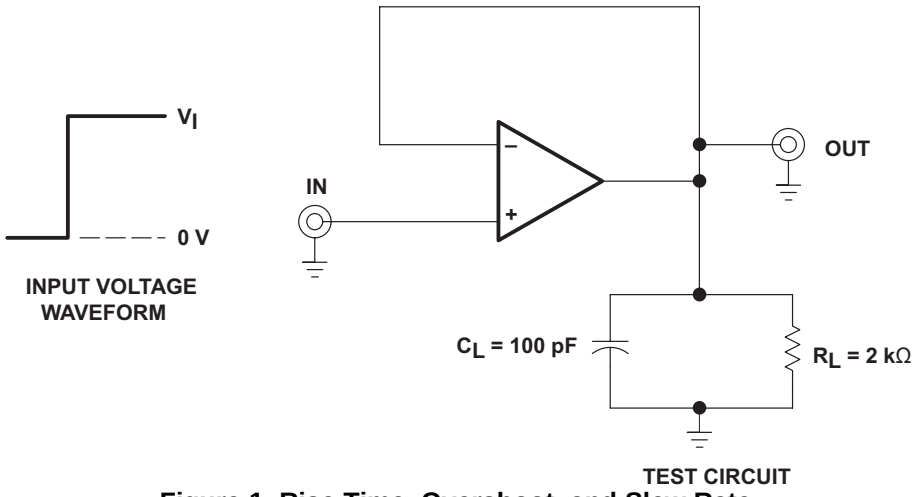

Figure 1. Rise Time, Overshoot, and Slew Rate

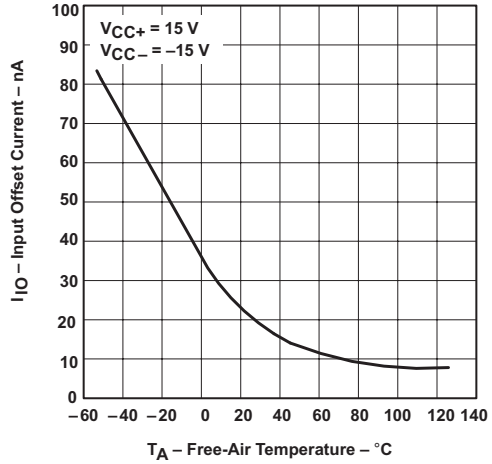

Figure 2. Input Offset Current vs Free-Air Temperature

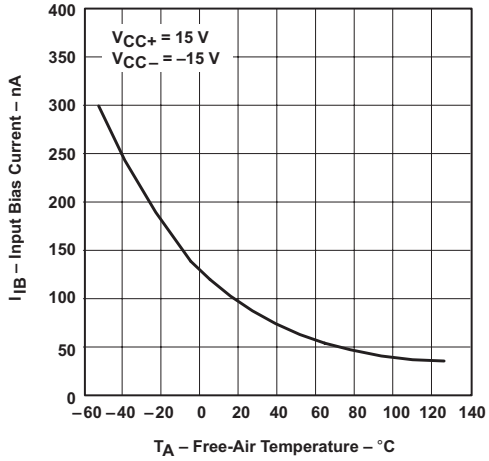

Figure 3. Input Bias Current vs Free-Air Temperature

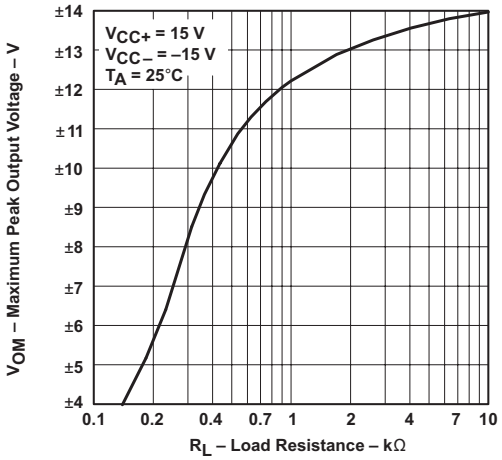

Figure 4. Maximum Output Voltage vs Load Resistance

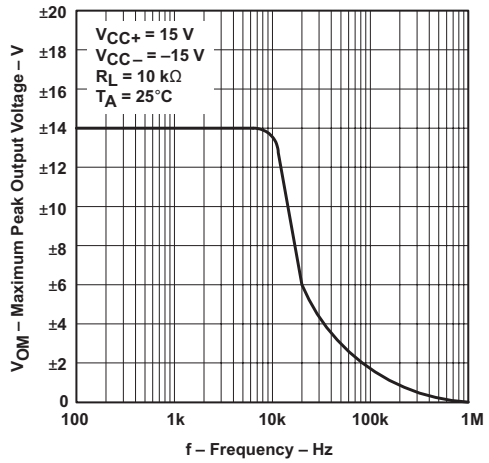

Figure 5. Maximum Peak Output Voltage vs Frequency

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Typical Characteristics (continued)

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

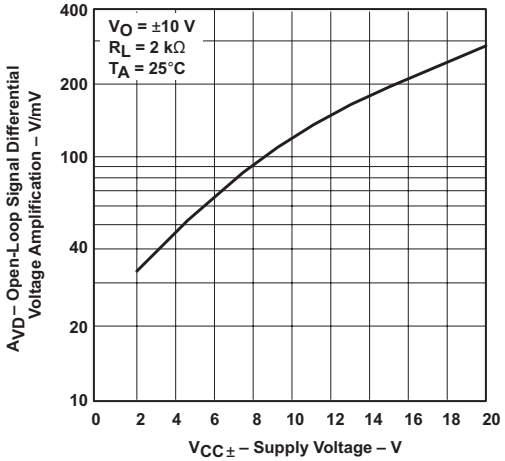


Figure 6. Open-Loop Signal Differential Voltage Amplification vs Supply Voltage

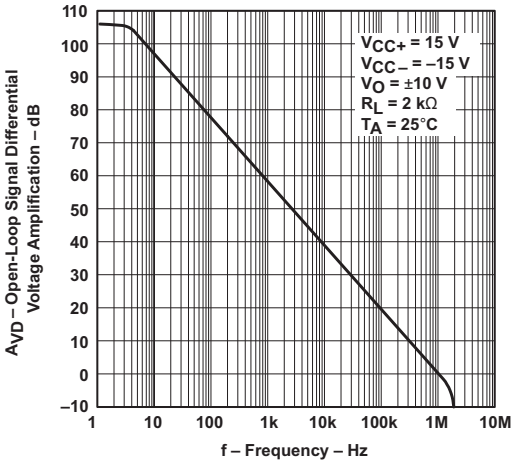


Figure 7. Open-Loop Large-Signal Differential Voltage Amplification vs Frequency

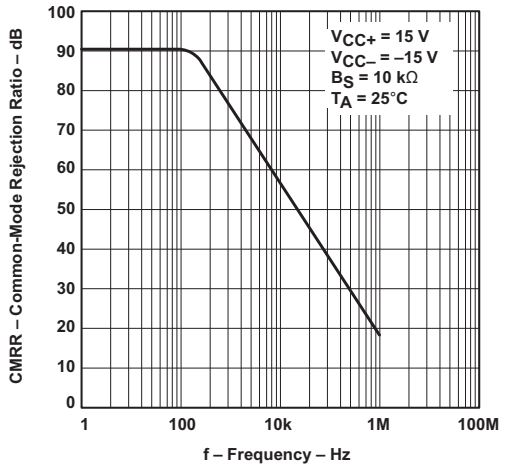


Figure 8. Common-Mode Rejection Ratio vs Frequency

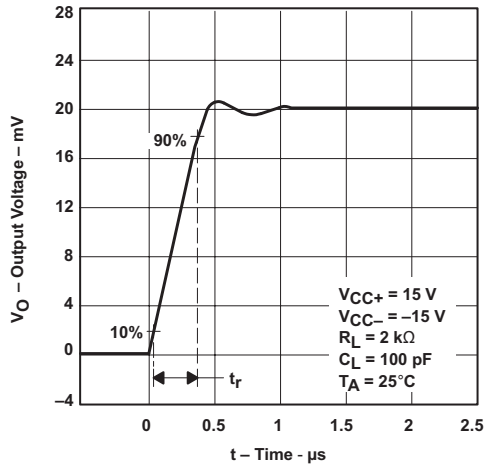


Figure 9. Output Voltage vs Elapsed Time

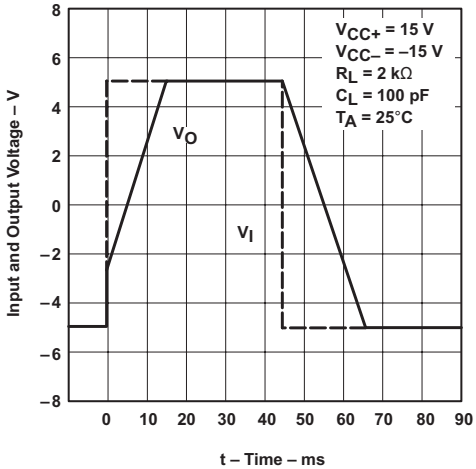


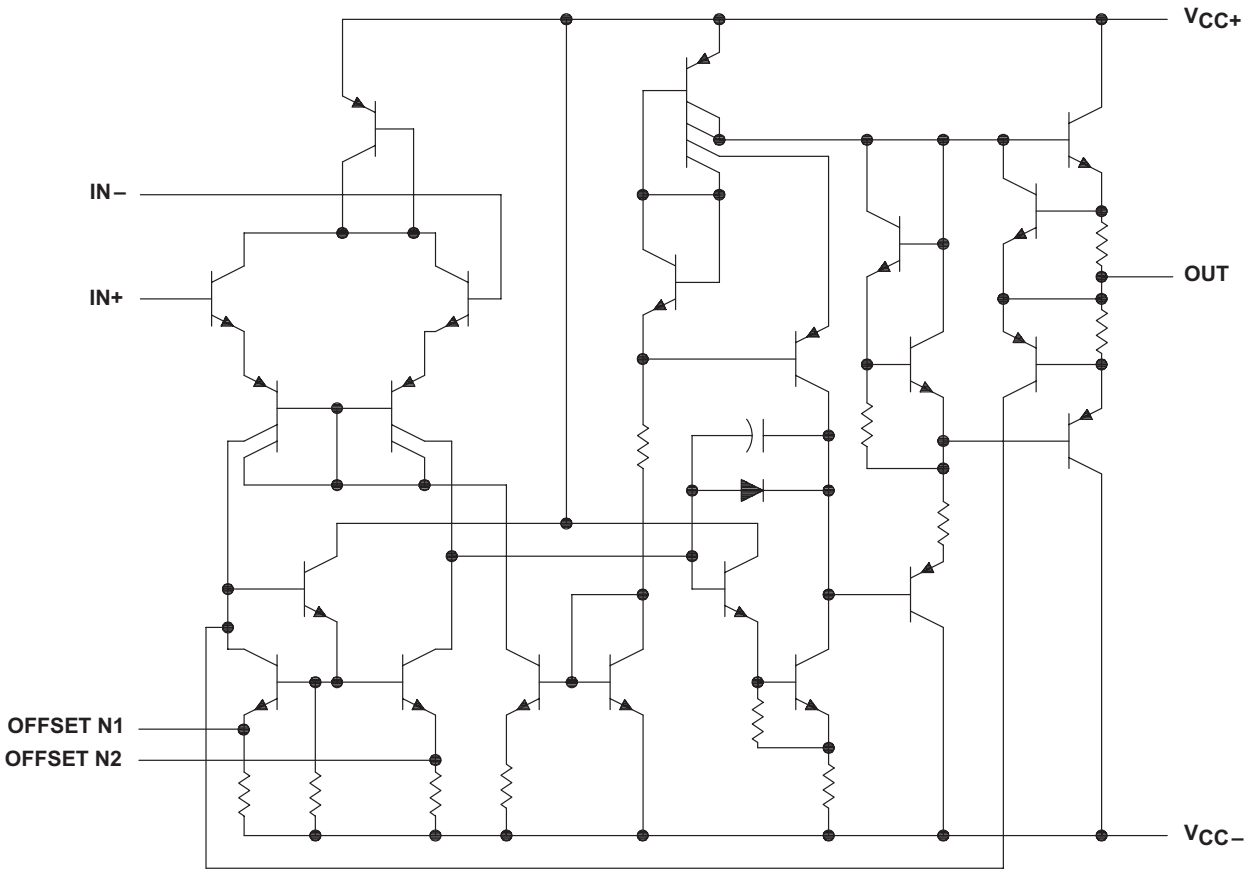
Figure 10. Voltage-Follower Large-Signal Pulse Response

7 Detailed Description

7.1 Overview

The μA741 has been a popular operational amplifier for over four decades. Typical open loop gain is 106 dB while driving a 2000-Ω load. Short circuit tolerance, offset voltage trimming, and unity-gain stability makes the μA741 useful for many applications.

7.2 Functional Block Diagram



Component Count	
Transistors	22
Resistors	11
Diode	1
Capacitor	1

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7.3 Feature Description

7.3.1 Offset-Voltage Null Capability

The input offset voltage of operational amplifiers (op amps) arises from unavoidable mismatches in the differential input stage of the op-amp circuit caused by mismatched transistor pairs, collector currents, current-gain betas (β), collector or emitter resistors and so forth. The input offset pins allow the designer to adjust for mismatches caused by external circuitry. See *Application and Implementation* for more details on design techniques.

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Feature Description (continued)

7.3.2 Slew Rate

The slew rate is the rate at which an operational amplifier can change an output when there is a change on the input. The µA741 device has a 0.5-V/µs slew rate. Parameters that vary significantly with operating voltages or temperature are shown in *Typical Characteristics*.

7.4 Device Functional Modes

The µA741 device is powered on when the power supply is connected. The device can operate as a single-supply or dual-supply operational amplifier depending on the application.

7.5 µA741Y Chip Information

When properly assembled, this chip displays characteristics similar to the µA741C device. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips can be mounted with conductive epoxy or a gold-silicon preform.

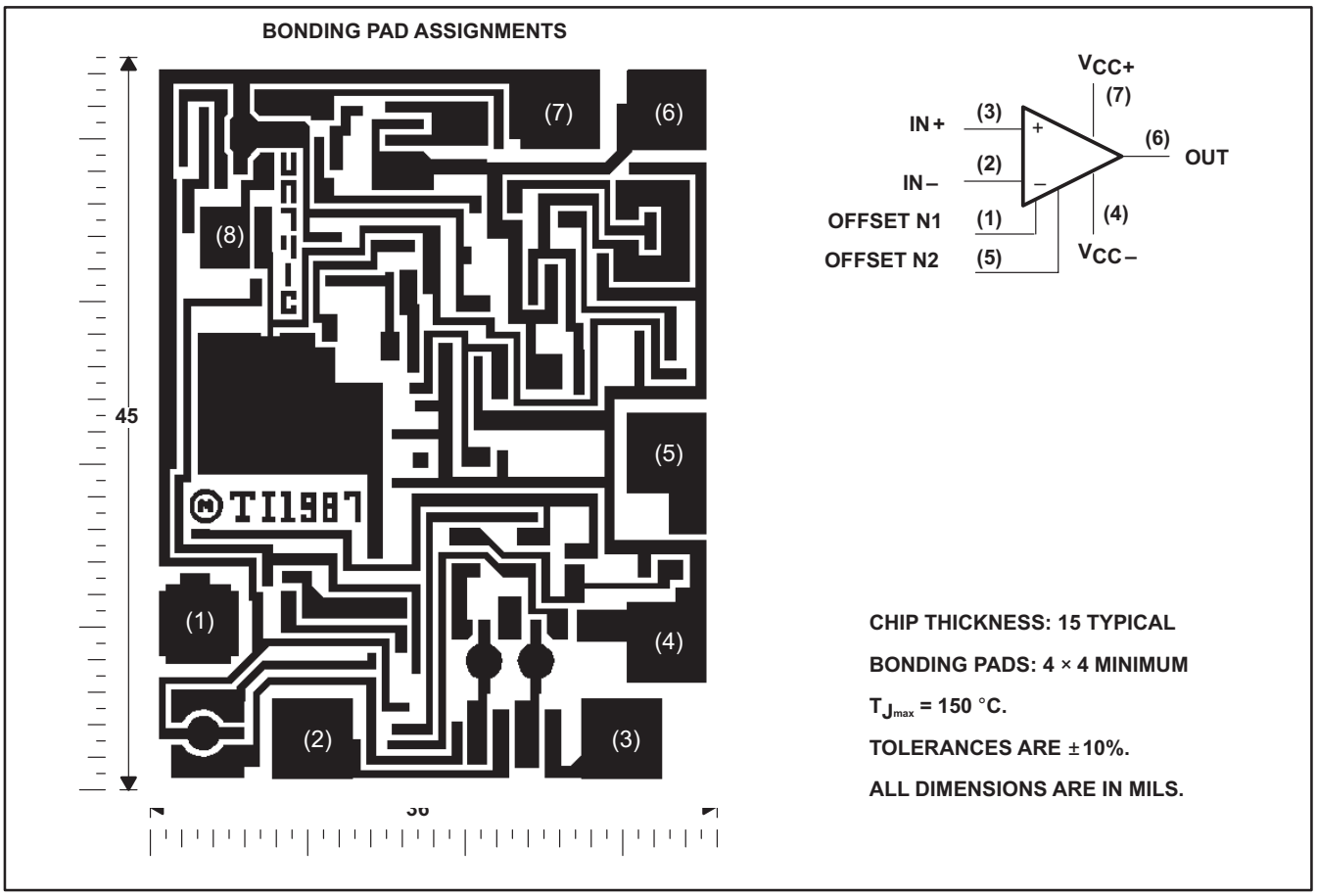

Figure 11. Bonding Pad Assignments

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The input offset voltage of operational amplifiers (op amps) arises from unavoidable mismatches in the differential input stage of the op-amp circuit caused by mismatched transistor pairs, collector currents, current-gain betas (β), collector or emitter resistors and so forth. The input offset pins allow the designer to adjust for mismatches resulting from external circuitry. These input mismatches can be adjusted by placing resistors or a potentiometer between the inputs as shown in Figure 12. A potentiometer can fine-tune the circuit during testing or for applications which require precision offset control. For more information about designing using the input-offset pins, see *Nulling Input Offset Voltage of Operational Amplifiers*.

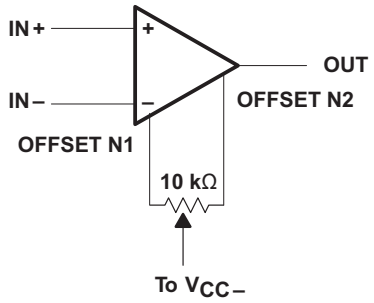

Figure 12. Input Offset Voltage Null Circuit

8.2 Typical Application

The voltage follower configuration of the operational amplifier is used for applications where a weak signal drives a relatively high current load. This circuit is also called a buffer amplifier or unity-gain amplifier. The inputs of an operational amplifier have a very high resistance which puts a negligible current load on the voltage source. The output resistance of the operational amplifier is almost negligible, so the resistance can provide as much current as necessary to the output load.

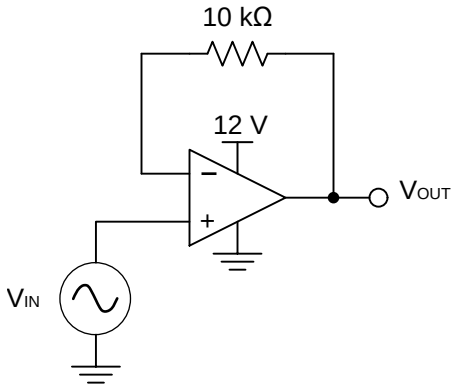

Figure 13. Voltage Follower Schematic

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Typical Application (continued)

8.2.1 Design Requirements

- Output range from 2 V to 11.5 V
- Input range from 2 V to 11.5 V
- Resistive feedback to negative input

8.2.2 Detailed Design Procedure

8.2.2.1 Output Voltage Swing

The output voltage of an operational amplifier is limited by the internal circuitry to some level below the supply rails. For this amplifier, the output voltage swing is within ±12 V, which accommodates the input and output voltage requirements.

8.2.2.2 Supply and Input Voltage

For correct operation of the amplifier, neither input must be higher than the recommended positive supply rail voltage or lower than the recommended negative supply rail voltage. The selected amplifier must be able to operate at the supply voltage that accommodates the inputs. Because the input for this application goes up to 11.5 V, the supply voltage must be 12 V. Using a negative voltage on the lower rail rather than ground allows the amplifier to maintain linearity for inputs below 2 V.

8.2.3 Application Curves for Output Characteristics

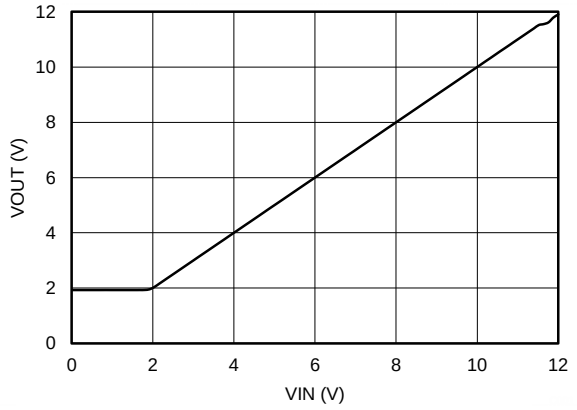

Figure 14. Output Voltage vs Input Voltage

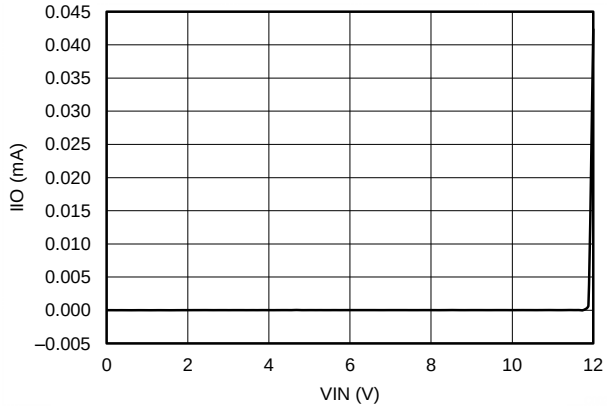

Figure 15. Current Drawn Input of Voltage Follower (I_{IO}) vs Input Voltage

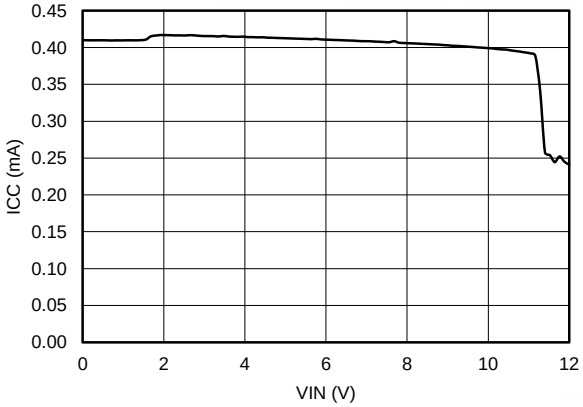

Figure 16. Current Drawn from Supply (I_{CC}) vs Input Voltage

9 Power Supply Recommendations

The μA741 device is specified for operation from ±5 to ±15 V; many specifications apply from 0°C to 70°C. *Typical Characteristics* presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

Place 0.1-μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies. For more detailed information on bypass capacitor placement, see *Layout Guidelines*.

CAUTION

Supply voltages larger than ±18 V can permanently damage the device (see *Absolute Maximum Ratings*).

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the operational amplifier. Bypass capacitors reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-μF ceramic bypass capacitors between each supply pin and ground, placed as close as possible to the device. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, see *Circuit Board Layout Techniques*.
- To reduce parasitic coupling, run the input traces as far away as possible from the supply or output traces. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close as possible to the device. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in *Layout Example*.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

10.2 Layout Example

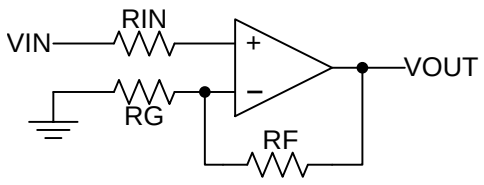

Figure 17. Operational Amplifier Schematic for Noninverting Configuration

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Layout Example (continued)

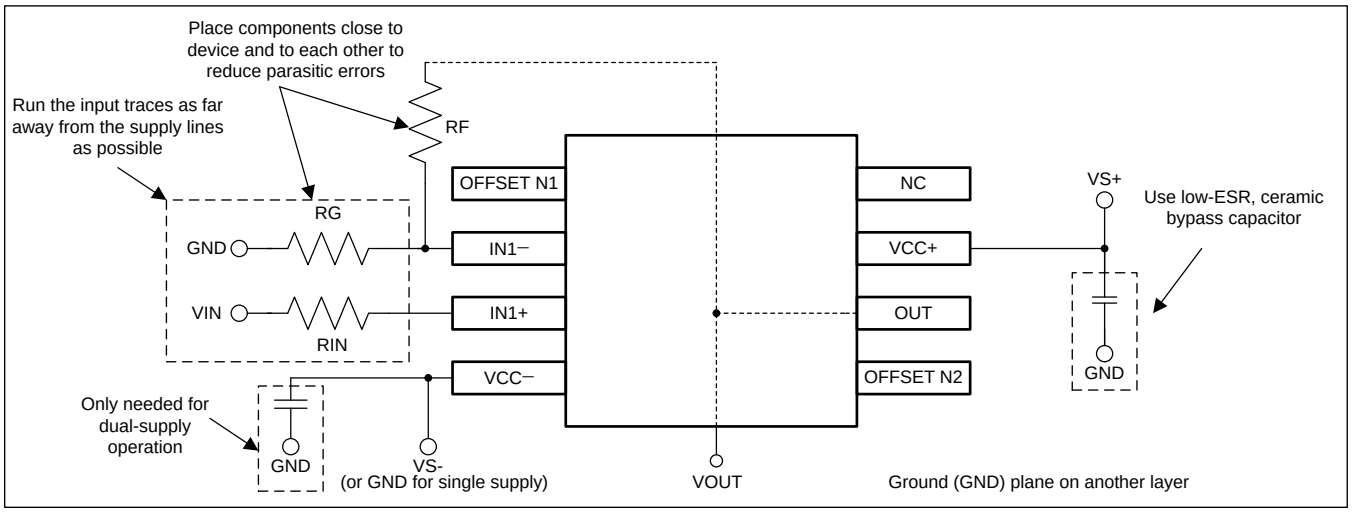

Figure 18. Operational Amplifier Board Layout for Noninverting Configuration

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Trademarks

All trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UA741CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UA741C	Samples
UA741CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UA741C	Samples
UA741CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UA741C	Samples
UA741CP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UA741CP	Samples
UA741CPE4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UA741CP	Samples
UA741CPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	U741	Samples
UA741CPSRE4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	U741	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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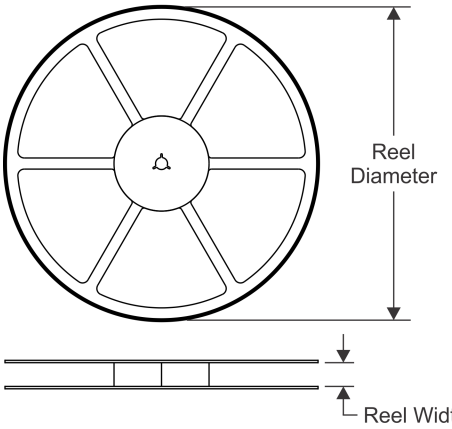
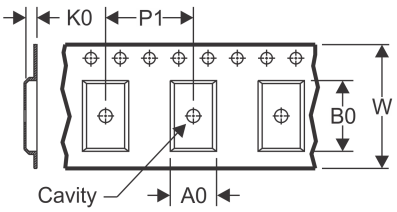
TAPE AND REEL INFORMATION

REEL DIMENSIONS

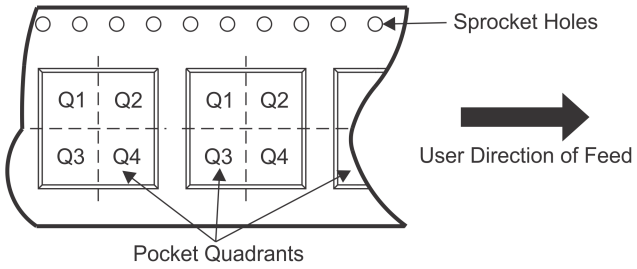


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

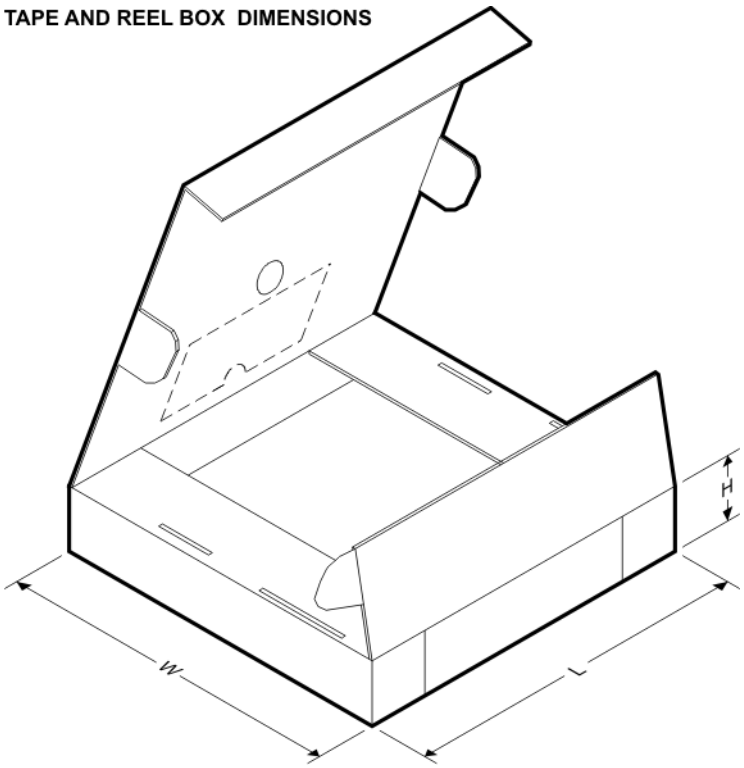
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UA741CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

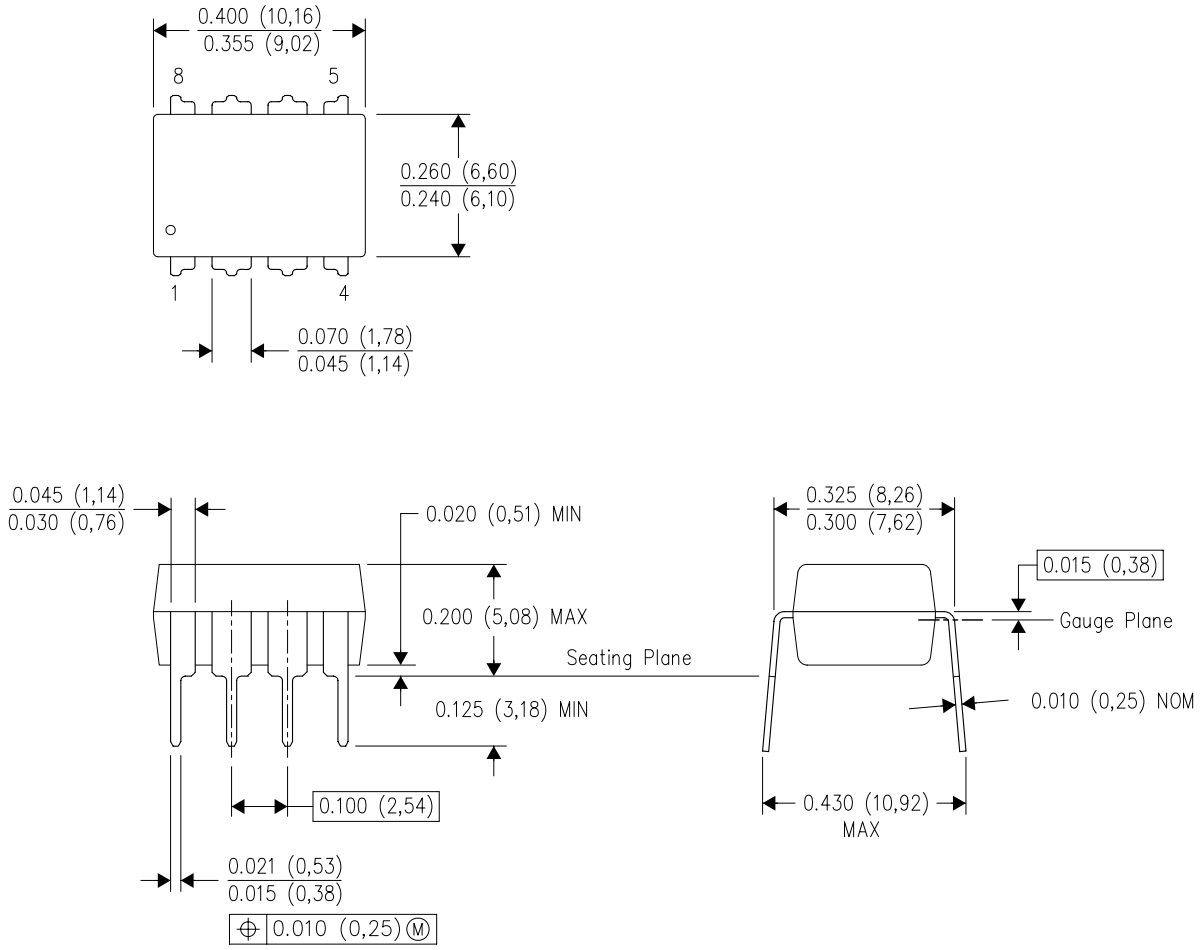
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

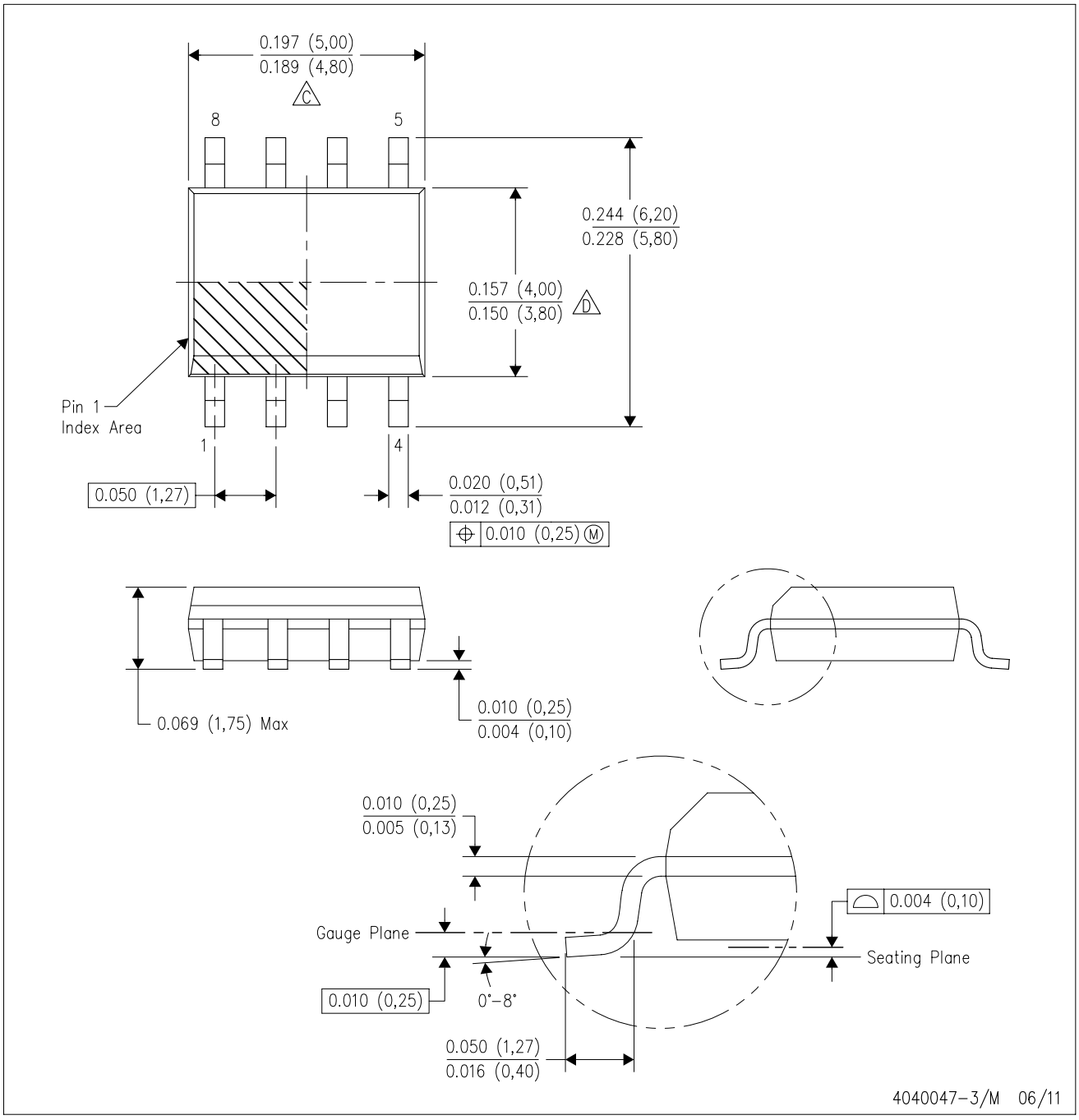
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UA741CDR	SOIC	D	8	2500	340.5	338.1	20.6

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



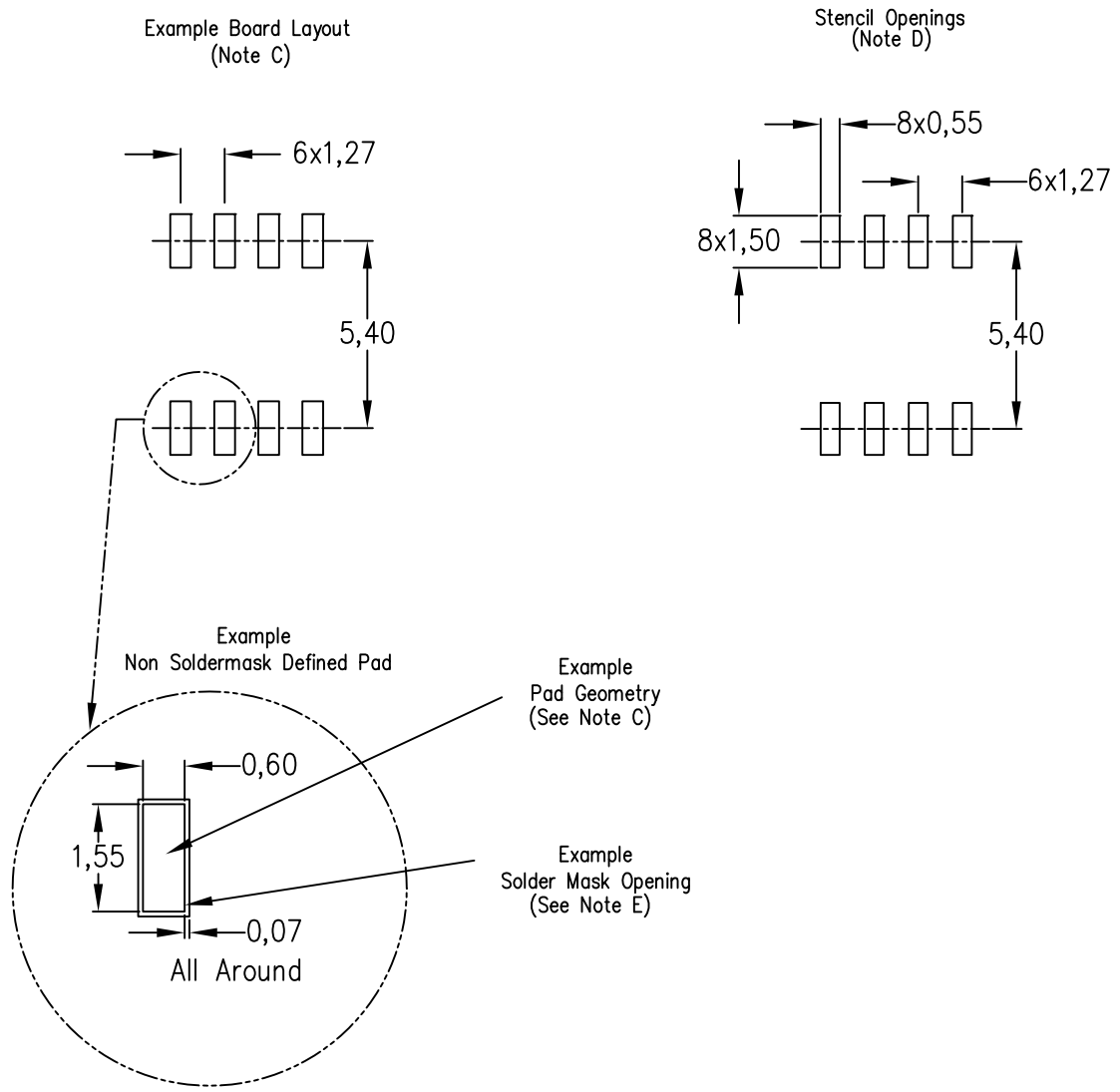
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

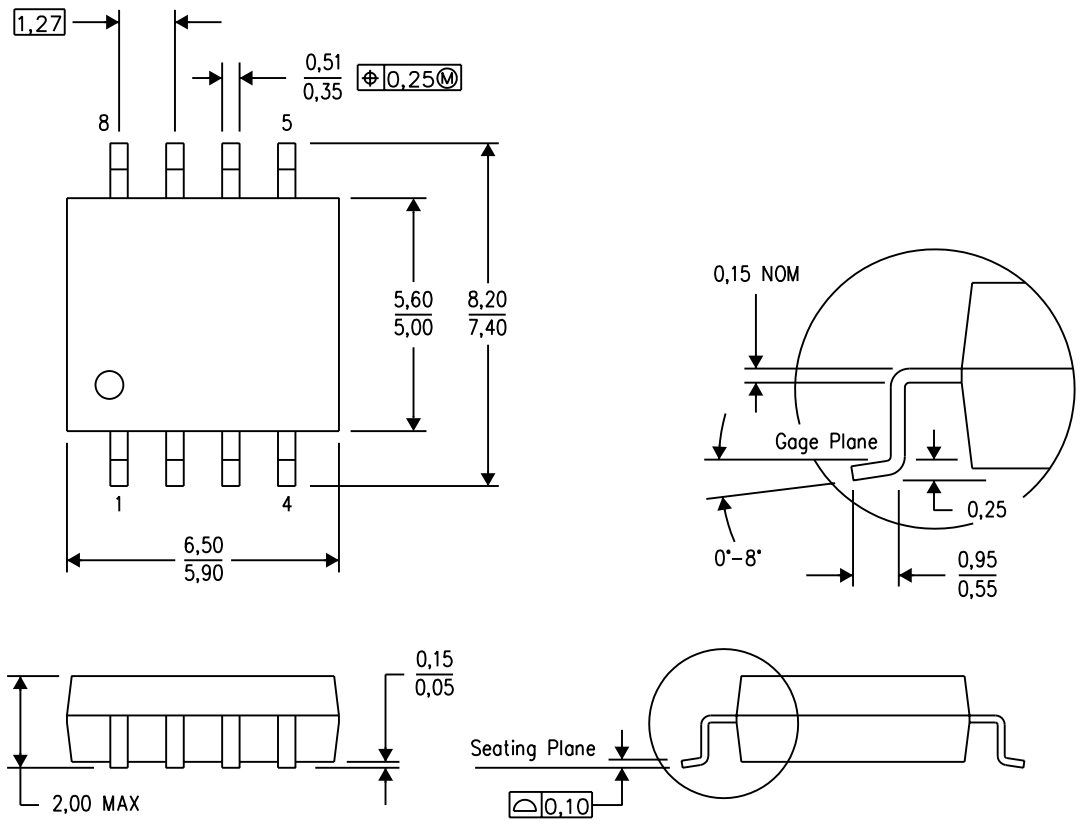
D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

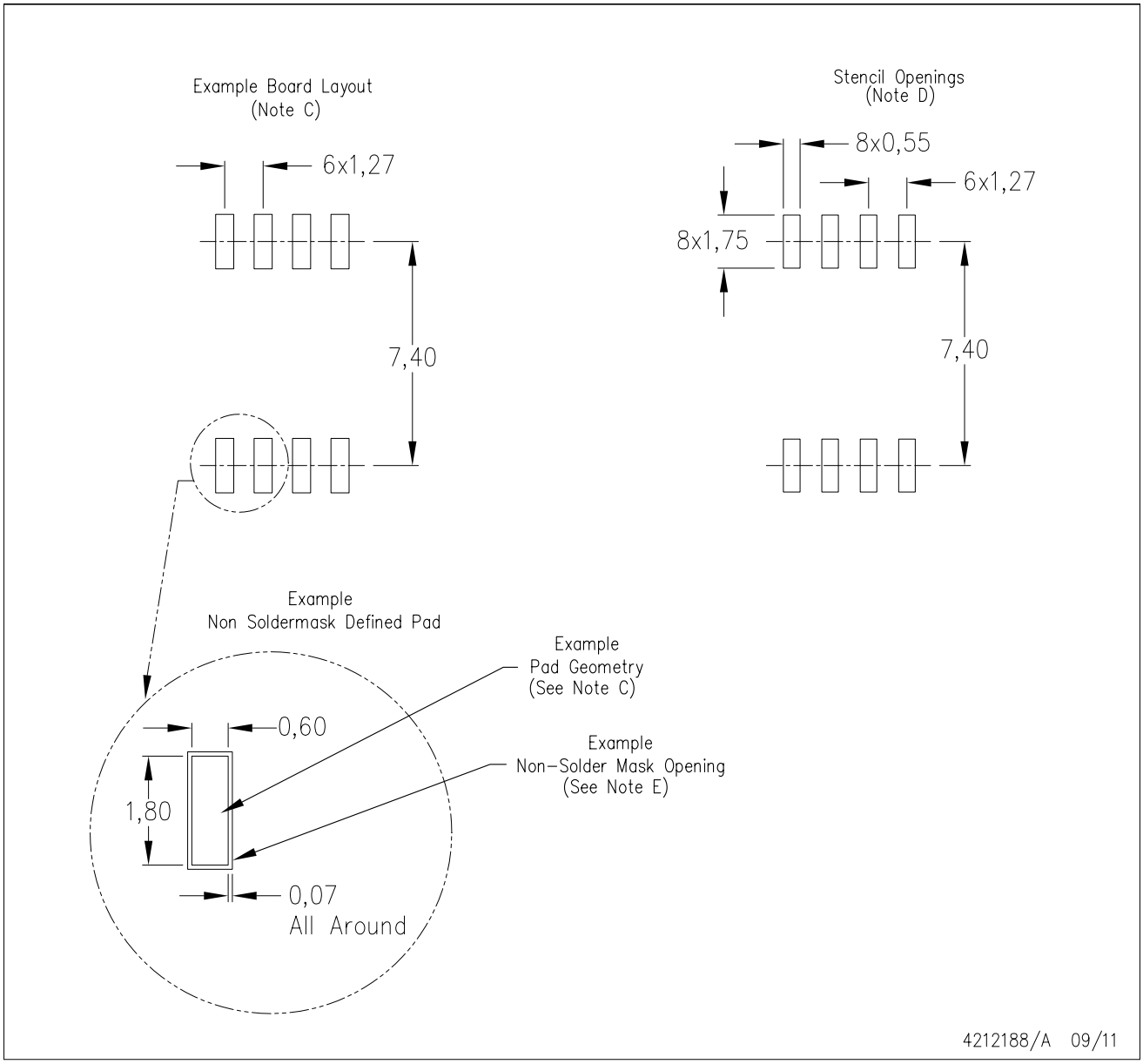
PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



4040063/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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National Semiconductor

December 2001

LF155/LF156/LF256/LF257/LF355/LF356/LF357 JFET Input Operational Amplifiers

General Description

These are the first monolithic JFET input operational amplifiers to incorporate well matched, high voltage JFETs on the same chip with standard bipolar transistors (BI-FET™ Technology). These amplifiers feature low input bias and offset currents/low offset voltage and offset voltage drift, coupled with offset adjust which does not degrade drift or common-mode rejection. The devices are also designed for high slew rate, wide bandwidth, extremely fast settling time, low voltage and current noise and a low 1/f noise corner.

Features

Advantages

- Replace expensive hybrid and module FET op amps
- Rugged JFETs allow blow-out free handling compared with MOSFET input devices
- Excellent for low noise applications using either high or low source impedance — very low 1/f corner
- Offset adjust does not degrade drift or common-mode rejection as in most monolithic amplifiers
- New output stage allows use of large capacitive loads (5,000 pF) without stability problems
- Internal compensation and large differential input voltage capability

Applications

- Precision high speed integrators
- Fast D/A and A/D converters
- High impedance buffers
- Wideband, low noise, low drift amplifiers
- Logarithmic amplifiers
- Photocell amplifiers
- Sample and Hold circuits

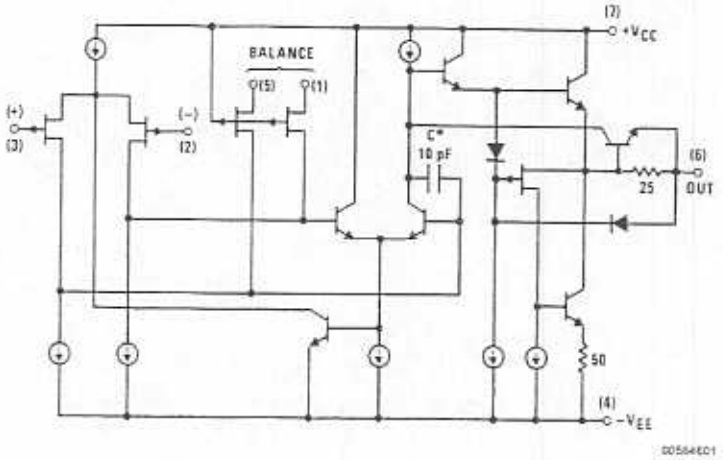
Common Features

- Low input bias current: 30pA
- Low Input Offset Current: 3pA
- High input impedance: $10^{12}\Omega$
- Low input noise current: $0.01\ pA/\sqrt{Hz}$
- High common-mode rejection ratio: 100 dB
- Large dc voltage gain: 106 dB

Uncommon Features

	LF155/ LF355	LF156/ LF256/ LF356	LF257/ LF357 (A_V=5)	Units
■ Extremely fast settling time to 0.01%	4	1.5	1.5	µs
■ Fast slew rate	5	12	50	V/µs
■ Wide gain bandwidth	2.5	5	20	MHz
■ Low input noise voltage	20	12	12	$nV/\sqrt{Hz}$

Simplified Schematic



*3pF in LF357 series

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

	LF155/6	LF256/7/LF356B	LF355/6/7
Supply Voltage	±22V	±22V	±18V
Differential Input Voltage	±40V	±40V	±30V
Input Voltage Range (Note 2)	±20V	±20V	±16V
Output Short Circuit Duration	Continuous	Continuous	Continuous
T_{JMAX}			
H-Package	150°C	115°C	115°C
N-Package		100°C	100°C
M-Package		100°C	100°C
Power Dissipation at T_A = 25°C (Notes 1, 8)			
H-Package (Still Air)	560 mW	400 mW	400 mW
H-Package (400 LF/Min Air Flow)	1200 mW	1000 mW	1000 mW
N-Package		670 mW	670 mW
M-Package		380 mW	380 mW
Thermal Resistance (Typical) θ_{JA}			
H-Package (Still Air)	160°C/W	160°C/W	160°C/W
H-Package (400 LF/Min Air Flow)	65°C/W	65°C/W	65°C/W
N-Package		130°C/W	130°C/W
M-Package		195°C/W	195°C/W
(Typical) θ_{JC}			
H-Package	23°C/W	23°C/W	23°C/W
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Soldering Information (Lead Temp.)			
Metal Can Package			
Soldering (10 sec.)	300°C	300°C	300°C
Dual-In-Line Package			
Soldering (10 sec.)	260°C	260°C	260°C
Small Outline Package			
Vapor Phase (60 sec.)		215°C	215°C
Infrared (15 sec.)		220°C	220°C
See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.			
ESD tolerance			
(100 pF discharged through 1.5kΩ)	1000V	1000V	1000V

DC Electrical Characteristics

(Note 3)

Symbol	Parameter	Conditions	LF155/6			LF256/7 LF356B			LF355/6/7			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	R_S=50Ω, T_A=25°C		3	5		3	5		3	10	mV
		Over Temperature			7			6.5			13	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	R_S=50Ω		5			5			5		µV/°C
$\Delta TC/\Delta V_{OS}$	Change in Average TC with V_{OS} Adjust	R_S=50Ω, (Note 4)		0.5			0.5			0.5		µV/°C per mV
I_{OS}	Input Offset Current	T_J=25°C, (Notes 3, 5)		3	20		3	20		3	50	pA
		$T_J \leq T_{HIGH}$			20			1			2	nA

DC Electrical Characteristics (Continued)

(Note 3)

Symbol	Parameter	Conditions	LF155/6			LF256/7 LF356B			LF355/6/7			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_B	Input Bias Current	T_J=25°C, (Notes 3, 5)		30	100		30	100		30	200	pA
		$T_J \leq T_{HIGH}$			50			5			8	nA
R_{IN}	Input Resistance	T_J=25°C		10^{12}			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	V_S=±15V, T_A=25°C	50	200		50	200		25	200		V/mV
		V_O=±10V, R_L=2k										
		Over Temperature	25			25			15			V/mV
V_O	Output Voltage Swing	V_S=±15V, R_L=10k	±12	±13		±12	±13		±12	±13		V
		V_S=±15V, R_L=2k	±10	±12		±10	±12		±10	±12		V
V_{CM}	Input Common-Mode Voltage Range	V_S=±15V	±11	+15.1 −12		±11	±15.1 −12		+10	+15.1 −12		V V
CMRR	Common-Mode Rejection Ratio		85	100		85	100		80	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 6)	85	100		85	100		80	100		dB

DC Electrical Characteristics

$T_A = T_J = 25°C$, $V_S = ±15V$

Parameter	LF155		LF355		LF156/256/257/356B		LF356		LF357		Units
	Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	Max	
Supply Current	2	4	2	4	5	7	5	10	5	10	mA

AC Electrical Characteristics

$T_A = T_J = 25°C$, $V_S = ±15V$

Symbol	Parameter	Conditions	LF155/355	LF156/256/356B	LF156/256/356/LF356B	LF257/357	Units
			Typ	Min	Typ	Typ	
SR	Slew Rate	LF155/6: A_V=1,	5	7.5	12		V/µs
		LF357: A_V=5				50	V/µs
GBW	Gain Bandwidth Product		2.5		5	20	MHz
t_s	Settling Time to 0.01%	(Note 7)	4		1.5	1.5	µs
e_n	Equivalent Input Noise Voltage	R_S=100Ω					
		f=100 Hz	25		15	15	$nV/\sqrt{Hz}$
		f=1000 Hz	20		12	12	$nV/\sqrt{Hz}$
i_n	Equivalent Input Current Noise	f=100 Hz	0.01		0.01	0.01	$pA/\sqrt{Hz}$
		f=1000 Hz	0.01		0.01	0.01	$pA/\sqrt{Hz}$
C_{IN}	Input Capacitance		3		3	3	pF

Notes for Electrical Characteristics

Note 1: The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum available power dissipation at any temperature is $P_D=(T_{JMAX}-T_A)/\theta_{JA}$ or the 25°C P_{DMAX}, whichever is less.

Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 3: Unless otherwise stated, these test conditions apply:

Notes for Electrical Characteristics (Continued)

	LF155/156	LF256/257	LF356B	LF355/6/7
Supply Voltage, V_S	$\pm 15V \le V_S \le \pm 20V$	$\pm 15V \le V_S \le \pm 20V$	$\pm 15V \le V_S \pm 20V$	$V_S = \pm 15V$
T_A	$-55°C \le T_A \le +125°C$	$-25°C \le T_A \le +85°C$	$0°C \le T_A \le +70°C$	$0°C \le T_A \le +70°C$
T_{HIGH}	+125°C	+85°C	+70°C	+70°C

and V_{OS}. I_B and I_{OS} are measured at $V_{CM} = 0$.

Note 4: The Temperature Coefficient of the adjusted input offset voltage changes only a small amount (0.5μV/°C typically) for each mV of adjustment from its original unadjusted value. Common-mode rejection and open loop voltage gain are also unaffected by offset adjustment.

Note 5: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, Pd. $T_J = T_A + \theta_{JA}$ Pd where θ_{JA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

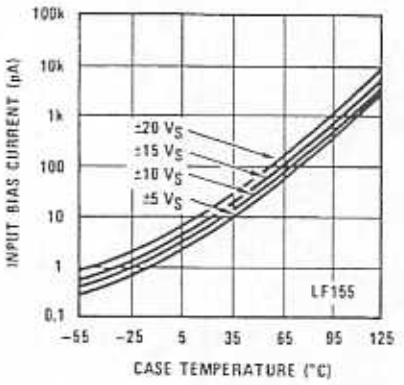
Note 6: Supply Voltage Rejection is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

Note 7: Settling time is defined here, for a unity gain inverter connection using 2 kΩ resistors for the LF155/6. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10V step input is applied to the inverter. For the LF357, $A_V = -5$, the feedback resistor from output to input is 2kΩ and the output step is 10V (See Settling Time Test Circuit).

Note 8: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

Typical DC Performance Characteristics Curves are for LF155 and LF156 unless otherwise specified.

Input Bias Current



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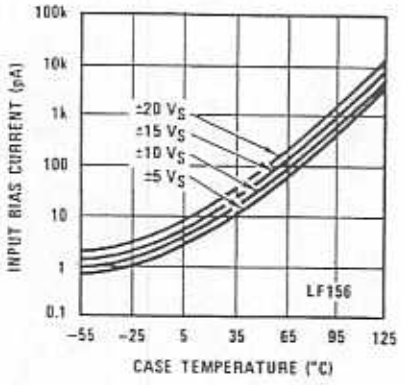
Input Bias Current



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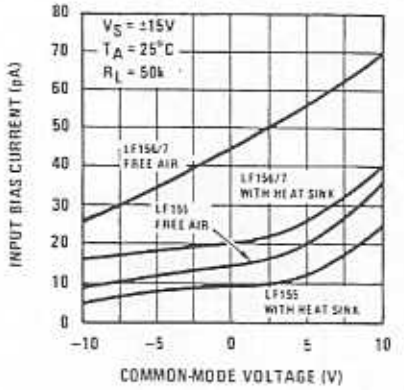
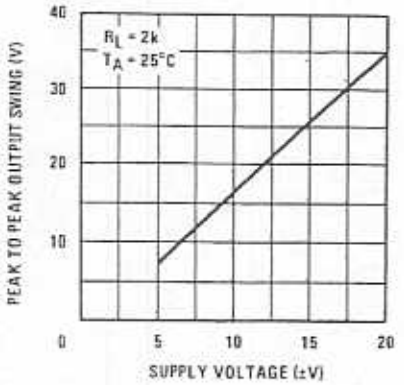
Input Bias Current



00564639

Voltage Swing



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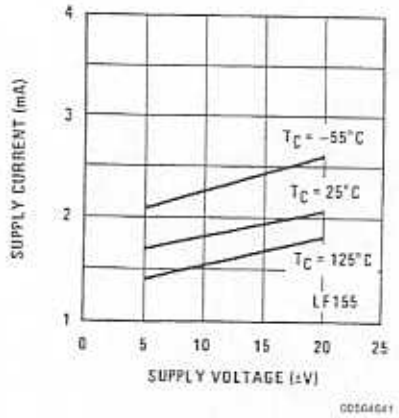
Typical DC Performance Characteristics

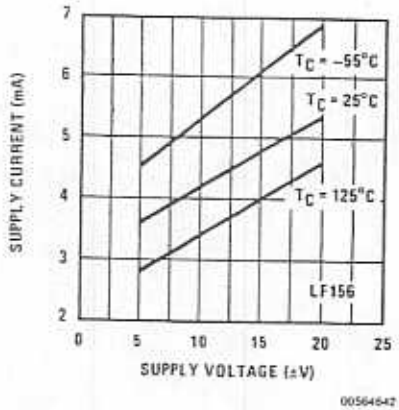
Curves are for LF155 and LF156 unless otherwise specified. (Continued)

Supply Current



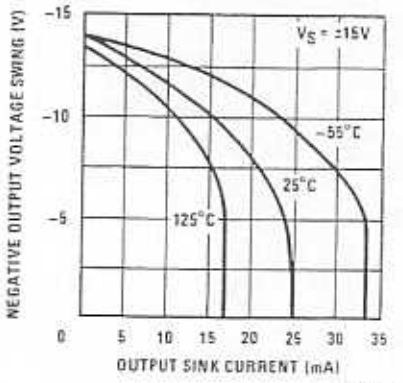
00564641

Supply Current



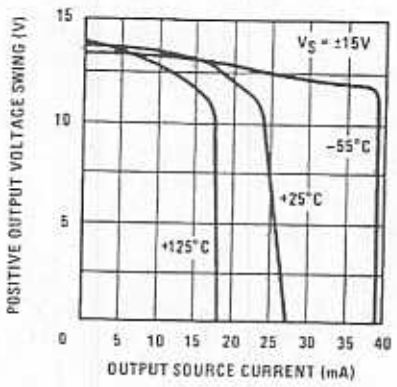
00564642

Negative Current Limit



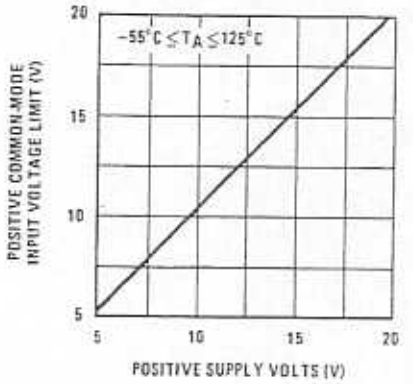
00564643

Positive Current Limit



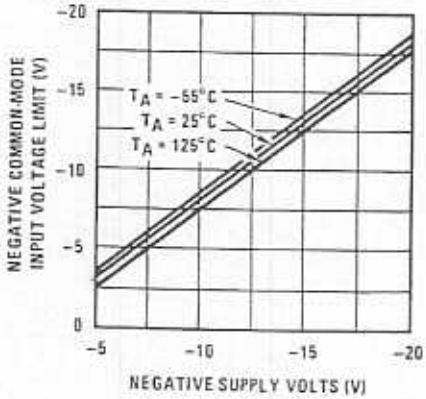
00564644

Positive Common-Mode Input Voltage Limit



00564645

Negative Common-Mode Input Voltage Limit

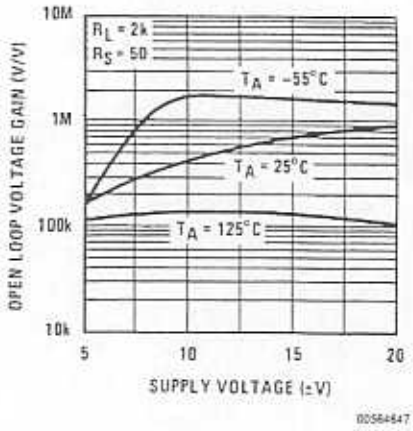


00564646

Typical DC Performance Characteristics

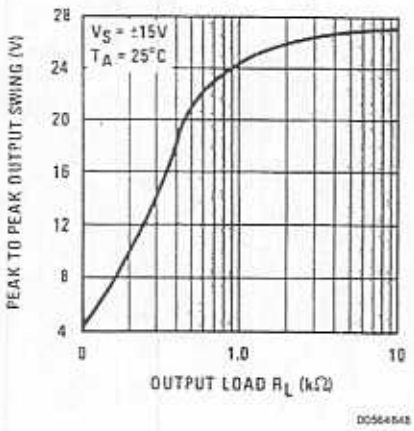
Curves are for LF155 and LF156 unless otherwise specified. (Continued)

Open Loop Voltage Gain



00564647

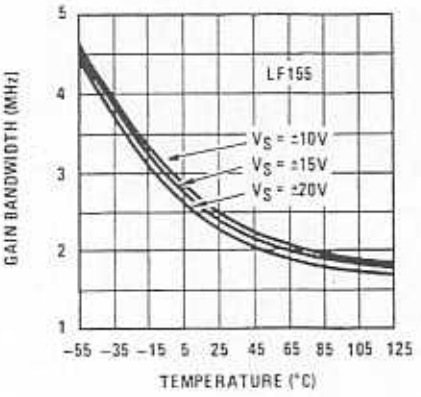
Output Voltage Swing



00564648

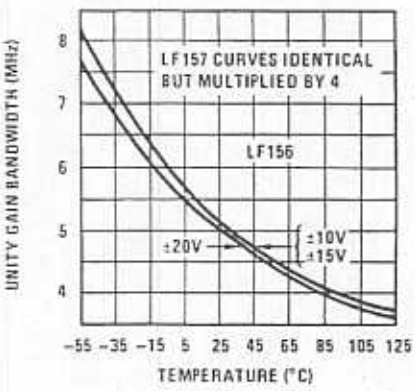
Typical AC Performance Characteristics

Gain Bandwidth



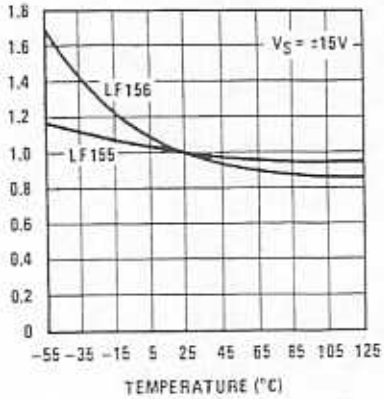
00564649

Gain Bandwidth



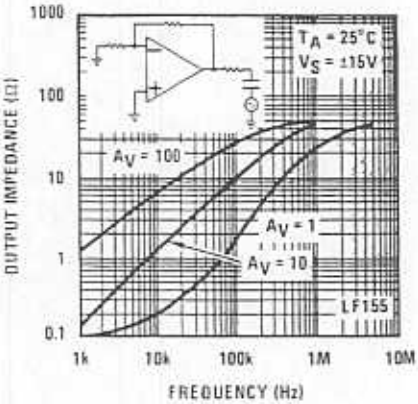
00564650

Normalized Slew Rate



00564651

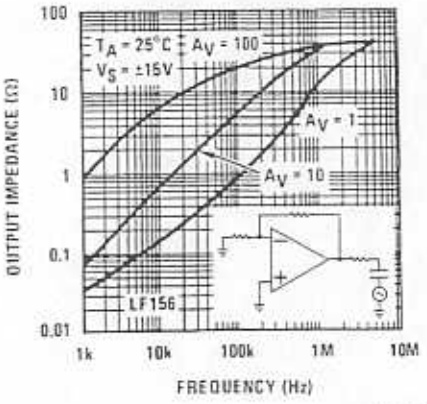
Output Impedance



00564652

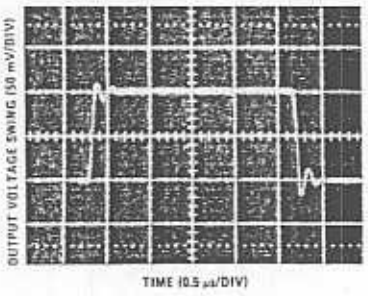
Typical AC Performance Characteristics (Continued)

Output Impedance



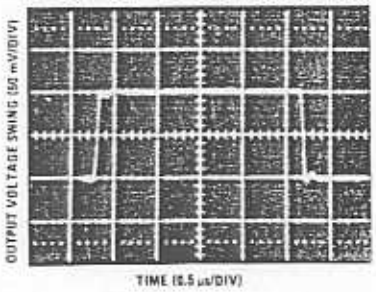
00564653

LF155 Small Signal Pulse Response, A_V = +1



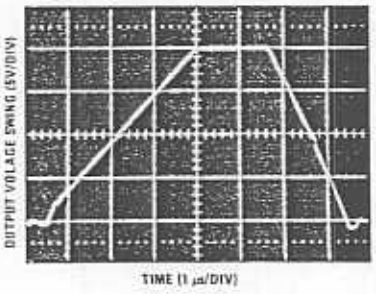
00564605

LF156 Small Signal Pulse Response, A_V = +1



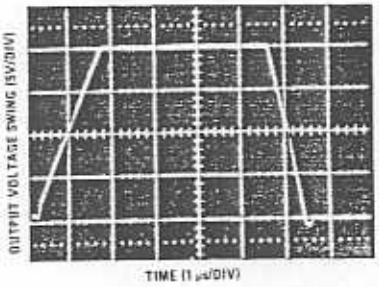
00564606

LF155 Large Signal Pulse Response, A_V = +1



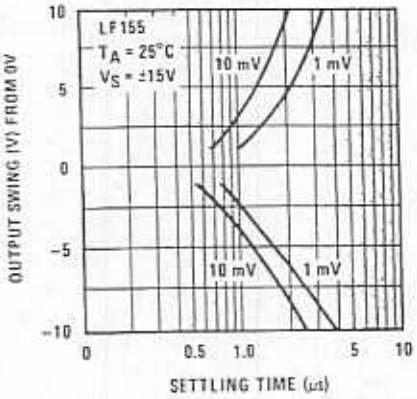
00564608

LF156 Large Signal Puls Response, A_V = +1



00564607

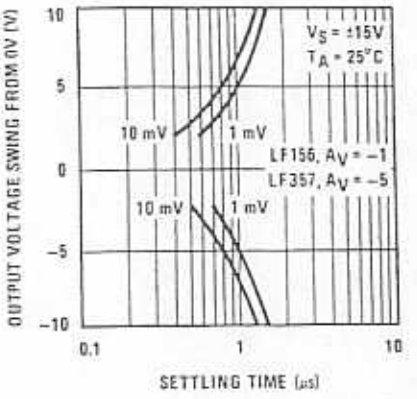
Inverter Settling Time



00564655

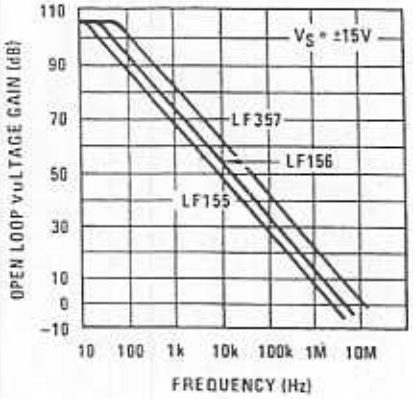
Typical AC Performance Characteristics (Continued)

Inverter Settling Time



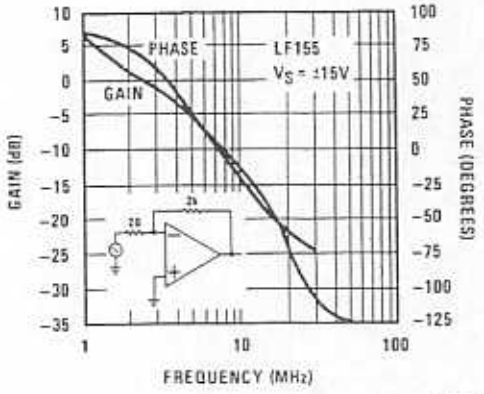
00564656

Open Loop Frequency Response



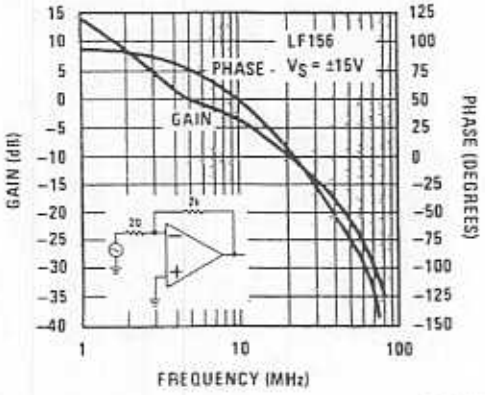
00564657

Bode Plot



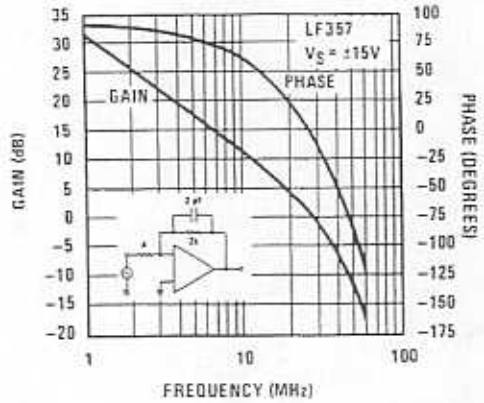
00564658

Bode Plot



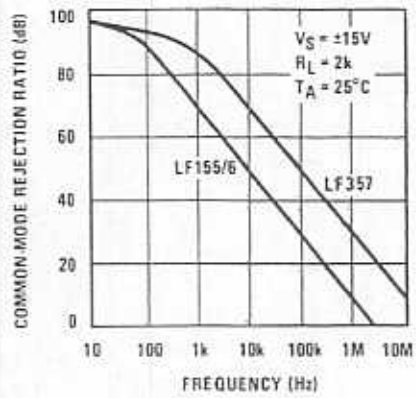
00564659

Bode Plot



00564660

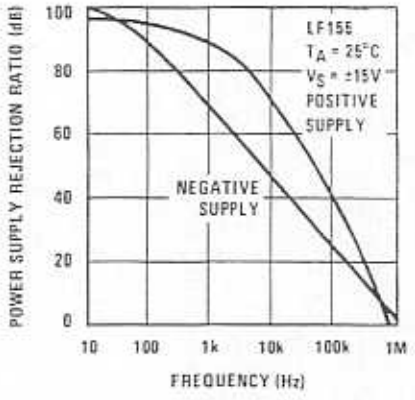
Common-Mode Rejection Ratio



00564661

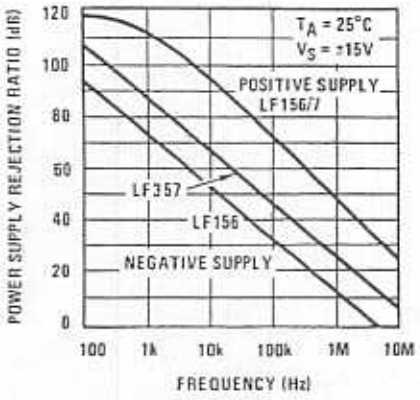
Typical AC Performance Characteristics (Continued)

Power Supply Rejection Ratio



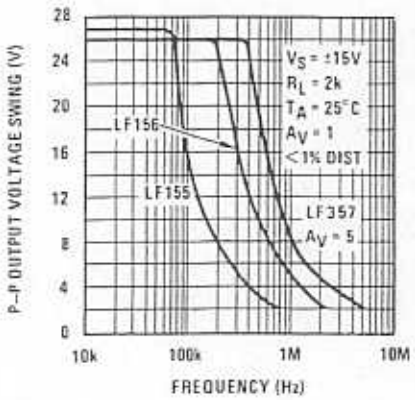
00564662

Power Supply Rejection Ratio



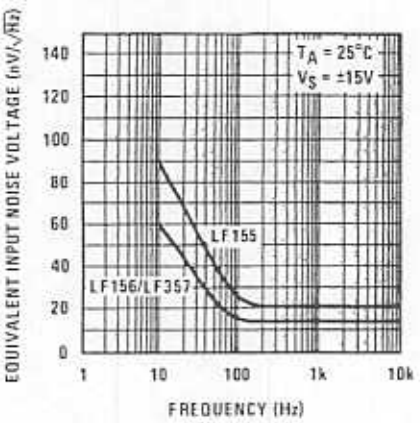
00564663

Undistorted Output Voltage Swing



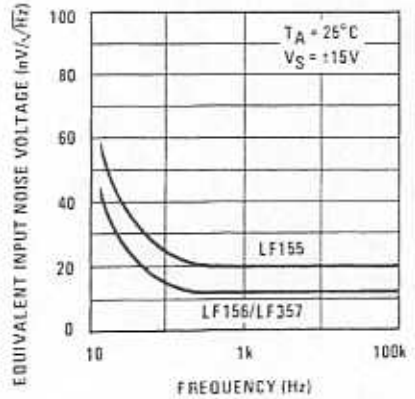
00564664

Equivalent Input Noise Voltage



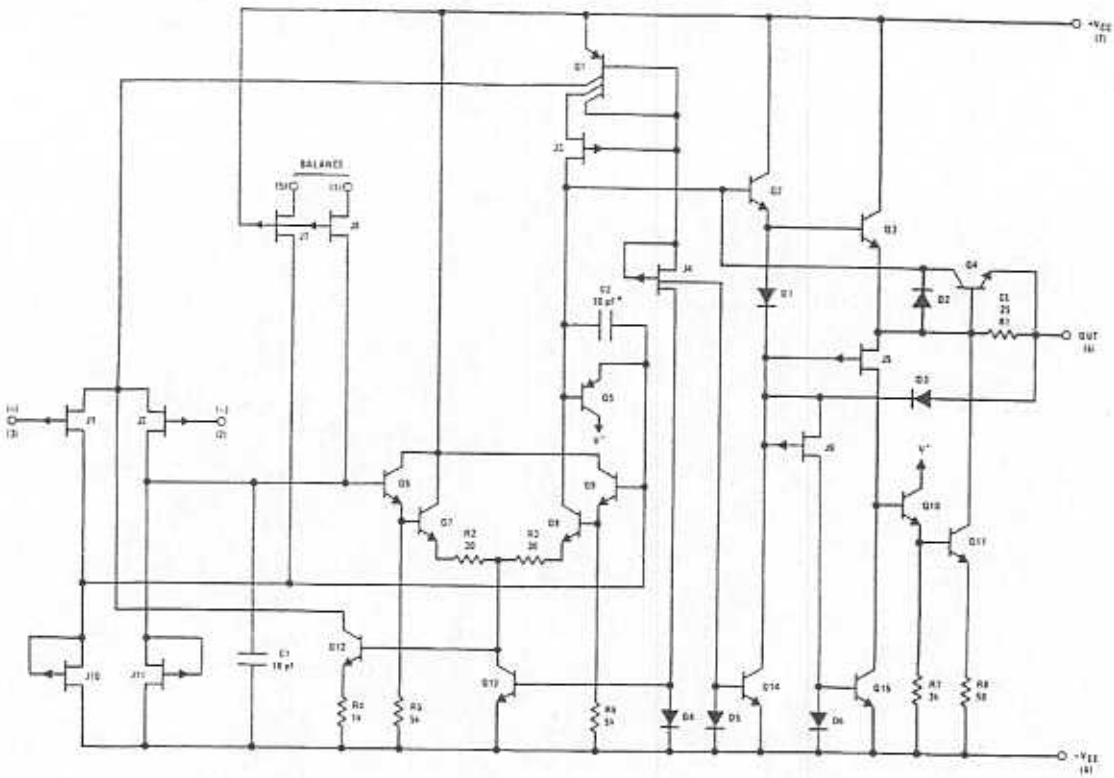
00564665

Equivalent Input Noise Voltage (Expanded Scale)



00564666

Detailed Schematic

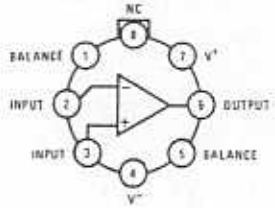


00564613

*C = 3pF in LF357 series.

Connection Diagrams (Top Views)

Metal Can Package (H)

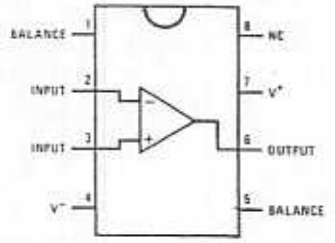


00564614

Order Number LF155H, LF156H, LF256H, LF257H, LF356BH, LF356H, or LF357H
See NS Package Number H08C

*Available per JM38510/11401 or JM38510/11402

Dual-In-Line Package (M and N)



00564629

Order Number LF356M, LF356MX, LF355N, or LF356N
See NS Package Number M08A or N08E

Application Hints

These are op amps with JFET input devices. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a

Application Hints (Continued)

reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

These amplifiers will operate with the common-mode input voltage equal to the positive supply. In fact, the common-mode voltage can exceed the positive supply by approximately 100 mV independent of supply voltage and over the full operating temperature range. The positive supply can therefore be used as a reference on an input as, for example, in a supply current monitor and/or limiter.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

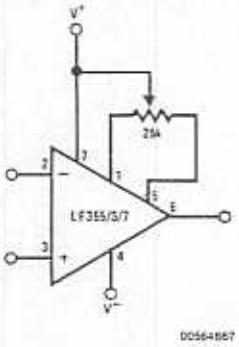
All of the bias currents in these amplifiers are set by FET current sources. The drain currents for the amplifiers are therefore essentially independent of supply voltage.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pickup" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Typical Circuit Connections

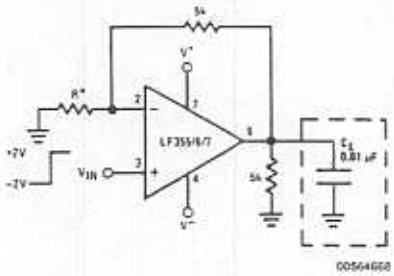
V_{OS} Adjustment



00564667

- V_{OS} is adjusted with a 25k potentiometer
- The potentiometer wiper is connected to V+
- For potentiometers with temperature coefficient of 100 ppm/°C or less the additional drift with adjust is = 0.5µV/°C/mV of adjustment
- Typical overall drift: 5µV/°C ±(0.5µV/°C/mV of adj.)

Driving Capacitive Loads



00564668

* LF155/6 R = 5k

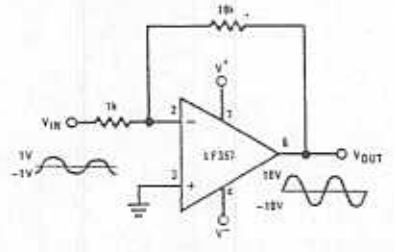
  LF357 R = 1.25k

  Due to a unique output stage design, these amplifiers have the ability to drive large capacitive loads and still maintain stability. $C_{L(MAX)} \approx 0.01\mu F$.

  Overshoot ≤ 20%

  Settling time (t_s) ≈ 5µs

LF357, A Large Power BW Amplifier



00564615

For distortion ≤ 1% and a 20 Vp-p V_{OUT} swing, power bandwidth is: 500kHz.

FAIRCHILD
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1N4001 - 1N4007

Features

- Low forward voltage drop.
- High surge current capability.

DO-41
COLOR BAND DENOTES CATHODE

General Purpose Rectifiers

Absolute Maximum Ratings*

T_A = 25°C unless otherwise noted

Symbol	Parameter	Value							Units
		4001	4002	4003	4004	4005	4006	4007	
V_{RRM}	Peak Repetitive Reverse Voltage	50	100	200	400	600	800	1000	V
$I_{F(AV)}$	Average Rectified Forward Current, .375 " lead length @ T_A = 75°C	1.0							A
I_{FSM}	Non-repetitive Peak Forward Surge Current 8.3 ms Single Half-Sine-Wave	30							A
T_{STG}	Storage Temperature Range	-55 to +175							°C
T_J	Operating Junction Temperature	-55 to +175							°C

*These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

Thermal Characteristics

Symbol	Parameter	Value	Units
P_D	Power Dissipation	3.0	W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	50	°C/W

Electrical Characteristics

T_A = 25°C unless otherwise noted

Symbol	Parameter	Device							Units
		4001	4002	4003	4004	4005	4006	4007	
V_F	Forward Voltage @ 1.0 A	1.1							V
I_{rr}	Maximum Full Load Reverse Current, Full Cycle T_A = 75°C	30							µA
I_R	Reverse Current @ rated V_R T_A = 25°C T_A = 100°C	5.0 500							µA µA
C_T	Total Capacitance V_R = 4.0 V, f = 1.0 MHz	15							pF

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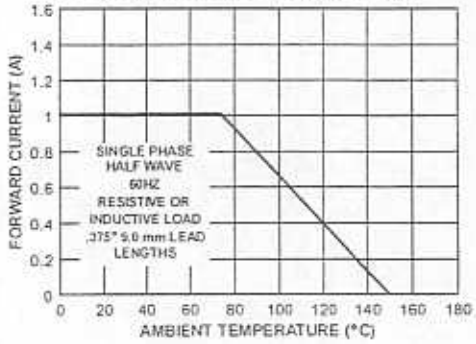
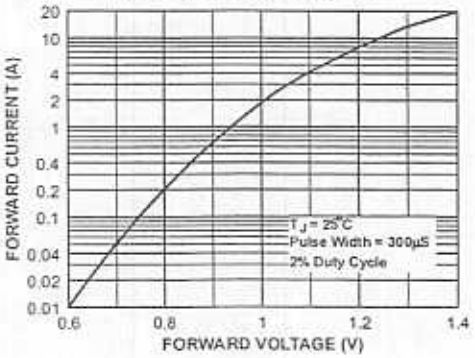
Typical Characteristics

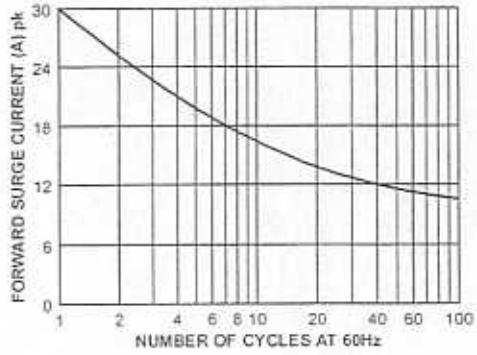
Forward Current Derating Curve



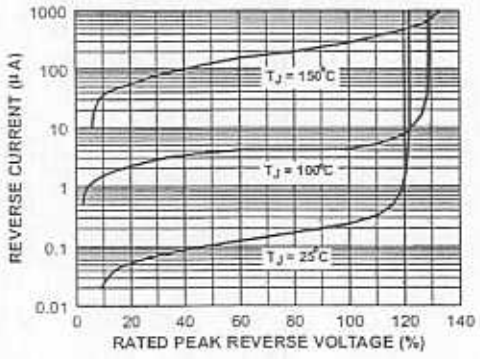
Forward Characteristics



Non-Repetitive Surge Current



Reverse Characteristics



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FAIRCHILD
SEMICONDUCTOR®

1N/FDLL 914/A/B / 916/A/B / 4148 / 4448

DO-35

LL-34

THE PLACEMENT OF THE EXPANSION GAP HAS NO RELATIONSHIP TO THE LOCATION OF THE CATHODE TERMINAL

COLOR BAND MARKING

DEVICE	1ST BAND	2ND BAND
FDLL914	BLACK	BROWN
FDLL914A	BLACK	GRAY
FDLL914B	BROWN	BLACK
FDLL916	BLACK	RED
FDLL916A	BLACK	WHITE
FDLL916B	BROWN	BROWN
FDLL4148	BLACK	BROWN
FDLL4448	BROWN	BLACK

Small Signal Diode

Absolute Maximum Ratings*

T_A = 25°C unless otherwise noted

Symbol	Parameter	Value	Units
V_{RRM}	Maximum Repetitive Reverse Voltage	100	V
$I_{F(AV)}$	Average Rectified Forward Current	200	mA
I_{FSM}	Non-repetitive Peak Forward Surge Current Pulse Width = 1.0 second Pulse Width = 1.0 microsecond	 1.0 4.0	 A A
T_{stg}	Storage Temperature Range	-65 to +200	°C
T_J	Operating Junction Temperature	175	°C

*These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

NOTES:
1) These ratings are based on a maximum junction temperature of 200 degrees C.
2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

Thermal Characteristics

Symbol	Characteristic	Max	Units
		1N/FDLL 914/A/B / 4148 / 4448	
P_D	Power Dissipation	500	mW
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	300	°C/W

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Electrical Characteristics

T_A = 25°C unless otherwise noted

Symbol	Parameter		Test Conditions	Min	Max	Units
V_R	Breakdown Voltage		I_R = 100 µA	100		V
			I_R = 5.0 µA	75		V
V_F	Forward Voltage	1N914B/4448	I_F = 5.0 mA	620	720	mV
		1N916B	I_F = 5.0 mA	630	730	mV
		1N914/916/4148	I_F = 10 mA		1.0	V
		1N914A/916A	I_F = 20 mA		1.0	V
		1N916B	I_F = 20 mA		1.0	V
		1N914B/4448	I_F = 100 mA		1.0	V
I_R	Reverse Current		V_R = 20 V		25	nA
			V_R = 20 V, T_A = 150°C		50	µA
			V_R = 75 V		5.0	µA
C_T	Total Capacitance					
		1N916A/B/4448	V_R = 0, f = 1.0 MHz		2.0	pF
		1N914A/B/4148	V_R = 0, f = 1.0 MHz		4.0	pF
t_{rr}	Reverse Recovery Time		I_F = 10 mA, V_R = 6.0 V (60mA), I_{rr} = 1.0 mA, R_L = 100Ω		4.0	ns

Typical Characteristics

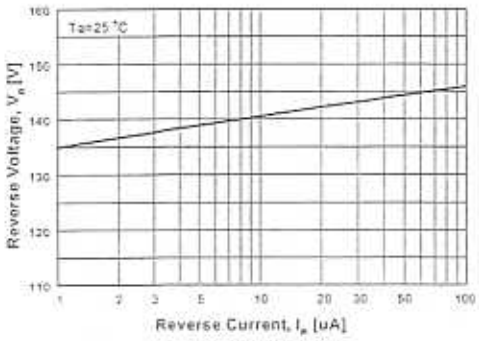
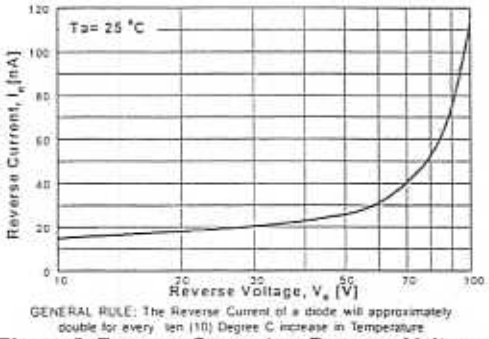


Figure 1. Reverse Voltage vs Reverse Current
BV - 1.0 to 100 uA



GENERAL RULE: The Reverse Current of a diode will approximately double for every ten (10) Degree C increase in Temperature

Figure 2. Reverse Current vs Reverse Voltage
IR - 10 to 100 V

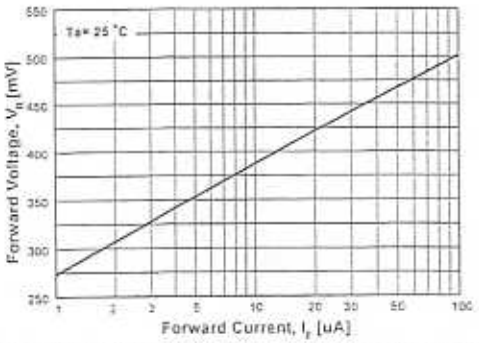


Figure 3. Forward Voltage vs Forward Current
VF - 1 to 100 uA

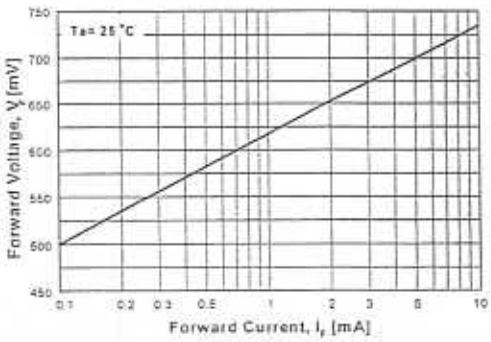


Figure 4. Forward Voltage vs Forward Current
VF - 0.1 to 10 mA

Typical Characteristics (continued)

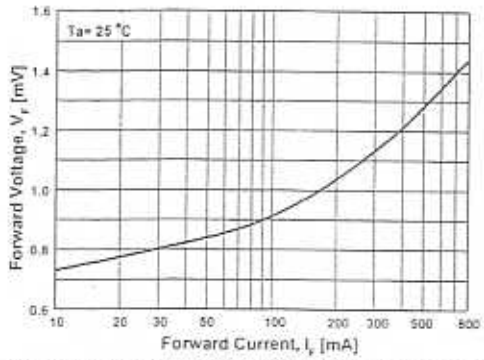


Figure 5. Forward Voltage vs Forward Current
VF - 10 to 800 mA

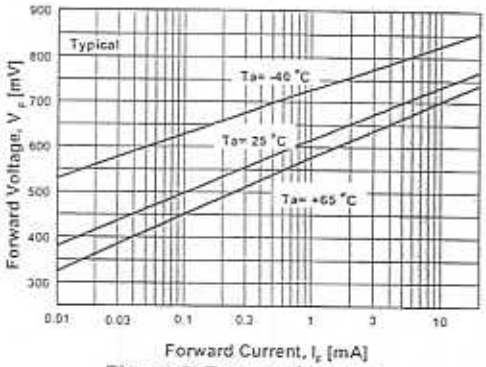


Figure 6. Forward Voltage
vs Ambient Temperature
VF - 0.01 - 20 mA (-40 to +65 Deg C)

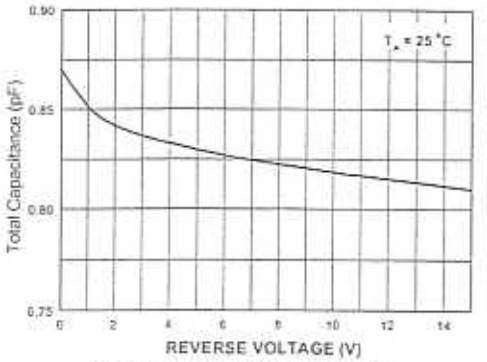


Figure 7. Total Capacitance

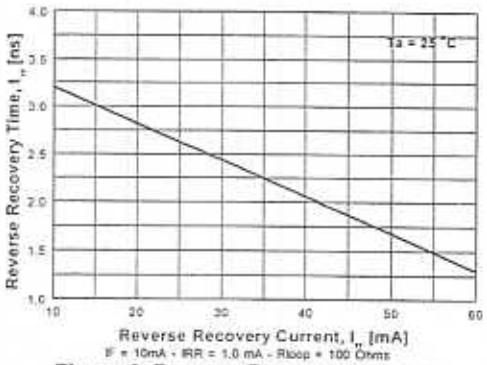


Figure 8. Reverse Recovery Time vs
Reverse Recovery Current

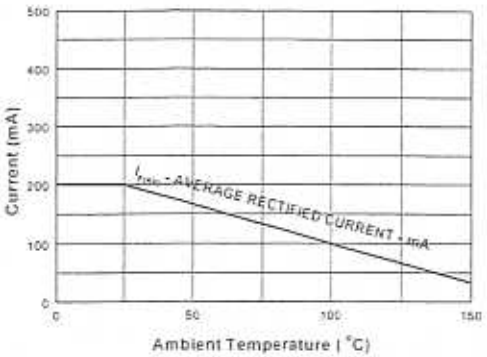


Figure 9. Average Rectified Current ($I_{F(AV)}$)
versus Ambient Temperature (T_A)

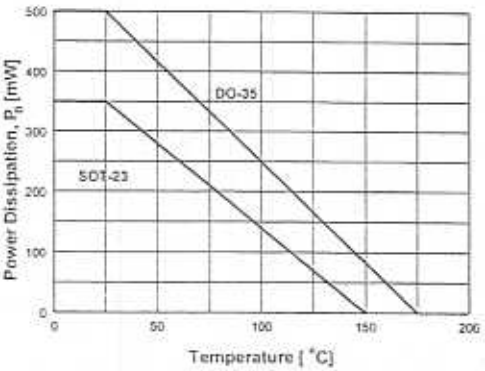


Figure 10. Power Derating Curve

Gold Bonded 1N34A Germanium Diodes

Optimized for Radio Frequency Response

Can be used in many AM, FM and TV-IF applications, replacing point contact devices.

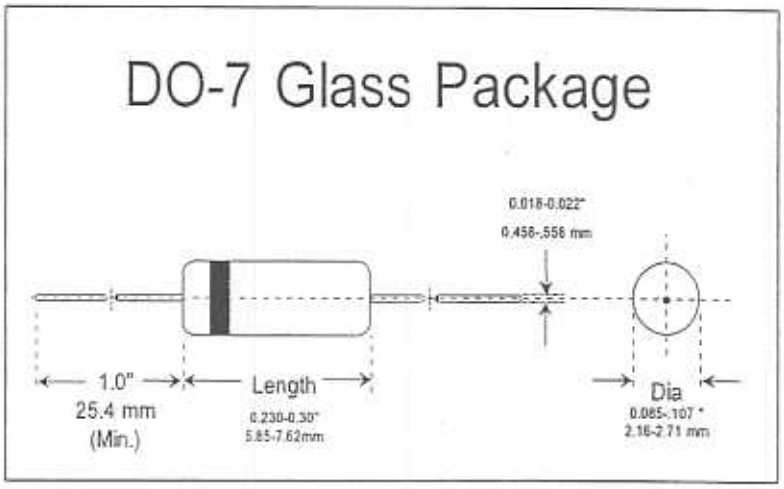
Applications

- AM/FM detectors
- Ratio detectors
- FM discriminators
- TV audio detectors
- RF input probes
- TV video detectors

Features

- Lower leakage current
- Flat junction capacitance
- High mechanical strength
- At least 1 million hours MTBF
- BKC's Sigma-Bond™ plating for problem free solderability

DO-7 Glass Package



Absolute Maximum Ratings at T_{amb} = 25 °C

Parameter	Symbols	Min.	Max.	Units
Peak Inverse Voltage (Repetitive), Measured @ I_R = 1 mA	PIV	**	65	Volts
Peak Forward Surge Current Non-Repetitive, t = 1 Second	I_{FSM}		0.5	Amps
Peak Forward Surge Current Repetitive	I_{FSR}		200	mA
Average Rectified Forward Current	I_O		50	mA
Operating and Storage Temperatures	$T_{J\&STG}$	-55	+75	°C

Electrical Characteristics at T_{amb} = 25 °C

Parameter	Test Conditions	Symbols	Min.	Max.	Units
Forward Voltage Drop	I_F = 5.0mA	V_F		1.0	Volts
	V_R = 10 Volts			30	µA
Reverse Leakage	V_R = 50 Volts	I_R		500	µA
Breakdown Voltage	Ir = 1.0 mA	PIV	65		Volts

Microsemi 6 Lake Street - Lawrence, MA 01841
Tel: 978-681-0392 - Fax: 978-681-9135

FAIRCHILD
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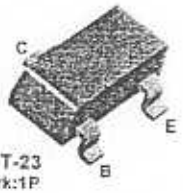
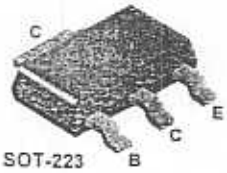
PN2222A MMBT2222A PZT2222A

TO-92

E B C



SOT-23
Mark:1P



SOT-223

NPN General Purpose Amplifier

- This device is for use as a medium power amplifier and switch requiring collector currents up to 500mA.
- Sourced from process 19.

Absolute Maximum Ratings * T_a=25°C unless otherwise noted

Symbol	Parameter	Value	Units
V_{CEO}	Collector-Emitter Voltage	40	V
V_{CBO}	Collector-Base Voltage	75	V
V_{EBO}	Emitter-Base Voltage	6.0	V
I_C	Collector Current	1.0	A
T_{STG}	Operating and Storage Junction Temperature Range	- 55 ~ 150	°C

* These ratings are limiting values above which the serviceability of any semiconductor device may be impaired

NOTES:
1) These ratings are based on a maximum junction temperature of 150 degrees C.
2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

Electrical Characteristics T_a=25°C unless otherwise noted

Symbol	Parameter	Test Condition	Min.	Max.	Units
Off Characteristics					
$BV_{(BR)CEO}$	Collector-Emitter Breakdown Voltage *	I_C = 10mA, I_B = 0	40		V
$BV_{(BR)CBO}$	Collector-Base Breakdown Voltage	I_C = 10μA, I_E = 0	75		V
$BV_{(BR)EBO}$	Emitter-Base Breakdown Voltage	I_E = 10μA, I_C = 0	6.0		V
I_{CEX}	Collector Cutoff Current	V_{CE} = 60V, $V_{EB(off)}$ = 3.0V		10	nA
I_{CBO}	Collector Cutoff Current	V_{CB} = 60V, I_E = 0 V_{CB} = 60V, I_E = 0, T_a = 125°C		0.01 10	μA μA
I_{EBO}	Emitter Cutoff Current	V_{EB} = 3.0V, I_C = 0		10	μA
I_{BL}	Base Cutoff Current	V_{CE} = 60V, $V_{EB(off)}$ = 3.0V		20	μA
On Characteristics					
h_{FE}	DC Current Gain	I_C = 0.1mA, V_{CE} = 10V I_C = 1.0mA, V_{CE} = 10V I_C = 10mA, V_{CE} = 10V I_C = 10mA, V_{CE} = 10V, T_a = -55°C I_C = 150mA, V_{CE} = 10V * I_C = 150mA, V_{CE} = 10V * I_C = 500mA, V_{CE} = 10V *	35 50 75 35 100 50 40	 300 	
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage *	I_C = 150mA, V_{CE} = 10V I_C = 500mA, V_{CE} = 10V		0.3 1.0	V V
$V_{BE(sat)}$	Base-Emitter Saturation Voltage *	I_C = 150mA, V_{CE} = 10V I_C = 500mA, V_{CE} = 10V	0.6	1.2 2.0	V V

* Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%

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Electrical Characteristics Ta=25°C unless otherwise noted (Continued)

Symbol	Parameter	Test Condition	Min.	Max.	Units
Small Signal Characteristics					
f_T	Current Gain Bandwidth Product	I_C = 20mA, V_{CE} = 20V, f = 100MHz	300		MHz
C_{obo}	Output Capacitance	V_{CB} = 10V, I_E = 0, f = 1MHz		8.0	pF
C_{ibo}	Input Capacitance	V_{EB} = 0.5V, I_C = 0, f = 1MHz		25	pF
$rb'C_c$	Collector Base Time Constant	I_C = 20mA, V_{CB} = 20V, f = 31.8MHz		150	pS
NF	Noise Figure	I_C = 100µA, V_{CE} = 10V, R_S = 1.0KΩ, f = 1.0KHz		4.0	dB
$Re(h_{ie})$	Real Part of Common-Emitter High Frequency Input Impedance	I_C = 20mA, V_{CE} = 20V, f = 300MHz		60	Ω
Switching Characteristics					
t_d	Delay Time	V_{CC} = 30V, $V_{EB(off)}$ = 0.5V, I_C = 150mA, I_{B1} = 15mA		10	ns
t_r	Rise Time			25	ns
t_s	Storage Time	V_{CC} = 30V, I_C = 150mA, I_{B1} = I_{B2} = 15mA		225	ns
t_f	Fall Time			60	ns

Thermal Characteristics T_a=25°C unless otherwise noted

Symbol	Parameter	Max.			Units
		PN2222A	*MMBT2222A	**PZT2222A	
P_D	Total Device Dissipation	625	350	1,000	mW
	Derate above 25°C	5.0	2.8	8.0	mW/°C
$R_{\theta JC}$	Thermal Resistance, Junction to Case	83.3			°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	200	357	125	°C/W

* Device mounted on FR-4 PCB 1.6" × 1.6" × 0.06".
** Device mounted on FR-4 PCB 36mm × 18mm × 1.5mm; mounting pad for the collector lead min. 6cm².

Spice Model

NPN (Is = 14.34f Xti = 3 Eg = 1.11 Vaf = 74.03 Bf = 255.9 Ne = 1.307 Ise = 14.34 Ikf = .2847 Xtb = 1.5 Br = 6.092 Isc = 0 Ikr = 0 Rc = 1 Cjc = 7.306p Mjc = .3416 Vjc = .75 Fc = .5 Cje = 22.01p Mje = .377 Vje = .75 Tr = 46.91n Tf = 411.1p Itf = .6 Vtf = 1.7 Xtf = 3 Rb = 10)

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Typical Characteristics

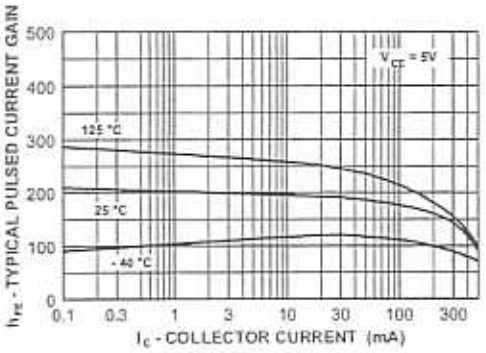

Figure 1. Typical Pulsed Current Gain vs Collector Current

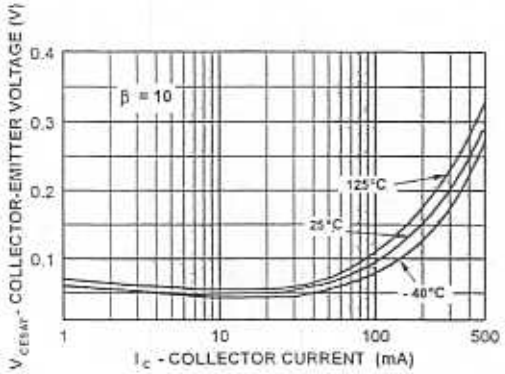

Figure 2. Collector-Emitter Saturation Voltage vs Collector Current

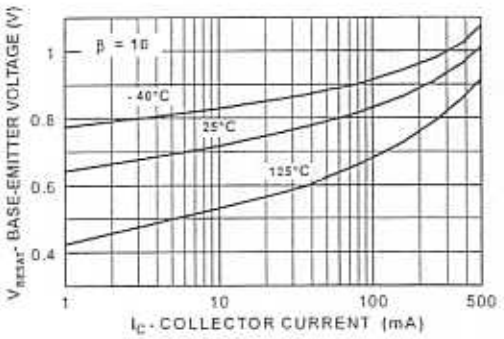

Figure 3. Base-Emitter Saturation Voltage vs Collector Current

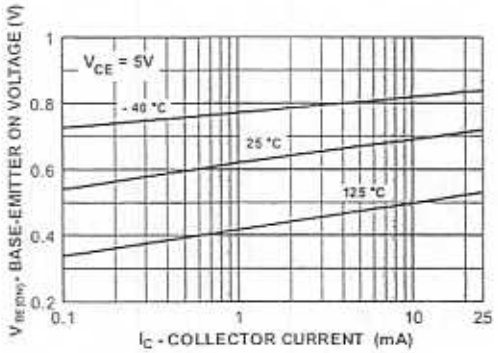

Figure 4. Base-Emitter On Voltage vs Collector Current

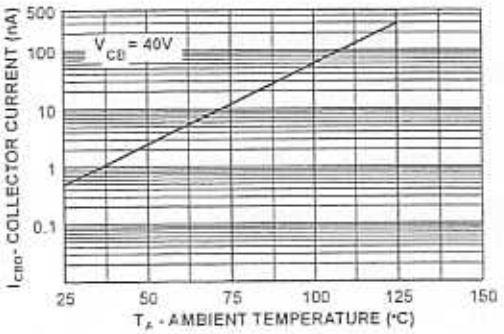

Figure 5. Collector Cutoff Current vs Ambient Temperature

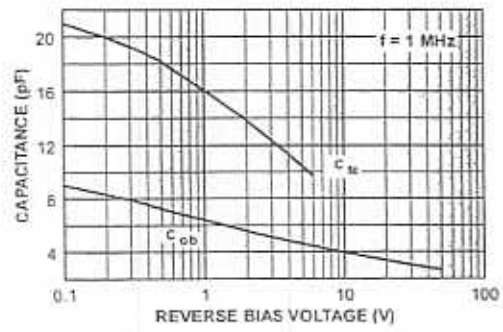

Figure 6. Emitter Transition and Output Capacitance vs Reverse Bias Voltage

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Typical Characteristics

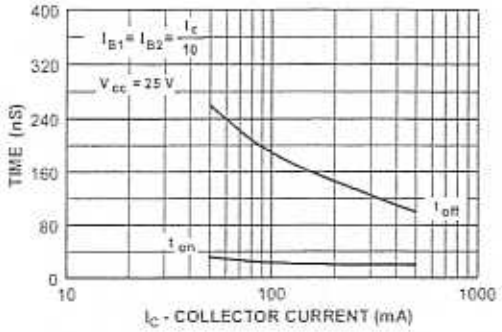

Figure 7. Turn On and Turn Off Times vs Collector Current

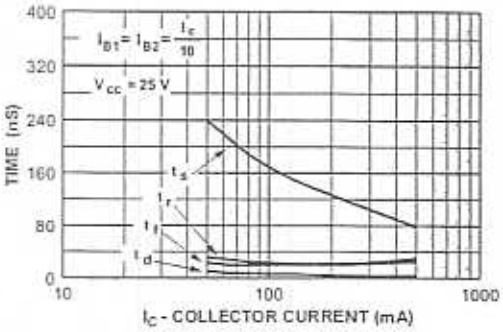

Figure 8. Switching Times vs Collector Current

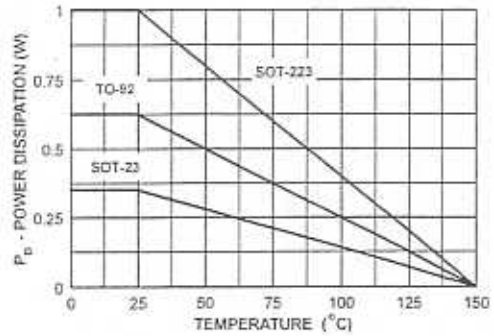

Figure 9. Power Dissipation vs Ambient Temperature

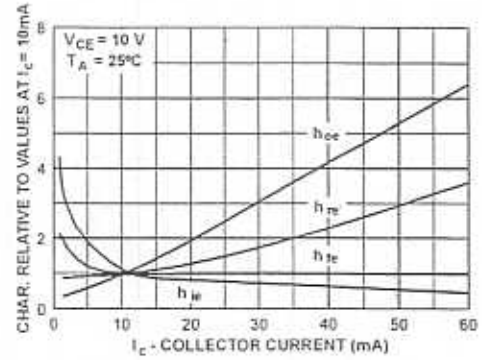

Figure 10. Common Emitter Characteristics

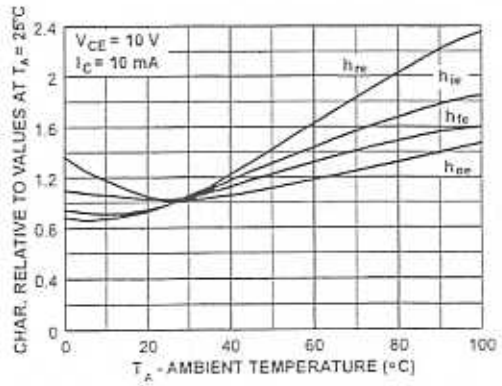

Figure 11. Common Emitter Characteristics

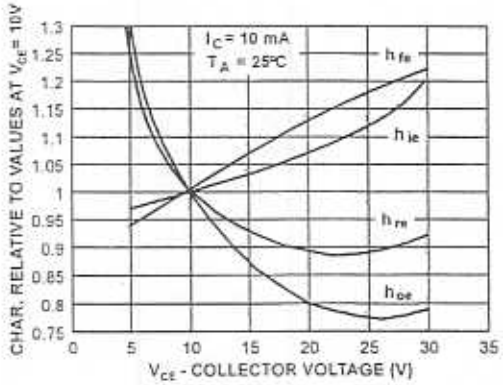

Figure 12. Common Emitter Characteristics

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MC14007UB

Dual Complementary Pair Plus Inverter

The MC14007UB multi–purpose device consists of three N–channel and three P–channel enhancement mode devices packaged to provide access to each device. These versatile parts are useful in inverter circuits, pulse–shapers, linear amplifiers, high input impedance amplifiers, threshold detectors, transmission gating, and functional gating.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low–power TTL Loads or One Low–power Schottky TTL Load Over the Rated Temperature Range
- Pin–for–Pin Replacement for CD4007A or CD4007UB
- This device has 2 outputs without ESD Protection. Anti–static precautions must be taken.

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 2.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 3.)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8–Second Soldering)	260	°C

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:
   Plastic "P and D/DW" Packages: – 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

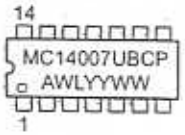
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

ON Semiconductor

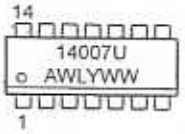
http://onsemi.com

MARKING DIAGRAMS

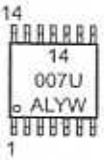
PDIP–14
P SUFFIX
CASE 646



SOIC–14
D SUFFIX
CASE 751A



TSSOP–14
DT SUFFIX
CASE 948G



SOEIAJ–14
F SUFFIX
CASE 965

A = Assembly Location
WL or L = Wafer Lot
YY or Y = Year
WW or W = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC14007UBCP	PDIP–14	2000/Box
MC14007UBD	SOIC–14	55/Rail
MC14007UBDR2	SOIC–14	2500/Tape & Reel
MC14007UBDT	TSSOP–14	96/Rail
MC14007UBF	SOEIAJ–14	See Note 1.
MC14007UBFEL	SOEIAJ–14	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

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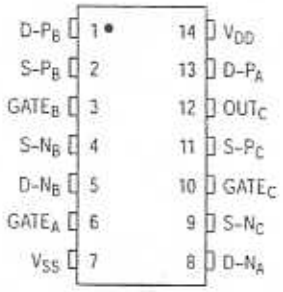
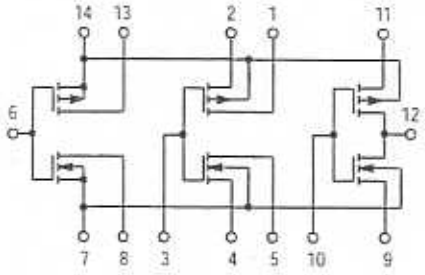
PIN ASSIGNMENT

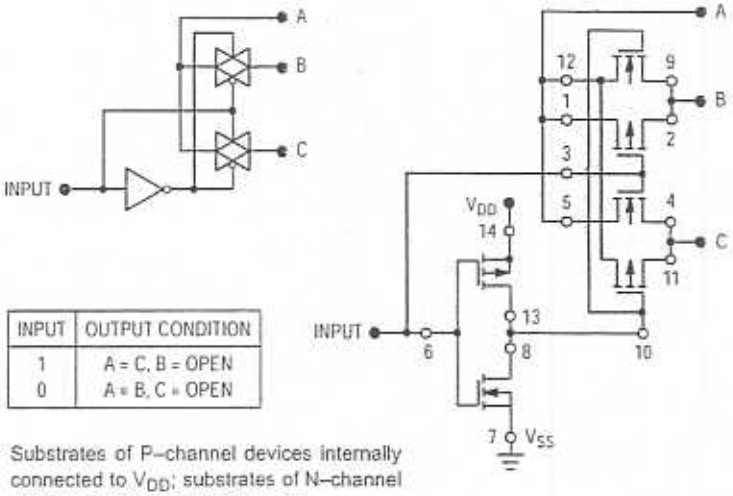


D = DRAIN
S = SOURCE

SCHEMATIC



V_{DD} = PIN 14
V_{SS} = PIN 7



INPUT	OUTPUT CONDITION
1	A = C, B = OPEN
0	A = B, C = OPEN

Substrates of P–channel devices internally connected to V_{DD}; substrates of N–channel devices internally connected to V_{SS}.

Figure 1. Typical Application: 2–Input Analog Multiplexer

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic		Symbol	V_{DD} Vdc	−55°C Min	−55°C Max	25°C Min	25°C Typ (4.)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage V_{in} = V_{DD} or 0	"0" Level	V_{OL}	5.0 10 15	— — —	0.05 0.05 0.05	— — —	0 0 0	0.05 0.05 0.05	— — —	0.05 0.05 0.05	Vdc
V_{in} = 0 or V_{DD}	"1" Level	V_{OH}	5.0 10 15	4.95 9.95 14.95	— — —	4.95 9.95 14.95	5.0 10 15	— — —	4.95 9.95 14.95	— — —	Vdc
Input Voltage (V_O = 4.5 Vdc) (V_O = 9.0 Vdc) (V_O = 13.5 Vdc)	"0" Level	V_{IL}	5.0 10 15	— — —	1.0 2.0 2.5	— — —	2.25 4.50 6.75	1.0 2.0 2.5	— — —	1.0 2.0 2.5	Vdc
(V_O = 0.5 Vdc) (V_O = 1.0 Vdc) (V_O = 1.5 Vdc)	"1" Level	V_{IH}	5.0 10 15	4.0 8.0 12.5	— — —	4.0 8.0 12.5	2.75 5.50 8.25	— — —	4.0 8.0 12.5	— — —	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	Source	I_{OH}	5.0 5.0 10 15	−3.0 −0.64 −1.6 −4.2	— — — —	−2.4 −0.51 −1.3 −3.4	−5.0 −1.0 −2.5 −10	— — — —	−1.7 −0.36 −0.9 −2.4	— — — —	mAdc
(V_{OL} = 0.4 Vdc) (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	Sink	I_{OL}	5.0 10 15	0.64 1.6 4.2	— — —	0.51 1.3 3.4	1.0 2.5 10	— — —	0.36 0.9 2.4	— — —	mAdc
Input Current		I_{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	µAdc
Input Capacitance (V_{in} = 0)		C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)		I_{DD}	5.0 10 15	— — —	0.25 0.5 1.0	— — —	0.0005 0.0010 0.0015	0.25 0.5 1.0	— — —	7.5 15 30	µAdc
Total Supply Current (5.) (6.) (Dynamic plus Quiescent, Per Gate) (C_L = 50 pF)		I_T	5.0 10 15	I_T = (0.7 µA/kHz) f + I_{DD}/6 I_T = (1.4 µA/kHz) f + I_{DD}/6 I_T = (2.2 µA/kHz) f + I_{DD}/6							µAdc

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
5. The formulas given are for the typical characteristics only at 25°C.
6. To calculate total supply current at loads other than 50 pF:

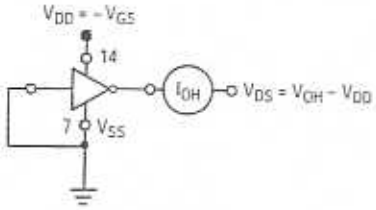
$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.003.

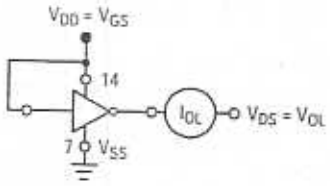
SWITCHING CHARACTERISTICS [7.] (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ [8.]	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (1.2 ns/pF) C_L + 30 ns		5.0	—	90	180	
t_{TLH} = (0.5 ns/pF) C_L + 20 ns		10	—	45	90	
t_{TLH} = (0.4 ns/pF) C_L + 15 ns		15	—	35	70	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.2 ns/pF) C_L + 15 ns		5.0	—	75	150	
t_{THL} = (0.5 ns/pF) C_L + 15 ns		10	—	40	80	
t_{THL} = (0.4 ns/pF) C_L + 10 ns		15	—	30	60	
Turn–Off Delay Time	t_{PLH}					ns
t_{PLH} = (1.5 ns/pF) C_L + 35 ns		5.0	—	60	125	
t_{PLH} = (0.2 ns/pF) C_L + 20 ns		10	—	30	75	
t_{PLH} = (0.15 ns/pF) C_L + 17.5 ns		15	—	25	55	
Turn–On Delay Time	t_{PHL}					ns
t_{PHL} = (1.0 ns/pF) C_L + 10 ns		5.0	—	60	125	
t_{PHL} = (0.3 ns/pF) C_L + 15 ns		10	—	30	75	
t_{PHL} = (0.2 ns/pF) C_L + 15 ns		15	—	25	55	

7. The formulas given are for the typical characteristics only. Switching specifications are for device connected as an inverter.
8. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.



All unused inputs connected to ground.



All unused inputs connected to ground.

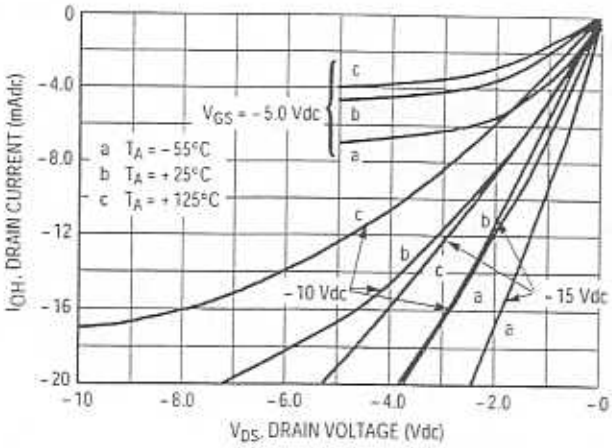


Figure 2. Typical Output Source Characteristics

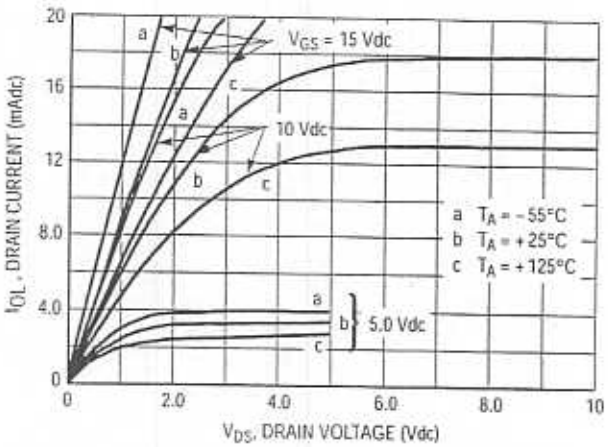


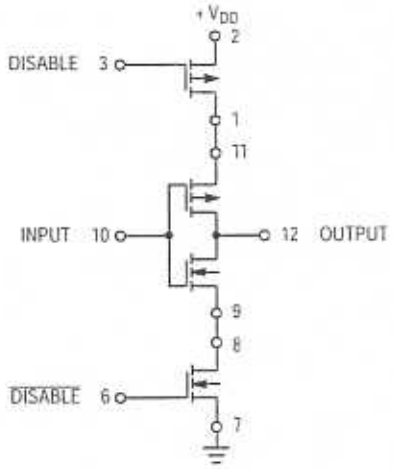
Figure 3. Typical Output Sink Characteristics

These typical curves are not guarantees, but are design aids.
Caution: The maximum current rating is 10 mA per pin.

Figure 4. Switching Time and Power Dissipation Test Circuit and Waveforms

APPLICATIONS

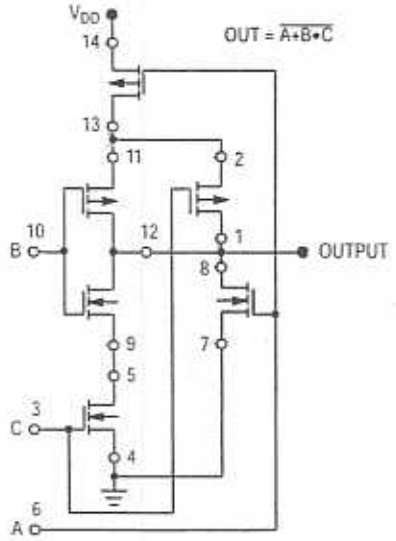
The MC14007UB dual pair plus inverter, which has access to all its elements offers a number of unique circuit applications. Figures 1, 5, and 6 are a few examples of the device flexibility.



INPUT	DISABLE	OUTPUT
1	0	0
0	0	1
X	1	OPEN

X = Don't Care

Figure 5. 3–State Buffer



Substrates of P–channel devices internally connected to V_{DD};
Substrates of N–channel devices internally connected to V_{SS}.

Figure 6. AOI Functions Using Tree Logic

FAIRCHILD
SEMICONDUCTOR TM

November 1995

2N7000 / 2N7002 / NDS7002A
N-Channel Enhancement Mode Field Effect Transistor

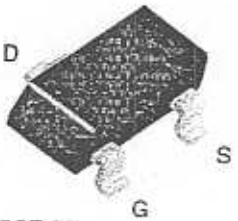
General Description

These N-Channel enhancement mode field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. These products have been designed to minimize on-state resistance while provide rugged, reliable, and fast switching performance. They can be used in most applications requiring up to 400mA DC and can deliver pulsed currents up to 2A. These products are particularly suited for low voltage, low current applications such as small servo motor control, power MOSFET gate drivers, and other switching applications.

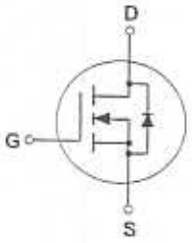
Features

- High density cell design for low $R_{DS(ON)}$.
- Voltage controlled small signal switch.
- Rugged and reliable.
- High saturation current capability.

TO-92
2N7000



SOT-23
(TO-236AB)
2N7002/NDS7002A



Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter	2N7000	2N7002	NDS7002A	Units
V_{DSS}	Drain-Source Voltage		60		V
V_{DGR}	Drain-Gate Voltage ($R_{GS} \leq 1$ MΩ)		60		V
V_{GSS}	Gate-Source Voltage - Continuous		±20		V
	- Non Repetitive (tp < 50µs)		±40		
I_D	Maximum Drain Current - Continuous	200	115	280	mA
	- Pulsed	500	800	1500	
P_D	Maximum Power Dissipation	400	200	300	mW
	Derated above 25°C	3.2	1.6	2.4	mW/°C
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to 150		-65 to 150	°C
T_L	Maximum Lead Temperature for Soldering Purposes, 1/16" from Case for 10 Seconds		300		°C
THERMAL CHARACTERISTICS					
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	312.5	625	417	°C/W

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Electrical Characteristics T_A = 25°C unless otherwise noted

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
OFF CHARACTERISTICS							
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 10 µA	All	60			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 48 V, V_{GS} = 0 V	2N7000			1	µA
		T_J=125°C				1	mA
		V_{DS} = 60 V, V_{GS} = 0 V	2N7002 NDS7002A			1	µA
		T_J=125°C				0.5	mA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 15 V, V_{DS} = 0 V	2N7000			10	nA
		V_{GS} = 20 V, V_{DS} = 0 V	2N7002 NDS7002A			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -15 V, V_{DS} = 0 V	2N7000			-10	nA
		V_{GS} = -20 V, V_{DS} = 0 V	2N7002 NDS7002A			-100	nA
ON CHARACTERISTICS (Note 1)							
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 1 mA	2N7000	0.8	2.1	3	V
		V_{DS} = V_{GS}, I_D = 250 µA	2N7002 NDS7002A	1	2.1	2.5	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 500 mA	2N7000		1.2	5	Ω
		T_J =125°C			1.9	9	
		V_{GS} = 4.5 V, I_D = 75 mA			1.8	5.3	
		V_{GS} = 10 V, I_D = 500 mA	2N7002		1.2	7.5	
		T_J =100°C			1.7	13.5	
		V_{GS} = 5.0 V, I_D = 50 mA			1.7	7.5	
		T_J =100C			2.4	13.5	
		V_{GS} = 10 V, I_D = 500 mA	NDS7002A		1.2	2	
		T_J =125°C			2	3.5	
		V_{GS} = 5.0 V, I_D = 50 mA			1.7	3	
		T_J =125°C			2.8	5	
$V_{DS(ON)}$	Drain-Source On-Voltage	V_{GS} = 10 V, I_D = 500 mA	2N7000		0.6	2.5	V
		V_{GS} = 4.5 V, I_D = 75 mA			0.14	0.4	
		V_{GS} = 10 V, I_D = 500mA	2N7002		0.6	3.75	
		V_{GS} = 5.0 V, I_D = 50 mA			0.09	1.5	
		V_{GS} = 10 V, I_D = 500mA	NDS7002A		0.6	1	
		V_{GS} = 5.0 V, I_D = 50 mA			0.09	0.15	

Electrical Characteristics T_A = 25°C unless otherwise noted

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
ON CHARACTERISTICS Continued (Note 1)							
$I_{D(ON)}$	On-State Drain Current	V_{GS} = 4.5 V, V_{DS} = 10 V	2N7000	75	600		mA
		V_{GS} = 10 V, $V_{DS} \geq 2\ V_{DS(on)}$	2N7002	500	2700		
		V_{GS} = 10 V, $V_{DS} \geq 2\ V_{DS(on)}$	NDS7002A	500	2700		
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 200 mA	2N7000	100	320		mS
		$V_{DS} \geq 2\ V_{DS(on)}$, I_D = 200 mA	2N7002	80	320		
		$V_{DS} \geq 2\ V_{DS(on)}$, I_D = 200 mA	NDS7002A	80	320		
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	All		20	50	pF
C_{oss}	Output Capacitance		All		11	25	pF
C_{rss}	Reverse Transfer Capacitance		All		4	5	pF
t_{on}	Turn-On Time	V_{DD} = 15 V, R_L = 25 Ω, I_D = 500 mA, V_{GS} = 10 V, R_{GEN} = 25	2N7000			10	ns
		V_{DD} = 30 V, R_L = 150 Ω, I_D = 200 mA, V_{GS} = 10 V, R_{GEN} = 25 Ω	2N700 NDS7002A			20	
t_{off}	Turn-Off Time	V_{DD} = 15 V, R_L = 25 Ω, I_D = 500 mA, V_{GS} = 10 V, R_{GEN} = 25	2N7000			10	ns
		V_{DD} = 30 V, R_L = 150 Ω, I_D = 200 mA, V_{GS} = 10 V, R_{GEN} = 25 Ω	2N700 NDS7002A			20	
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS							
I_S	Maximum Continuous Drain-Source Diode Forward Current		2N7002			115	mA
			NDS7002A			280	
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		2N7002			0.8	A
			NDS7002A			1.5	
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 115 mA (Note 1)	2N7002		0.88	1.5	V
		V_{GS} = 0 V, I_S = 400 mA (Note 1)	NDS7002A		0.88	1.2	

Note:
1. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

2N7000 / 2N7002 / NDS7002A

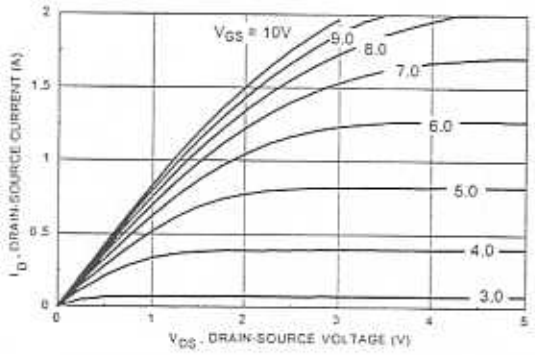

Figure 1. On-Region Characteristics

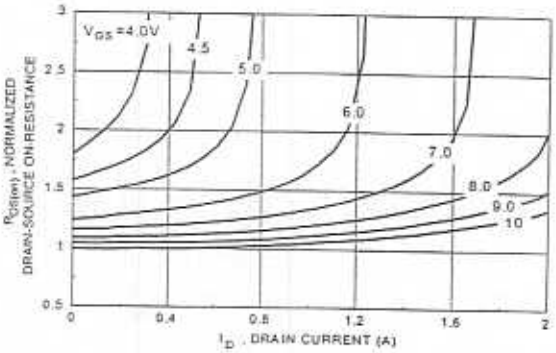

Figure 2. On-Resistance Variation with Gate Voltage and Drain Current

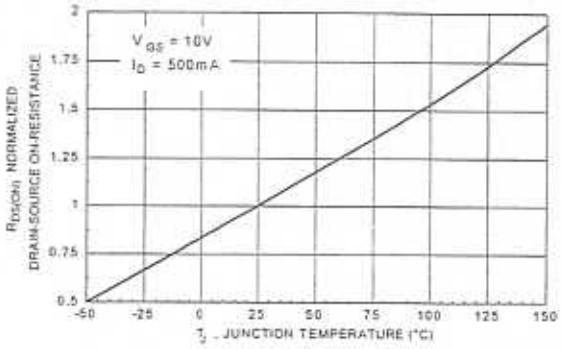

Figure 3. On-Resistance Variation with Temperature

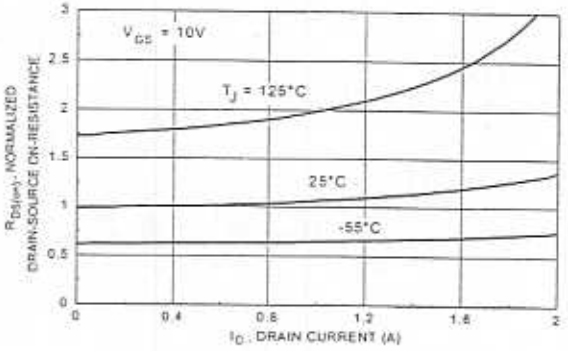

Figure 4. On-Resistance Variation with Drain Current and Temperature

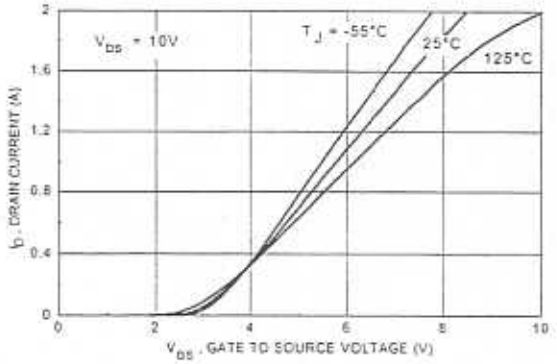

Figure 5. Transfer Characteristics

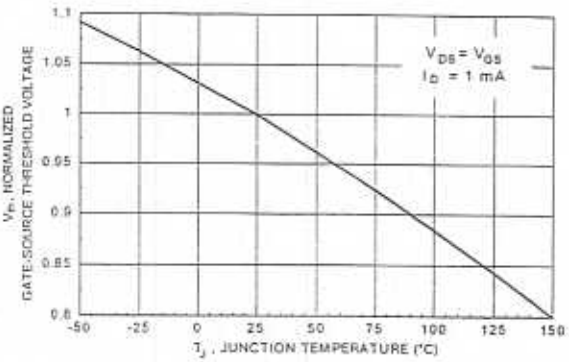

Figure 6. Gate Threshold Variation with Temperature

Typical Electrical Characteristics (continued)

2N7000 / 2N7002 /NDS7002A

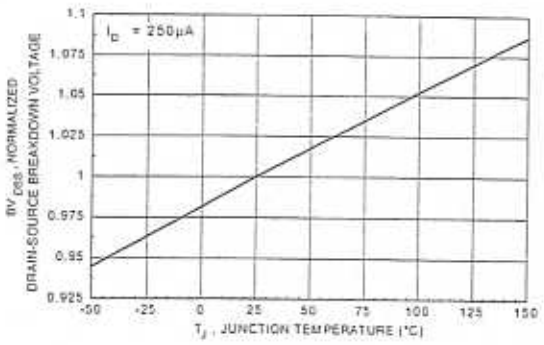

Figure 7. Breakdown Voltage Variation with Temperature

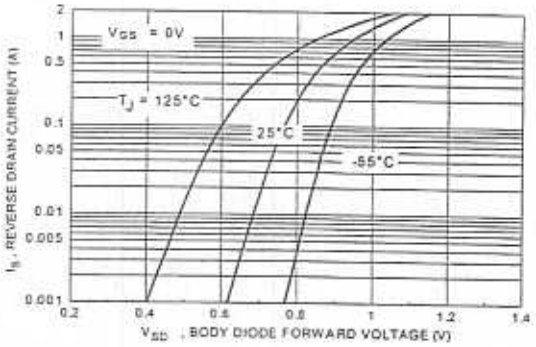

Figure 8. Body Diode Forward Voltage Variation with

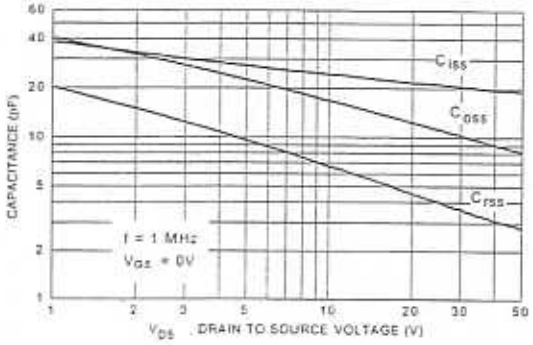

Figure 9. Capacitance Characteristics

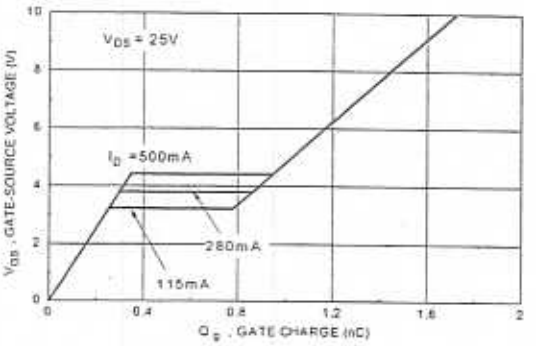

Figure 10. Gate Charge Characteristics

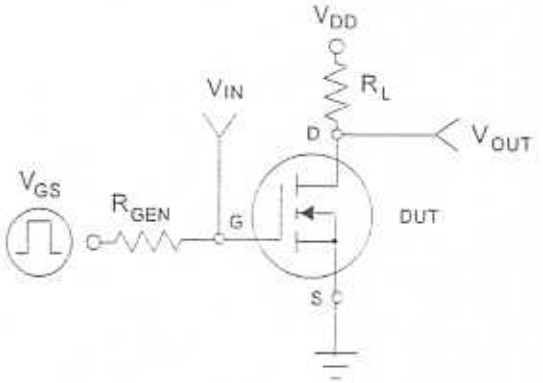

Figure 11.

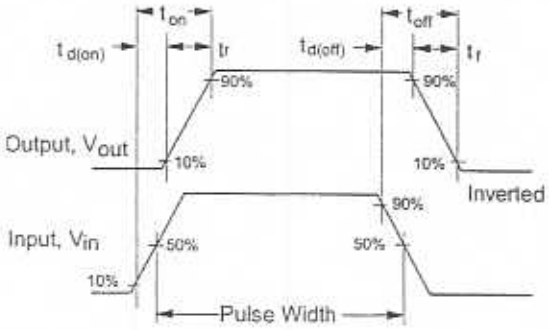

Figure 12. Switching Waveforms

Typical Electrical Characteristics (continued)

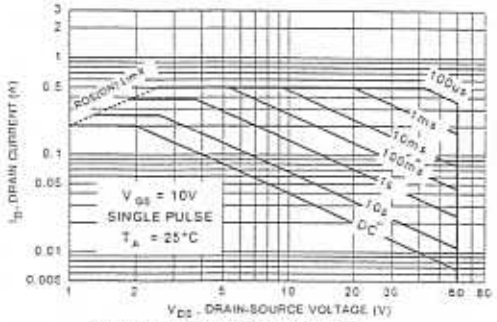

Figure 13. 2N7000 Maximum Safe Operating Area

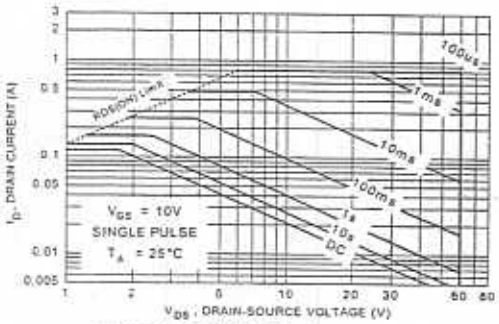

Figure 14. 2N7002 Maximum Safe Operating Area

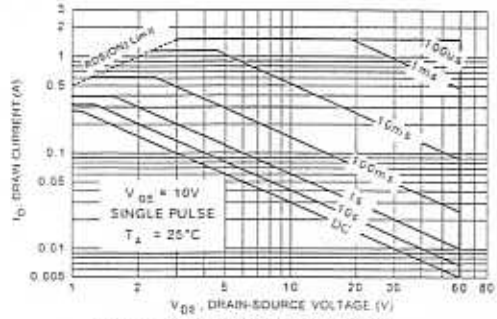

Figure 15. NDS7000A Maximum Safe Operating Area

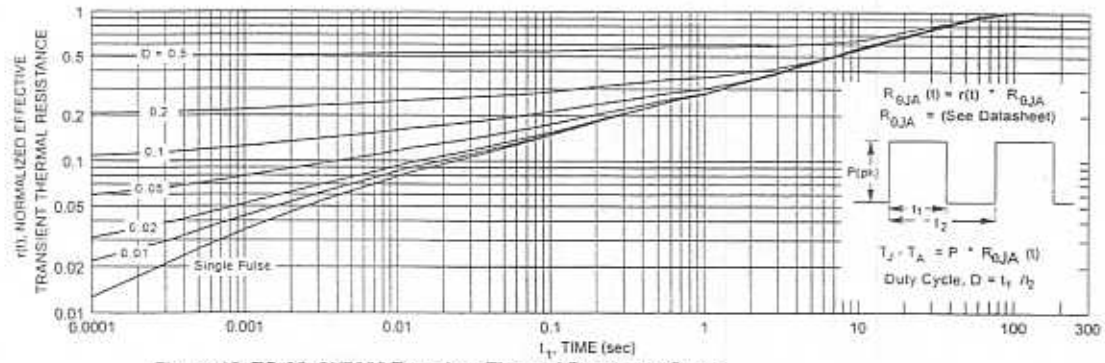

Figure 16. TO-92, 2N7000 Transient Thermal Response Curve

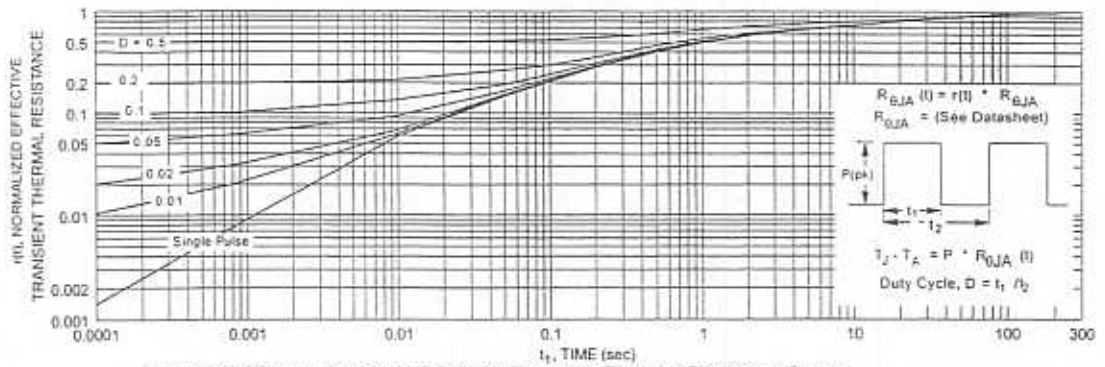

Figure 17. SOT-23, 2N7002 / NDS7002A Transient Thermal Response Curve