Due: 2-19-2015, 5:00PM

Homeworks will not be received after due.

Instructor: Sam Palermo

Solve the following problems from the Sedra/Smith text:

2.65, 2.78, 2.86, 2.92, 2.111, 2.117, 2.125

Simulate 2.111 in PSpice using the ua741 model.
### Section 2.4: Difference Amplifiers

2.59 Figure P2.59 shows a circuit that provides an output voltage $v_o$ whose value can be varied by turning the wiper of the 100-kΩ potentiometer. Find the range over which $v_o$ can be varied. If the potentiometer is a “20-turn” device, find the change in $v_o$ corresponding to each turn of the pot.

<table>
<thead>
<tr>
<th>Case</th>
<th>$G_0$ (V/V)</th>
<th>$A$ (V/V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>a</td>
<td>-1</td>
<td>10</td>
</tr>
<tr>
<td>b</td>
<td>+1</td>
<td>10</td>
</tr>
<tr>
<td>c</td>
<td>-1</td>
<td>100</td>
</tr>
<tr>
<td>d</td>
<td>+10</td>
<td>10</td>
</tr>
<tr>
<td>e</td>
<td>-10</td>
<td>100</td>
</tr>
<tr>
<td>f</td>
<td>-10</td>
<td>1000</td>
</tr>
<tr>
<td>g</td>
<td>+1</td>
<td>2</td>
</tr>
</tbody>
</table>

(a) 1 V/V  
(b) 5 V/V  
(c) 100 V/V  
(d) 0.5 V/V

2.62 For the circuit shown in Fig. P2.62, express $v_o$ as a function of $v_1$ and $v_2$. What is the input resistance seen by $v_1$ alone? By $v_2$ alone? By a source connected between the two input terminals? By a source connected to both input terminals simultaneously?

![Figure P2.62](image)

2.63 Consider the difference amplifier of Fig. 2.16 with the two input terminals connected together to an input common-mode signal source. For $R_2/R_1 = R_3/R_2$, show that the input common-mode resistance is $(R_3 + R_1)/(R_1 + R_2)$.

2.64 Consider the circuit of Fig. 2.16, and let each of the $v_1$ and $v_2$ signal sources have a series resistance $R_s$. What condition must apply in addition to the condition in Eq. (2.15) in order for the amplifier to function as an ideal difference amplifier?

2.65 For the difference amplifier shown in Fig. P2.62, let all the resistors be 10 kΩ ± 5%. Find an expression for the worst-case common-mode gain that results. Evaluate this for $x = 0.1, 1$, and 5. Also, evaluate the resulting CMRR in each case. Neglect the effect of resistor tolerances on $A_v$.

2.66 For the difference amplifier of Fig. 2.16, show that if each resistor has a tolerance of ±100ε% (i.e., for, say, a 5% resistor, $ε = 0.05$) then the worst-case CMRR is given approximately by

\[
\text{CMRR} \approx 20 \log \left( \frac{K + 1}{4ε} \right)
\]

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* = difficult problem; ** = more difficult; *** = very challenging; D = design problem
(a) Assuming ideal op amps, sketch the voltage waveforms at nodes B and C for a 1-V peak-to-peak sine wave applied at A. Also sketch $v_o$.

(b) What is the voltage gain $v_o/v_i$?

(c) Assuming that the op amps operate from ±15-V power supplies and that their output saturates at ±14 V (in the manner shown in Fig. 1.14), what is the largest sine-wave output that can be accommodated? Specify both its peak-to-peak and rms values.

*2.78 The two circuits in Fig. P2.78 are intended to function as voltage-to-current converters; that is, they supply the load impedance $Z_L$ with a current proportional to $v_i$ and independent of the value of $Z_L$. Show that this is indeed the case, and find for each circuit $i_o$ as a function of $v_i$. Comment on the differences between the two circuits.

Section 2.5: Integrators and Differentiators

2.79 A Miller integrator incorporates an ideal op amp, a resistor $R$ of 10 kΩ, and a capacitor $C$ of 1 nF. A sine-wave signal is applied to its input.

(a) At what frequency (in Hz) are the input and output signals equal in amplitude?

(b) At that frequency, how does the phase of the output sine wave relate to that of the input?

(c) If the frequency is lowered by a factor of 10 from that found in (a), by what factor does the output voltage change, and in what direction (smaller or larger)?

(d) What is the phase relation between the input and output in situation (c)?

D 2.80 Design a Miller integrator with a time constant of 1 s and an input resistance of 100 kΩ. A dc voltage of −1 volt is applied at the input at time 0, at which moment $v_o = -10$ V. How long does it take the output to reach 0 V? +10 V?

2.81 An op-amp-based inverting integrator is measured at 10 kHz to have a voltage gain of −100 V/V. At what frequency is its gain reduced to −1 V/V? What is the integrator time constant?

D 2.82 Design a Miller integrator that has a unity-gain frequency of 10 krad/s and an input resistance of 100 kΩ. Sketch the output you would expect for the situation in which, with output initially at 0 V, a 2-V, 100-μs pulse is applied to the input. Characterize the output that results when a sine wave $2 \sin 10^6t$ is applied to the input.

D 2.83 Design a Miller integrator whose input resistance is 10 kΩ and unity-gain frequency is 100 kHz. What components are needed? For long-term stability, a feedback resistor is introduced across the capacitor to limit the dc gain.
to 40 dB. What is its value? What is the associated lower 3-dB frequency? Sketch and label the output that results with a 10-μs, 1-V positive-input pulse (initially at 0 V) with (a) no dc stabilization (but with the output initially at 0 V) and (b) the feedback resistor connected.

*2.84 A Miller integrator whose input and output voltages are initially zero and whose time constant is 1 ms is driven by the signal shown in Fig. P2.84. Sketch and label the output waveform that results. Indicate what happens if the input levels are ±2 V, with the time constant the same (1 ms) and with the time constant raised to 2 ms.

![Figure P2.84](image)

2.85 Consider a Miller integrator having a time constant of 1 ms and an output that is initially zero, when fed with a string of pulses of 10-μs duration and 1-V amplitude rising from 0 V (see Fig. P2.85). Sketch and label the output waveform resulting. How many pulses are required for an output voltage change of 1 V?

![Figure P2.85](image)

*2.86 Figure P2.86 shows a circuit that performs a low-pass STC function. Such a circuit is known as a first-order, low-pass active filter. Derive the transfer function and show that the dc gain is \((-R_f/R_1)\) and the 3-dB frequency \(\omega_b = 1/CR_1\). Design the circuit to obtain an input resistance of 10 kΩ, a dc gain of 40 dB, and a 3-dB frequency of 1 kHz. At what frequency does the magnitude of the transfer function reduce to unity?

![Figure P2.86](image)

*2.87 Show that a Miller integrator implemented with an op amp with open-loop gain \(A_o\) has a low-pass STC transfer function. What is the pole frequency of the STC function? How does this compare with the pole frequency of the ideal integrator? If an ideal Miller integrator is fed with a -1-V pulse signal with a width \(T = CR\), what will the output voltage be at \(t = T\)? Assume that at \(t = 0, V_o = 0\). Repeat for an integrator with an op amp having \(A_o = 1000\).

2.88 A differentiator utilizes an ideal op amp, a 10-kΩ resistor, and a 1-nF capacitor. What is the frequency \(f_o\) (in Hz) at which its input and output sine-wave signals have equal magnitude? What is the output signal for a 1-V peak-to-peak sine-wave input with frequency equal to \(10f_o\)?

2.89 An op-amp differentiator with 1-ms time constant is driven by the rate-controlled step shown in Fig. P2.89. Assuming \(V_o\) to be zero initially, sketch and label its waveform.

![Figure P2.88](image)

\(\text{Note: } \text{Multisim/PSpice; } * = \text{difficult problem; } ** = \text{more difficult; } *** = \text{very challenging; D = design problem}\)
2.90 An op-amp differentiator, employing the circuit shown in Fig. 2.27(a), has \( R = 20 \, \text{k}\Omega \) and \( C = 0.1 \, \mu\text{F} \). When a triangle wave of \( \pm 1 \, \text{V} \) peak amplitude at 1 kHz is applied to the input, what form of output results? What is its frequency? What is its peak amplitude? What is its average value? What value of \( R \) is needed to cause the output to have a 12-V peak amplitude?

2.91 Use an ideal op amp to design a differentiation circuit for which the time constant is \( 10^{-3} \, \text{s} \) using a 10-nF capacitor. What are the gains and phase shifts found for this circuit at one-tenth and 10 times the unity-gain frequency? A series input resistor is added to limit the gain magnitude at high frequencies to 100 V/V. What is the associated 3-dB frequency? What gain and phase shift result at 10 times the unity-gain frequency?

D 2.92 Figure P2.92 shows a circuit that performs the high-pass, single-time-constant function. Such a circuit is known as a first-order high-pass active filter. Derive the transfer function and show that the high-frequency gain is \((-R_2/R_1)\) and the 3-dB frequency \( \omega_2 = 1/CR_1 \). Design the circuit to obtain a high-frequency input resistance of 1 k\(\Omega\), a high-frequency gain of 40 dB, and a 3-dB frequency of 2 kHz. At what frequency does the magnitude of the transfer function reduce to unity?

Figure P2.92

D **2.93** Derive the transfer function of the circuit in Fig. P2.93 (for an ideal op amp) and show that it can be written in the form

\[
\frac{V_o}{V_i} = \frac{-R_2/R_1}{1 + (\omega_2/\omega_1)(1 + j(\omega_2/\omega_1))}
\]

where \( \omega_1 = 1/C_1R_1 \) and \( \omega_2 = 1/C_3R_2 \). Assuming that the circuit is designed such that \( \omega_2 \gg \omega_1 \), find approximate expressions for the transfer function in the following frequency regions:

1. \( \omega \ll \omega_1 \)
2. \( \omega_1 \ll \omega \ll \omega_2 \)
3. \( \omega \gg \omega_2 \)

Figure P2.93

Use these approximations to sketch a Bode plot for the magnitude response. Observe that the circuit performs as an amplifier whose gain rolls off at the low-frequency end in the manner of a high-pass STC network, and at the high-frequency end in the manner of a low-pass STC network. Design the circuit to provide a gain of 40 dB in the “middle-frequency range,” a low-frequency 3-dB point at 200 Hz, a high-frequency 3-dB point at 200 kHz, and an input resistance (at \( \omega \gg \omega_1 \)) of 2 k\(\Omega\).

Section 2.6: DC Imperfections

2.94 An op amp wired in the inverting configuration with the input grounded, having \( R_2 = 100 \, \text{k}\Omega \) and \( R_1 = 2 \, \text{k}\Omega \), has an output dc voltage of \(-0.2 \, \text{V}\). If the input bias current is known to be very small, find the input offset voltage.

2.95 A noninverting amplifier with a gain of 100 uses an op amp having an input offset voltage of \( \pm 2 \, \text{mV} \). Find the output when the input is \( 0.01 \sin \omega t \), volts.

2.96 A noninverting amplifier with a closed-loop gain of 1000 is designed using an op amp having an input offset voltage of 3 mV and output saturation levels of \( \pm 12 \, \text{V} \). What is the maximum amplitude of the sine wave that can be applied at the input without the output clipping? If the amplifier is
can be as large as 1 mV of unknown polarity, what range of offset current is possible?

2.106 A Miller integrator with \( R = 10 \text{ k\Omega} \) and \( C = 10 \text{ nF} \) is implemented by using an op amp with \( V_{OS} = 2 \text{ mV} \), \( I_{P} = 0.1 \mu\text{A} \), and \( I_{OS} = 20 \text{ nA} \). To provide a finite dc gain, a 1-M\( \Omega \) resistor is connected across the capacitor.

(a) To compensate for the effect of \( I_{P} \), a resistor is connected in series with the positive-input terminal of the op amp. What should its value be?
(b) With the resistor of (a) in place, find the worst-case dc output voltage of the integrator when the input is grounded.

Section 2.7: Effect of Finite Open-Loop Gain and Bandwidth on Circuit Performance

2.107 The data in the following table apply to internally compensated op amps. Fill in the blank entries.

<table>
<thead>
<tr>
<th>( A_0 )</th>
<th>( f_b ) (Hz)</th>
<th>( f_r ) (Hz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>( 10^2 )</td>
<td>( 10^2 )</td>
<td>( 10^4 )</td>
</tr>
<tr>
<td>( 10^3 )</td>
<td>( 10^3 )</td>
<td>( 10^6 )</td>
</tr>
<tr>
<td>( 2 \times 10^3 )</td>
<td>( 10^{-1} )</td>
<td>( 10^6 )</td>
</tr>
<tr>
<td>( 10 )</td>
<td>( 10 )</td>
<td>( 10^6 )</td>
</tr>
</tbody>
</table>

2.108 A measurement of the open-loop gain of an internally compensated op amp at very low frequencies shows it to be 98 dB; at 100 kHz, this shows it is 40 dB. Estimate values for \( A_0, f_b \), and \( f_r \).

2.109 Measurements of the open-loop gain of a compensated op amp intended for high-frequency operation indicate that the gain is \( 4 \times 10^3 \) at 100 kHz and \( 20 \times 10^3 \) at 10 kHz. Estimate its 3-dB frequency, its unity-gain frequency, and its dc gain.

2.110 Measurements made on the internally compensated amplifiers listed below provide the dc gain and the frequency at which the gain has dropped by 20 dB. For each, what are the 3 dB and unity-gain frequencies?
(a) \( 2 \times 10^3 \text{ V/V} \) and \( 5 \times 10^2 \text{ Hz} \)
(b) \( 20 \times 10^3 \text{ V/V} \) and 10 Hz
(c) \( 1800 \text{ V/V} \) and 0.1 MHz
(d) \( 100 \text{ V/V} \) and 0.1 GHz
(e) \( 25 \text{ V/mV} \) and 250 kHz

2.111 An inverting amplifier with nominal gain of \(-50 \text{ V/V} \) employs an op amp having a dc gain of \( 10^3 \) and a unity-gain frequency of \( 10^4 \text{ Hz} \). What is the 3-dB frequency of the closed-loop amplifier? What is its gain at 0.1\( f_{os} \) and at 10\( f_{os} \)?

2.112 A particular op amp, characterized by a gain-bandwidth product of 20 MHz, is operated with a closed-loop gain of \(+100 \text{ V/V} \). What 3-dB bandwidth results? At what frequency does the closed-loop amplifier exhibit a \(-6^\circ \) phase shift? A \(-84^\circ \) phase shift?

2.113 Find the \( f_r \) required for internally compensated op amps to be used in the implementation of closed-loop amplifiers with the following nominal dc gains and 3-dB bandwidths:
(a) \(-50 \text{ V/V} \); 100 kHz
(b) \(+50 \text{ V/V} \); 100 kHz
(c) \(+2 \text{ V/V} \); 5 MHz
(d) \(-2 \text{ V/V} \); 5 MHz
(e) \(-1000 \text{ V/V} \); 10 kHz
(f) \(+1 \text{ V/V} \); 1 MHz
(g) \(-1 \text{ V/V} \); 1 MHz

2.114 A noninverting op-amp circuit with a gain of 96 \( \text{ V/V} \) is found to have a 3-dB frequency of 8 kHz. For a particular system application, a bandwidth of 32 kHz is required. What is the highest gain available under these conditions?

2.115 Consider a unity-gain follower utilizing an internally compensated op amp with \( f_r = 2 \text{ MHz} \). What is the 3-dB frequency of the follower? At what frequency is the gain of the follower 1% below its low-frequency magnitude? If the input to the follower is a 1-V step, find the 10% to 90% rise time of the output voltage. (Note: The step response of STC low-pass networks is discussed in Appendix E. Specifically, note that the 10%–90% rise time of a low-pass STC circuit with a time constant \( r \) is \( 2.2r \)).

D 2.116 It is required to design a noninverting amplifier with a dc gain of 10. When a step voltage of 100 mV is applied at the input, it is required that the output be within 1% of its final value of 1 V in at most 200 ns. What must the \( f_r \) of the op amp be? (Note: The step response of STC low-pass networks is discussed in Appendix E.)

D 2.117 This problem illustrates the use of cascaded closed-loop amplifiers to obtain an overall bandwidth greater than can be achieved using a single-stage amplifier with the same overall gain.
(a) Show that cascading two identical amplifier stages, each having a low-pass STC frequency response with a 3-dB frequency \( f_f \), results in an overall amplifier with a 3-dB frequency given by

\[
\text{\( f_{\text{3dB}} = \sqrt{2-1f_f} \)}
\]

(b) It is required to design a noninverting amplifier with a dc gain of 40 dB utilizing a single internally compensated op amp with \( f_f = 2 \text{ MHz} \). What is the 3-dB frequency obtained?

(c) Redesign the amplifier of (b) by cascading two identical noninverting amplifiers each with a dc gain of 20 dB. What is the 3-dB frequency of the overall amplifier? Compare this to the value obtained in (b) above.

D **2.118** A designer, wanting to achieve a stable gain of 100 V/V at 5 MHz, considers her choice of amplifier topologies. What unity-gain frequency would a single operational amplifier require to satisfy her need? Unfortunately, the best available amplifier has an \( f_f \) of 40 MHz. How many such amplifiers connected in a cascade of identical noninverting stages would she need to achieve her goal? What is the 3-dB frequency of each stage she can use? What is the overall 3-dB frequency?

2.119 Consider the use of an op amp with a unity-gain frequency, \( f_f \), in the realization of:

(a) An inverting amplifier with dc gain of magnitude \( K \).

(b) A noninverting amplifier with a dc gain of \( K \).

In each case find the 3-dB frequency and the gain–bandwidth product (GBP \( = \text{Gain} \times f_{\text{3dB}} \)). Comment on the results.

42.120 Consider an inverting summer with two inputs \( V_1 \) and \( V_2 \) and with \( V_c = -(V_1 + 3V_2) \). Find the 3-dB frequency of each of the gain functions \( V_c/V_1 \) and \( V_c/V_2 \) in terms of the op amp \( f_f \). \( \text{(Hint: In each case, the other input to the summer can be set to zero—an application of superposition.)} \)

Section 2.8: Large-Signal Operation of Op Amps

2.121 A particular op amp using \( \pm 15 \text{ V} \) supplies operates linearly for outputs in the range \(-14 \text{ V} \) to \(+14 \text{ V} \). If used in an inverting amplifier configuration of gain \(-100 \), what is the rms value of the largest possible sine wave that can be applied at the input without output clipping?

2.122 Consider an op amp connected in the inverting configuration to realize a closed-loop gain of \(-100 \text{ V/V} \) utilizing resistors of 1 k\( \Omega \) and 100 k\( \Omega \). A load resistance \( R_L \) is connected from the output to ground, and a low-frequency sine-wave signal of peak amplitude \( V_p \) is applied to the input. Let the op amp be ideal except that its output voltage saturates at \( \pm 10 \text{ V} \) and its output current is limited to the range \( \pm 20 \text{ mA} \).

(a) For \( R_L = 1 \text{ k} \Omega \), what is the maximum possible value of \( V_p \) while an undistorted output sinusoid is obtained?

(b) Repeat (a) for \( R_L = 200 \Omega \).

(c) If it is desired to obtain an output sinusoid of 10-V peak amplitude, what minimum value of \( R_L \) is allowed?

2.123 An op amp having a slew rate of 10 V/\( \mu \text{s} \) is to be used in the unity-gain follower configuration, with input pulses that rise from 0 to 2 V. What is the shortest pulse that can be used while ensuring full-amplitude output? For such a pulse, describe the output resulting.

2.124 For operation with 10-V output pulses with the requirement that the sum of the rise and fall times represent only 20\% of the pulse width (at half-amplitude), what is the slew-rate requirement for an op amp to handle pulses 2 \( \mu \text{s} \) wide? \( \text{(Note: The rise and fall times of a pulse signal are usually measured between the 10\%- and 90\%-height points.)} \)

2.125 What is the highest frequency of a triangle wave of 10-V peak-to-peak amplitude that can be reproduced by an op amp whose slew rate is 20 V/\( \mu \text{s} \)? For a sine wave of the same frequency, what is the maximum amplitude of output signal that remains undistorted?

2.126 For an amplifier having a slew rate of 40 V/\( \mu \text{s} \), what is the highest frequency at which a 20-V peak-to-peak sine wave can be produced at the output?

D **2.127** In designing with op amps one has to check the limitations on the voltage and frequency ranges of operation of the closed-loop amplifier, imposed by the op-amp finite bandwidth (\( f_f \)), slew rate (SR), and output saturation (\( V_{\text{sat}} \)). This problem illustrates the point by considering the use of an op amp with \( f_f = 20 \text{ MHz} \), SR = 10 V/\( \mu \text{s} \), and \( V_{\text{sat}} = 10 \text{ V} \) in the design of a noninverting amplifier with a nominal gain of 10. Assume a sine-wave input with peak amplitude \( V_i \).

(a) If \( V_i = 0.5 \text{ V} \), what is the maximum frequency before the output distorts?

(b) If \( f = 200 \text{ kHz} \), what is the maximum value of \( V_i \) before the output distorts?

(c) If \( V_i = 50 \text{ mV} \), what is the useful frequency range of operation?

(d) If \( f = 50 \text{ kHz} \), what is the useful input voltage range?

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**Notes:**
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