

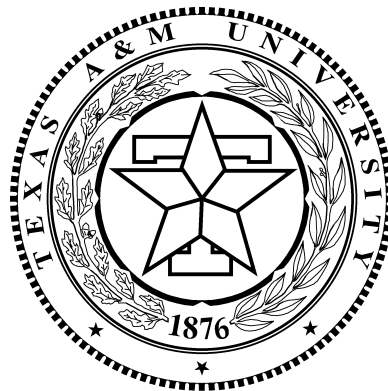
ECEN 325

Electronics

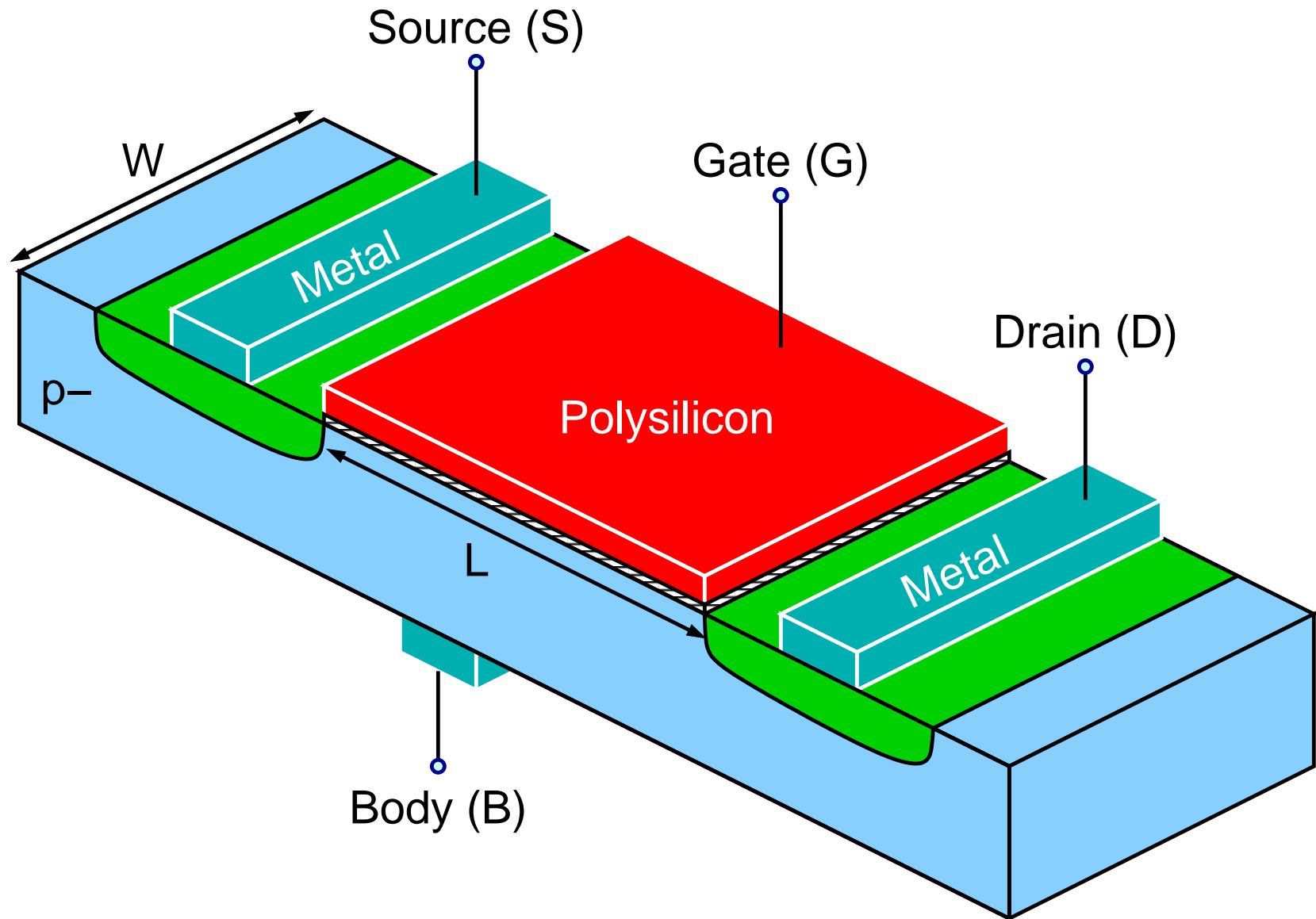
MOS Field-Effect Transistors

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Texas A&M University
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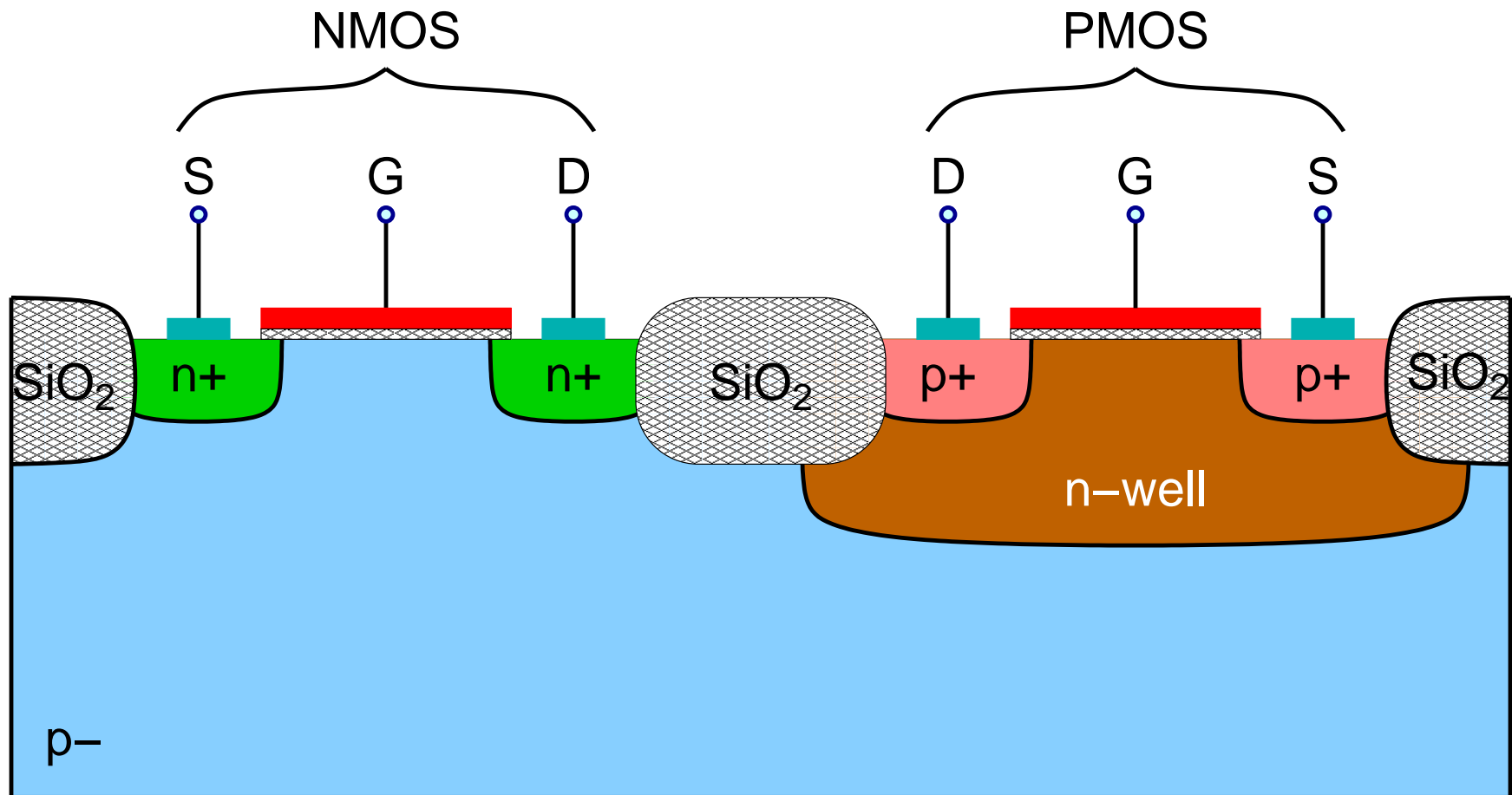


NMOS Physical Structure



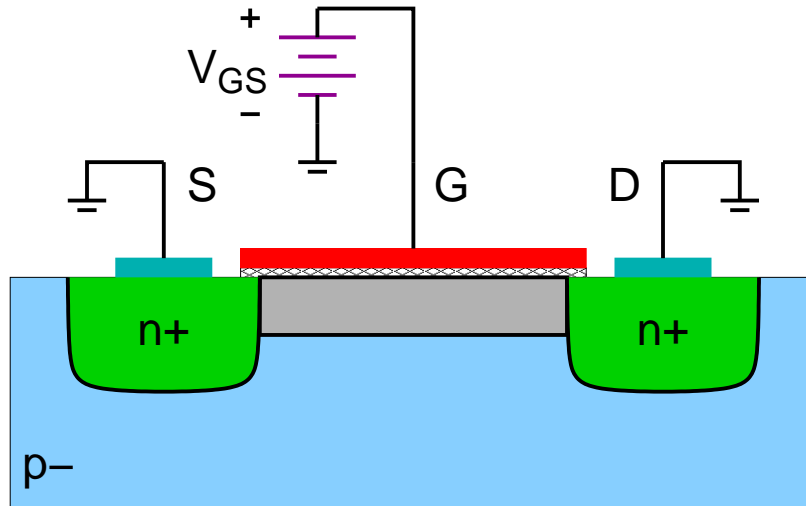
CMOS Physical Structure

Cross-section



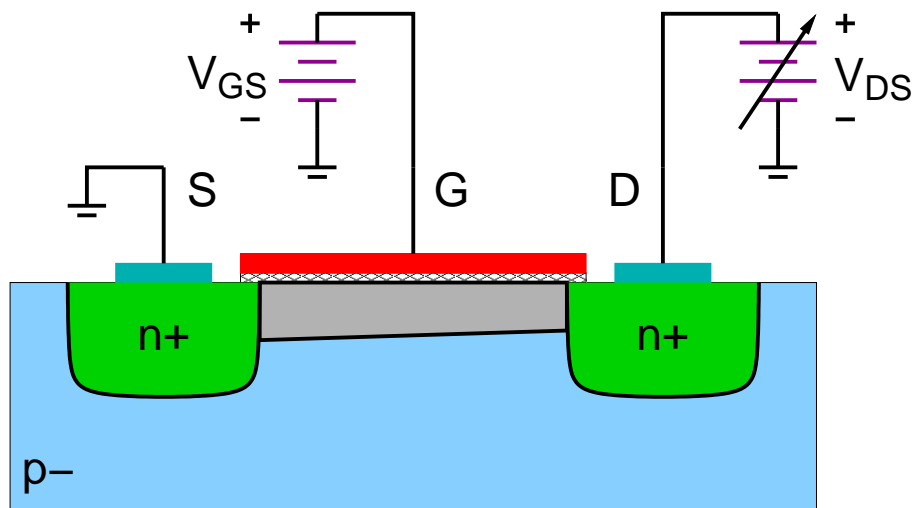
Physical Operation

NMOS



$$V_{GS} > V_{tn}$$

$$V_{DS} = 0$$

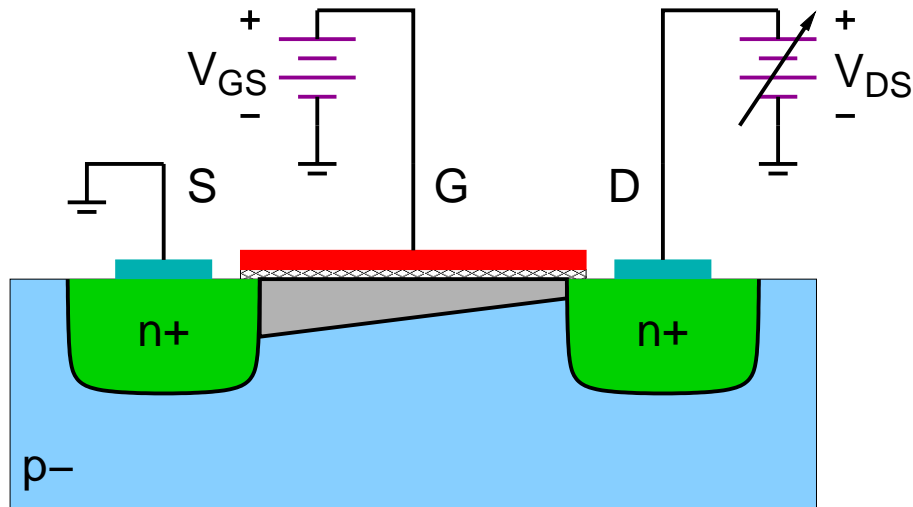


$$V_{GS} > V_{tn}$$

$$V_{DS} : \text{very small}$$

Physical Operation

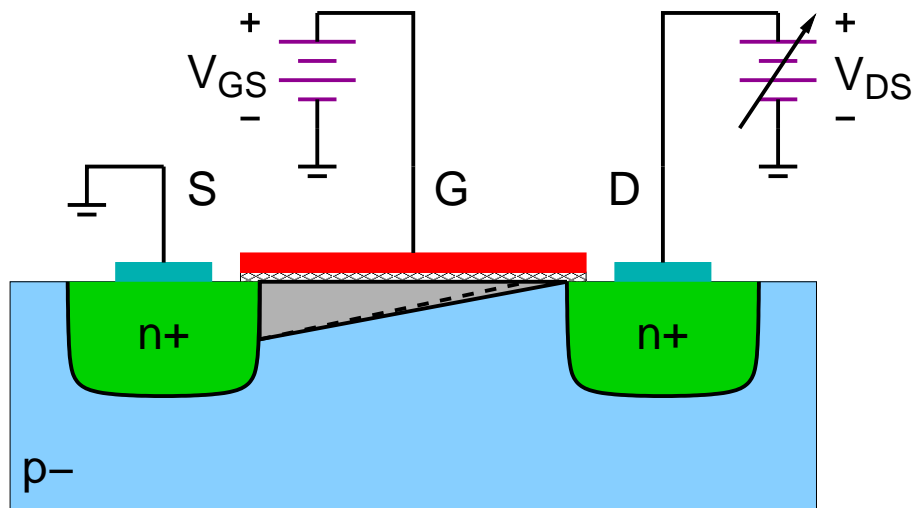
NMOS



$$V_{GS} > V_{tn}$$

$$V_{DS} < V_{ov}$$

$$V_{ov} = V_{GS} - V_{tn}$$



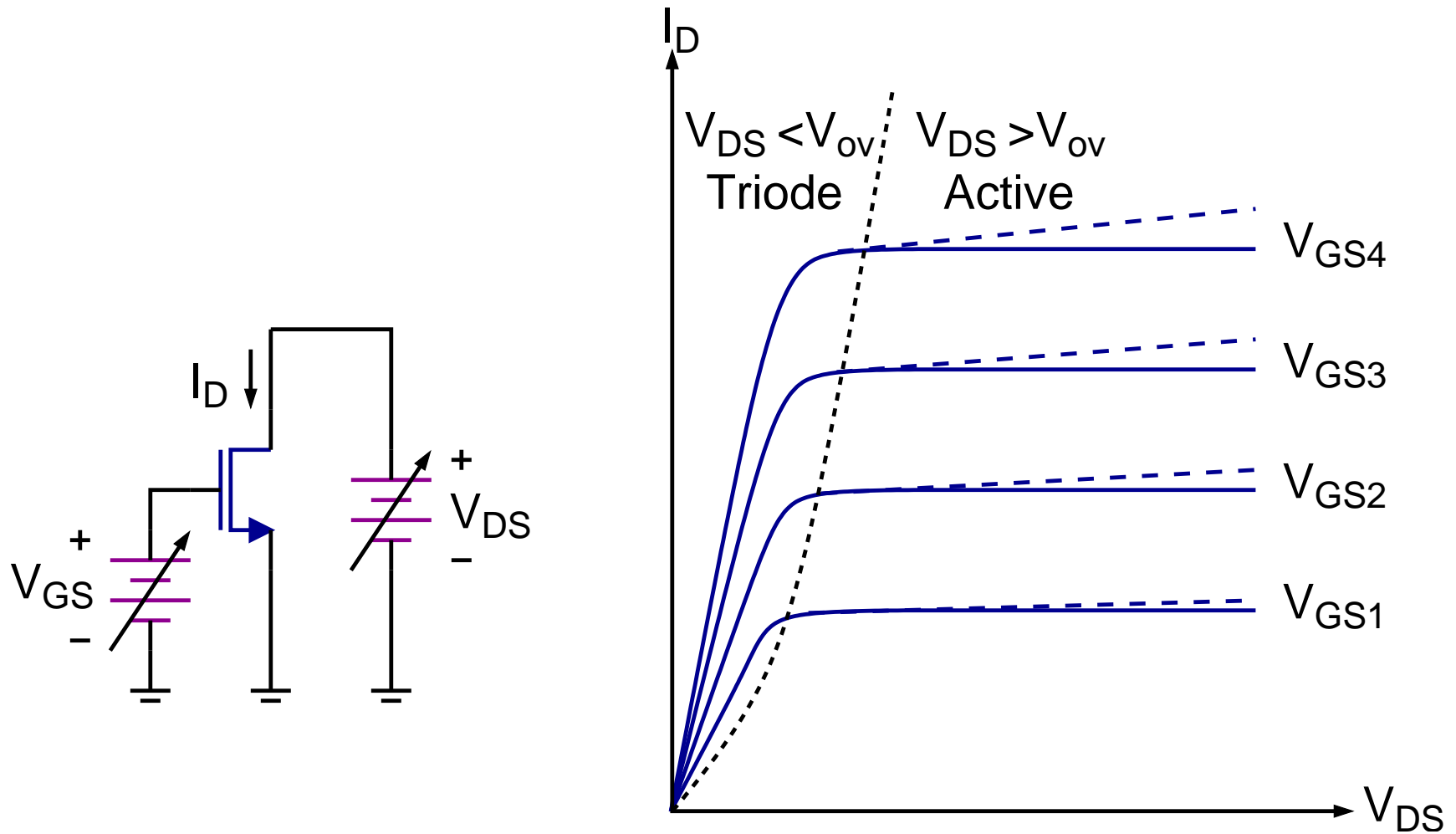
$$V_{GS} > V_{tn}$$

$$V_{DS} > V_{ov}$$

$$V_{ov} = V_{GS} - V_{tn}$$

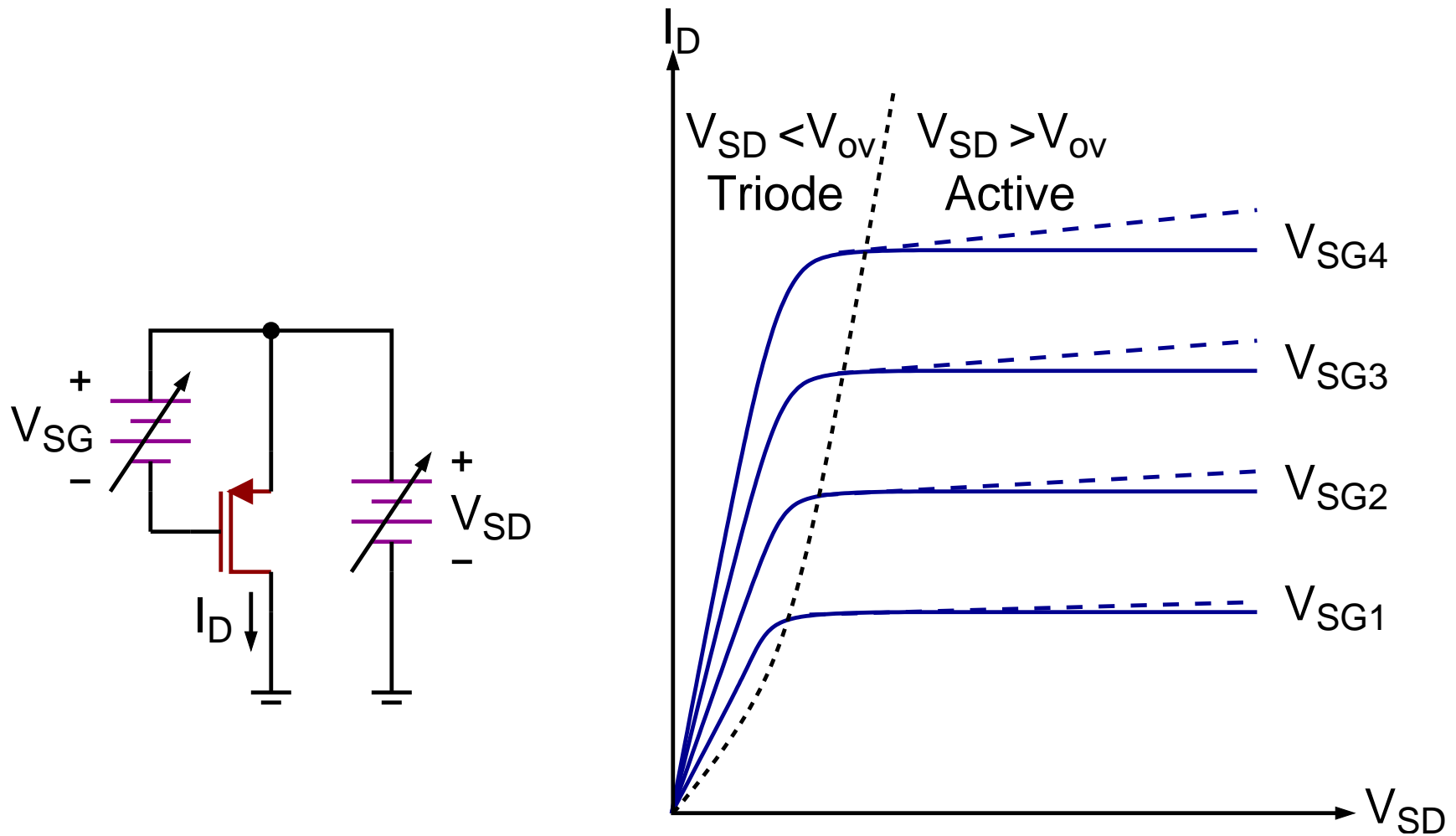
I_D - V_{DS} Characteristics

NMOS

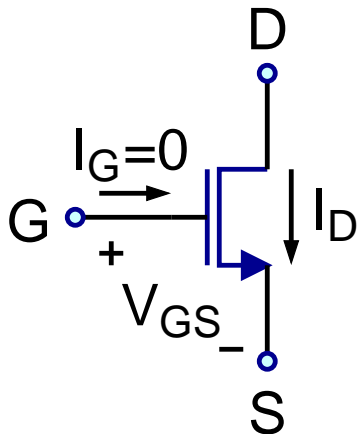


I_D - V_{SD} Characteristics

PMOS



NMOS DC Operation



$$V_{ov} = V_{GS} - V_{tn}$$

- Cutoff: $V_{GS} < V_{tn}$, $I_D = 0$

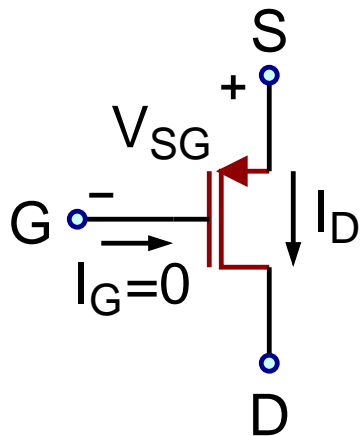
- Triode (linear) region: $V_{DS} < V_{ov}$

$$I_D = k'_n \frac{W}{L} \left(V_{ov} V_{DS} - \frac{V_{DS}^2}{2} \right)$$

- Active (saturation) region: $V_{DS} > V_{ov}$

$$I_D = \frac{k'_n}{2} \frac{W}{L} V_{ov}^2$$

PMOS DC Operation



- Cutoff: $V_{SG} < |V_{tp}|$, $I_D = 0$

- Triode (linear) region: $V_{SD} < V_{ov}$

$$I_D = k'_p \frac{W}{L} \left(V_{ov} V_{SD} - \frac{V_{SD}^2}{2} \right)$$

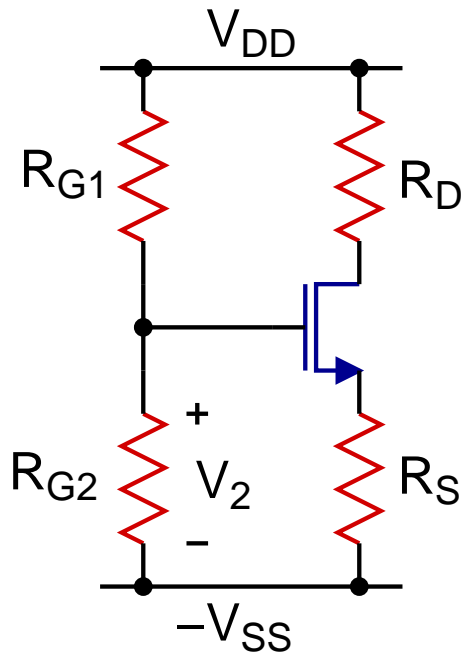
$$V_{ov} = V_{SG} - |V_{tp}|$$

- Active (saturation) region: $V_{SD} > V_{ov}$

$$I_D = \frac{k'_p}{2} \frac{W}{L} V_{ov}^2$$

MOSFET DC Biasing

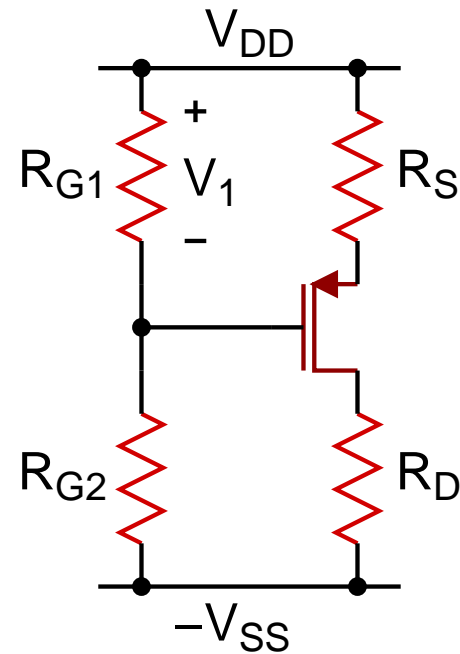
Resistive



$$V_2 = \frac{R_{G2}(V_{DD} + V_{SS})}{R_{G1} + R_{G2}}$$

$$V_2 = V_{GSn} + R_S I_{Dn}$$

$$I_{Dn} = \frac{k'_n W}{2 L} (V_{GSn} - V_{tn})^2$$



$$V_1 = \frac{R_{G1}(V_{DD} + V_{SS})}{R_{G1} + R_{G2}}$$

$$V_1 = V_{SGp} + R_S I_{Dp}$$

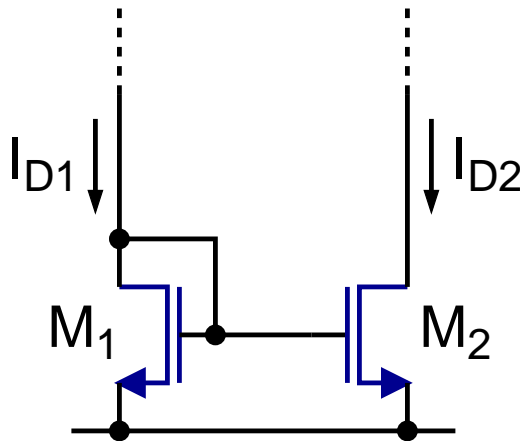
$$I_{Dp} = \frac{k'_p W}{2 L} (V_{SGp} - V_{tp})^2$$

Assuming $V_{GS1} > V_{tn}$

$$V_{GS1} = V_{DS1} \Rightarrow V_{DS1} > V_{GS1} - V_{tn}$$

$\Rightarrow M_1$ is ACTIVE

$$\Rightarrow I_{D1} = \frac{k'_n}{2} \left(\frac{W}{L}\right)_1 (V_{GS1} - V_{tn})^2$$



Assuming M_2 is ACTIVE

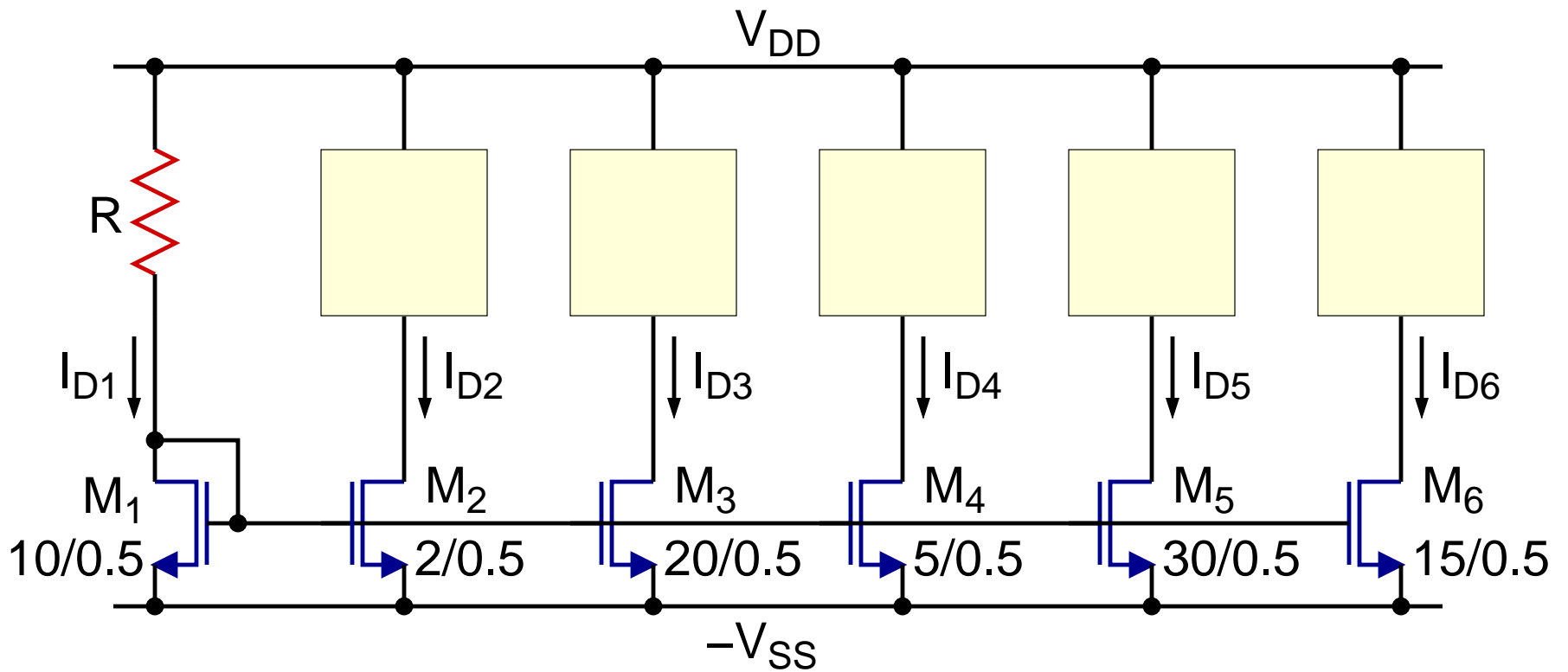
$$I_{D2} = \frac{k'_n}{2} \left(\frac{W}{L}\right)_2 (V_{GS2} - V_{tn})^2$$

Since $V_{GS1} = V_{GS2}$

$$\frac{I_{D1}}{I_{D2}} = \frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_2}$$

NMOS Current Mirror

Example

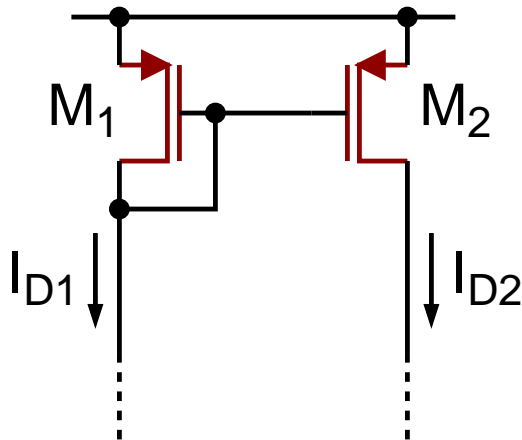


$$\left. \begin{aligned} V_{DD} + V_{SS} &= R_1 I_{D1} + V_{GS1} \\ I_{D1} &= \frac{k'_n}{2} \frac{10}{0.5} (V_{GS1} - V_{tn})^2 \end{aligned} \right\} \Rightarrow \text{Find } I_{D1}$$

Assuming that all transistors are ACTIVE:

$$I_{D2} = \frac{I_{D1}}{5} \quad I_{D3} = 2I_{D1} \quad I_{D4} = \frac{I_{D1}}{2}$$

$$I_{D5} = 3I_{D1} \quad I_{D6} = \frac{3}{2}I_{D1}$$



Assuming $V_{SG1} > |V_{tp}|$

$$V_{SG1} = V_{SD1} \Rightarrow V_{SD1} > V_{SG1} - |V_{tp}|$$

$\Rightarrow M_1$ is ACTIVE

$$\Rightarrow I_{D1} = \frac{k'_p}{2} \left(\frac{W}{L} \right)_1 (V_{SG1} - |V_{tp}|)^2$$

Assuming M_2 is ACTIVE

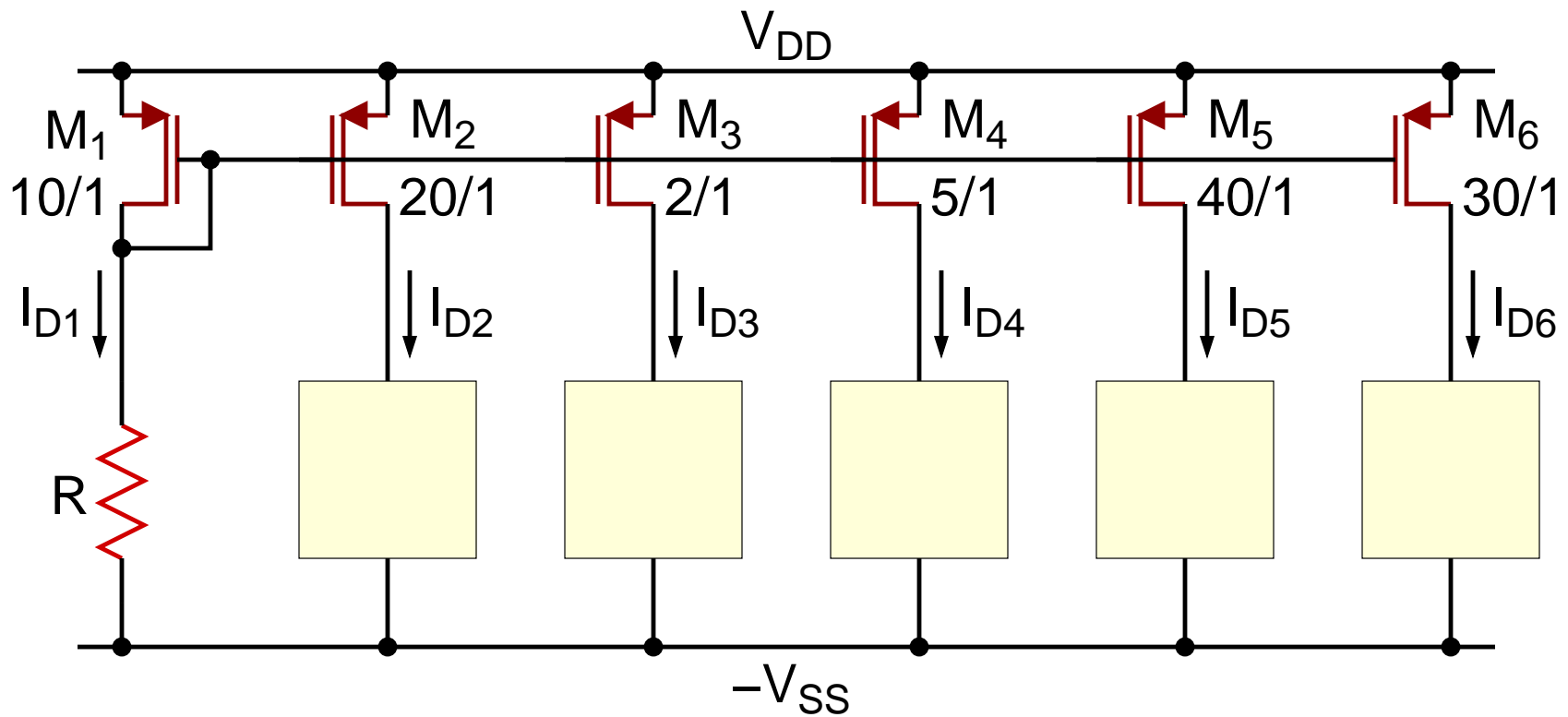
$$I_{D2} = \frac{k'_p}{2} \left(\frac{W}{L} \right)_2 (V_{SG2} - |V_{tp}|)^2$$

Since $V_{SG1} = V_{SG2}$

$$\frac{I_{D1}}{I_{D2}} = \frac{\left(\frac{W}{L} \right)_1}{\left(\frac{W}{L} \right)_2}$$

PMOS Current Mirror

Example



$$\left. \begin{aligned} V_{DD} + V_{SS} &= R_1 I_{D1} + V_{SG1} \\ I_{D1} &= \frac{k'_p}{2} \frac{10}{1} (V_{SG1} - |V_{tp}|)^2 \end{aligned} \right\} \Rightarrow \text{Find } I_{D1}$$

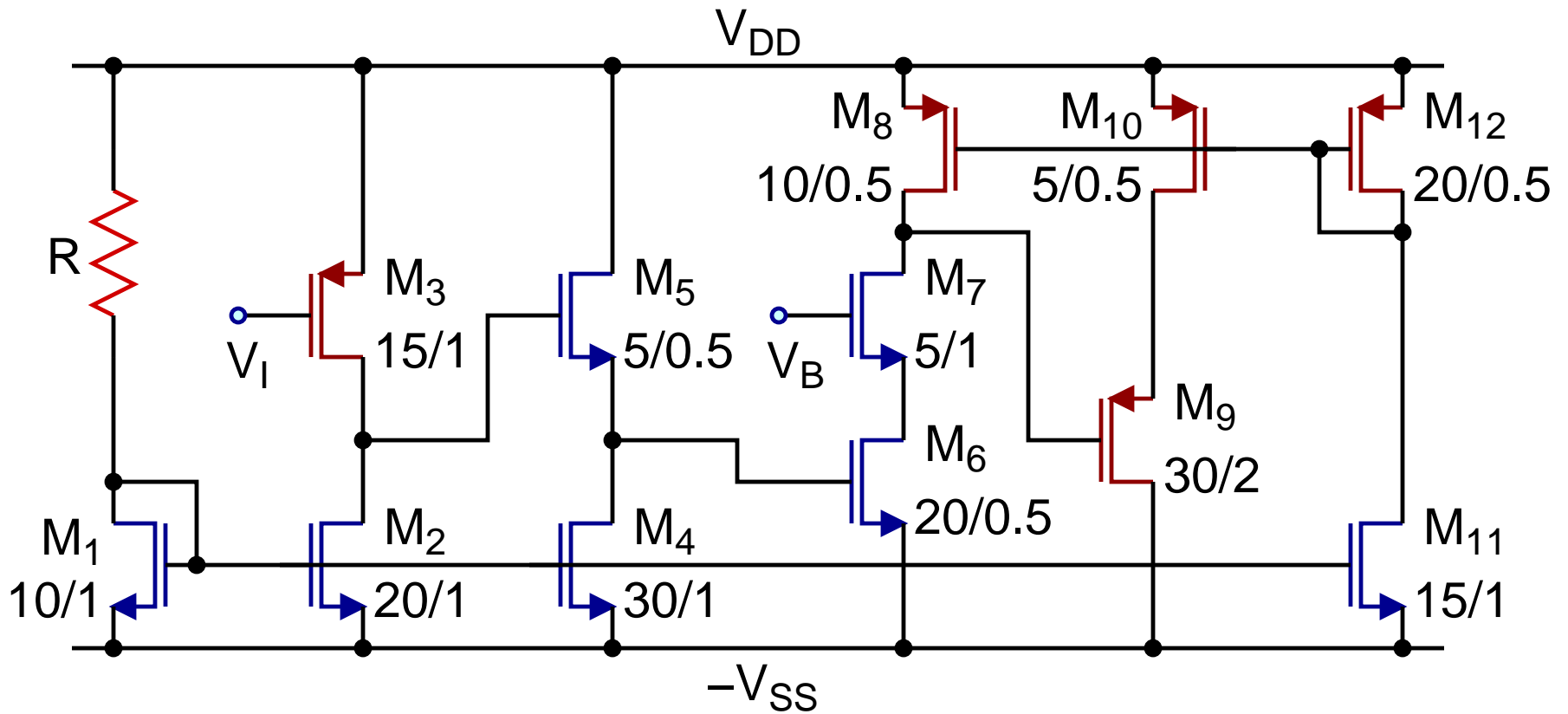
Assuming that all transistors are ACTIVE:

$$I_{D2} = 2I_{D1} \quad I_{D3} = \frac{I_{D1}}{5} \quad I_{D4} = \frac{I_{D1}}{2}$$

$$I_{D5} = 4I_{D1} \quad I_{D6} = 3I_{D1}$$

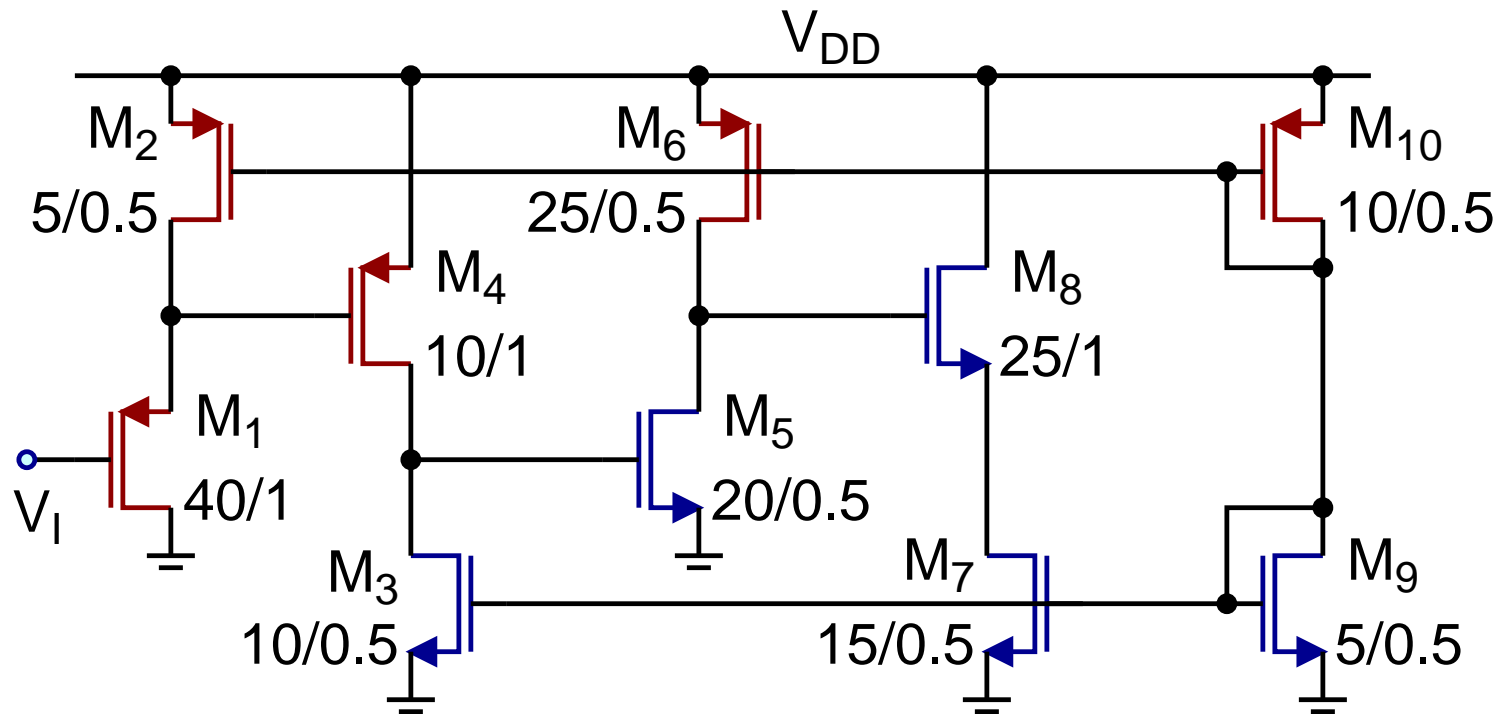
Current Mirror Biasing

Example 1



Current Mirror Biasing

Example 2

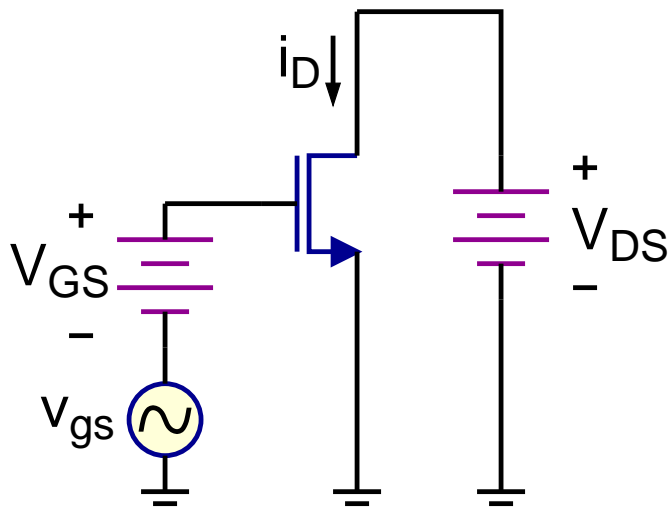


MOSFET Small-Signal Operation

$$\begin{aligned} i_D &= \frac{k'_n W}{2 L} (V_{GS} + v_{gs} - V_t)^2 = \frac{k'_n W}{2 L} (V_{ov} + v_{gs})^2 \\ &= \frac{k'_n W}{2 L} V_{ov}^2 + k'_n \frac{W}{L} V_{ov} v_{gs} + \frac{k'_n W}{2 L} v_{gs}^2 \end{aligned}$$

Assume $v_{gs} \ll 2V_{ov}$, then

$$\begin{aligned} i_D &\approx I_D + k'_n \frac{W}{L} V_{ov} v_{gs} \\ &= I_D + g_m v_{gs} \\ &= I_D + i_d \end{aligned}$$



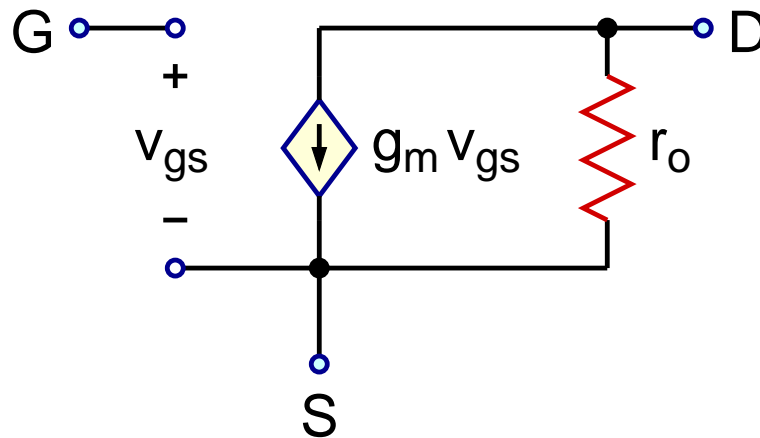
$$g_m = k'_n \frac{W}{L} V_{ov}$$

Small-Signal Model

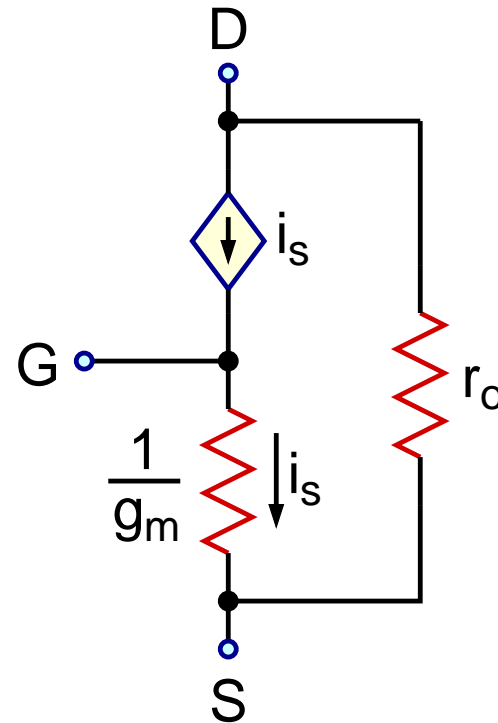
NMOS

$$g_m = k'_n \frac{W}{L} V_{ov} = \sqrt{2k'_n \frac{W}{L} I_D}$$

$$r_o = \frac{V_A}{I_D} = \frac{1}{\lambda_n I_D}$$



π model



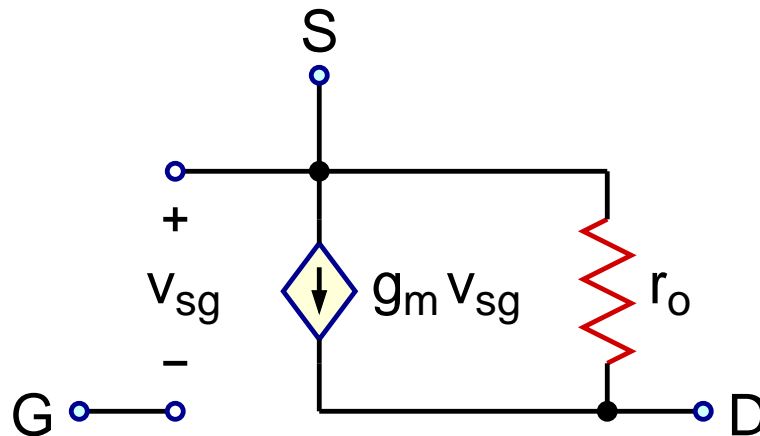
T model

Small-Signal Model

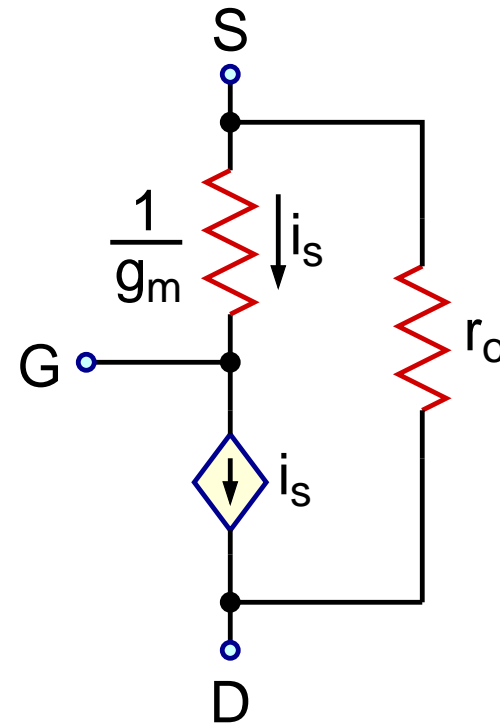
PMOS

$$g_m = k'_p \frac{W}{L} V_{ov} = \sqrt{2k'_p \frac{W}{L} I_D}$$

$$r_o = \frac{|V_A|}{I_D} = \frac{1}{|\lambda_p| I_D}$$



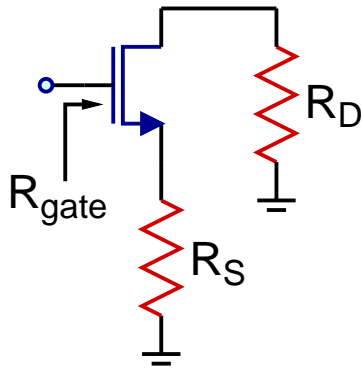
π model



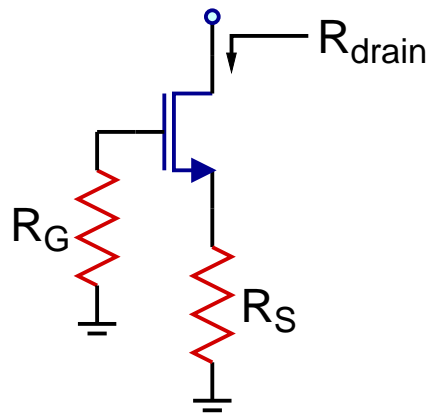
T model

MOS Node Resistances

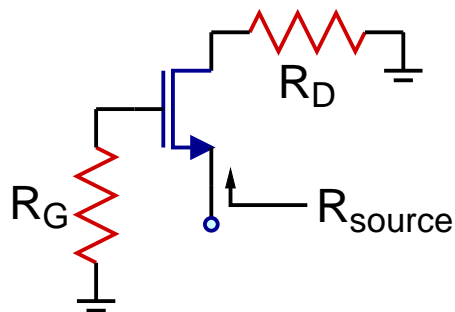
AC, $r_o = \infty$



$$R_{\text{gate}} = \infty$$



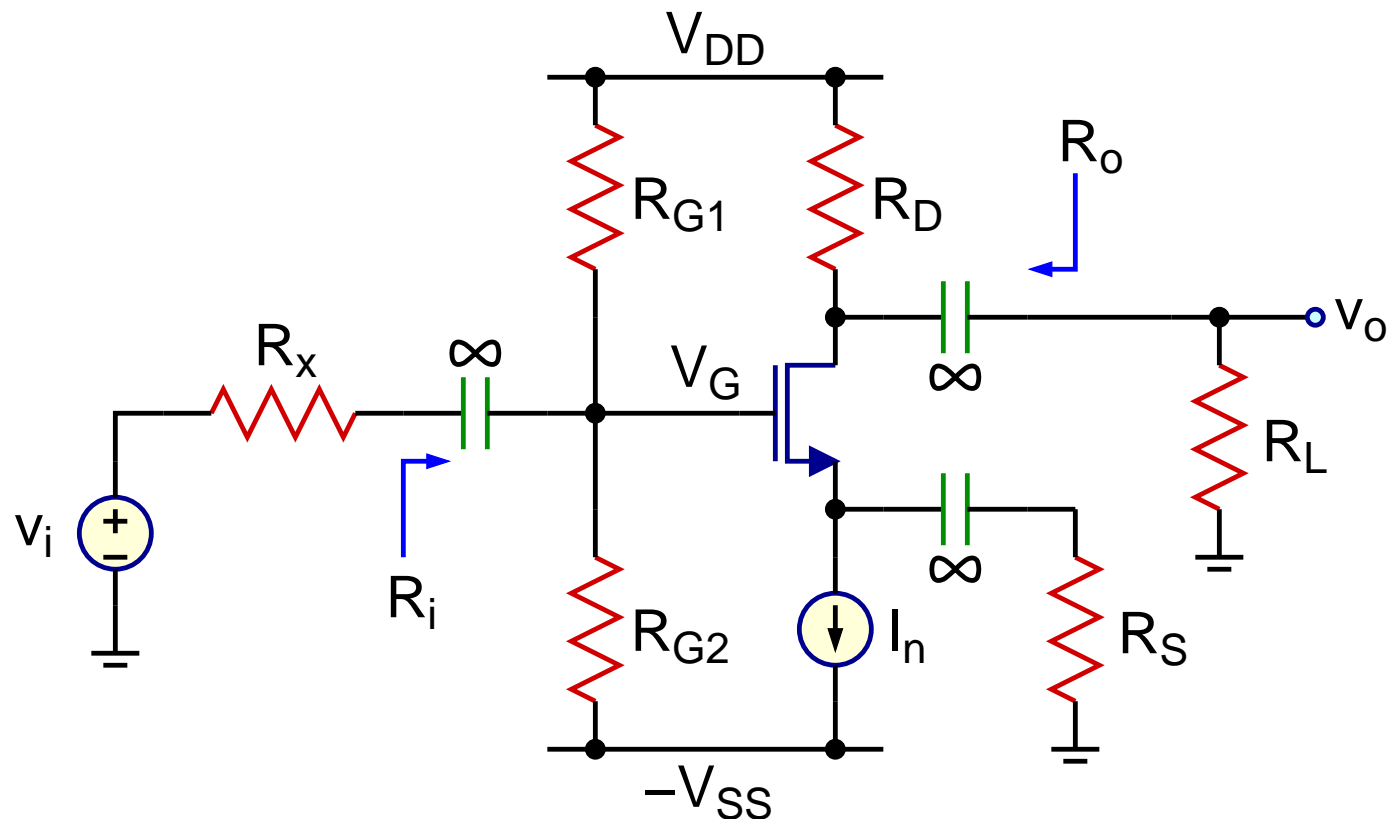
$$R_{\text{drain}} = \infty$$



$$R_{\text{source}} = \frac{1}{g_m}$$

Common-Source Amplifier

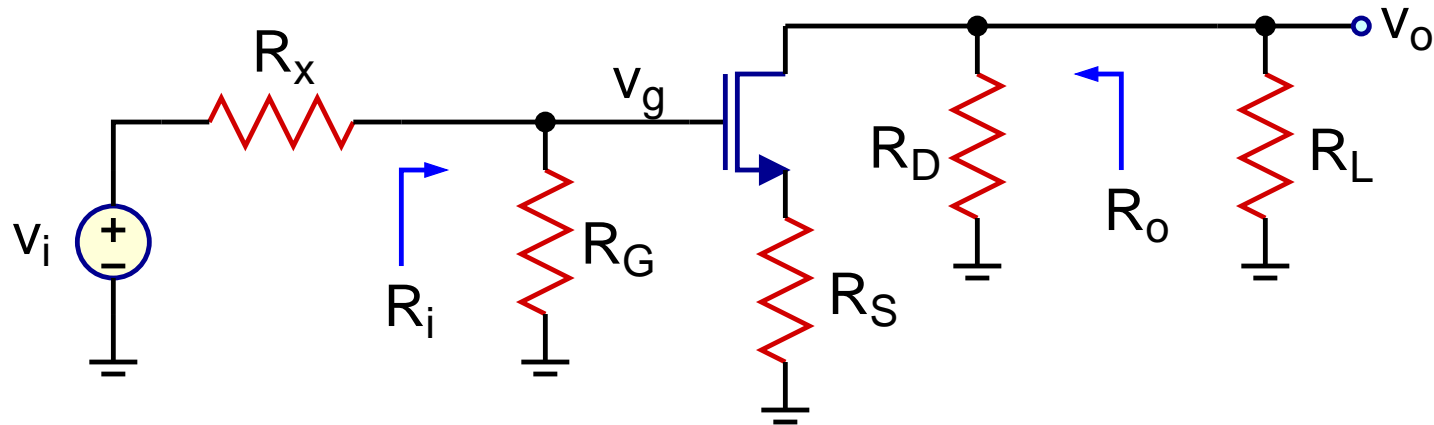
Discrete



$$I_D = I_n \quad , \quad V_G = -V_{SS} + \frac{R_{G2}}{R_{G1} + R_{G2}} (V_{DD} + V_{SS})$$

Common-Source Amplifier

AC equivalent, $r_o = \infty$



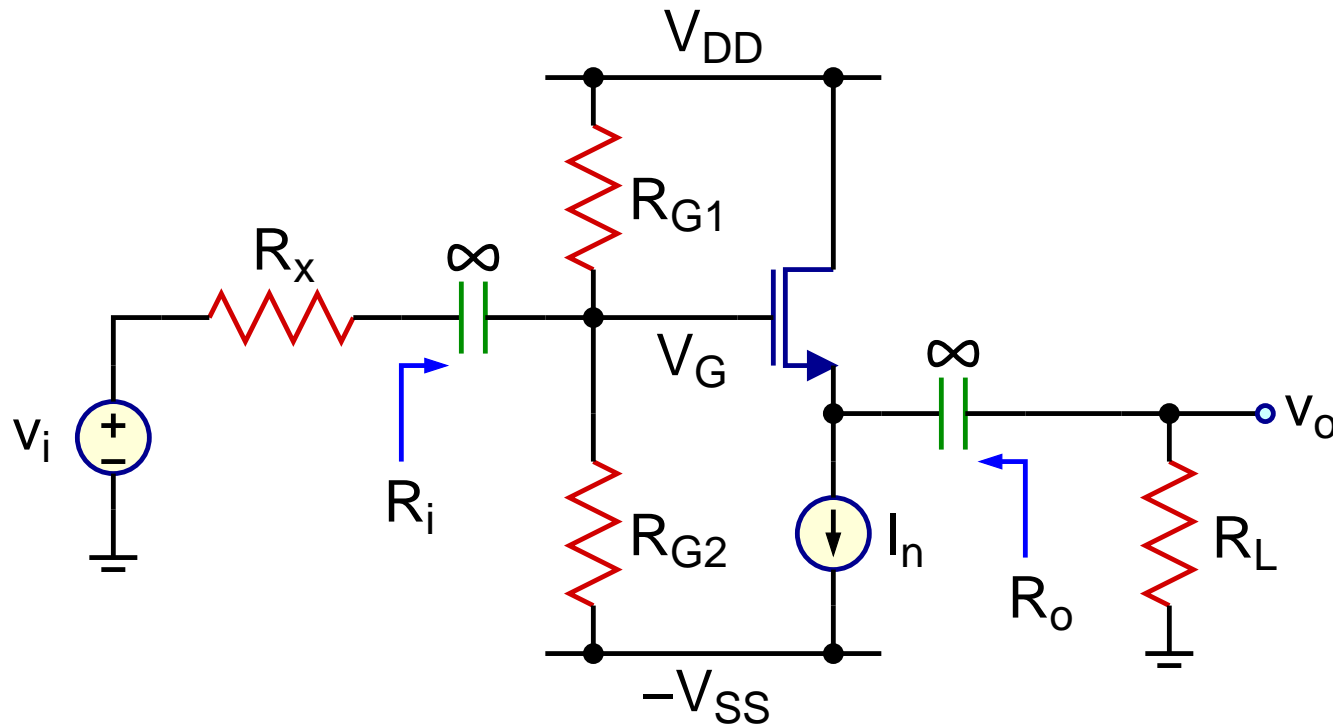
$$R_i = R_G \parallel R_{\text{gate}} = R_{G1} \parallel R_{G2} \parallel R_{\text{gate}}$$

$$R_o = R_D \parallel R_{\text{drain}}$$

$$\frac{v_g}{v_i} = \frac{R_i}{R_x + R_i}, \quad \frac{v_o}{v_g} = -\frac{R_D \parallel R_L}{\frac{1}{g_m} + R_S}$$

Common-Drain Amplifier

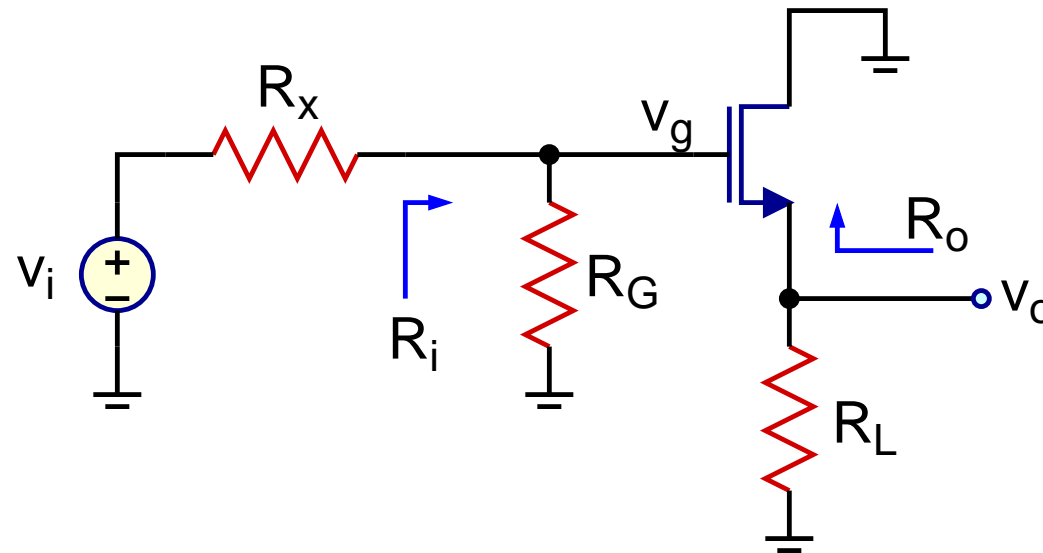
Discrete



$$I_D = I_n \quad , \quad V_G = -V_{SS} + \frac{R_{G2}}{R_{G1} + R_{G2}} (V_{DD} + V_{SS})$$

Common-Drain Amplifier

AC equivalent, $r_o = \infty$



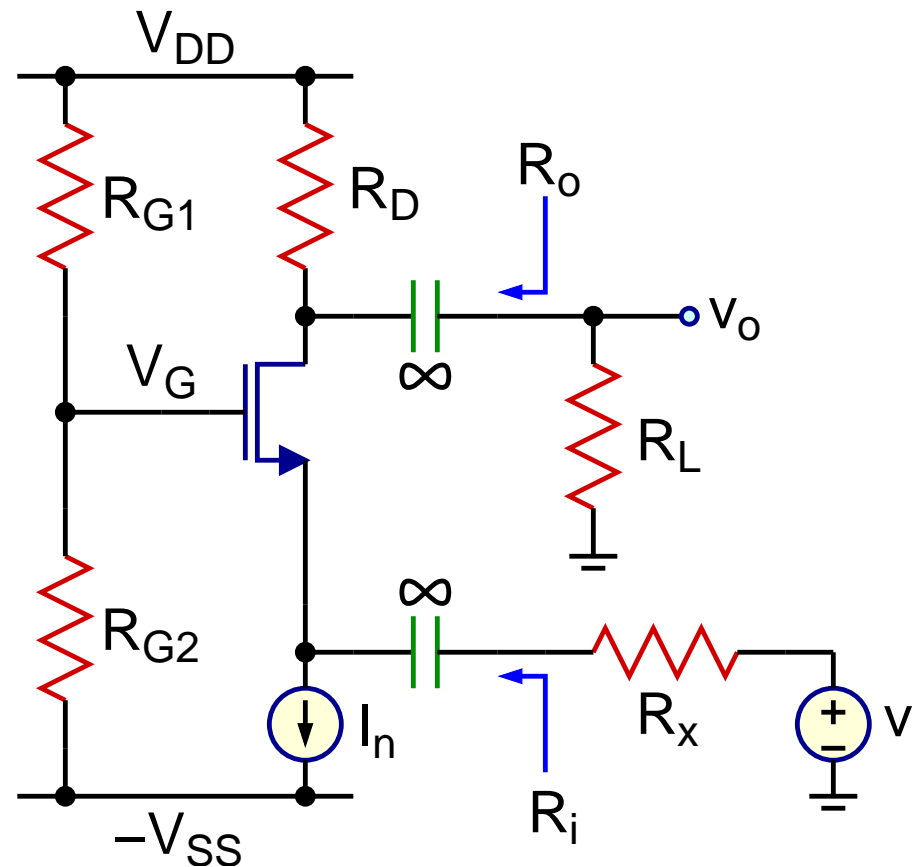
$$R_i = R_G \parallel R_{\text{gate}} = R_{G1} \parallel R_{G2} \parallel R_{\text{gate}}$$

$$R_o = R_{\text{source}}$$

$$\frac{v_g}{v_i} = \frac{R_i}{R_x + R_i}, \quad \frac{v_o}{v_g} = \frac{R_L}{\frac{1}{g_m} + R_L}$$

Common-Gate Amplifier

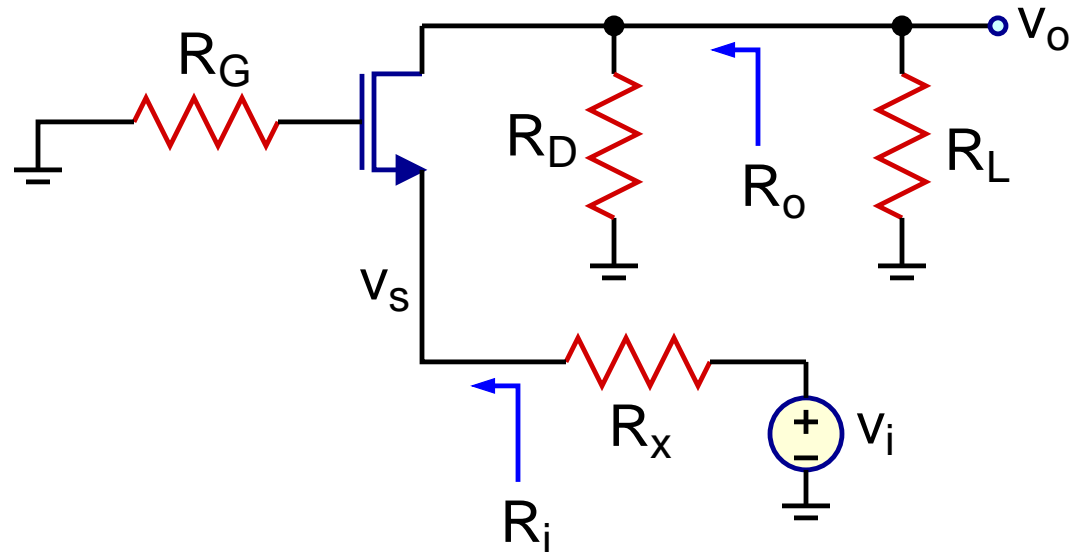
Discrete



$$I_D = I_n \quad , \quad V_G = -V_{SS} + \frac{R_{G2}}{R_{G1} + R_{G2}}(V_{DD} + V_{SS})$$

Common-Gate Amplifier

AC equivalent, $r_o = \infty$



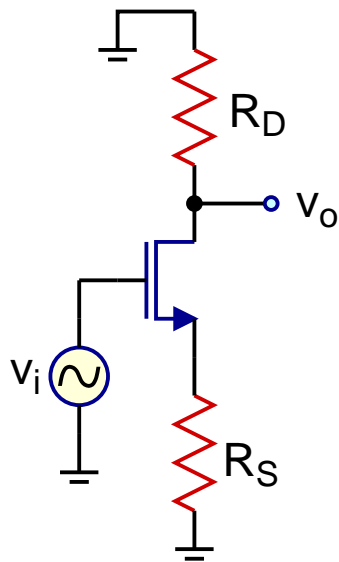
$$R_i = R_{\text{source}}$$

$$R_o = R_D \parallel R_{\text{drain}}$$

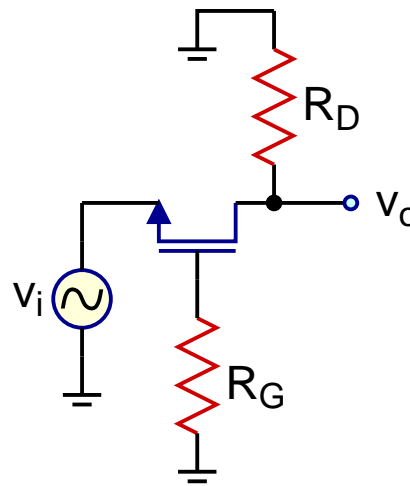
$$\frac{v_s}{v_i} = \frac{R_i}{R_x + R_i}, \quad \frac{v_o}{v_s} = \frac{R_D \parallel R_L}{R_{\text{source}}}$$

MOSFET Amplifiers - Summary

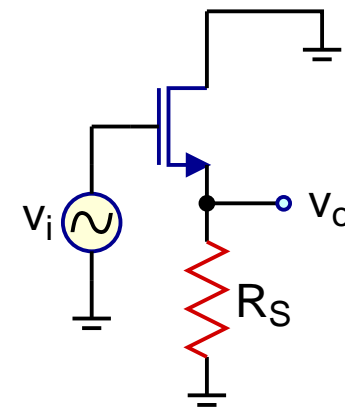
AC, $r_o = \infty$



$$\frac{v_o}{v_i} = -\frac{R_D}{\frac{1}{g_m} + R_S}$$



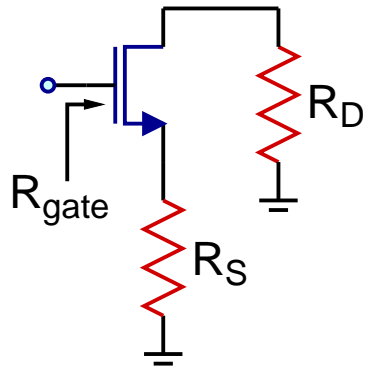
$$\frac{v_o}{v_i} = \frac{R_D}{R_{\text{source}}}$$



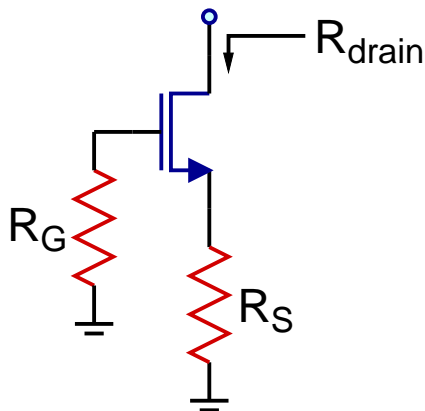
$$\frac{v_o}{v_i} = \frac{R_S}{\frac{1}{g_m} + R_S}$$

MOS Node Resistances

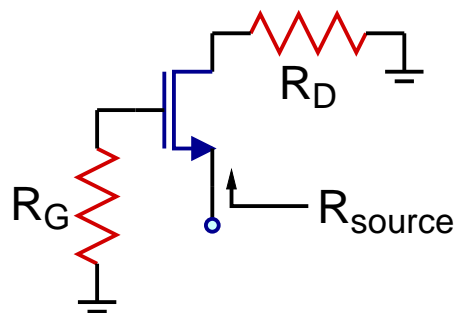
AC, r_o finite



$$R_{\text{gate}} = \infty$$



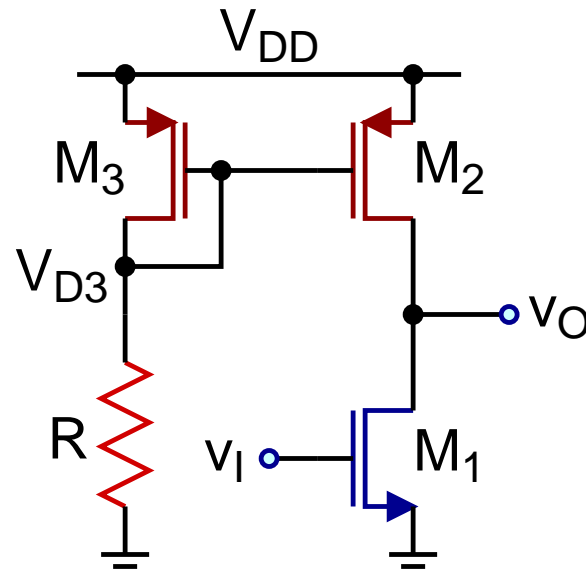
$$R_{\text{drain}} = g_m r_o R_S + r_o + R_S$$



$$R_{\text{source}} = \left(\frac{1}{g_m} \parallel r_o \right) \left(1 + \frac{R_D}{r_o} \right)$$

Common-Source Amplifier

Integrated

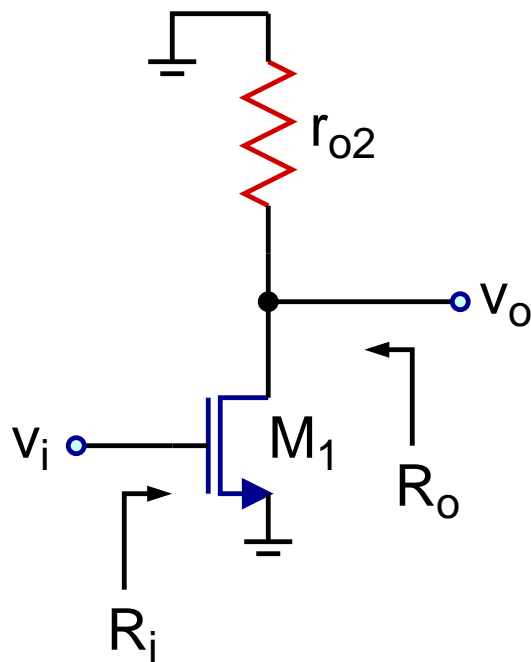


$$I_{D3} = \frac{k'_p}{2} \left(\frac{W}{L}\right)_3 (V_{DD} - V_{D3} - |V_{tp}|)^2 = \frac{V_{D3}}{R}$$

$$\frac{I_{D2}}{I_{D3}} = \frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_3}, \quad I_{D1} = I_{D2}$$

Common-Source Amplifier

AC equivalent



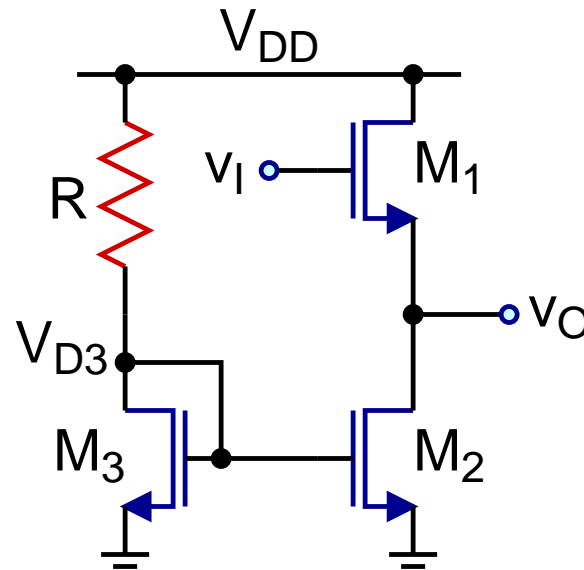
$$\frac{v_o}{v_i} = -\frac{r_{o1} \parallel r_{o2}}{1/g_{m1}}$$

$$R_i = \infty$$

$$R_o = r_{o1} \parallel r_{o2}$$

Common-Drain Amplifier

Integrated

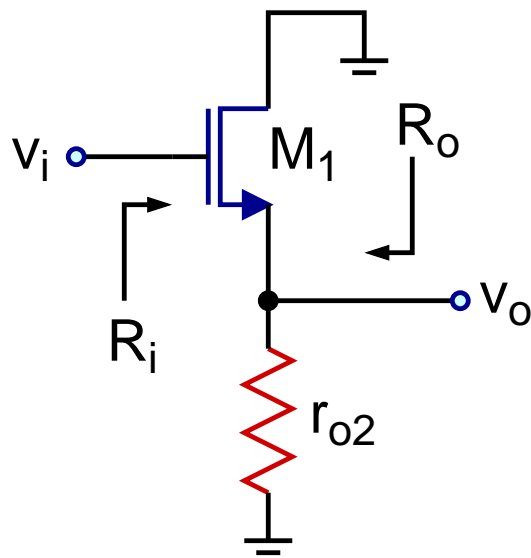


$$I_{D3} = \frac{k'_n}{2} \left(\frac{W}{L} \right)_3 (V_{D3} - V_{tn})^2 = \frac{V_{DD} - V_{D3}}{R}$$

$$\frac{I_{D2}}{I_{D3}} = \frac{\left(\frac{W}{L} \right)_2}{\left(\frac{W}{L} \right)_3}, \quad I_{D1} = I_{D2}$$

Common-Drain Amplifier

AC Equivalent

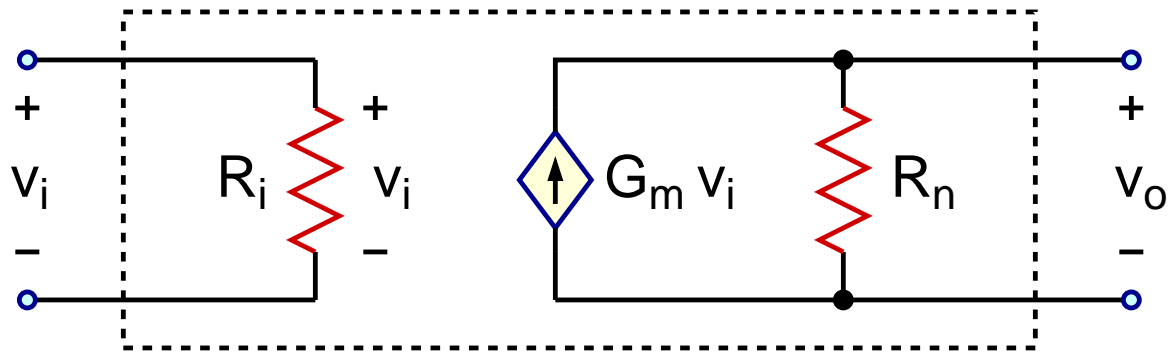
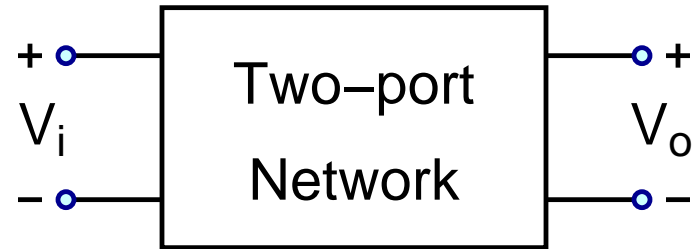


$$\frac{v_o}{v_i} = \frac{r_{o1} \parallel r_{o2}}{\frac{1}{g_{m1}} + (r_{o1} \parallel r_{o2})}$$

$$R_i = \infty$$

$$R_o = \frac{1}{g_{m1}} \parallel r_{o1} \parallel r_{o2}$$

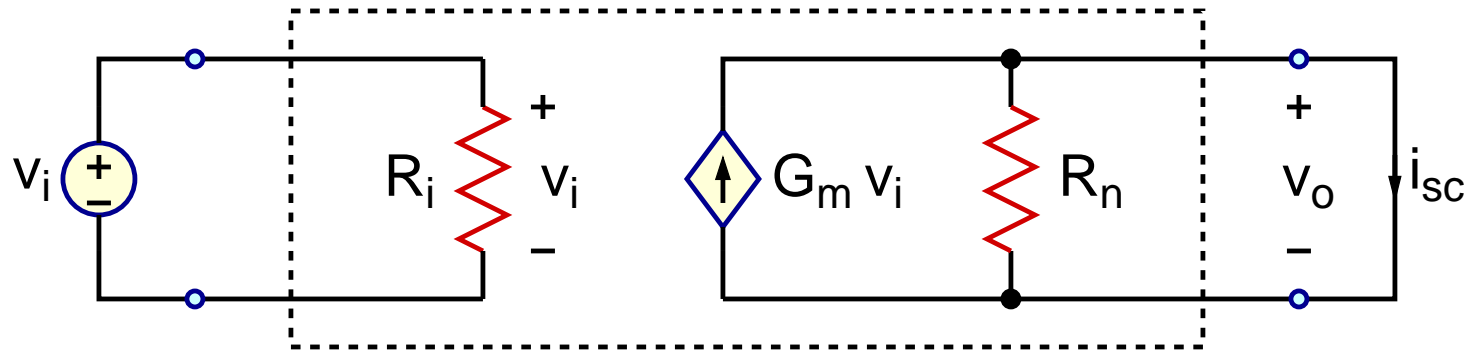
Two-Port Modeling of Amplifiers



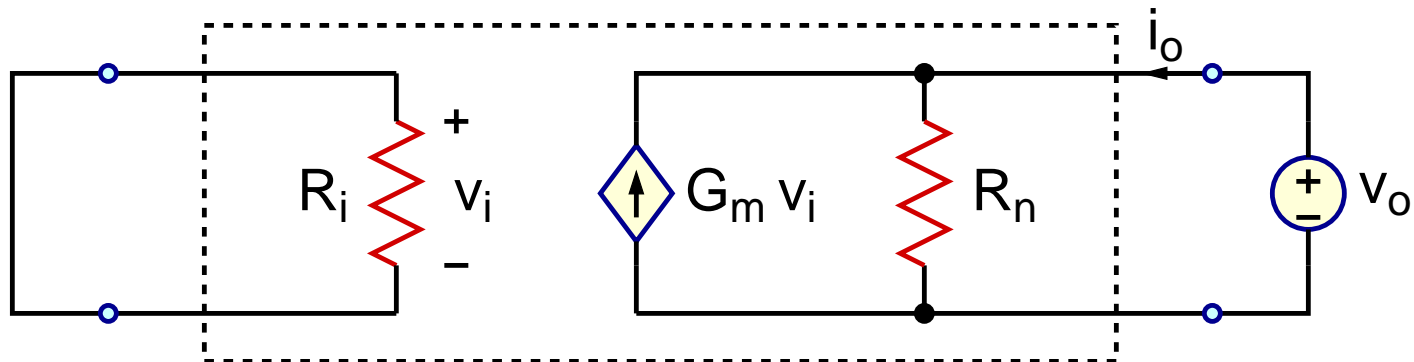
$$\frac{V_o}{V_i} = G_m R_n$$

Two-Port Modeling of Amplifiers

G_m & R_n



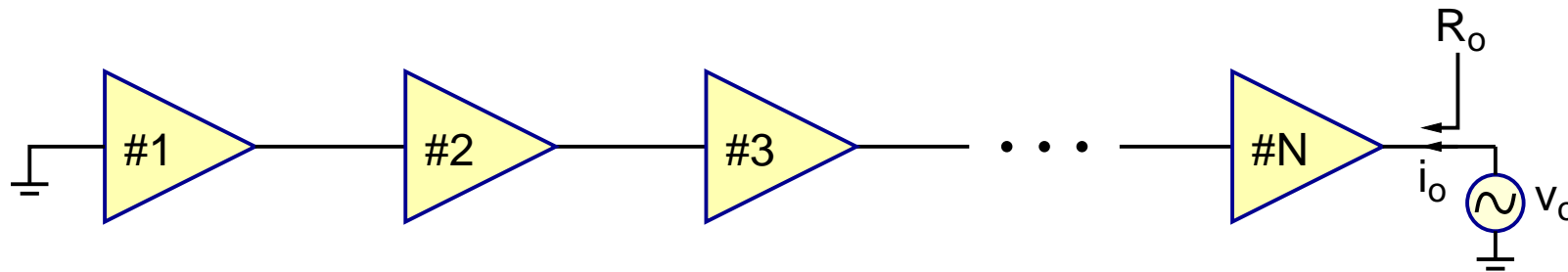
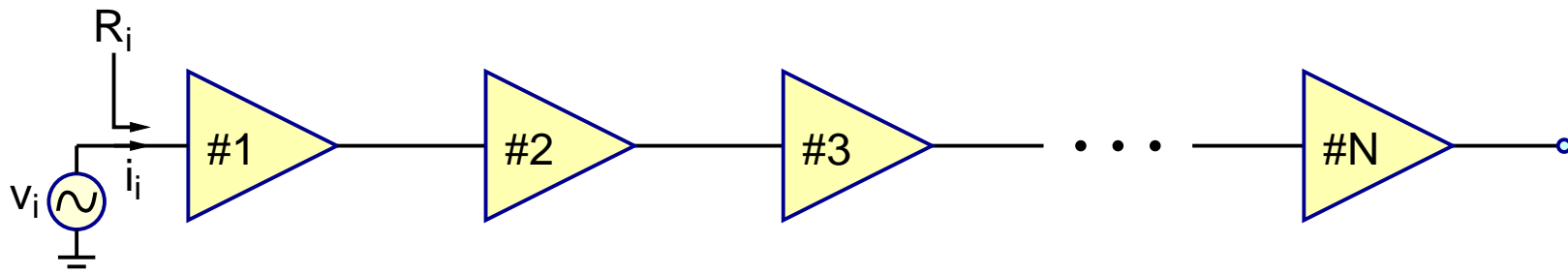
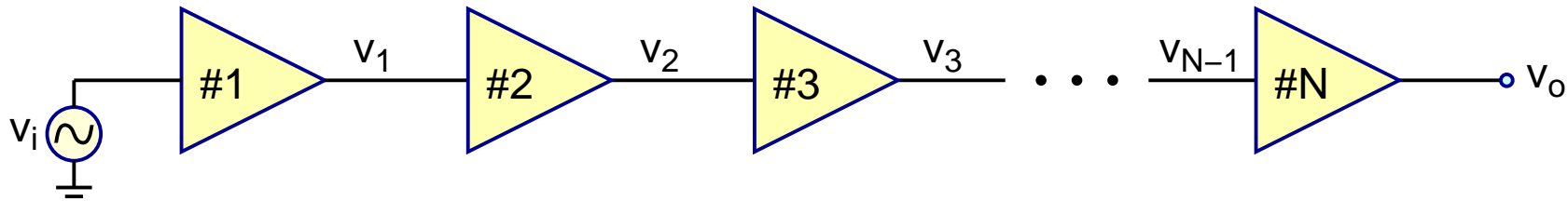
$$G_m = \frac{i_{sc}}{V_i} \Big|_{V_o=0}$$



$$R_n = \frac{V_o}{i_o} \Big|_{V_i=0}$$

Two-Port Modeling of Amplifiers

Multistage



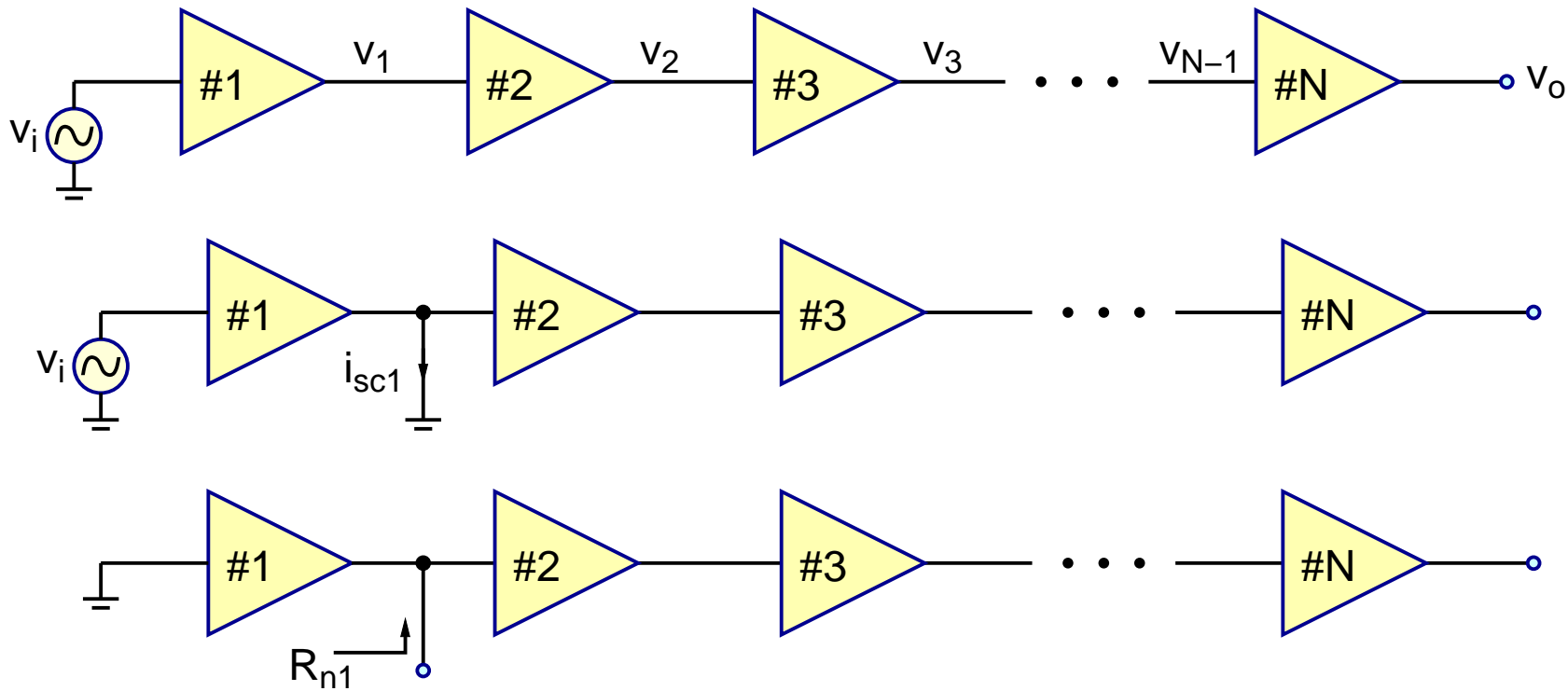
$$\frac{V_o}{V_i} = \frac{V_1}{V_i} \frac{V_2}{V_1} \dots \frac{V_o}{V_{N-1}}$$

$$R_i = \frac{V_i}{i_i}$$

$$R_o = \frac{V_o}{i_o}$$

Two-Port Modeling of Amplifiers

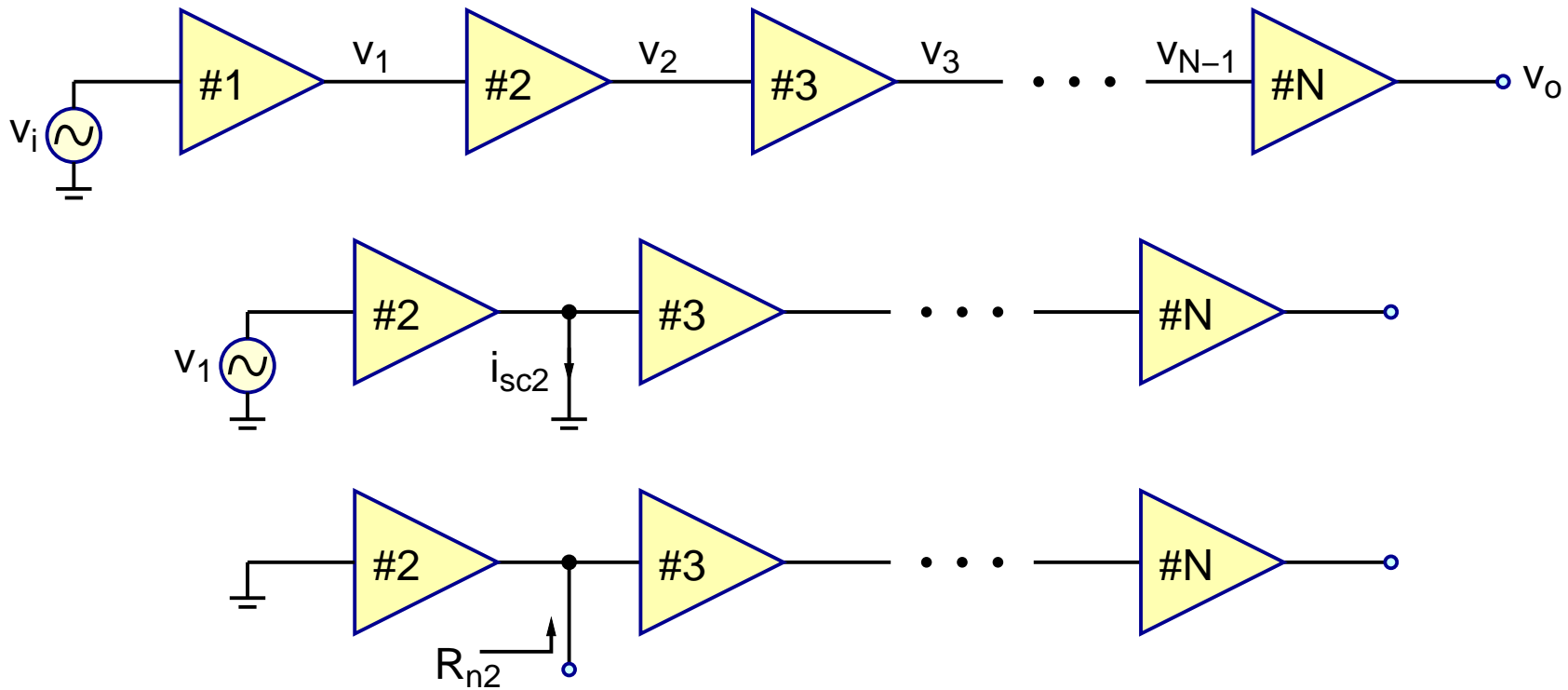
Multistage



$$G_{m1} = \frac{i_{sc1}}{v_i} \quad \frac{v_1}{v_i} = G_{m1}R_{n1}$$

Two-Port Modeling of Amplifiers

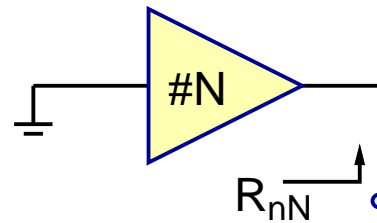
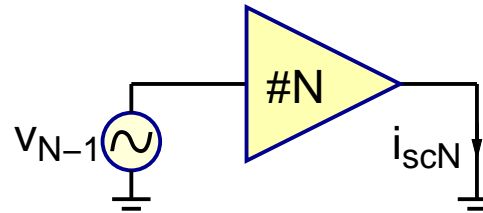
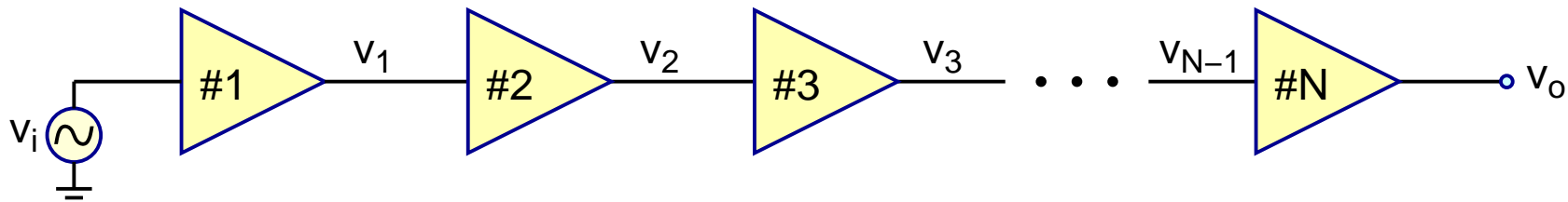
Multistage



$$G_{m2} = \frac{i_{sc2}}{v_1} \quad \frac{v_2}{v_1} = G_{m2}R_{n2}$$

Two-Port Modeling of Amplifiers

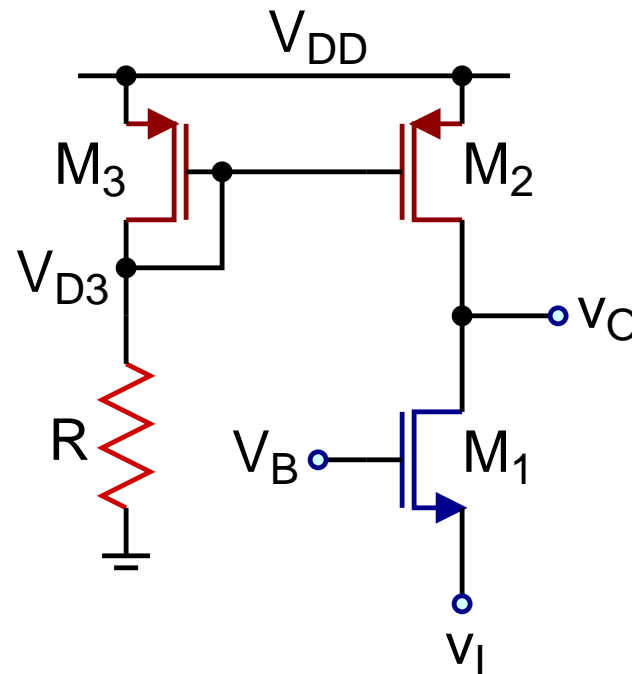
Multistage



$$G_{mN} = \frac{i_{scN}}{v_{N-1}} \quad \frac{v_o}{v_{N-1}} = G_{mN} R_{nN}$$

Common-Gate Amplifier

Integrated

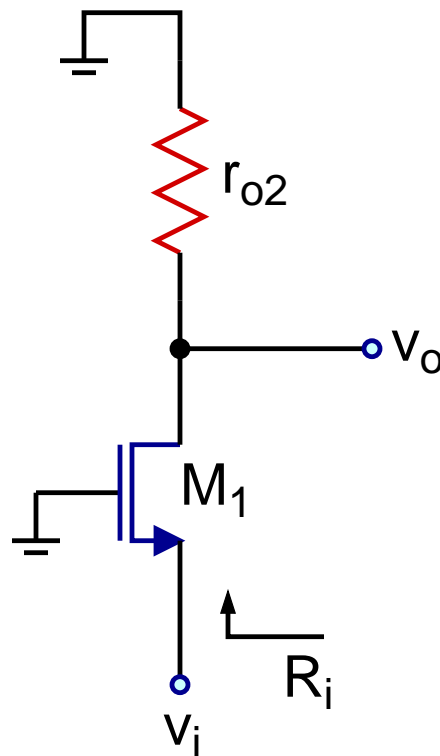


$$I_{D3} = \frac{k'_p}{2} \left(\frac{W}{L}\right)_3 (V_{DD} - V_{D3} - |V_{tp}|)^2 = \frac{V_{D3}}{R}$$

$$\frac{I_{D2}}{I_{D3}} = \frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_3}, \quad I_{D1} = I_{D2}$$

Common-Gate Amplifier

AC Equivalent



$$R_i = \left(\frac{1}{g_{m1}} \parallel r_{o1} \right) \left(1 + \frac{r_{o2}}{r_{o1}} \right)$$

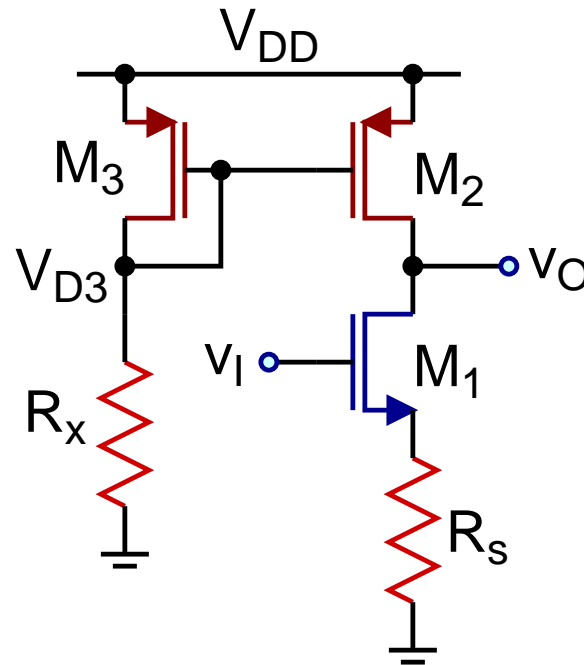
$$G_m = g_{m1} + \frac{1}{r_{o1}}$$

$$R_n = r_{o1} \parallel r_{o2}$$

$$\frac{V_o}{V_i} = G_m R_n$$

Common-Source Amplifier - SD

Integrated

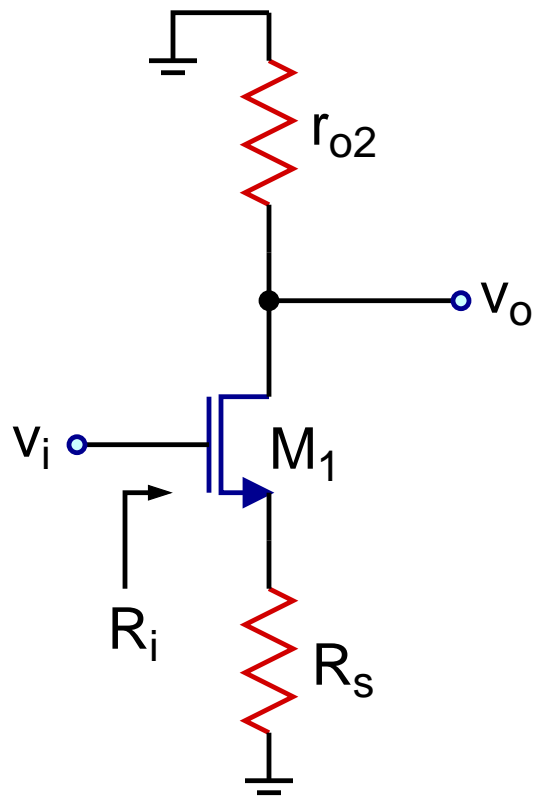


$$I_{D3} = \frac{k'_p}{2} \left(\frac{W}{L}\right)_3 (V_{DD} - V_{D3} - |V_{tp}|)^2 = \frac{V_{D3}}{R_x}$$

$$\frac{I_{D2}}{I_{D3}} = \frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_3}, \quad I_{D1} = I_{D2}$$

Common-Source Amplifier - SD

AC equivalent



$$R_i = \infty$$

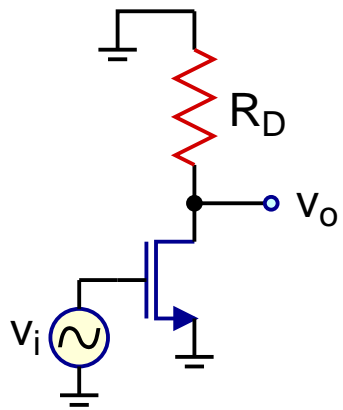
$$G_m = \frac{-g_{m1}}{1 + g_{m1}R_s + (R_s/r_{o1})}$$

$$R_n = r_{o2} \parallel (R_s + r_{o1} + g_{m1}R_sr_{o1})$$

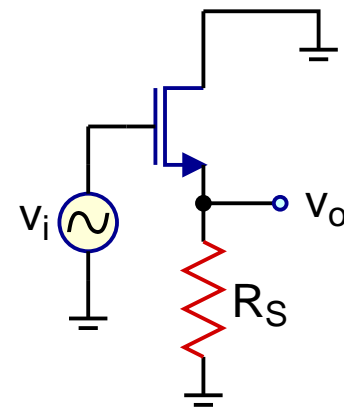
$$\frac{V_o}{V_i} = G_m R_n$$

MOSFET Amplifiers- Summary

AC, r_o finite



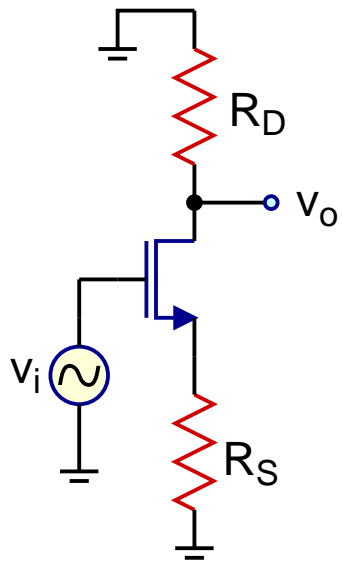
$$\frac{v_o}{v_i} = -\frac{R_D \parallel r_o}{\frac{1}{g_m}}$$



$$\frac{v_o}{v_i} = \frac{R_S \parallel r_o}{\frac{1}{g_m} + (R_S \parallel r_o)}$$

MOSFET Amplifiers - Summary

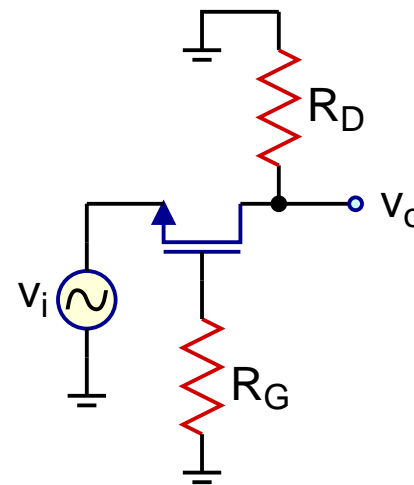
AC, r_o finite



$$G_m = \frac{-g_m}{1 + g_m R_S + \frac{R_S}{r_o}}$$

$$R_n = R_D \parallel (g_m r_o R_S + r_o + R_S)$$

$$\frac{v_o}{v_i} = G_m R_n$$



$$G_m = g_m + \frac{1}{r_o}$$

$$R_n = R_D \parallel r_o$$

$$\frac{v_o}{v_i} = G_m R_n$$