ECEN326: Electronic Circuits
Spring 2022

Lab 1 Graphical Design Approach

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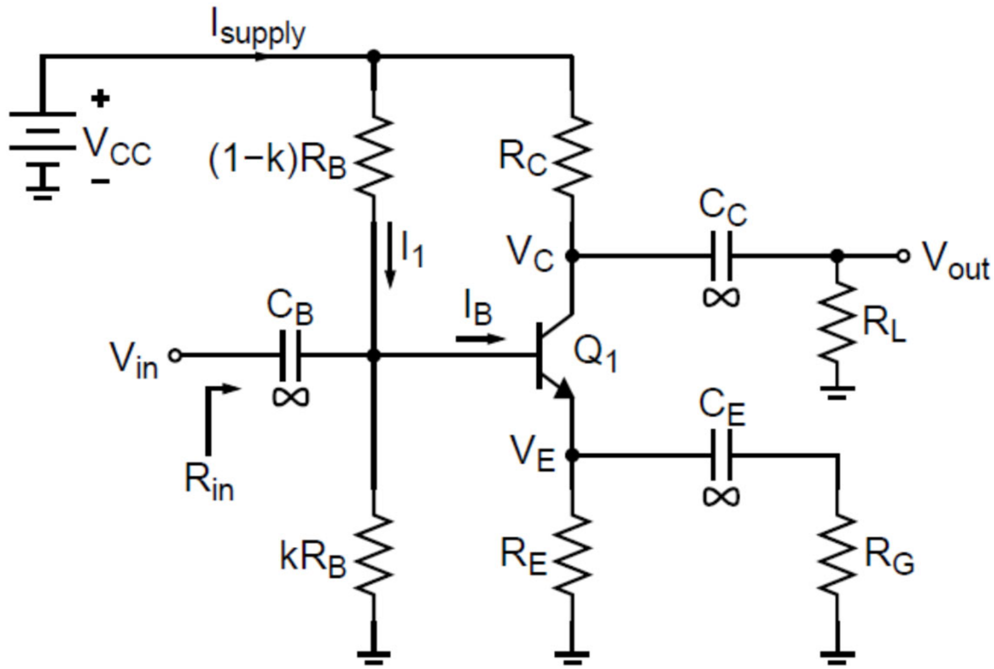
Common Emitter Amp w/ Emitter Resistor



$$A_v = -\frac{\alpha\left(R_C \| R_L\right)}{r_e + R_E \| R_G} = -\frac{g_m\left(R_C \| R_L\right)}{1 + \dfrac{g_m\left(R_E \| R_G\right)}{\alpha}}$$

$$R_{in} = kR_B \| (1-k)R_B \| \left[(\beta+1)\left(r_e + R_E \| R_G\right)\right]$$

Typical Design Specifications

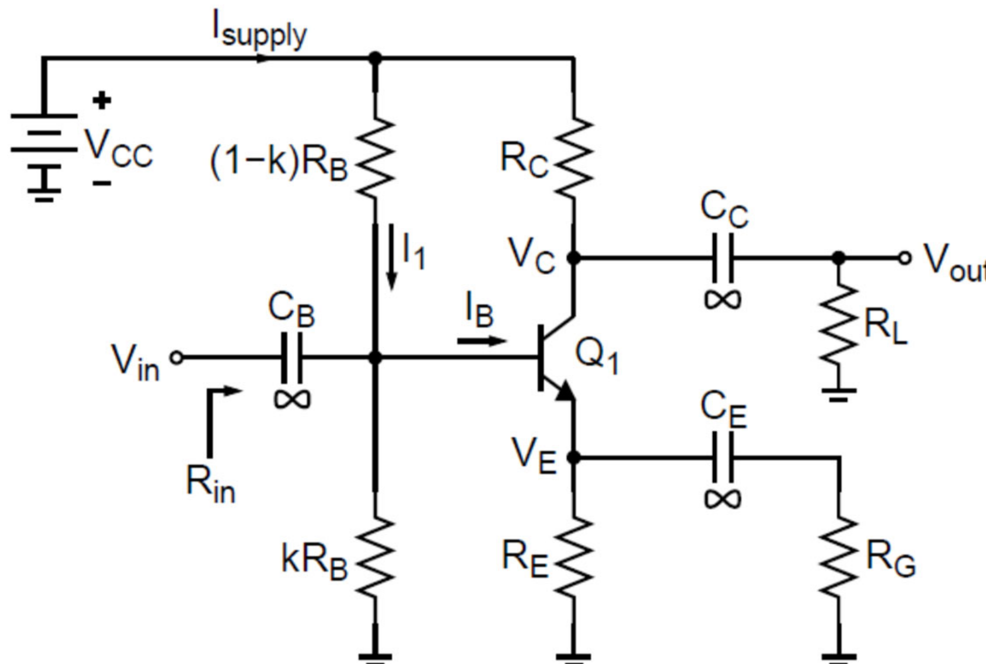
- Loaded voltage gain, A_v
- Max output swing, v_{omax}
  - This must be satisfied at a given linearity (total harmonic distortion)
- Input resistance, R_{in}
- Power Supply, V_{CC}
- Min Emitter Voltage for β robustness, V_E

How to set DC Biasing Conditions?

- In order to meet all design specifications, the DC biasing conditions (I_C, R_C) must be set appropriately
- Can transform design specifications into functions of I_C & R_C and graph them to find acceptable solution space

R_{in}, V_{CC}, & Neg. v_{omax} Specifications

- R_{in} Spec



$$R_{in} = kR_B \| (1-k)R_B \| \left[(\beta+1)\left(r_e + R_E \| R_G\right)\right] \approx \beta\left(R_E \| R_G\right)$$

$$R_E \| R_G \approx \frac{R_{in}}{\beta}$$

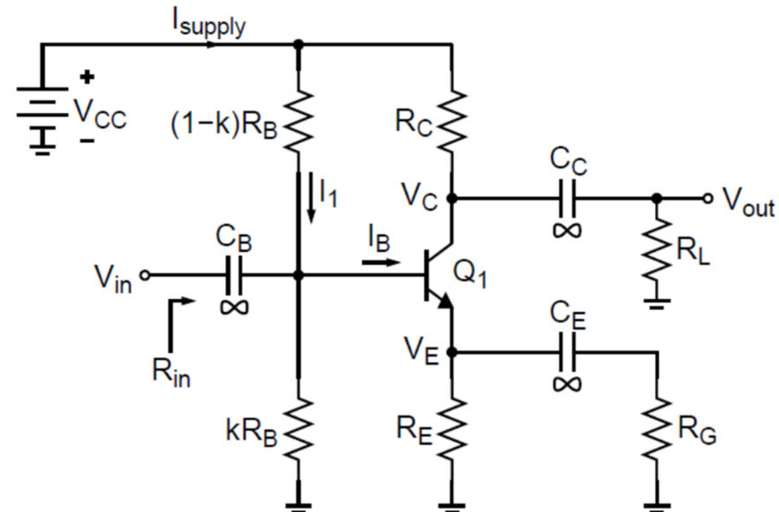
- Input resistance is primarily set by $R_E || R_G$

R_{in}, V_{CC}, & Neg. v_{omax} Specifications

- Need a minimum V_{CE} to keep transistor in active mode with maximum negative swing

Set $V_{CE\min} = 300mV$

* Note if the specs are relaxed enough, it is often good to set $V_{CE\min} = 500mV$ for margin.



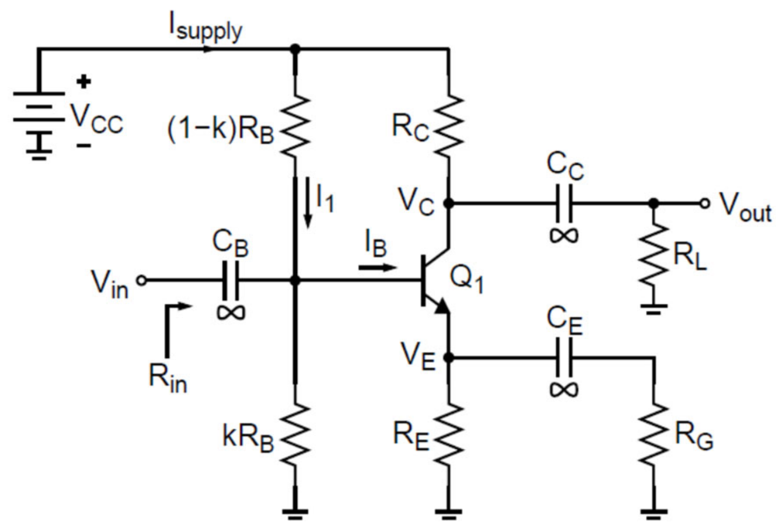
- V_{CC} Spec (w/ max negative swing)

$$V_{CC} = V_E + V_{CE\min} + v_{o\max} + I_C R_C$$

$$V_{CE\min} = V_{CC} - I_C R_C - v_{o\max} - V_E \geq 300mV$$

R_{in}, V_{CC}, & Neg. v_{omax} Specifications

- Can solve for I_C



$$\boxed{I_C \le \frac{V_{CC} - v_{o\max} - 0.3V - V_E}{R_C}}$$

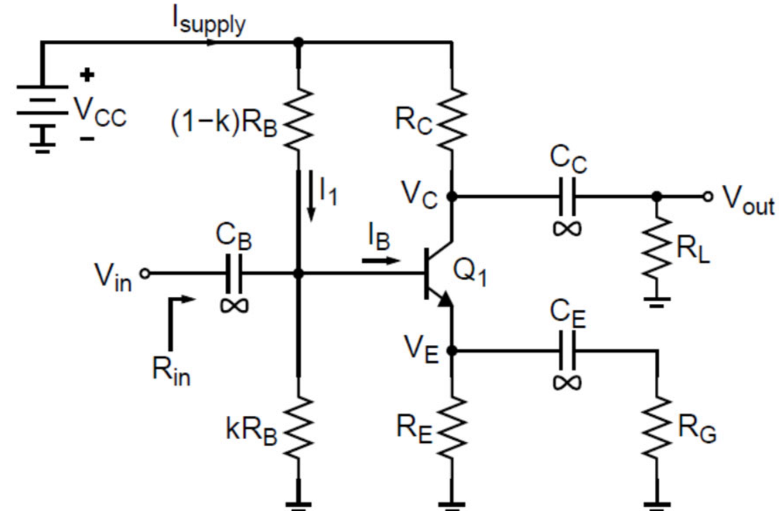
- Minimum negative AC Swing constraint sets an upper bound on I_C

Pos. v_{omax} Specification

- Need to insure with a positive swing that the output signal doesn't clip the power supply

$$V_{CC} - I_C R_C + v_{o\max} \le V_{CC}$$

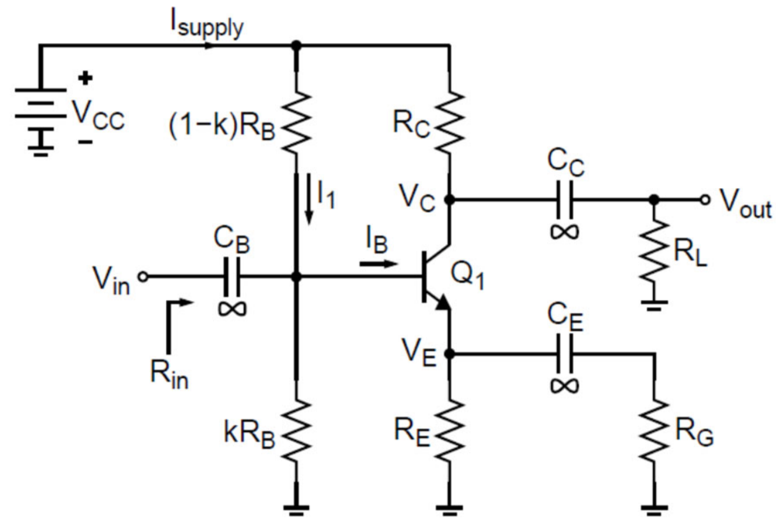
$$\boxed{I_C \ge \frac{v_{o\max}}{R_C}}$$



- Positive AC Swing constraint sets a lower bound on I_C
- Additional linearity constraint (harmonic distortion) generally sets a tighter bound

Gain Specification

$$|A_v| = \left|\frac{v_o}{v_i}\right| \leq \frac{g_m(R_C \| R_L)}{1 + \frac{g_m(R_E \| R_G)}{\alpha}} = \frac{\frac{I_C}{V_{th}}(R_C \| R_L)}{1 + \left(\frac{I_C}{V_{th}}\right)\frac{(R_E \| R_G)}{\alpha}}$$

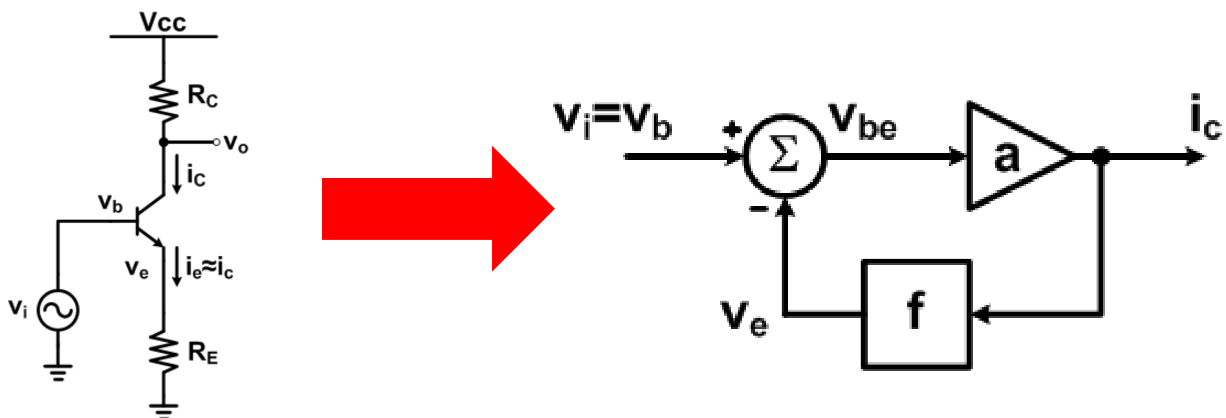


$$\boxed{I_C \geq \frac{|A_v| V_{th}}{R_C \| R_L - \frac{|A_v|(R_E \| R_G)}{\alpha}} = \frac{|A_v| V_{th}}{R_C \| R_L - \frac{|A_v| R_{in}}{\alpha\beta}}}$$

- Gain constraint sets a lower bound on I_C

Harmonic Distortion Specification

- Need a minimum amount of bias current to insure that the AC swing doesn't distort



Model a as a system which distorts

$$i_c = a v_{be} = a_1 v_{be} + a_2 v_{be}^2 + a_3 v_{be}^3 + \ldots$$

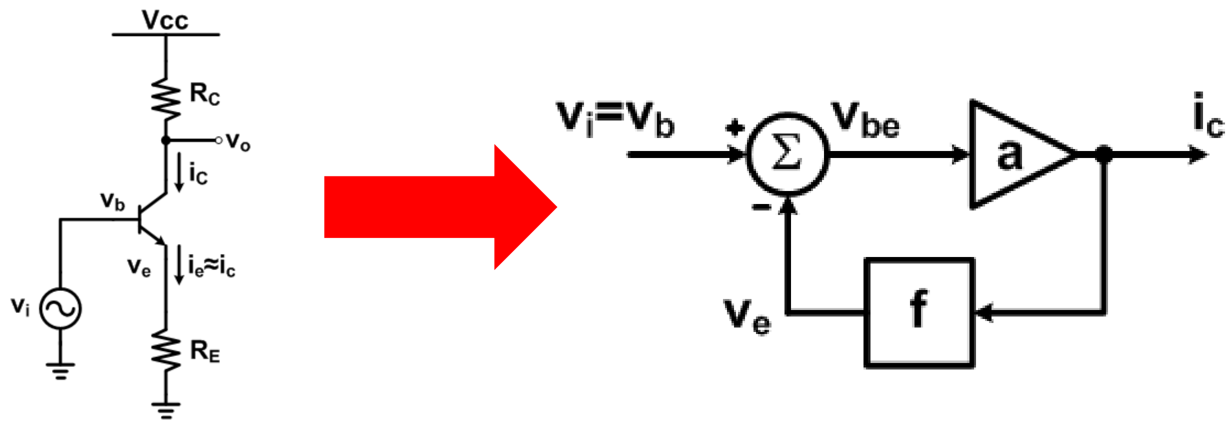
$$\text{where} \quad a_1 = g_m, \quad a_2 = \frac{1}{2}\frac{I_{CQ}}{V_{th}^2}, \quad \ldots$$

$$\text{Here} \quad v_{be} = v_b - v_e \approx v_b - f i_c$$

$$\text{where} \quad f = R_E$$

*This analysis is for a general CE Amp, in our specific circuit $R_C \Rightarrow R_C || R_L$ and $R_E \Rightarrow R_E || R_G$

Harmonic Distortion Specification



We want to express i_c as a function of v_b because that is our input

$$i_c = bv_b = b_1 v_b + b_2 v_b^2 + b_3 v_b^3 + \ldots.$$

Can show that *

$$b_1 = \frac{g_m}{1+g_m R_E}, \quad b_2 = \frac{1}{2}\frac{I_{CQ}}{V_{th}^2\left(1+g_m R_E\right)^3}, \quad \ldots$$

- For single-ended amplifiers with low-distortion, HD2 will dominate the distortion terms

The second-order harmonic distortion is

$$HD2 = \frac{1}{2}\frac{b_2}{b_1^2} i_{c\max} = \frac{1}{4}\left(\frac{1}{1+g_m R_E}\right)\left(\frac{i_{c\max}}{I_{CQ}}\right)$$

*This analysis is for a general CE Amp, in our specific circuit $R_C \Rightarrow R_C || R_L$ and $R_E \Rightarrow R_E || R_G$

Harmonic Distortion Specification

To satisfy a given HD2 specification

$$i_{c\max} \le 4HD2(1+g_m R_E)I_{CQ}$$

$$I_C \ge \frac{\frac{v_{o\max}}{R_C}}{4HD2(1+g_m R_E)} \approx \frac{\frac{v_{o\max}}{R_C}}{4HD2\left(\frac{I_C}{V_{th}}\right)R_E}$$

$$I_C \ge \frac{1}{2}\sqrt{\frac{V_{th}v_{o\max}}{R_C R_E HD2}}$$

$$\text{Using} \quad R_E \approx \frac{R_{in}}{\beta}$$

$$\boxed{I_C \ge \frac{1}{2}\sqrt{\frac{V_{th}v_{o\max}\beta}{(R_C \| R_L)R_{in}HD2}}}$$

*This analysis is for a general CE Amp, in our specific circuit $R_C \Rightarrow R_C||R_L$ and $R_E \Rightarrow R_E||R_G$

- HD2 will dominate, but is not the only distortion term, so you need to use a slightly larger current or put some margin in the HD2 value relative to the THD spec

Key CE Amp Design Equation Summary

$$\text{Neg. Swing, Rin, V}_{\text{CC}}: \quad I_C \le \frac{V_{CC} - v_{o\,\max} - 0.3V - V_E}{R_C}$$

$$\text{Pos. Swing}: \quad I_C \ge \frac{v_{o\,\max}}{R_C}$$

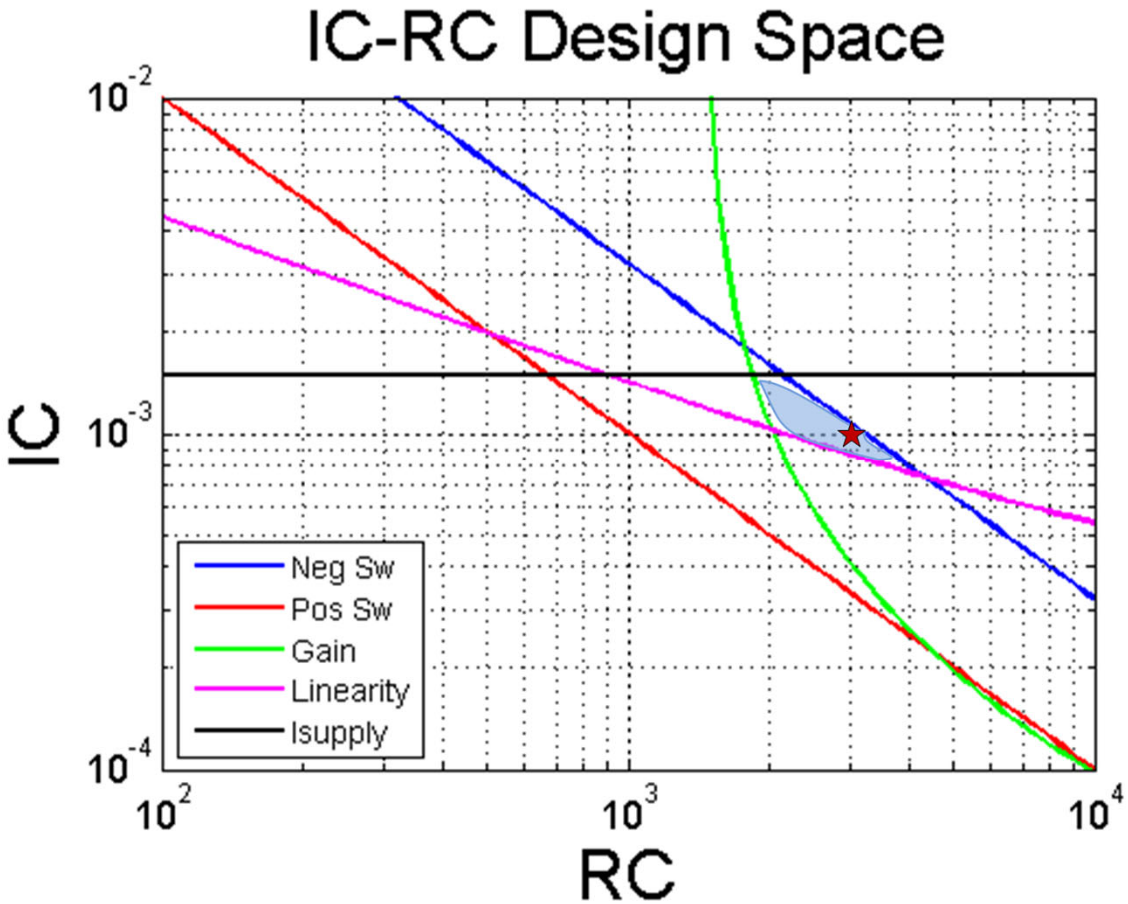
$$\text{Gain}: \quad I_C \ge \frac{|A_v| V_{th}}{R_C \| R_L - \dfrac{|A_v| R_{in}}{\alpha\beta}}$$

$$\text{Harmonic Distortion}: \quad I_C \ge \frac{1}{2}\sqrt{\frac{V_{th} v_{o\,\max} \beta}{(R_C \| R_L) R_{in} HD2}}$$

Design Example - Specifications

- $|A_v| \geq |-20|$
- $R_{in} \geq 10k\Omega$
- $R_L = 20k\Omega$
- $V_{omax} = 1V_{pk}$ w/ THD $\leq$ 5% (-26.0dB)
- $V_{CC} = 5V$
- $V_E \geq 0.5V$
- Isupply $\leq$ 1.5mA
- Nominal operation at 5kHz

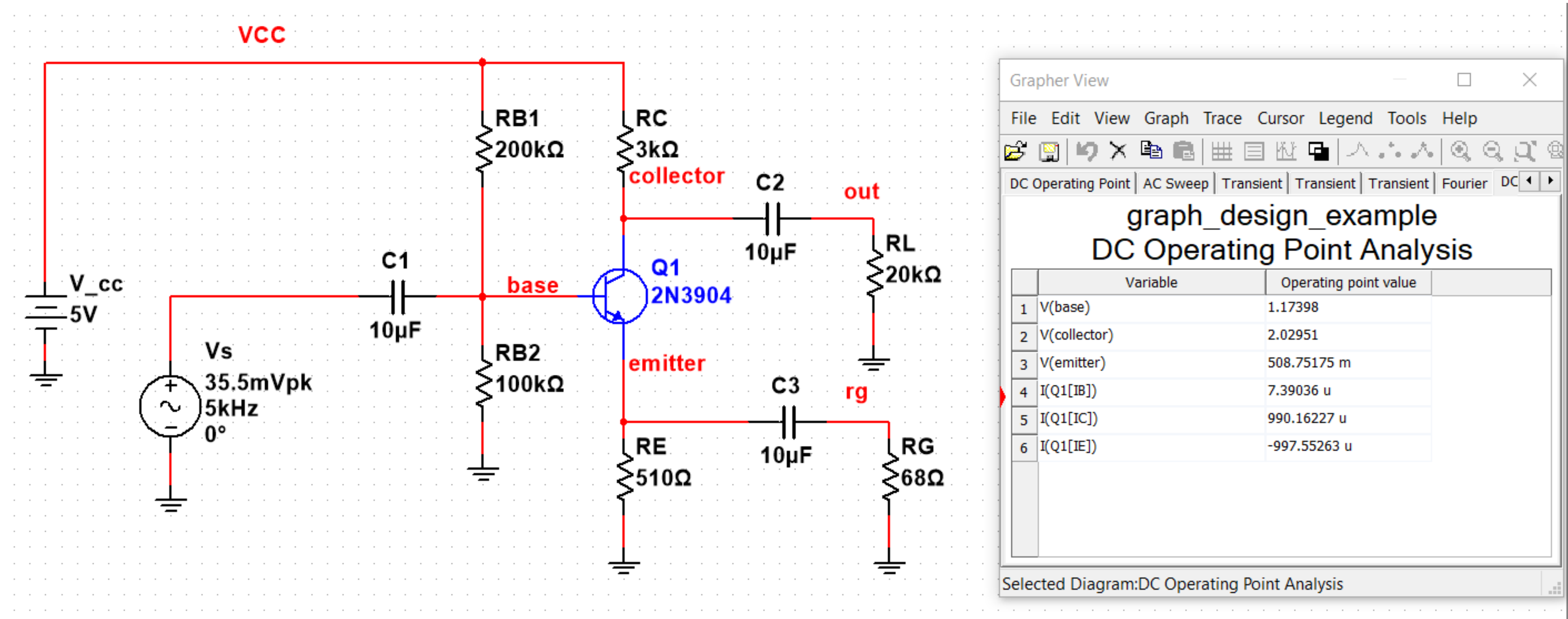
Design Equation Plots



Plots done with β=150

- Chosen design point is I_C=1mA, R_C=3kΩ

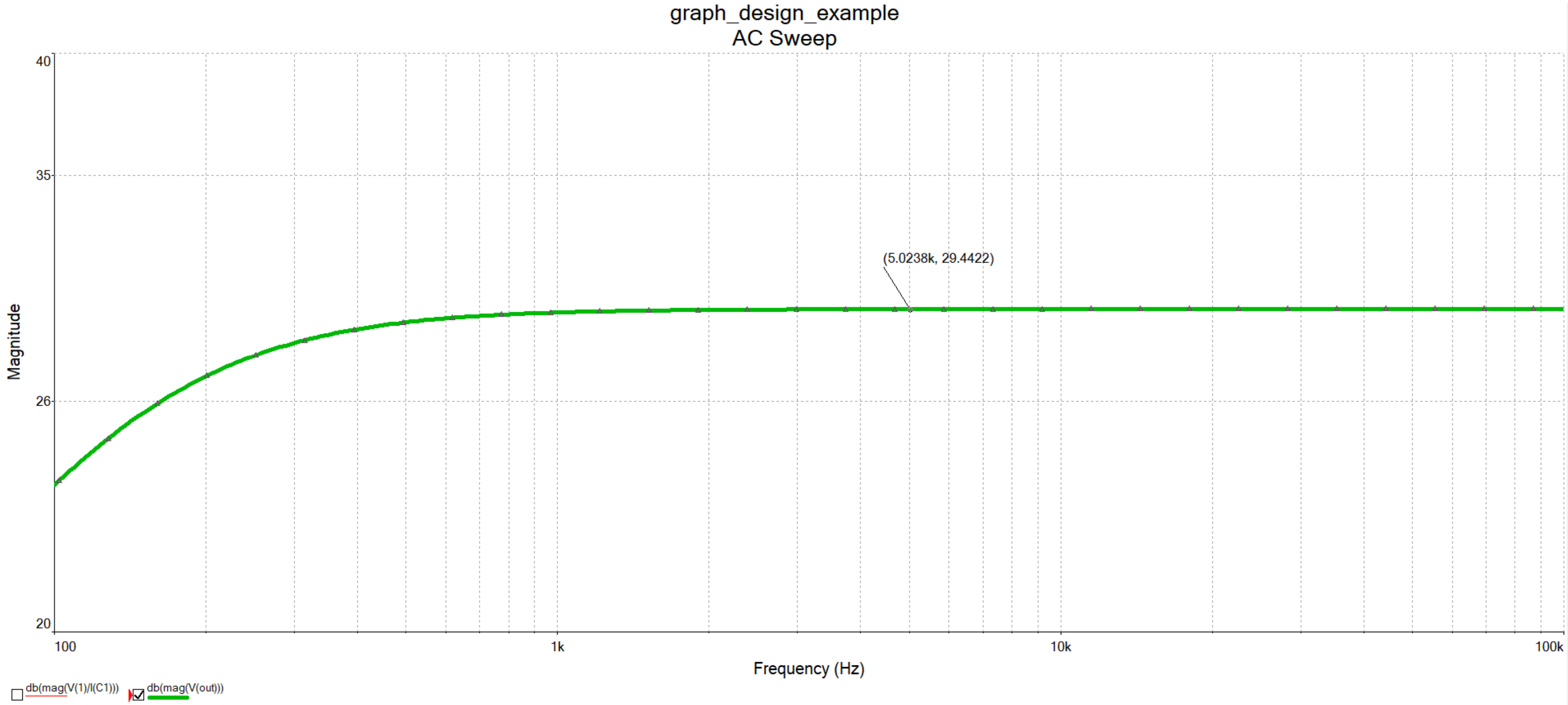
DC Operating Points



	Variable	Operating point value
1	V(base)	1.17398
2	V(collector)	2.02951
3	V(emitter)	508.75175 m
4	I(Q1[IB])	7.39036 u
5	I(Q1[IC])	990.16227 u
6	I(Q1[IE])	-997.55263 u

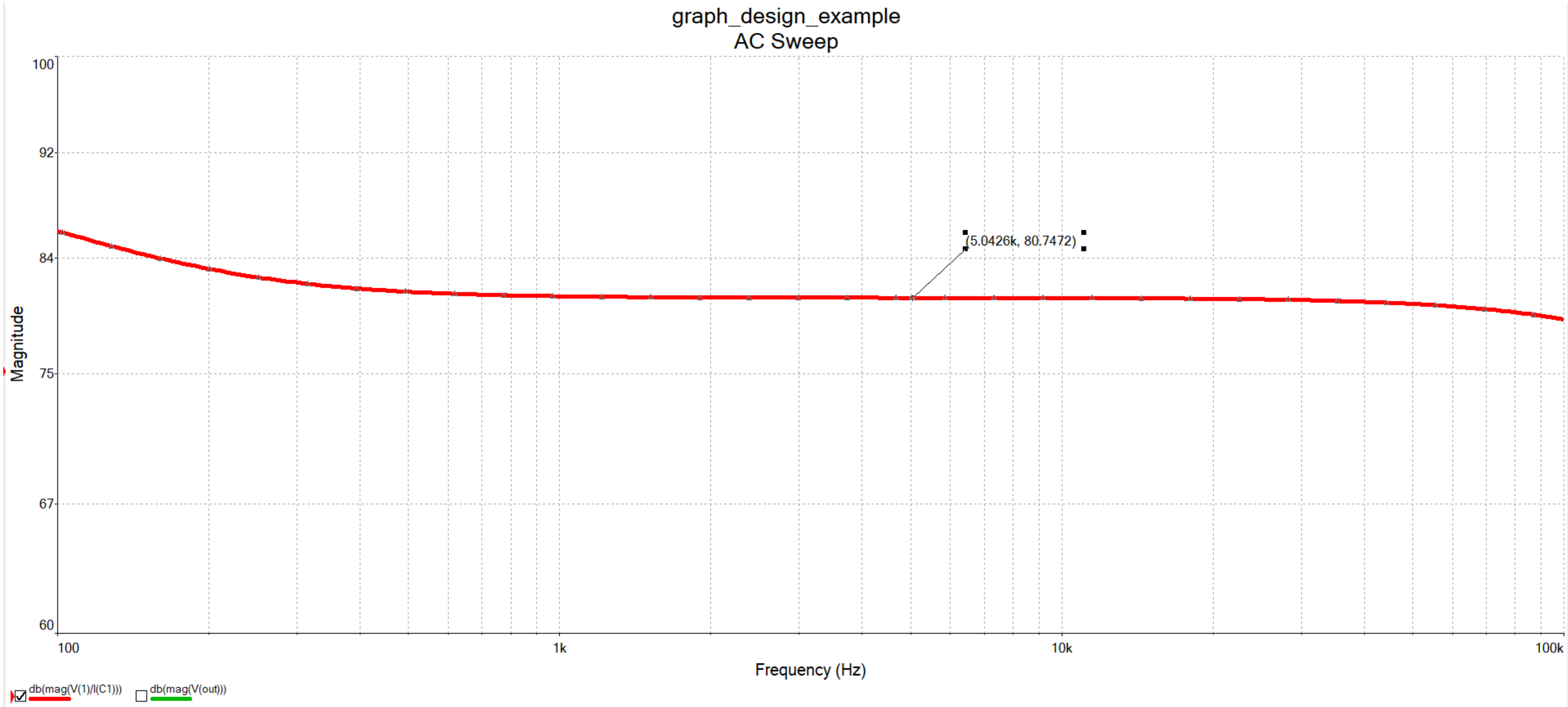
- R_E is set with $V_E = I_E R_E$
- R_G is set as R_{in}/β
- DC bias points must be reasonable for the circuit to work as designed!

AC Gain



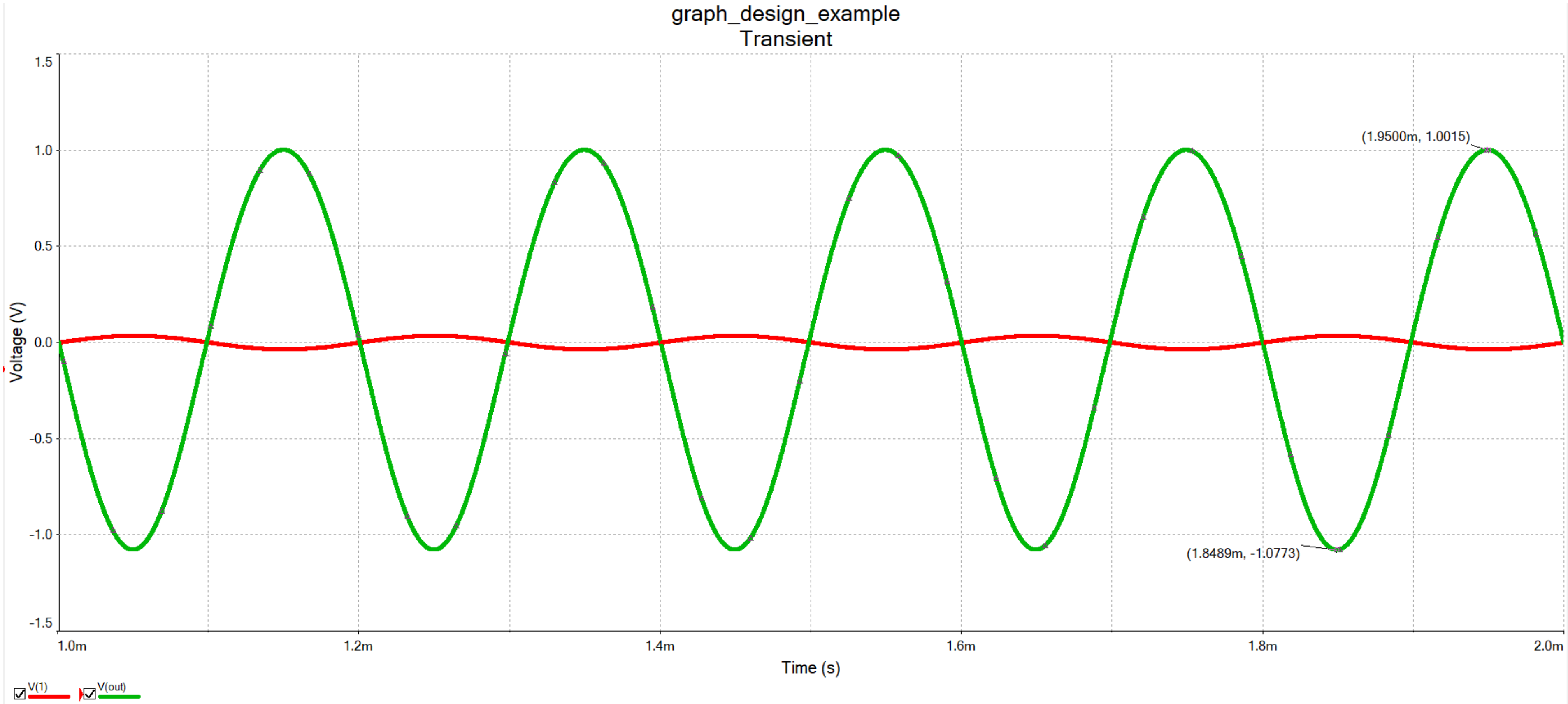
- $|A_v|$ =29.4dB=29.5V/V

R_{in}



- $R_{in} = 80.7dB\Omega = 10.8k\Omega$

Transient Response

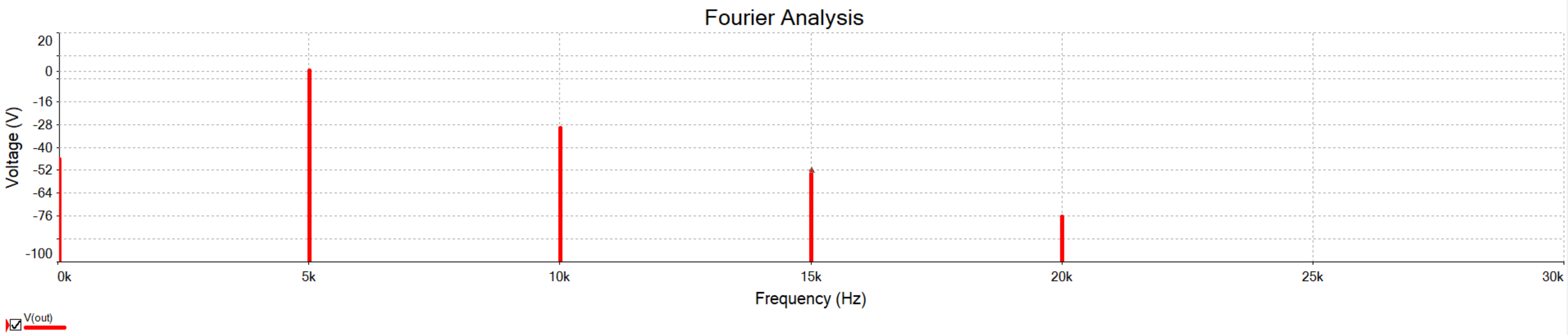


- Response with 35.5mV$_{pk}$ input signal
- Signal is beginning to compress

Total Harmonic Distortion

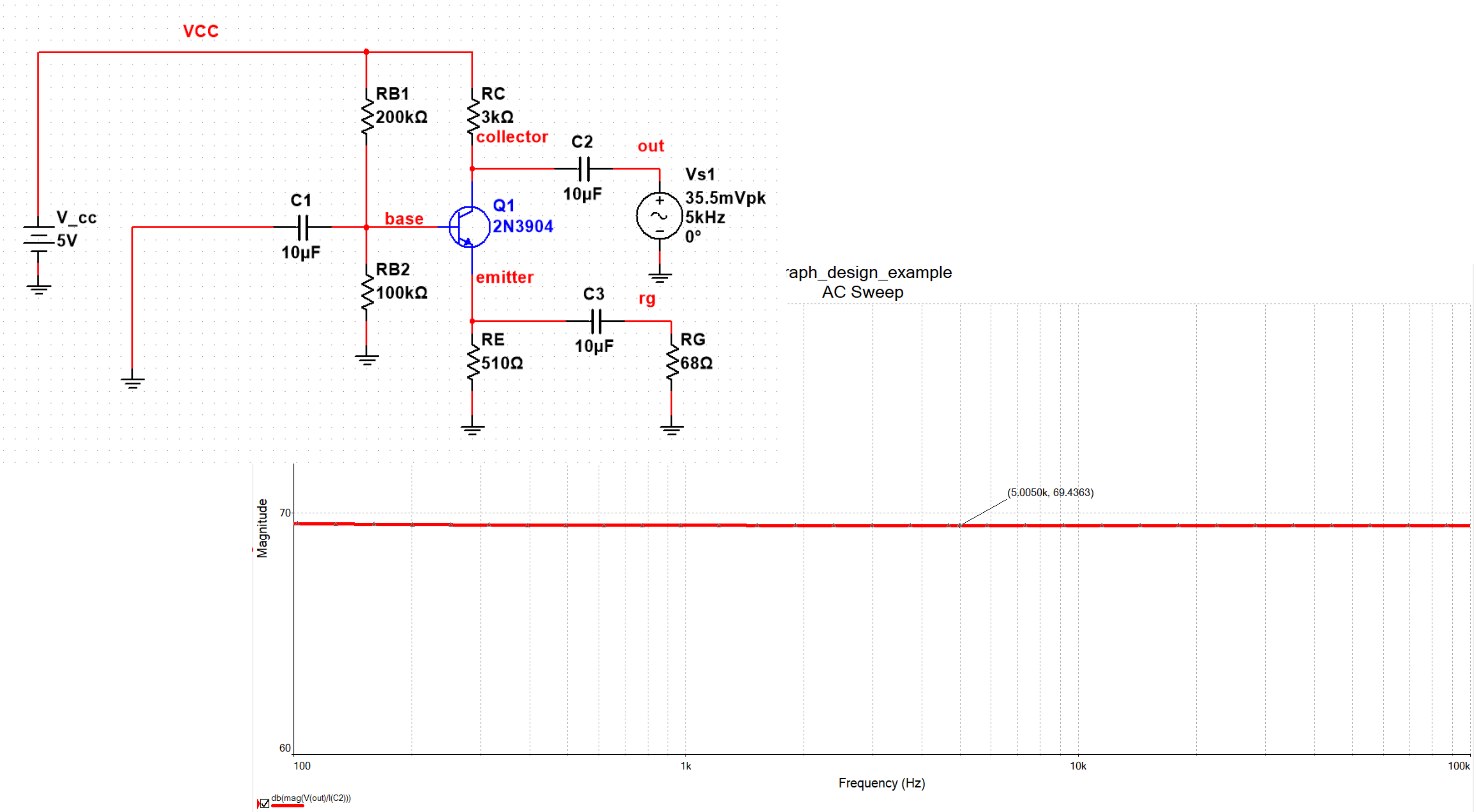
graph_design_example

1	Fourier analysis for V(out					
2	DC component:	0.00476869				
3	No. Harmonics:	10				
4	THD:	3.15844 %				
5	Grid size:	256				
6	Interpolation Degree:	1				
7						
8	Harmonic	Frequency	Magnitude	Phase	Norm. Mag	Norm. Phase
9	0	0	0.00476869	0	0.00457648	0
10	1	5000	1.042	-178.38	1	0
11	2	10000	0.0328185	93.9458	0.0314957	272.327
12	3	15000	0.00245989	-175.03	0.00236074	3.34859
13	4	20000	0.000150432	-84.251	0.000144369	94.1302
14	5	25000	8.29323e-006	10.0916	7.95896e-006	188.473
15	6	30000	4.13012e-006	-6.1577	3.96365e-006	172.224
16	7	35000	3.15322e-006	1.56041	3.02612e-006	179.942



- THD = 3.16% = -30dB

R_{out}



- R_{out} = 69.4dBΩ = 2.95kΩ ≈ R_C

Lab1 Design Specs

- $|A_v| \geq |-15|$
- $R_{in} \geq 5k\Omega$
- $R_L = 10k\Omega$
- $V_{omax} = 1V_{pk}$ w/ THD $\leq$ 5% (-26.0dB)
- $V_{CC} = 5V$
- $V_E \geq 0.5V$
- Isupply $\leq$ 4mA
- Nominal operation at 5kHz