ECEN 326
Fall 2015 Lab Policy

Section 500: T 11:00 AM – 01:50 PM (CVLB 423)
Section 501: F 11:30 AM – 02:20 PM (CVLB 423)

TA: Noah Hae-woong Yang
Office: WERC 015F
Office Hours: W 3 – 5PM
Email: hwyang@tamu.edu

Grading:
  Pre-labs 40%
  • One report per person
  • SPICE simulation verification takes 50% of the Pre-lab grade
  • Due at the beginning of the lab. Pre-lab will be quickly reviewed by TA as the lab starts.
  • No late pre-labs will be accepted without a valid excuse (24 hrs in advance)

Lab Reports 50%
  • One report per group/person
  • Double-side printing is highly recommended
  • Due at the beginning of the following lab sessions, 30% penalty for one day late and after that no credit

Lab Performance 10%
  • Punctuality - Lab experiments get started and finished on time
  • Violation of the Safety Rules such as bringing in food/drink in the lab is NOT taken lightly

Policies
  • Pre-labs may be hand written but they need to be legible and understandable.
  • Pre-labs must be:
    ➢ Clean sheet of paper (do not use paper that has been previously used for printing unrelated text)
    ➢ Clear handwriting (consider typing the text part of your pre-labs)
    ➢ Follow the same components labeling as in the lab manual
    ➢ Numbered equations
    ➢ Boxed final results
  • Reports must be TYPED, please do not cut-and-paste from the lab manual. Make sure all plots/schematics have white background by inverting colors if necessary. The grader cannot read scale or result curve if the background remains black
  • Plots/Pictures need to have captions, axis names, and annotations if needed.
  • No food or drink in the lab
### ECEN 326 Lab Schedule, Fall of 2015 (Subject to change)

<table>
<thead>
<tr>
<th>Lab No.</th>
<th>Lab Time</th>
<th>Report Due</th>
<th>Topic</th>
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</table>
| 1       | Sep 17, T 11AM-1:50PM  
          Sep 18, F 11:30AM-2:20PM | Beginning of next lab | Design of a Common-Emitter BJT Amplifier |
| 2       | Sep 24, T 11AM-1:50PM  
          Sep 25, F 11:30AM-2:20PM | Beginning of next lab | Design of a Three-Stage BJT Amplifier |
| 3       | Oct 1, T 11AM-1:50PM  
          Oct 2, F 11:30AM-2:20PM | Beginning of next lab | Design of a Common-Source MOSFET Amplifier with a Source Follower |
| 4       | Oct 8, T 11AM-1:50PM  
          Oct 9, F 11:30AM-2:20PM | Beginning of next lab | Design of a BJT Differential Amplifier |
| 5       | Oct 15, T 11AM-1:50PM  
          Oct 16, F 11:30AM-2:20PM | Beginning of next lab | Design of a MOS Differential Amplifier |
| 6       | Oct 22, T 11AM-1:50PM  
          Oct 23, F 11:30AM-2:20PM | Beginning of next lab | Design of Current Mirrors |
| 7       | Oct 29, T 11AM-1:50PM  
          Oct 30, F 11:30AM-2:20PM | Beginning of next lab | Design of a BJT Operational Transconductance Amplifier |
| 8       | Nov 5, T 11AM-1:50PM  
          Nov 6, F 11:30AM-2:20PM | Beginning of next lab | Frequency Response of a Common-Emitter BJT Amplifier |
| 9       | Nov 12, T 11AM-1:50PM  
          Nov 13, F 11:30AM-2:20PM | Beginning of next lab | Frequency Response of a Cascode BJT Amplifier |
| 10      | Nov 19, T 11AM-1:50PM  
          Nov 20, F 11:30AM-2:20PM | Beginning of next lab | Design of a BJT Shunt-Series Feedback Amplifier |
| 11      | Dec 3, T 11AM-1:50PM  
          Dec 4, F 11:30AM-2:20PM | Dec 11 | Design of a Two-Stage Amplifier with Miller Compensation (Extra credit) |