ECEN 326 Lab 2
Design of a Three-Stage BJT Amplifier

Circuit Topology

Figure 1 shows the three-stage amplifier to be designed in this lab. The first stage is a common-emitter amplifier, which is followed by a common-base stage. This combination is known as the cascode amplifier. An emitter follower is added as the final stage.

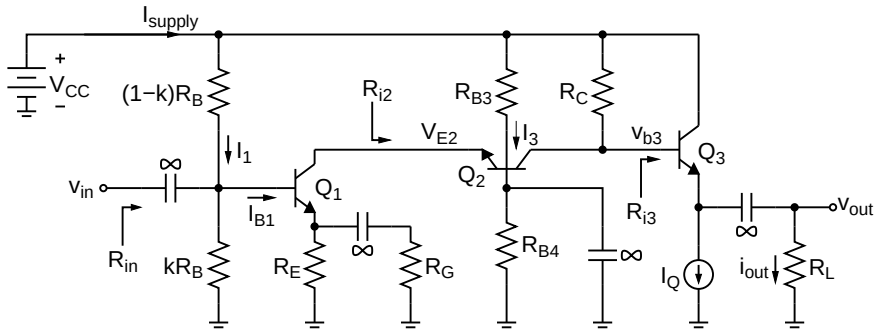

Figure 1: Cascode amplifier with an emitter follower

For β-insensitive DC biasing, the base current of Q_1 (I_{B1}) should be negligible compared to I_1:

$$I_{B1} \ll I_1 \;\Rightarrow\; \frac{I_{C1}}{\beta} \ll \frac{V_{CC}}{R_B} \;\Rightarrow\; N\frac{I_{C1}}{\beta} = \frac{V_{CC}}{R_B} \;\Rightarrow\; R_B = \frac{\beta V_{CC}}{NI_{C1}}, \quad N \geq 10 \tag{1}$$

Small-signal AC voltage gain (A_v) can be expressed as

$$A_v = \left|\frac{v_{out}}{v_{in}}\right| = \frac{R_{i2}}{r_{e1} + (R_E \parallel R_G)} \frac{R_C \parallel R_{i3}}{R_{i2}} A_F \;\Rightarrow\; r_{e1} + (R_E \parallel R_G) = \frac{R_C \parallel R_{i3}}{A_v} A_F \tag{2}$$

where

$$A_F = \frac{v_{out}}{v_{b3}} = \frac{R_L}{r_{e3} + R_L} \tag{3}$$

$$R_{i3} = (\beta + 1)(r_{e3} + R_L) \tag{4}$$

Input resistance of the amplifier (R_{in}) can be calculated as

$$R_{in} = kR_B \parallel (1-k)R_B \parallel (\beta+1)[r_{e1} + (R_E \parallel R_G)] \approx k(1-k)R_B \parallel \beta[r_{e1} + (R_E \parallel R_G)] \tag{5}$$

Substituting R_B from (1) and $[r_{e1} + (R_E \parallel R_G)]$ from (2) into (5) results in

$$R_{in} = \left(k(1-k)\frac{\beta V_{CC}}{NI_{C1}}\right) \parallel \left(\beta \frac{R_C \parallel R_{i3}}{A_v} A_F\right) = \frac{\beta}{\dfrac{NI_{C1}}{k(1-k)V_{CC}} + \dfrac{A_v}{(R_C \parallel R_{i3})A_F}} \tag{6}$$

The small-signal AC voltage gain from v_{in} to v_{e2} is less than unity. Therefore, the AC signal swing at v_{e2} can be assumed to be limited by the maximum input signal amplitude ($V_{i,max}$), which can be calculated by dividing the required output swing to the gain specification. To avoid clipping at v_{e2}, the DC bias at V_{E2} can be chosen as

$$V_{E2} \geq V_{E1} + V_{CE,sat} + V_{i,max} \tag{7}$$

To maximize the available output swing, load-line analysis needs to be performed. Assume that Q_2's DC operating point is set to (I_{C2}, V_{CE2}). From Fig. 1

$$V_{CC} \approx I_{C2}R_C + V_{CE2} + V_{E2} \;\Rightarrow\; V_{CE2} = V_{CC} - I_{C2}R_C - V_{E2} \tag{8}$$

Please note that the above expression is valid only if $I_{C2} \gg I_{B3}$. Since I_{C3} is usually a large current, this requirement usually determines the minimum amount of I_{C2}. AC load line equation for Q_2 (see Fig. 2) can be obtained as

$$\frac{i_{c2} - I_{C2}}{v_{ce2} - V_{CE2}} \approx -\frac{1}{R_C \parallel R_{i3}} \tag{9}$$

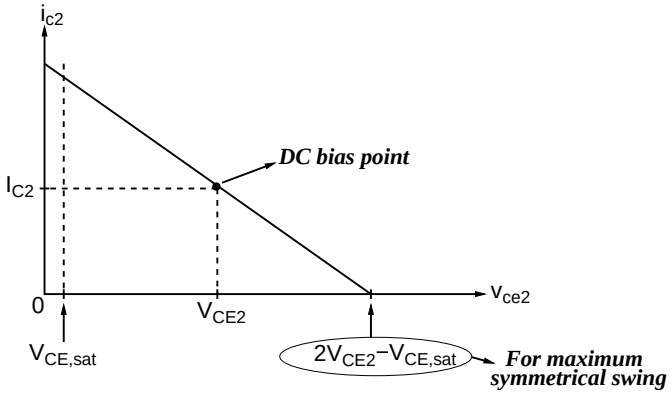

Figure 2: AC load line

Evaluating the load-line equation at the point $(i_{c2}, v_{ce2}) = (0, 2V_{CE2} - V_{CE,sat})$,

$$\frac{0 - I_{C2}}{2V_{CE2} - V_{CE,sat} - V_{CE2}} = -\frac{1}{R_C \parallel R_{i3}} \tag{10}$$

which can be arranged as

$$I_{C2}(R_C \parallel R_{i3}) = V_{CE2} - V_{CE,sat} \tag{11}$$

Substituting V_{CE2} from (8) into (11) results in

$$I_{C2} = \frac{V_X}{R_C + (R_C \parallel R_{i3})} = I_{C1} \tag{12}$$

where

$$V_X = V_{CC} - V_{E2} - V_{CE,sat} \tag{13}$$

0-to-peak voltage swing at the output can be calculated as

$$V_{sw} = I_{C2}(R_C \parallel R_{i3})A_F = \frac{V_X}{2 + \dfrac{R_C}{R_{i3}}} A_F \tag{14}$$

Substituting I_{C1} in (12) into (6), R_{in} can be expressed as

$$R_{in} = \frac{\beta(R_C \parallel R_{i3})}{\dfrac{NV_X}{k(1-k)V_{CC}} \dfrac{1}{2 + \dfrac{R_C}{R_{i3}}} + \dfrac{A_v}{A_F}} \tag{15}$$

The final stage is an emitter follower, which should be designed to deliver the specified voltage swing to the load. Assuming large signals, KCL at the output node results in

$$i_{C3} = I_Q + i_{out} \tag{16}$$

where i_{out} is a sine wave and I_Q is a DC current. Since $i_{C3} > 0$ for Q_3 to be active, i_{out} cannot be lower than $-I_Q$ during the negative cycle of the sine wave. Using the specifications for the output swing and load resistor, I_Q can be determined from

$$I_Q \geq \frac{\text{0-to-peak output swing}}{R_L} \tag{17}$$

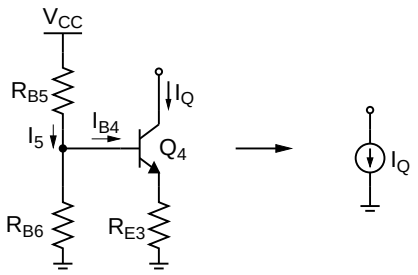

Figure 3: DC current source

The current source can be designed using the circuit in Fig. 3, where I_Q can be calculated from

$$I_Q = \frac{V_{CC}\dfrac{R_{B6}}{R_{B5}+R_{B6}} - 0.7}{R_{E3}} \tag{18}$$

In general, all DC bias points in the circuit should be insensitive to variations in β. Therefore, R_{B3}, R_{B4}, R_{B5} and R_{B6} should be chosen such that:

$$I_{B2} \ll I_3 \tag{19}$$

$$I_{B4} \ll I_5 \tag{20}$$

Design Procedure

1. Choose I_Q such that (17) is satisfied.
2. Since $I_{C3} = I_Q$, calculate A_F and R_{i3} from (3) and (4).
3. Choose the value of V_{E1}, and then find V_{E2} from (7).
4. Calculate V_X from (13), and k from $k = (V_{E1} + 0.7)/V_{CC}$. Also choose N such that $N \geq 10$.
5. Determine the minimum value of R_C using the specification for the desired input resistance ($R_{in,d}$):

$$\frac{\beta(R_C \parallel R_{i3})}{\dfrac{NV_X}{k(1-k)V_{CC}}\dfrac{1}{2+\dfrac{R_C}{R_{i3}}} + \dfrac{A_v}{A_F}} \geq R_{in,d}$$

   which can be arranged as

$$R_C^2\left(\beta R_{i3} - R_{in,d}\frac{A_v}{A_F}\right) + R_C\left(2\beta R_{i3} - 3R_{in,d}\frac{A_v}{A_F} - QR_{in,d}\right)R_{i3} - R_{i3}^2 R_{in,d}\left(Q + 2\frac{A_v}{A_F}\right) \geq 0$$

   where

$$Q = \frac{NV_X}{k(1-k)V_{CC}}$$

6. Determine the maximum value of R_C using the specification for the desired output voltage swing ($V_{sw,d}$):

$$\frac{V_X}{2+\dfrac{R_C}{R_{i3}}}A_F \geq V_{sw,d} \;\Rightarrow\; R_C \leq R_{i3}\left(\frac{V_X A_F}{V_{sw,d}} - 2\right)$$

7. Choose R_C, then calculate $I_{C2} = I_{C1}$ from (12). Make sure that $I_{C2} \gg I_Q/\beta$, if not, repeat the steps above (as many steps as necessary) to obtain an acceptable I_{C2}.
8. Calculate R_B and R_E

$$R_B = \frac{\beta V_{CC}}{NI_{C1}} \quad , \quad R_E = \frac{V_E}{I_{C1}}$$

9. Find R_G from (2), which can be arranged as

$$R_G = \frac{1}{\frac{1}{\left(\frac{R_C \parallel R_{i3}}{A_v} A_F - r_{e1}\right)} - \frac{1}{R_E}}$$

10. Choose V_{E4} such that $V_{E4} + V_{CE,sat} \leq V_{E3} - V_{out,0-to-peak}$, then calculate $R_{E3} \approx V_{E4}/I_Q$.

11. Find R_{B3}, R_{B4}, R_{B5} and R_{B6} while (19) and (20) are satisfied.

Calculations and Simulations

Using 2N3904 BJTs, design the 3-stage amplifier in Fig. 1 with the following specifications:

$V_{CC} = 5\ V$	$R_L = 100\ \Omega$	Operating frequency: 5 kHz
$\lvert A_v \rvert = 30$	$R_{in} \geq 3k\ \Omega$	Zero-to-peak un-clipped swing at $V_{out} \geq 1.5\ V$
$I_{supply} \leq 20\ mA$	$V_{E1} \geq 1\ V$	$V_{E4} \geq 0.5\ V$

1. Show all your calculations, design procedure, and final component values.
2. Verify your results using a circuit simulator. Submit all necessary simulation plots showing that the specifications are satisfied. Also provide the circuit schematic with DC bias points annotated.
3. Using a circuit simulator, perform Fourier analysis and determine the input and the output signal amplitudes resulting in 5% total harmonic distortion (THD) at the output. Provide the simulation results.

Measurements

1. Construct the amplifier you designed.
2. Measure I_C, V_C, V_B and V_E for all transistors. If any DC bias value is significantly different than the one obtained from simulations, modify your circuit to get the desired DC bias before you move onto the next step.
3. Measure I_{supply}, A_v and R_{in}.
4. Measure the maximum un-clipped output signal amplitude.
5. Find the input signal amplitude resulting in 5% THD measurement at the output.

Report

1. Include calculations, schematics, simulation plots, and measurement plots.
2. Prepare a table showing calculated, simulated and measured results.
3. Compare the results and comment on the differences.

Demonstration

1. Construct the amplifier you designed on your breadboard and bring it to your lab session.
2. Your name and UIN must be written on the side of your breadboard.
3. Submit your report to your TA at the beginning of your lab session.
4. Measure I_{supply}, A_v and R_{in}.
5. Apply the input signal resulting in 5% THD at the output from your earlier measurements. Show the input and output waveforms, and THD measurement at the output.