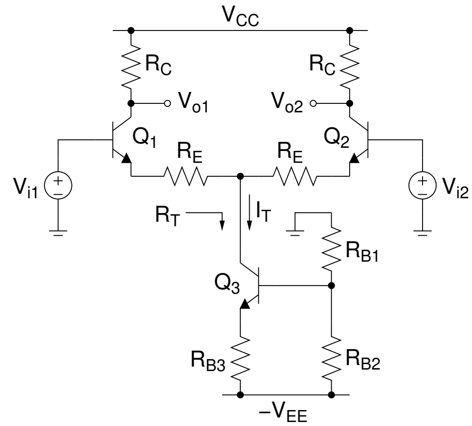
ECEN 326 Lab 4
Design of a BJT Differential Amplifier

Circuit Topology

The following figure shows a typical BJT differential amplifier. Assume $\beta \geq 100$ and $V_A = 75\ V$.



The tail current source (I_T) can be calculated from

$$I_T \approx \frac{\dfrac{R_{B2}}{R_{B1}+R_{B2}} V_{EE} - 0.7}{R_{B3}}$$

provided that $I_{B3} \ll I_{R_{B2}}$. DC collector currents of Q_1 and Q_2 are

$$I_{C1} = I_{C2} \approx \frac{I_T}{2}$$

Assuming $r_{o1}, r_{o2} \gg R_C, R_E,$ small-signal differential-mode gain can be obtained as

$$A_{dm} = \frac{v_{od}}{v_{id}} \approx -\frac{R_C}{r_{e1} + R_E}$$

where $r_{e1} \approx V_T / I_{C1}$. Common-mode gain can be found as

$$A_{cm} = \frac{v_{oc}}{v_{ic}} \approx -\frac{R_C}{r_{e1} + R_E + 2R_T}$$

where

$$R_T = r_{o3} + R_{BB} + g_{m3} \frac{r_{\pi 3}}{r_{\pi 3} + (R_{B1} \parallel R_{B2})} r_{o3} R_{BB}$$

$$R_{BB} = R_{B3} \parallel (r_{\pi 3} + (R_{B1} \parallel R_{B2}))$$

Common-mode rejection ratio (CMRR), differential-mode input resistance (R_{id}) and common-mode input resistance (R_{ic}) are given by

$$\text{CMRR} = 20 \log \left| \frac{A_{dm}}{A_{cm}} \right|$$

$$R_{id} \approx 2(\beta + 1)(R_E + r_{e1})$$

$$R_{ic} \approx (\beta + 1)(2R_T \parallel r_{o1})$$

Because of mismatches between the transistors and load resistors, a non-zero differential output voltage will result when the differential input voltage is zero. We may refer this output offset voltage back to the input as

$$V_{OS} = \frac{V_o}{A_{dm}}$$

V_{OS} is known as the input-referred offset voltage. Since the two sources of the offset voltage are uncorrelated, it can be estimated as

$$V_{OS} = V_T \sqrt{\left(\frac{\Delta R_C}{R_C}\right)^2 + \left(\frac{\Delta I_S}{I_S}\right)^2}$$

Calculations and Simulations

Design a BJT differential amplifier with the following specifications:

$V_{ic} = 0\ V$	$I_{supply} \leq 3\ mA$	Zero-to-peak un-clipped swing at $V_{o1} \geq 2.5\ V$
$V_{CC} = V_{EE} = 5\ V$	$\lvert A_{dm}\rvert = 40$	Operating frequency: 1 kHz
$R_{id} \geq 20\ k\Omega$	CMRR $\geq 70\ dB$	

1. Show all your calculations and final component values.
2. Verify your results using a circuit simulator. Submit all necessary simulation plots showing that the specifications are satisfied. Also provide the circuit schematic with DC bias points annotated.
3. Using a circuit simulator, perform Fourier analysis and determine the differential input and output signal amplitudes resulting in 1% and 5% total harmonic distortion (THD) at the differential output. Provide the simulation results.

Measurements

1. Construct the amplifier you designed.
2. Connect V_{i1} and V_{i2} to ground and record all DC quiescent voltages and currents.
3. Measure I_{supply} and the output offset voltage $V_{o1} - V_{o2}$.
4. Apply differential input signals to the amplifier.
5. Measure the maximum un-clipped output signal amplitude at V_{o1}.
6. Measure A_{dm} and R_{id}.
7. Find the input signal amplitudes resulting in 1% and 5% THD measurements at the output.
8. Apply common input signals to the amplifier, measure A_{cm} and calculate CMRR.

Report

1. Include calculations, schematics, simulation plots, and measurement plots.
2. Prepare a table showing calculated, simulated and measured results.
3. Compare the results and comment on the differences.

Demonstration

1. Construct the amplifier you designed on your breadboard and bring it to your lab session.
2. Your name and UIN must be written on the side of your breadboard.
3. Submit your report to your TA at the beginning of your lab session.
4. Apply differential input signals to the amplifier, measure A_{dm} and R_{id}.
5. Apply the input signals resulting in 1% and 5% THD at the output from your earlier measurements. Show the input and output waveforms, and THD measurements at the output.
6. Apply common input signals to the amplifier, measure A_{cm} and calculate CMRR.