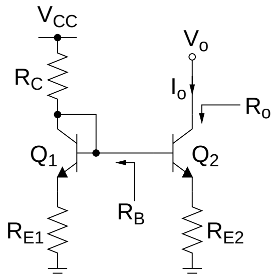
ECEN 326 Lab 6
Design of Current Mirrors

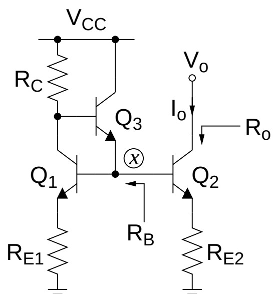
Circuit Topologies

NPN Simple Current Mirror:



$$I_o \approx \frac{V_{CC} - 0.7}{R_C + R_{E1}}\,\frac{R_{E1}}{R_{E2}}\,, \quad V_{o,min} = V_{CE2,sat} + I_o R_{E2}$$
$$R_o = g'_{m2} r_{o2} R'_E + r_{o2} + R'_E$$
$$g'_{m2} = g_{m2}\frac{r_{\pi 2}}{r_{\pi 2} + R_B}\,, \quad R'_E = R_{E2} \parallel (r_{\pi 2} + R_B)$$
$$R_B = R_C \parallel (r_{e1} + R_{E1})$$

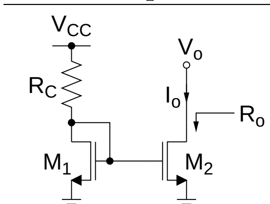
NPN Simple Current Mirror with β Helper:



$$I_o \approx \frac{V_{CC} - 1.4}{R_C + R_{E1}}\,\frac{R_{E1}}{R_{E2}}\,, \quad V_{o,min} = V_{CE2,sat} + I_o R_{E2}$$
$$R_o = g'_{m2} r_{o2} R'_E + r_{o2} + R'_E$$
$$g'_{m2} = g_{m2}\frac{r_{\pi 2}}{r_{\pi 2} + R_B}\,, \quad R'_E = R_{E2} \parallel (r_{\pi 2} + R_B)$$
$$R_B = \left(\frac{R_C}{\beta+1} + \frac{(\beta+1) r_{e1}}{N}\right) \parallel \left[\frac{r_{e1} + R_{E1}}{\beta}\left(1 + \frac{(\beta+1)^2 r_{e1}}{N R_C}\right)\right] \parallel (\beta+1)(r_{e1} + R_{E1})$$

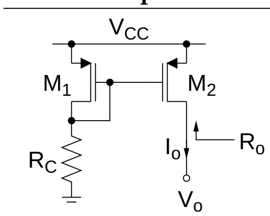
N : Number of base terminals connected to the node $\otimes$

NMOS Simple Current Mirror:



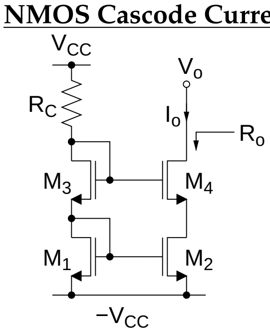
$$I_{D1} = \frac{V_{CC} - V_{GS1}}{R_C} = \frac{k'_n}{2}\left(\frac{W}{L}\right)_1 (V_{GS1} - V_{tn})^2\,, \quad V_{tn} < V_{GS1} < V_{CC}$$
$$I_o = \frac{(W/L)_2}{(W/L)_1} I_{D1}\,, \quad V_{o,min} = V_{GS1} - V_{tn} = V_{ov1}$$
$$R_o = r_{o2}$$

PMOS Simple Current Mirror:



$$I_{D1} = \frac{V_{CC} - V_{SG1}}{R_C} = \frac{k'_p}{2}\left(\frac{W}{L}\right)_1 (V_{SG1} - |V_{tp}|)^2\,, \quad |V_{tp}| < V_{SG1} < V_{CC}$$
$$I_o = \frac{(W/L)_2}{(W/L)_1} I_{D1}\,, \quad V_{o,max} = V_{CC} - (V_{SG1} - |V_{tp}|) = V_{CC} - V_{ov1}$$
$$R_o = r_{o2}$$

NMOS Cascode Current Mirror:



$$(W/L)_1 = (W/L)_3\,, \quad (W/L)_2 = (W/L)_4$$
$$I_{D1} = \frac{2V_{CC} - 2V_{GS1}}{R_C} = \frac{k'_n}{2}\left(\frac{W}{L}\right)_1 (V_{GS1} - V_{tn})^2\,, \quad V_{tn} < V_{GS1} < \frac{V_{CC}}{2}$$
$$I_o = \frac{(W/L)_2}{(W/L)_1} I_{D1}\,, \quad V_{o,min} = -V_{CC} + V_{GS1} + V_{ov1} = -V_{CC} + 2V_{ov1} + V_{tn}$$
$$R_o = g_{m4} r_{o4} r_{o2} + r_{o4} + r_{o2}$$

Calculations and Simulations

The following table shows transistor device parameters. Use $V_{CC} = 5V$ for all calculations.

NPN 2N3904	NMOS CD4007N	PMOS CD4007P
$\beta = 140$ $V_{CE,sat} = 0.2\ V$ $V_A = 75\ V$	$k_n' = 70\ \mu A/V^2$ $V_{tn} = 1.4\ V$ $W = 170\ \mu m$ $L = 10\ \mu m$ $\lambda_n = 0.016\ V^{-1}$	$k_p' = 15\ \mu A/V^2$ $V_{tp} = -1.65\ V$ $W = 360\ \mu m$ $L = 10\ \mu m$ $\lambda_p = 0.01\ V^{-1}$

1. Calculate R_C, R_o, and the output operating voltage range for the current mirrors in the following table:

(a)	NPN Simple Current Mirror	$R_{E1} = R_{E2} = 100\Omega$	$I_o = 1mA$
(b)	NPN Simple Current Mirror with β Helper	$R_{E1} = R_{E2} = 100\Omega$	$I_o = 1mA$
(c)	NPN Simple Current Mirror with β Helper	$R_{E1} = 100\Omega$, $R_{E2} = 50\Omega$, $Q_2 = 2 \times Q_1$ †	$I_o = 2mA$
(d)	NMOS Simple Current Mirror	$(W/L)_1 = (W/L)_2 = 170\mu/10\mu$	$I_o = 100\mu A$
(e)	NMOS Simple Current Mirror	$(W/L)_1 = 170\mu/10\mu$, $(W/L)_2 = 340\mu/10\mu$	$I_o = 200\mu A$
(f)	PMOS Simple Current Mirror	$(W/L)_1 = (W/L)_2 = 360\mu/10\mu$	$I_o = 100\mu A$
(g)	NMOS Cascode Current Mirror	$W/L = 170\mu/10\mu$	$I_o = 100\mu A$

† Q_2 is composed of two transistors (each identical to Q_1) connected in parallel.

2. For each current mirror, perform DC simulation by sweeping V_o from 0 to V_{CC} (for the cascode mirror, from $-V_{CC}$ to V_{CC}), and plot the output current I_o.

3. For each current mirror, perform AC simulation while $V_{o,dc} = 2V$, and plot the output resistance R_o.

4. Submit all simulation plots and the circuit schematics with DC bias points annotated (@ $V_o = 2V$).

Measurements

1. Construct all current mirrors you designed.

2. For each circuit, measure I_o, R_o and the output operating voltage range.

Report

1. Include calculations, schematics, simulation plots, and measurement plots.

2. Prepare a table showing calculated, simulated and measured results.

3. Compare the results and comment on the differences.

Demonstration

1. Construct all current mirrors you designed on your breadboard and bring it to your lab session.

2. Your name and UIN must be written on the side of your breadboard.

3. Submit your report to your TA at the beginning of your lab session.

4. For each circuit, measure I_o, R_o and the output operating voltage range.