# ECEN326: Electronic Circuits
# Fall 2022

## Lecture 3: Differential Amplifiers


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# Announcements

- HW
  - HW3 due today
- Reading
  - Razavi Chapter 10

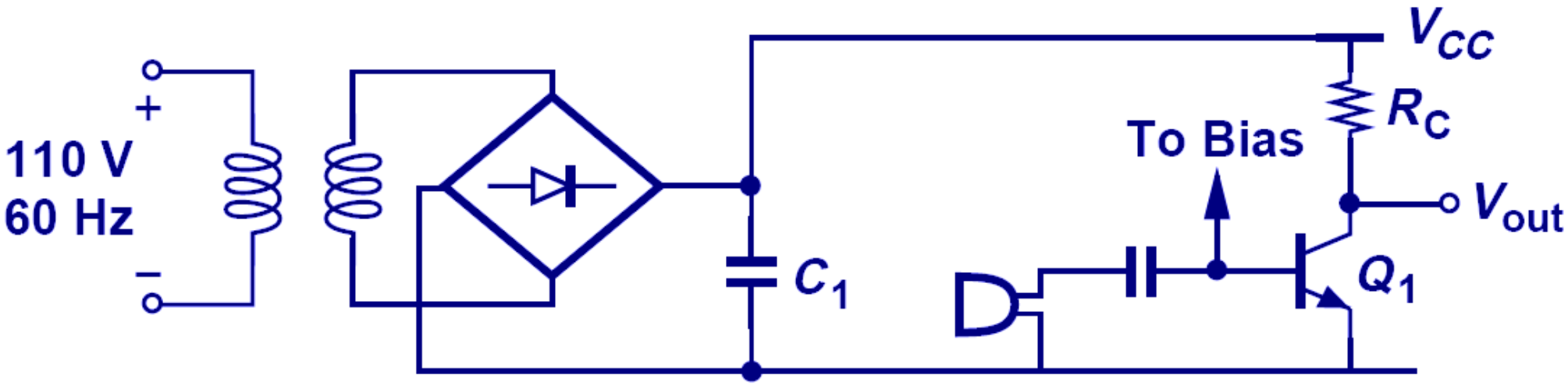
# Exam 1

- In class on Feb 24
- 9:35 – 11:00 (10 extra minutes)
- Closed book w/ one standard note sheet
- 8.5”x11” front & back
- Bring your calculator
- Covers through Lecture 3
- Sample Exam1s posted on website

# Agenda

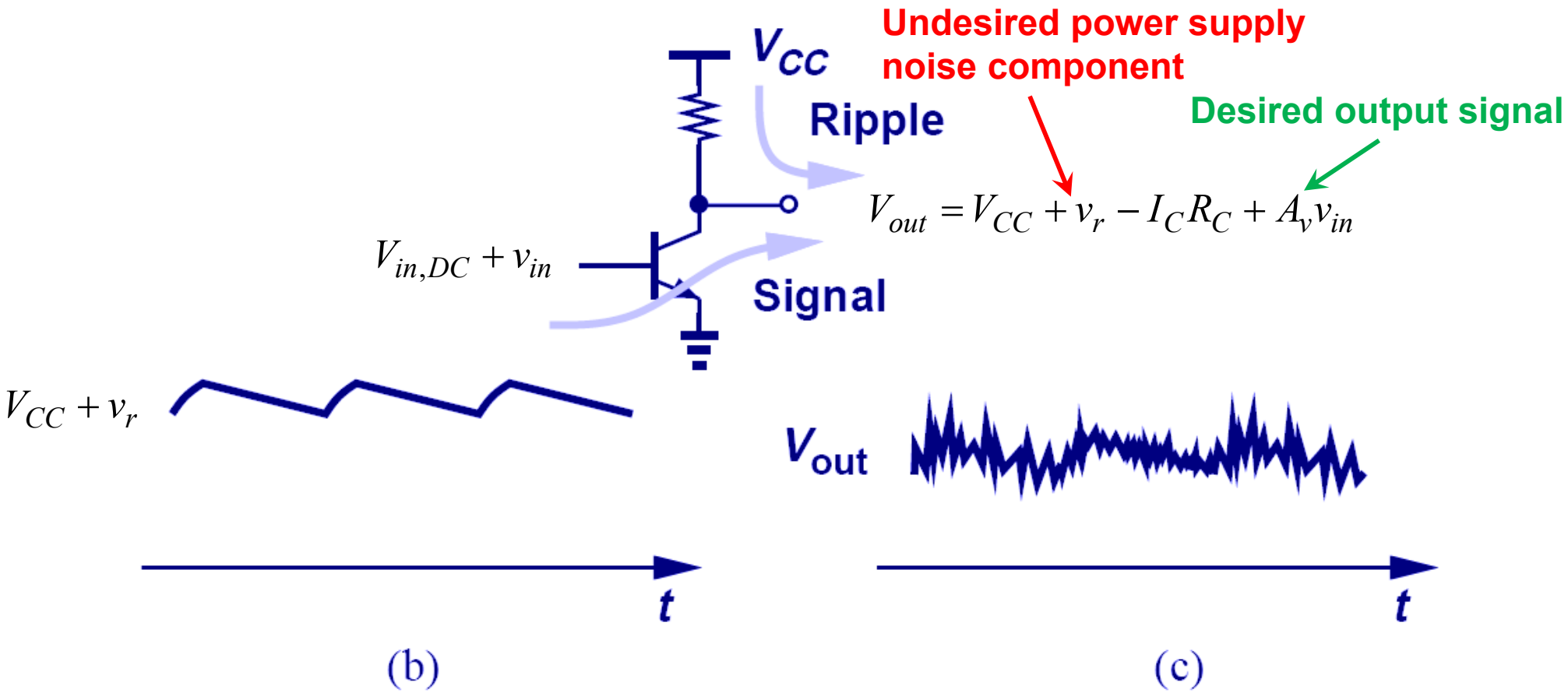
- General considerations
- Bipolar differential pair
- MOS differential pair
- Cascode differential amplifiers
- Common-mode rejection
- Differential pair with active load

# Audio Amplifier Example



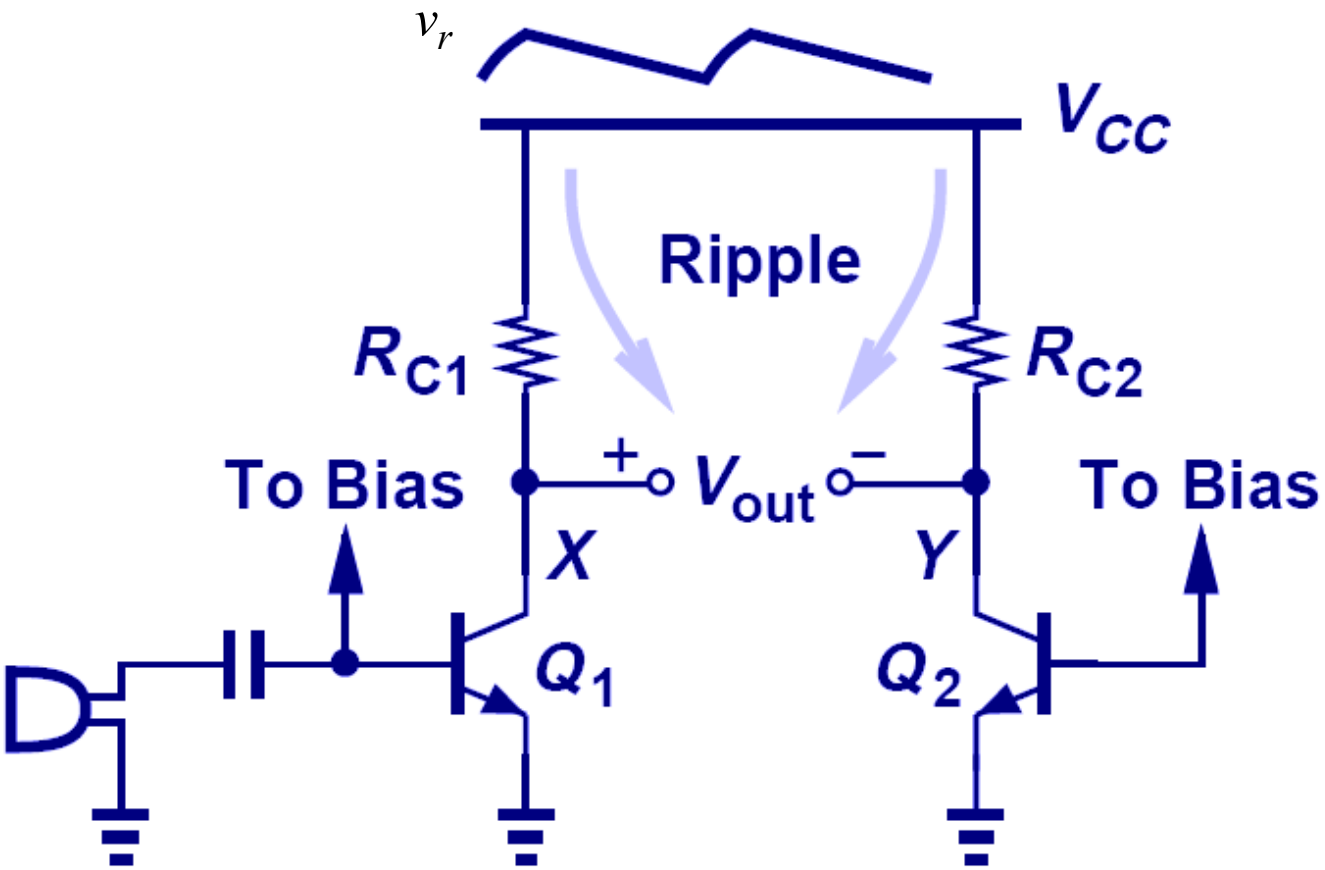

- **An audio amplifier is constructed above that takes on a rectified AC voltage as its supply and amplifies an audio signal from a microphone.**

# "Humming" Noise in Audio Amplifier Example




- However, $V_{CC}$ contains a ripple from rectification that leaks to the output and is perceived as a "humming" noise by the user.

# Supply Ripple Rejection



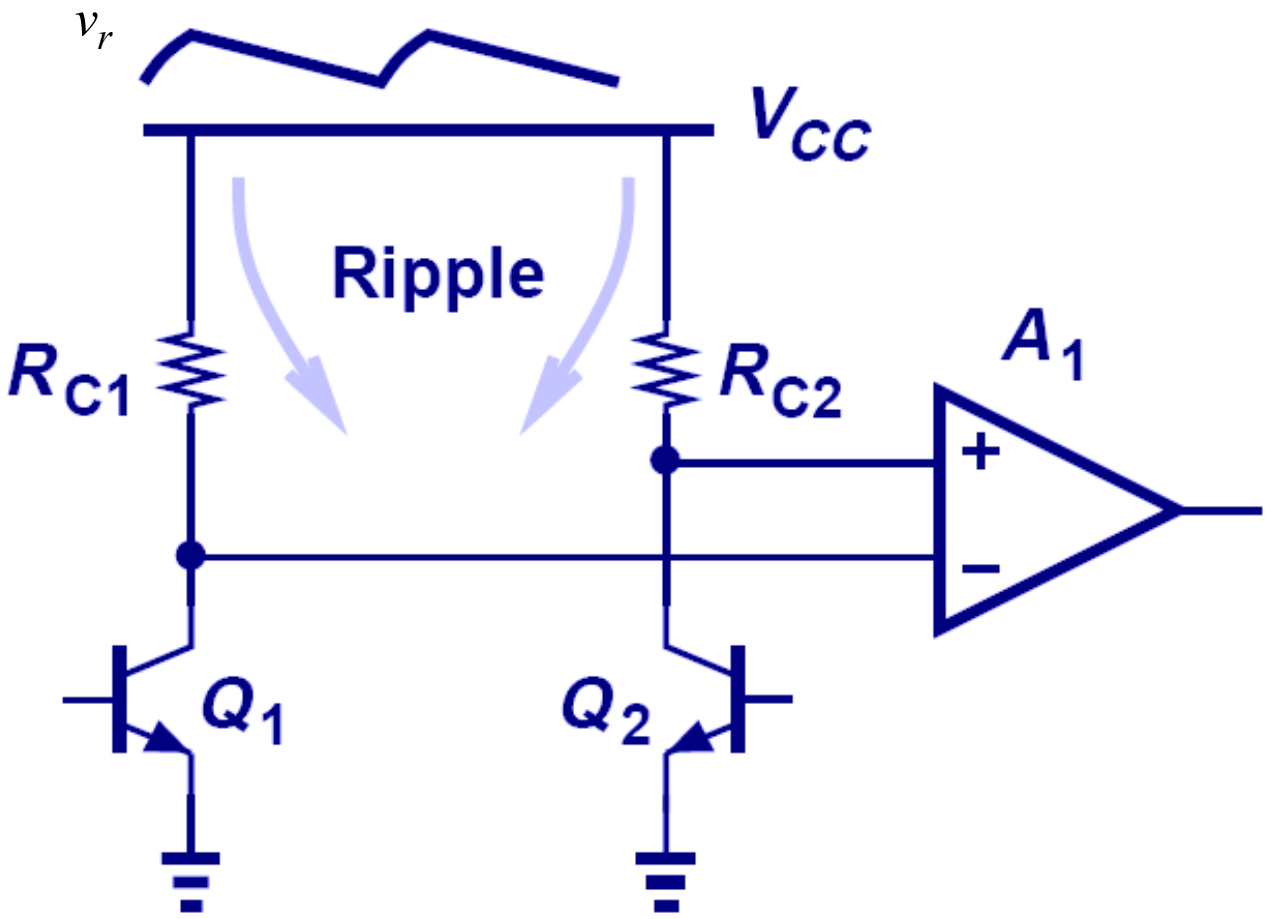

$$v_X = A_v v_{in} + v_r$$

$$v_Y = v_r$$

$$v_X - v_Y = A_v v_{in}$$

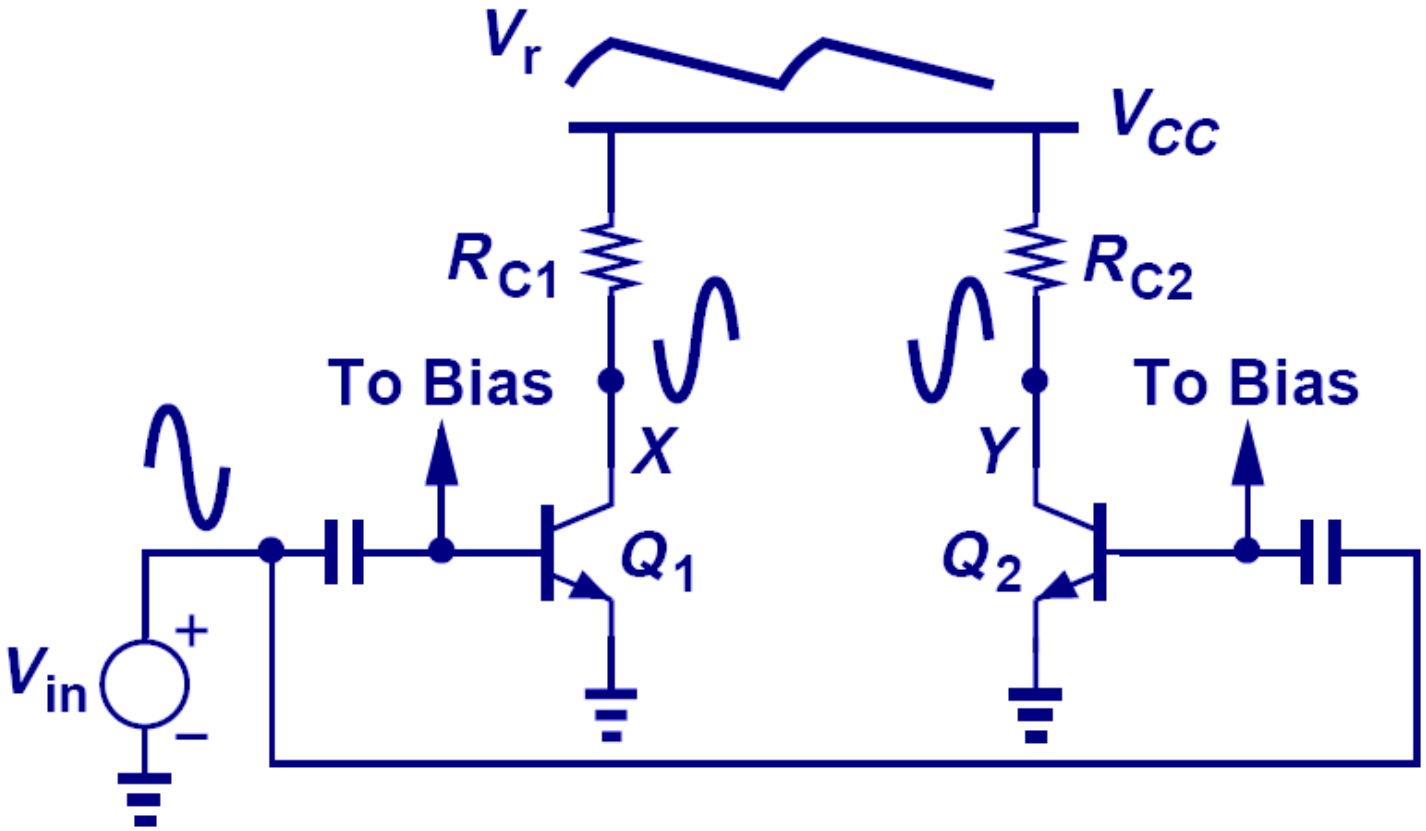
- Since both node X and Y contain the ripple, $v_r$, their difference will be free of ripple.

# Ripple-Free Differential Output




- Since the signal is taken as a difference between two nodes, an amplifier that senses differential signals is needed.
- How can we construct this differential amplifier?

# Common Inputs to Differential Amplifier



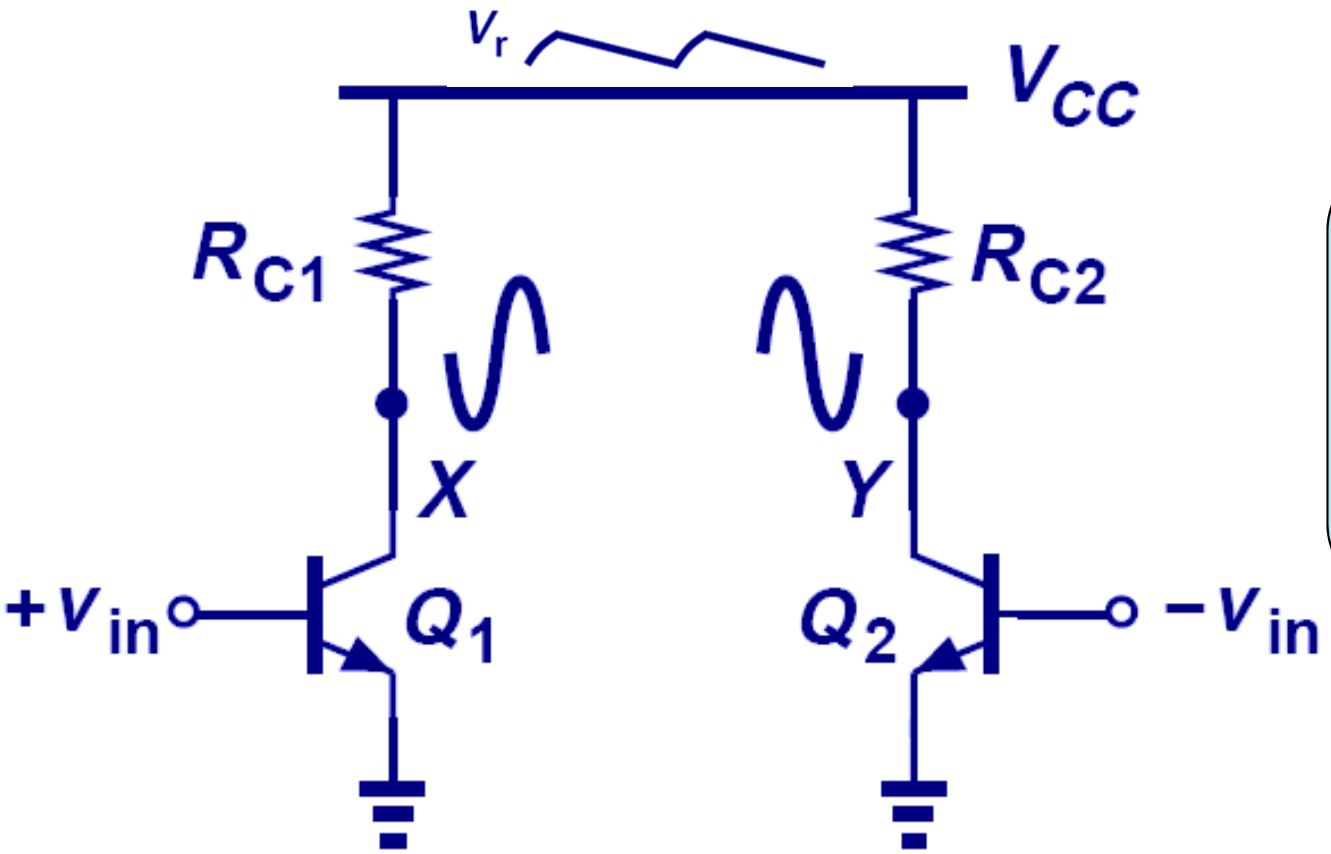

$$v_X = A_v v_{in} + v_r$$

$$v_Y = A_v v_{in} + v_r$$

$$v_X - v_Y = 0$$

- **Signals cannot be applied in phase to the inputs of a differential amplifier, since the outputs will also be in phase, producing zero differential output.**

# Differential Inputs to Differential Amplifier



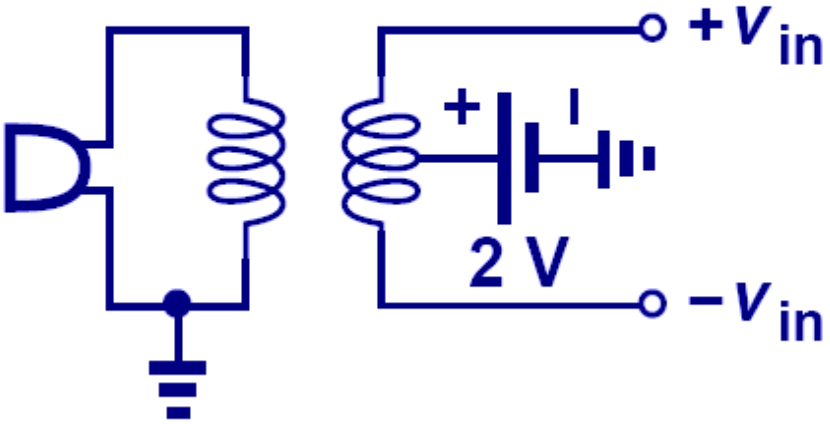

$$v_X = A_v v_{in} + v_r$$

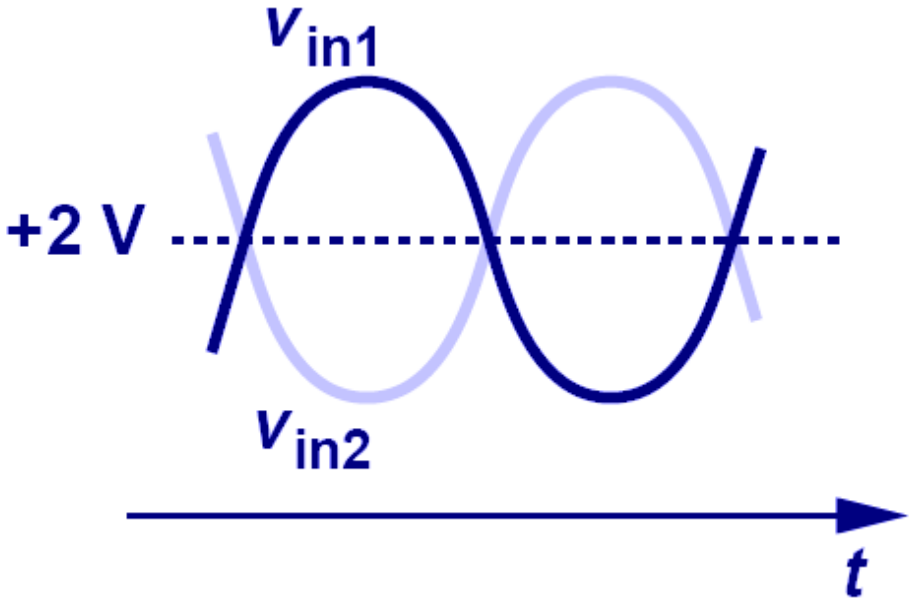
$$v_Y = -A_v v_{in} + v_r$$

$$v_X - v_Y = 2A_v v_{in}$$

- When the inputs are applied differentially, the outputs are 180° out of phase; enhancing each other when sensed differentially.
- Provides twice the output swing of the original amplifier

# Differential Signals

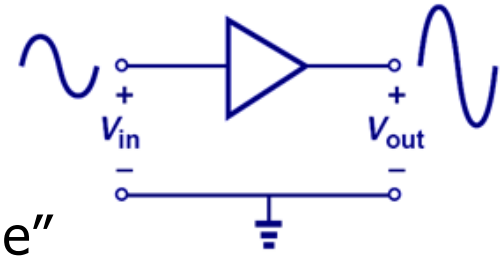


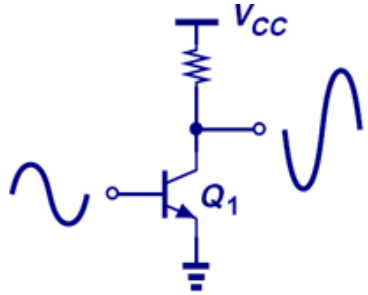




- A pair of differential signals can be generated, among other ways, by a transformer.
- Differential signals have the property that they share the same average value to ground and are equal in magnitude but opposite in phase.

# Single-ended vs. Differential Signals

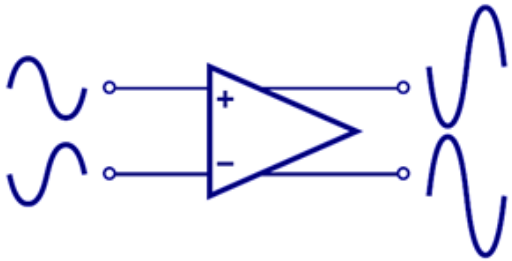
- Single-Ended Signals
  - Measured with respect to the common ground
  - Reside on one "line" or node

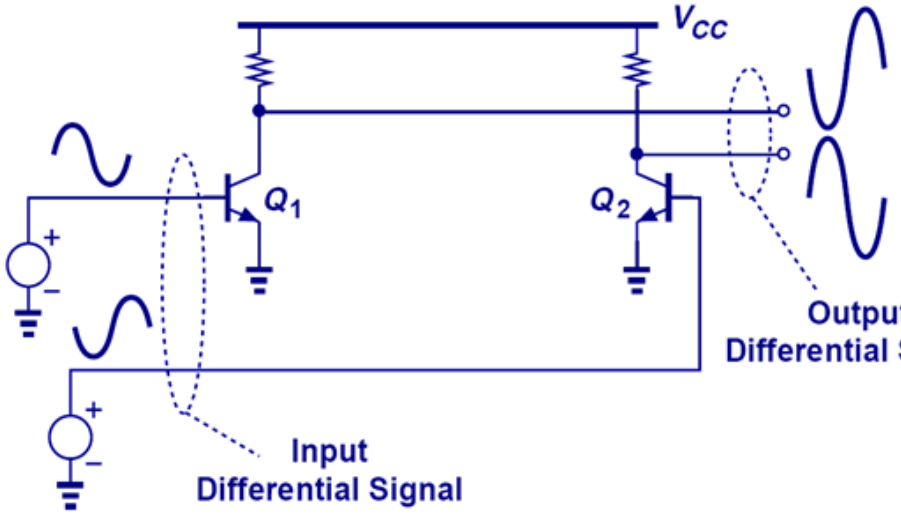



$$V_{out} = V_o \sin \omega t + V_{CM}$$

- Differential Signals
  - Measured between two nodes
  - Reside on two differential "lines" or nodes




$$V_1 = V_o \sin \omega t + V_{CM}$$

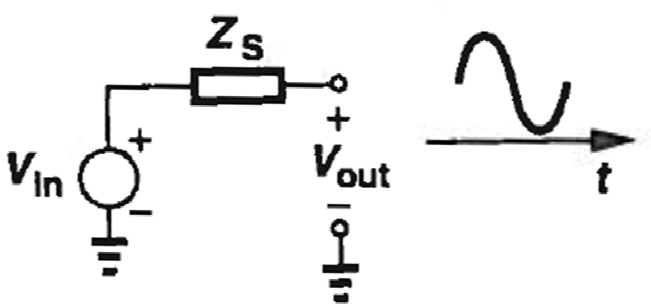
$$V_2 = -V_o \sin \omega t + V_{CM}$$

$$V_1 - V_2 = 2V_o \sin \omega t$$

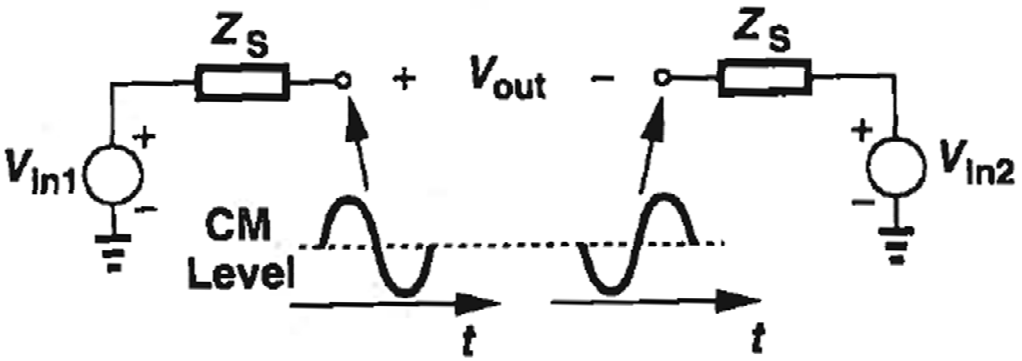
# Single-Ended & Differential Signals

- A single-ended signal is measured with respect to a fixed potential (ground)
- A differential signal is measured between two equal and opposite signals which swing around a fixed potential (common-mode level)
- You can decompose differential signals into a differential mode (difference) and a common-mode (average)

Single-Ended Signal



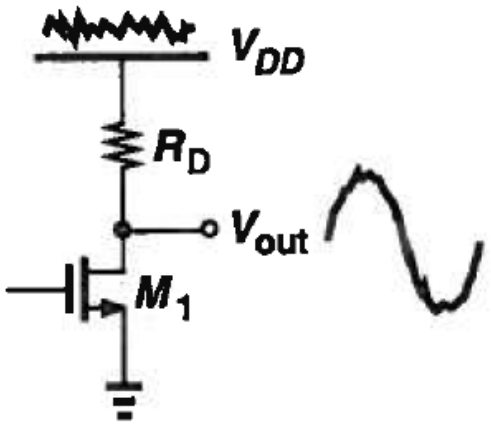

Differential Signal




$$V_{DM} = V_{out}^{+} - V_{out}^{-} \qquad V_{CM} = \frac{V_{out}^{+} + V_{out}^{-}}{2}$$

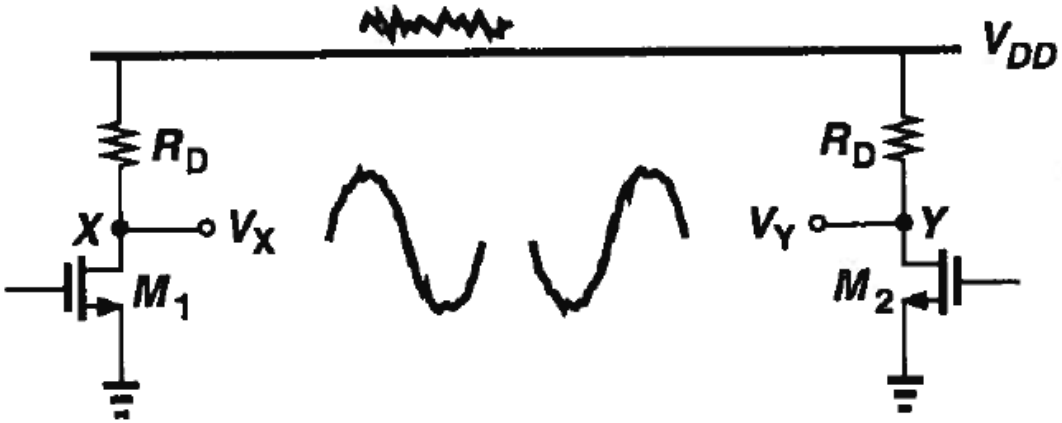
# Single-Ended & Differential Amplifiers

- Differential signaling advantages
  - Common-mode noise rejection
  - Higher (ideally double) potential output swing
  - Simpler biasing
  - Improved linearity
- Main disadvantage is area, which is roughly double
  - Although, to get the same performance in single-ended designs, we often have to increase the area dramatically




Max Output Swing

$$V_{DD} - (V_{GS} - V_{Tn})$$

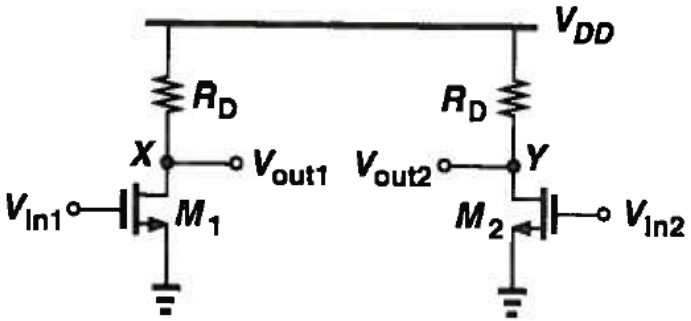


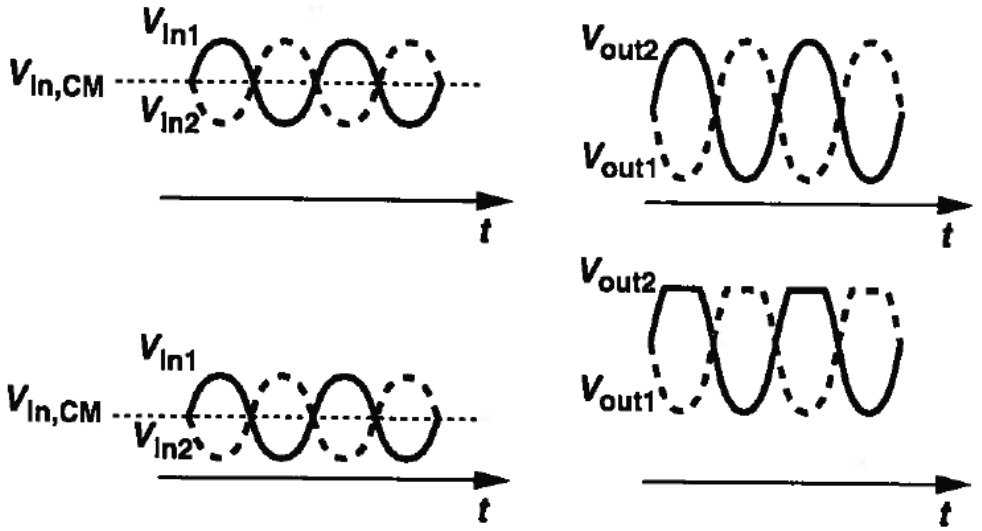

Max Output Swing

$$2(V_{DD} - (V_{GS} - V_{Tn}))$$

# Common-Mode Level Sensitivity

- A design which uses two single-ended amplifiers to realize a differential amplifier is very sensitive to the common-mode input level
- The transistors' bias current and transconductance can vary dramatically with the common-mode input
  - Impacts small-signal gain
  - Changes the output common-mode, which impacts the maximum output swing

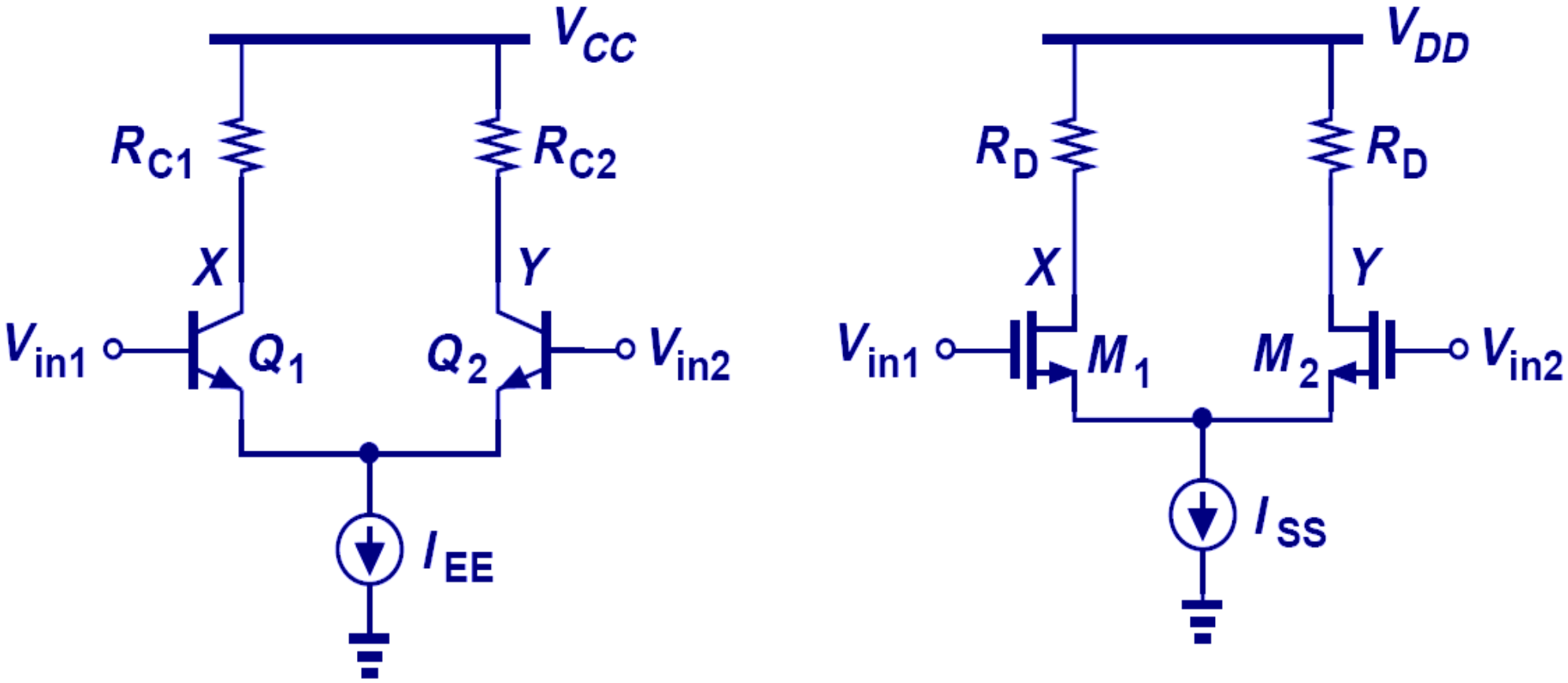


# Agenda

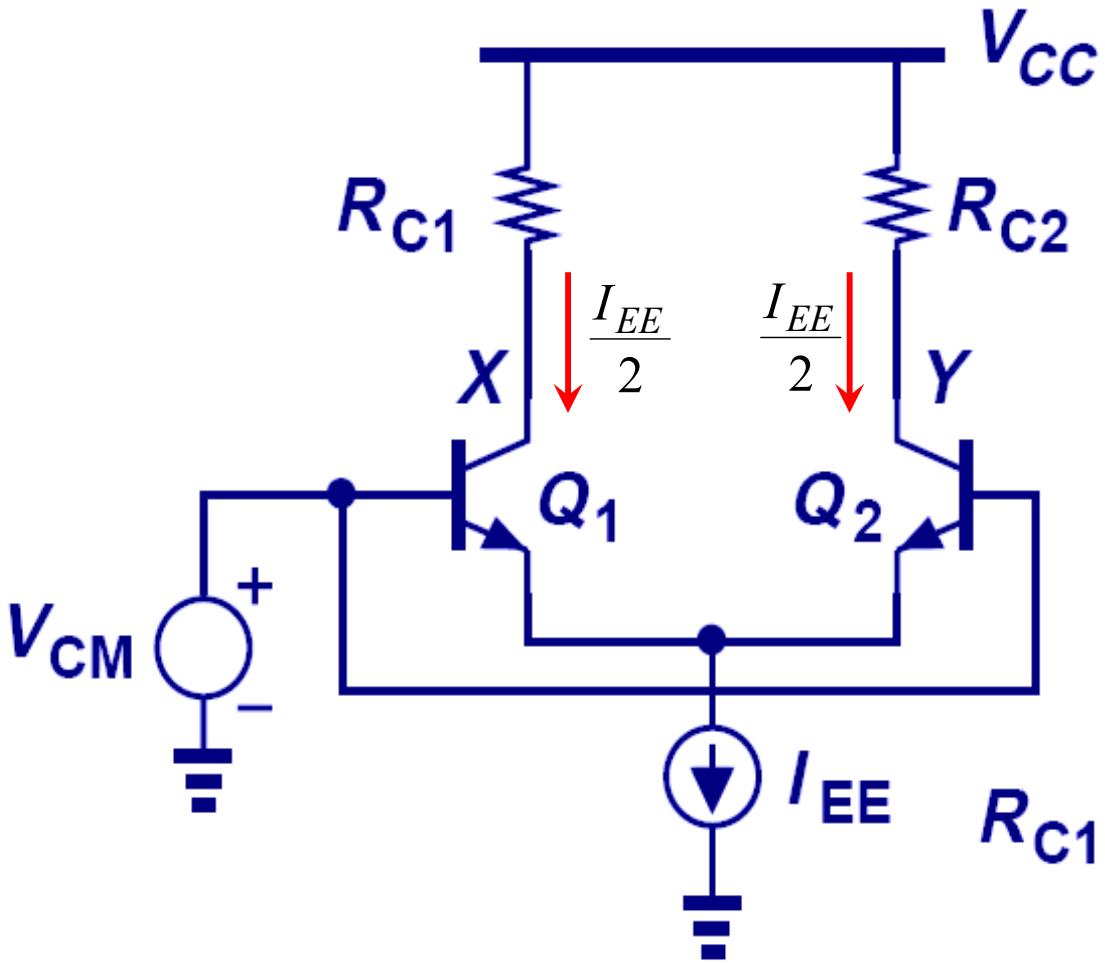
- General considerations
- Bipolar differential pair
- MOS differential pair
- Cascode differential amplifiers
- Common-mode rejection
- Differential pair with active load

# Differential Pair




- **With the addition of a tail current, the circuits above operate as an elegant, yet robust differential pair.**

# Common-Mode Response




Assuming $\alpha = 1$ for simplicity

$$V_{BE1} = V_{BE2}$$

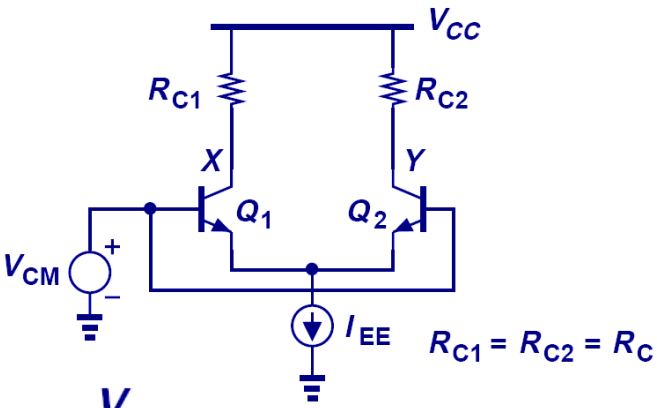
$$I_{C1} = I_{C2} = \frac{I_{EE}}{2}$$

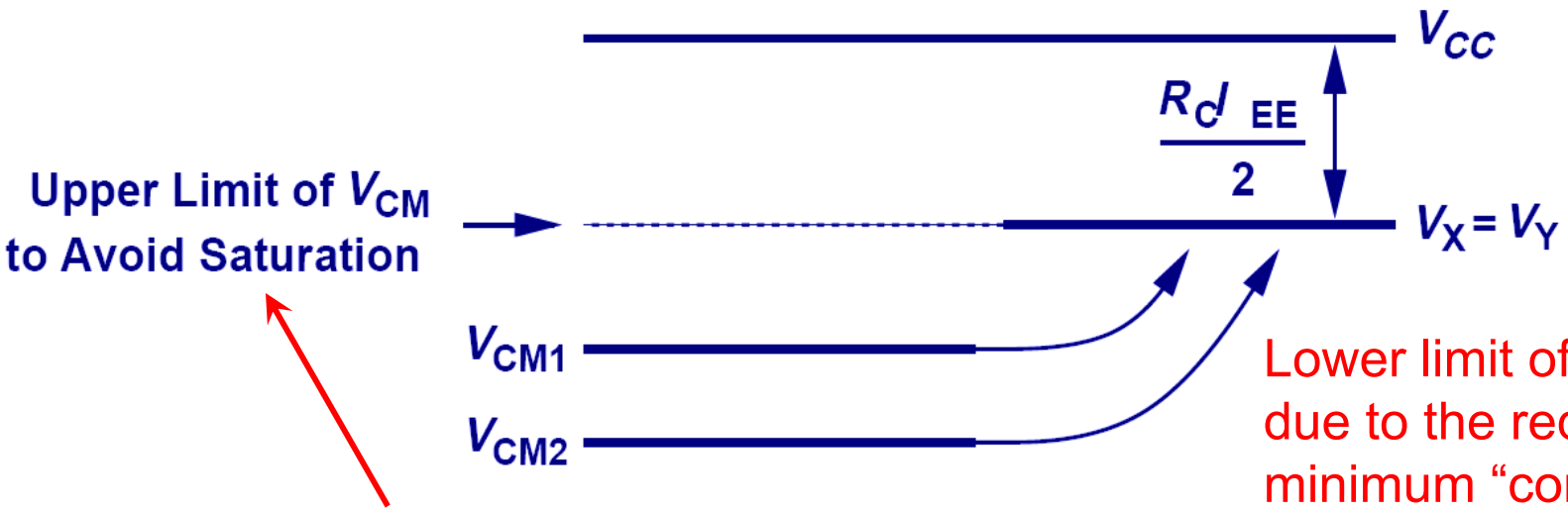
$$V_X = V_Y = V_{CC} - R_C \frac{I_{EE}}{2}$$

$R_{C1} = R_{C2} = R_C$

# Common-Mode Rejection

- **Due to the fixed tail current source, the input common-mode value can vary without changing the output common-mode value.**

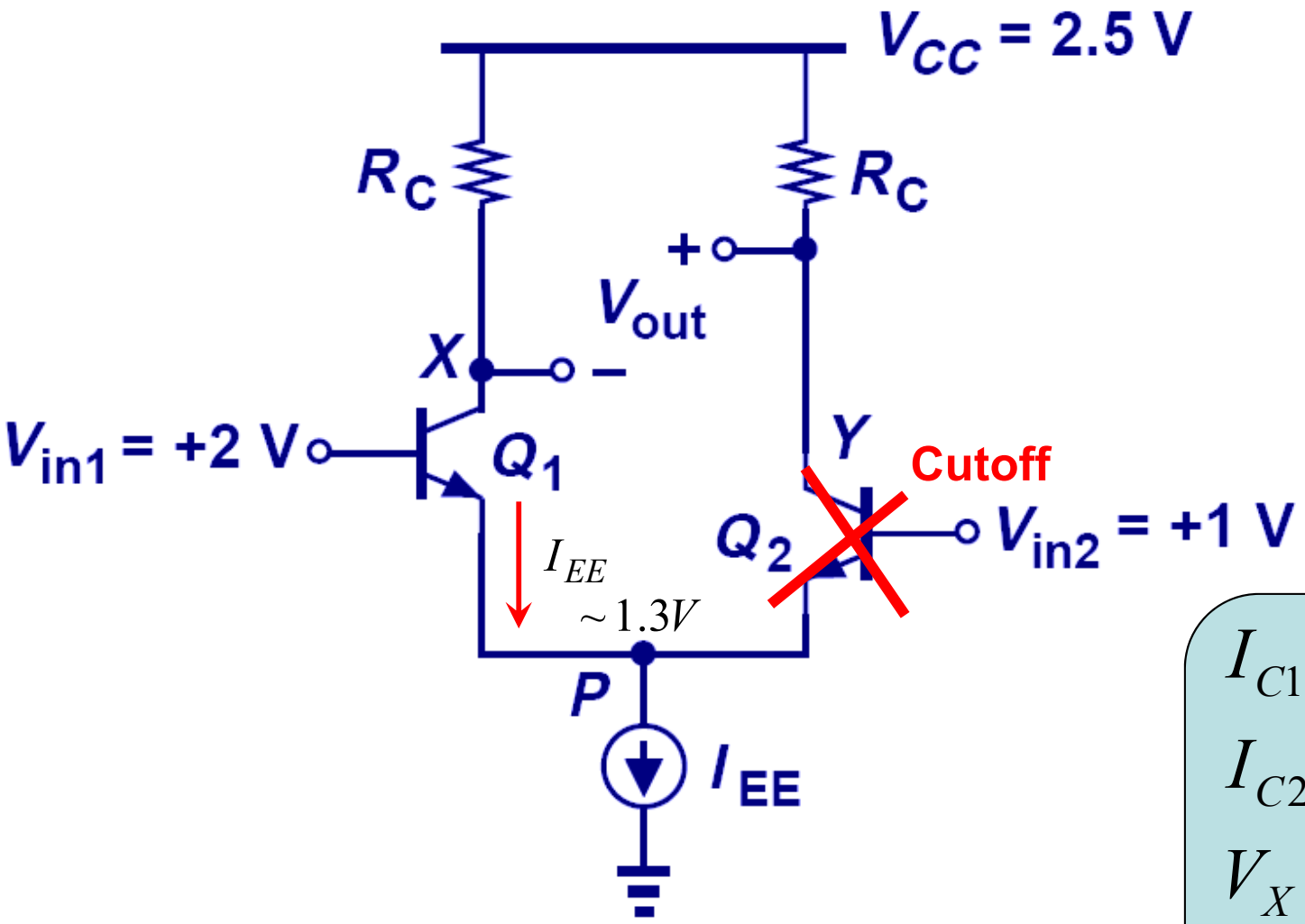



Lower limit of $V_{CM}$ also occurs due to the requirement of a minimum "compliance" voltage across a real current source

- Assuming $V_{BC}$=0 for saturation ($V_{CE}$~0.7V)
- Often we allow for $V_{BC}$=0.4V or $V_{CE}$~0.3V and still consider "active" mode operation, although this is formally "soft saturation"
- In any problems, I'll make it clear what assumptions to use

# Differential Response I – Big Differential Input



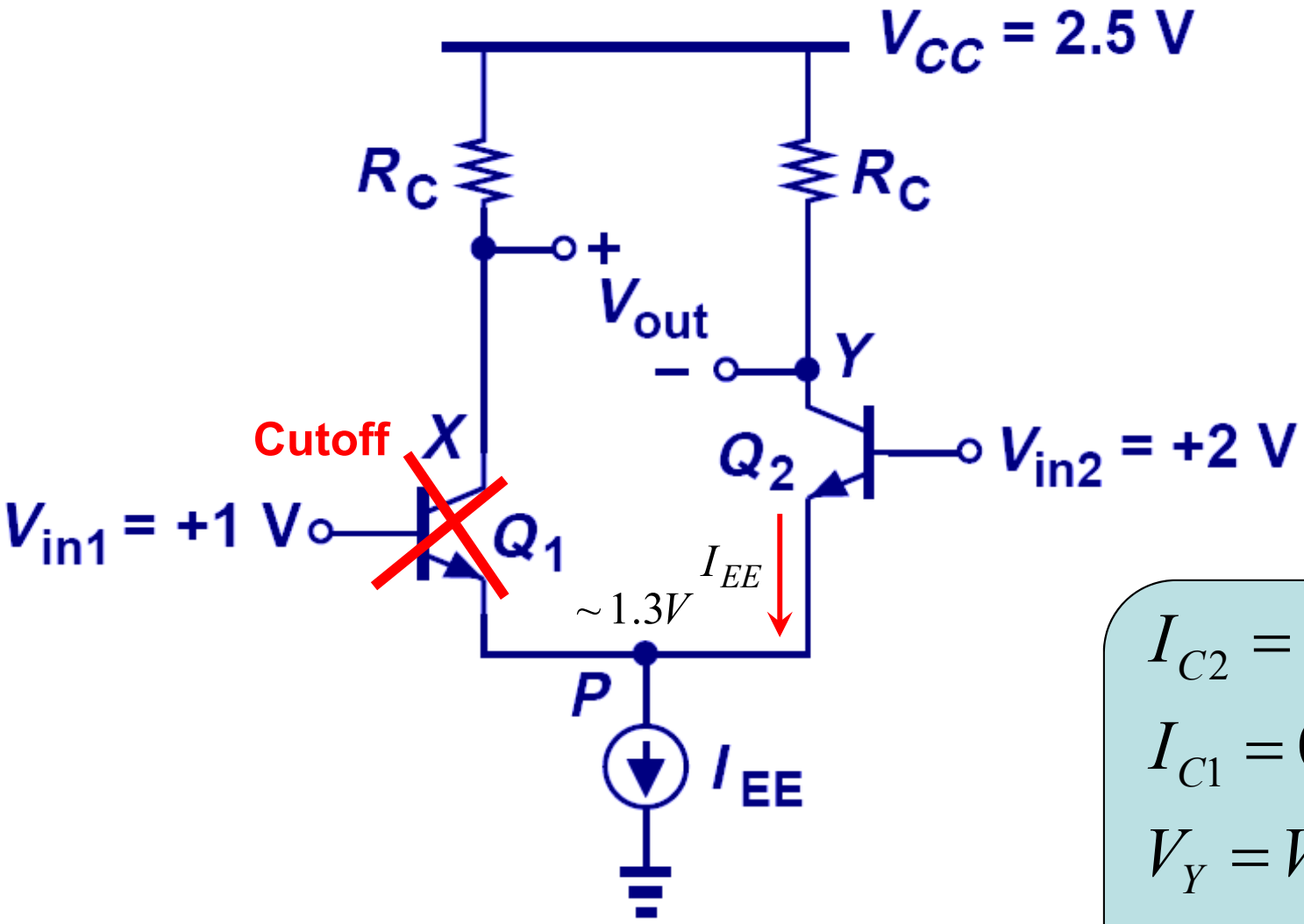

$$I_{C1} = I_{EE}$$

$$I_{C2} = 0$$

$$V_X = V_{CC} - R_C I_{EE}$$

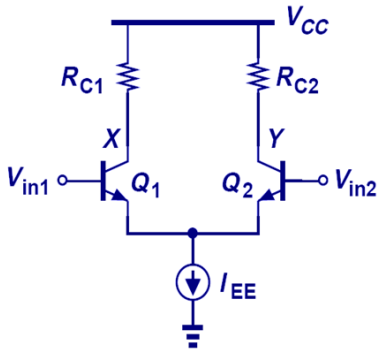
$$V_Y = V_{CC}$$

# Differential Response II – Big Differential Input



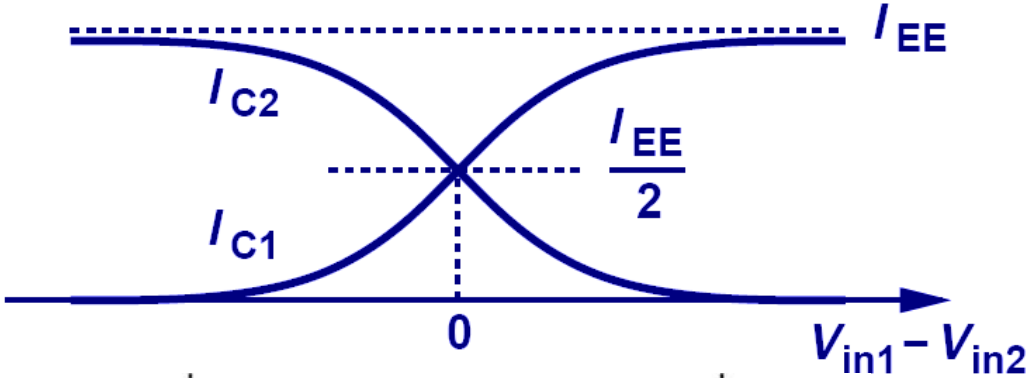

$$I_{C2} = I_{EE}$$
$$I_{C1} = 0$$
$$V_Y = V_{CC} - R_C I_{EE}$$
$$V_X = V_{CC}$$

# Differential Pair Characteristics

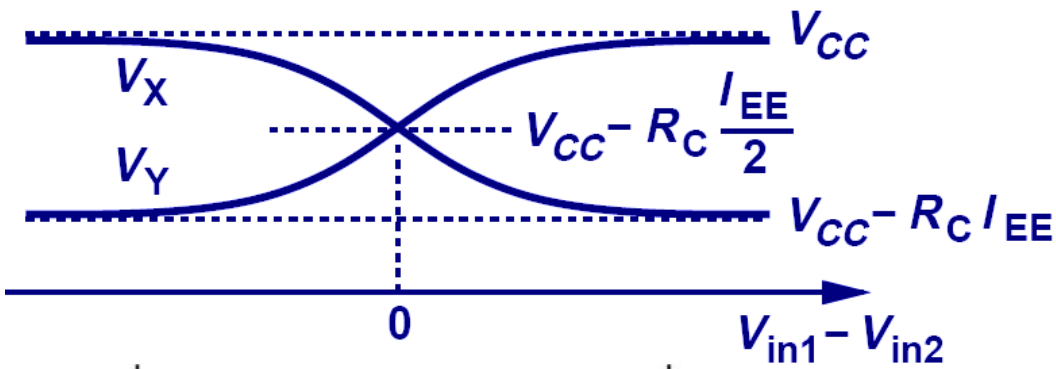


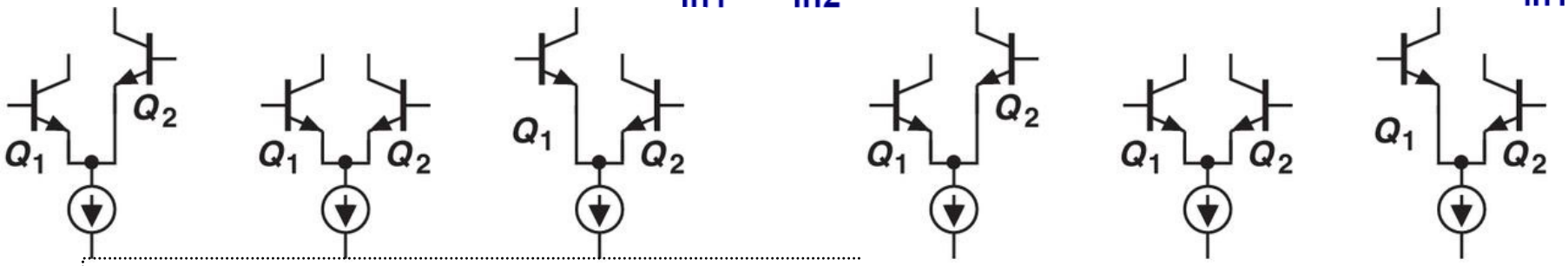

$$\text{Output Common Mode} = V_{CC} - R_C \frac{I_{EE}}{2}$$

Transistor Currents



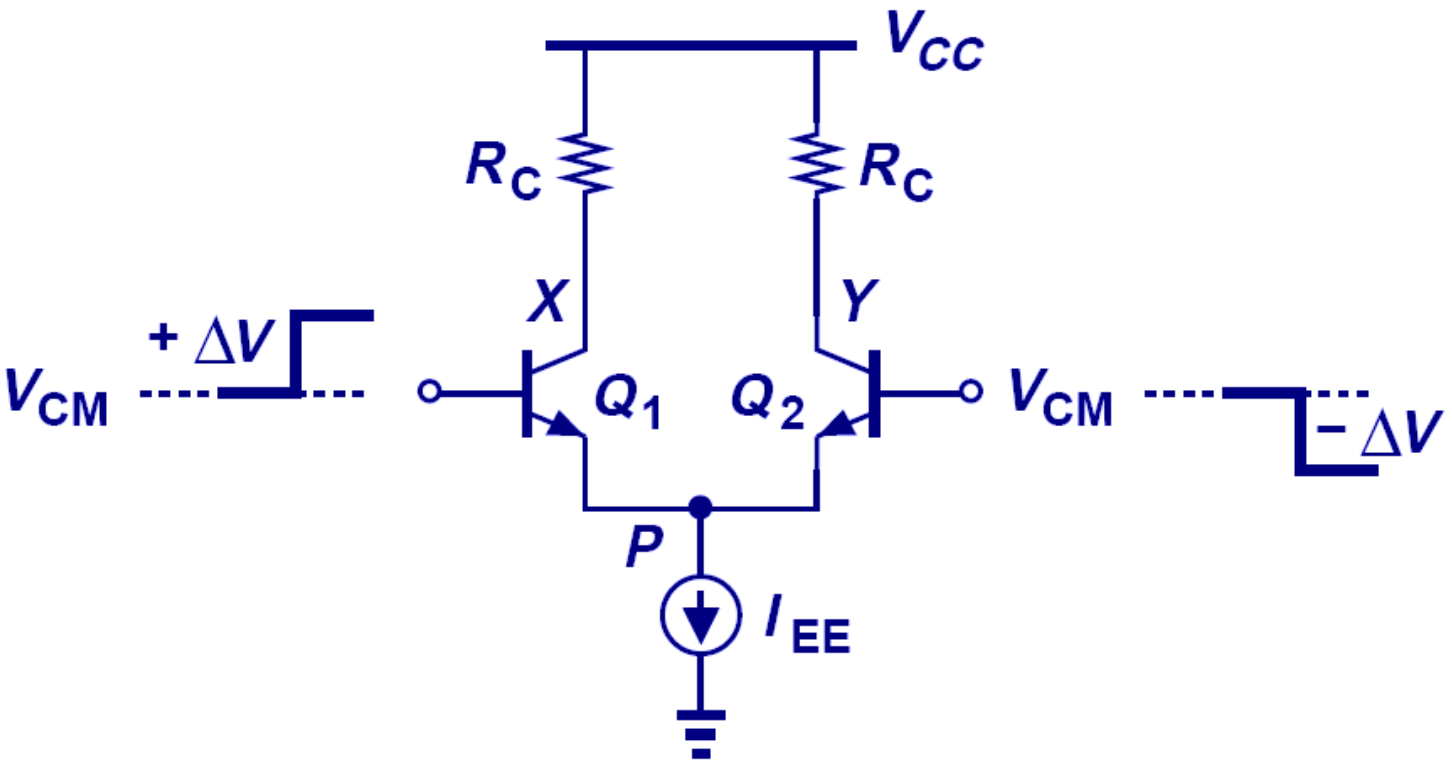

Output Voltages




- **None-zero differential input produces variations in output currents and voltages, whereas common-mode input produces no variations.**

# Small-Signal Analysis

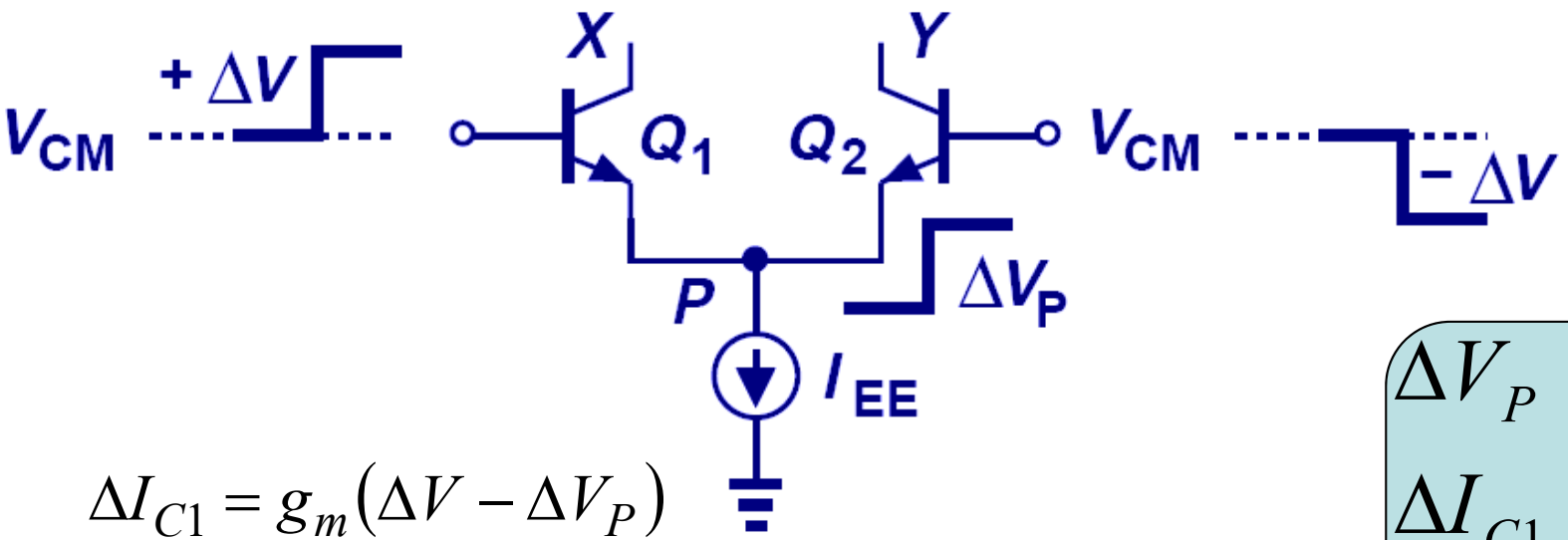



$$I_{C1} = \frac{I_{EE}}{2} + \Delta I$$

$$I_{C2} = \frac{I_{EE}}{2} - \Delta I$$

- Since the input to $Q_1$ and $Q_2$ rises and falls by the same amount, and their bases are tied together, the rise in $I_{C1}$ has the same magnitude as the fall in $I_{C2}$.

# Virtual Ground




$$\Delta I_{C1} = g_m(\Delta V - \Delta V_P)$$

$$\Delta I_{C2} = -g_m(\Delta V + \Delta V_P)$$

Because $\Delta I_{C1} = -\Delta I_{C2}$

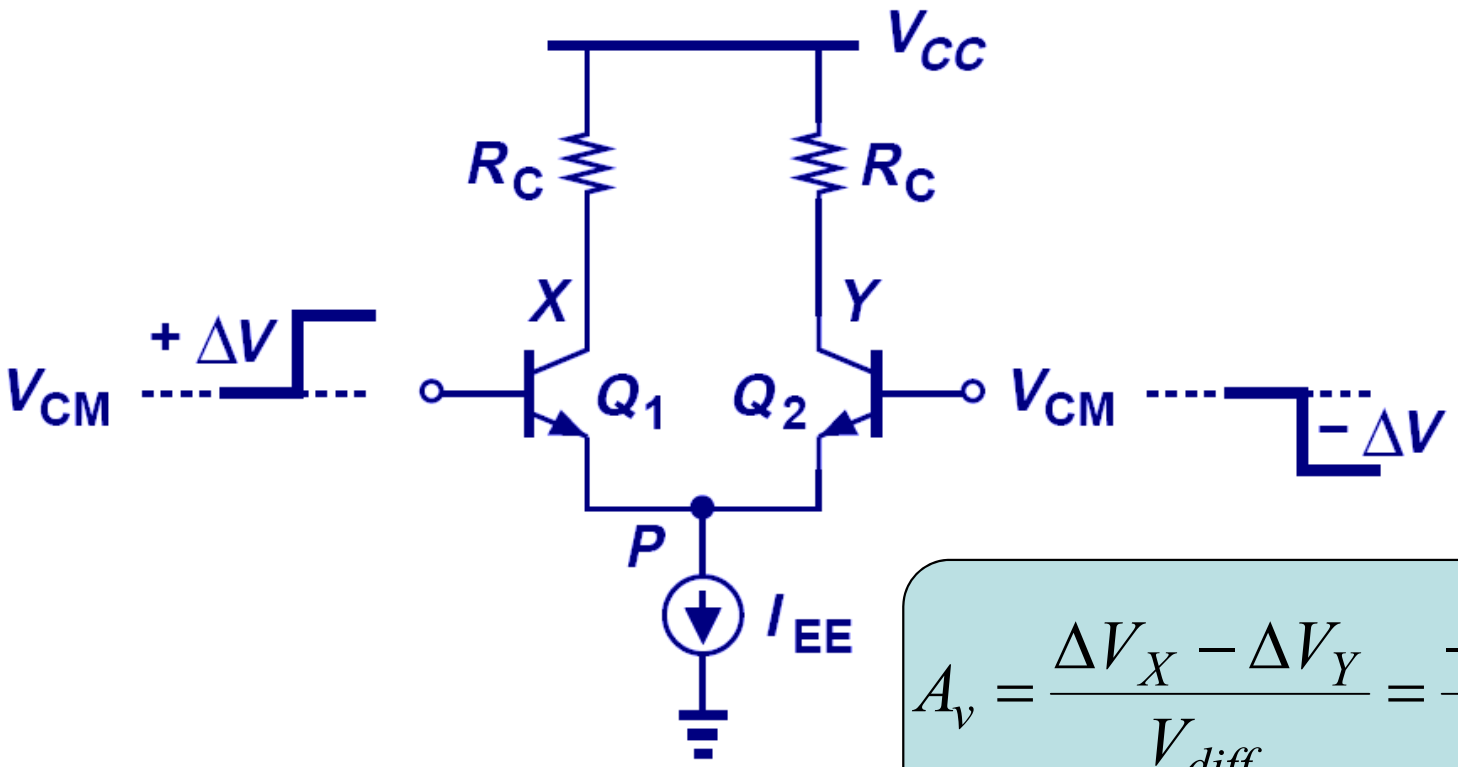
$$\Delta V_P = 0$$

$$\Delta I_{C1} = g_m \Delta V$$

$$\Delta I_{C2} = -g_m \Delta V$$

- **For small changes at inputs, the $g_m$'s are the same, and the respective increase and decrease of $I_{C1}$ and $I_{C2}$ are the same, node P must stay constant to accommodate these changes. Therefore, node P can be viewed as AC ground.**

# Small-Signal Differential Gain




$$\Delta I_{C1} = g_m \Delta V$$

$$\Delta I_{C2} = -g_m \Delta V$$

$$\Delta V_X = -g_m \Delta V R_C$$

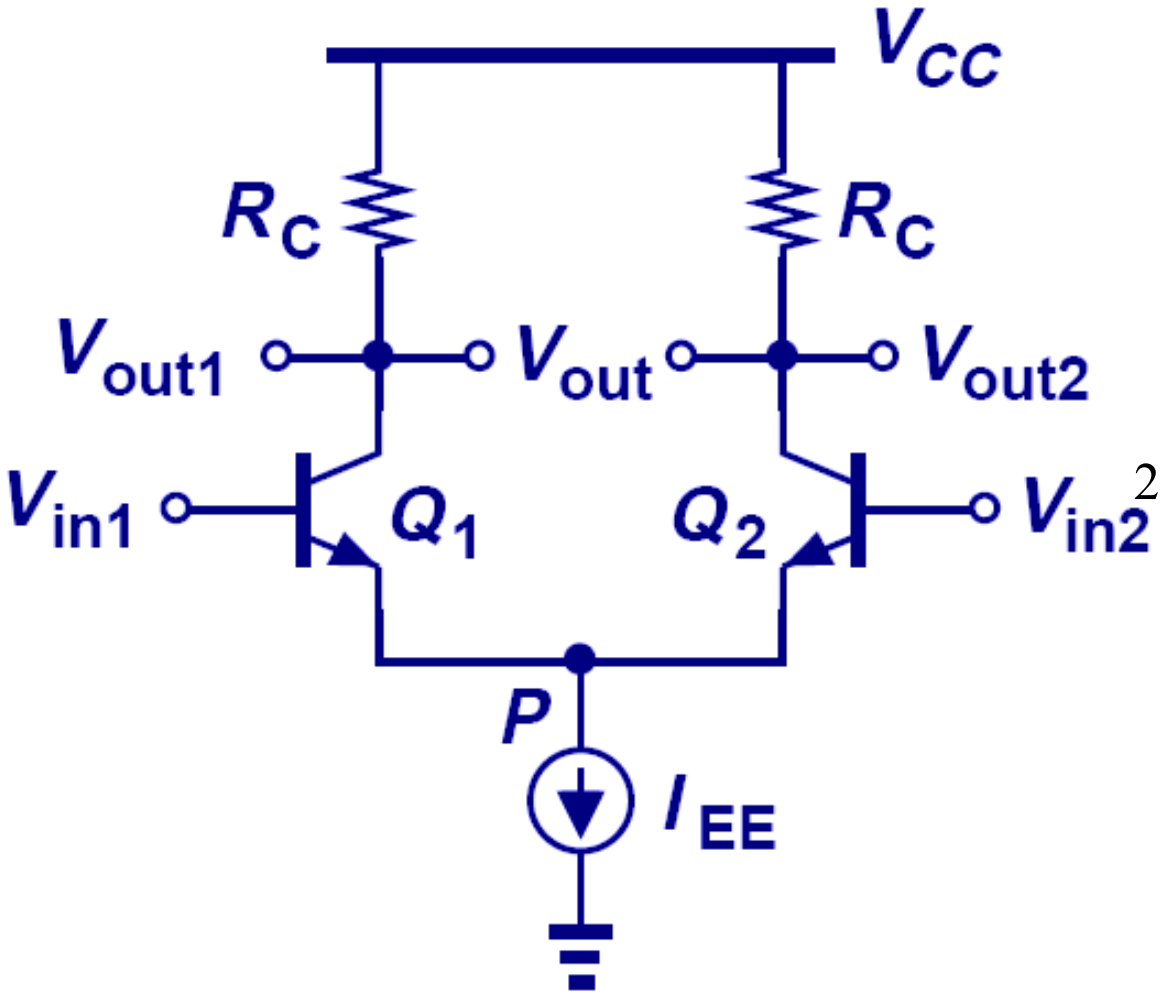
$$\Delta V_Y = g_m \Delta V R_C$$

$$A_v = \frac{\Delta V_X - \Delta V_Y}{V_{diff}} = \frac{-2g_m \Delta V R_C}{2\Delta V} = -g_m R_C$$

- **Since the output changes by $-2g_m\Delta VR_C$ and input by $2\Delta V$, the small signal gain is $-g_mR_C$, similar to that of the CE stage. However, to obtain same gain as the CE stage, power dissipation is doubled.**

# Large Signal Analysis

- Objective: Find expressions for $I_{C1}$ and $I_{C2}$ as a function of the differential input $V_{in1}$-$V_{in2}$
  - This can then be used to find the differential output voltage




1. Using $I_C = I_S e^{\frac{V_{BE}}{V_T}}$

$$V_{BE1} = V_T \ln\left(\frac{I_{C1}}{I_S}\right)$$

$$V_{BE2} = V_T \ln\left(\frac{I_{C2}}{I_S}\right)$$

2. Writing a KVL around the input network

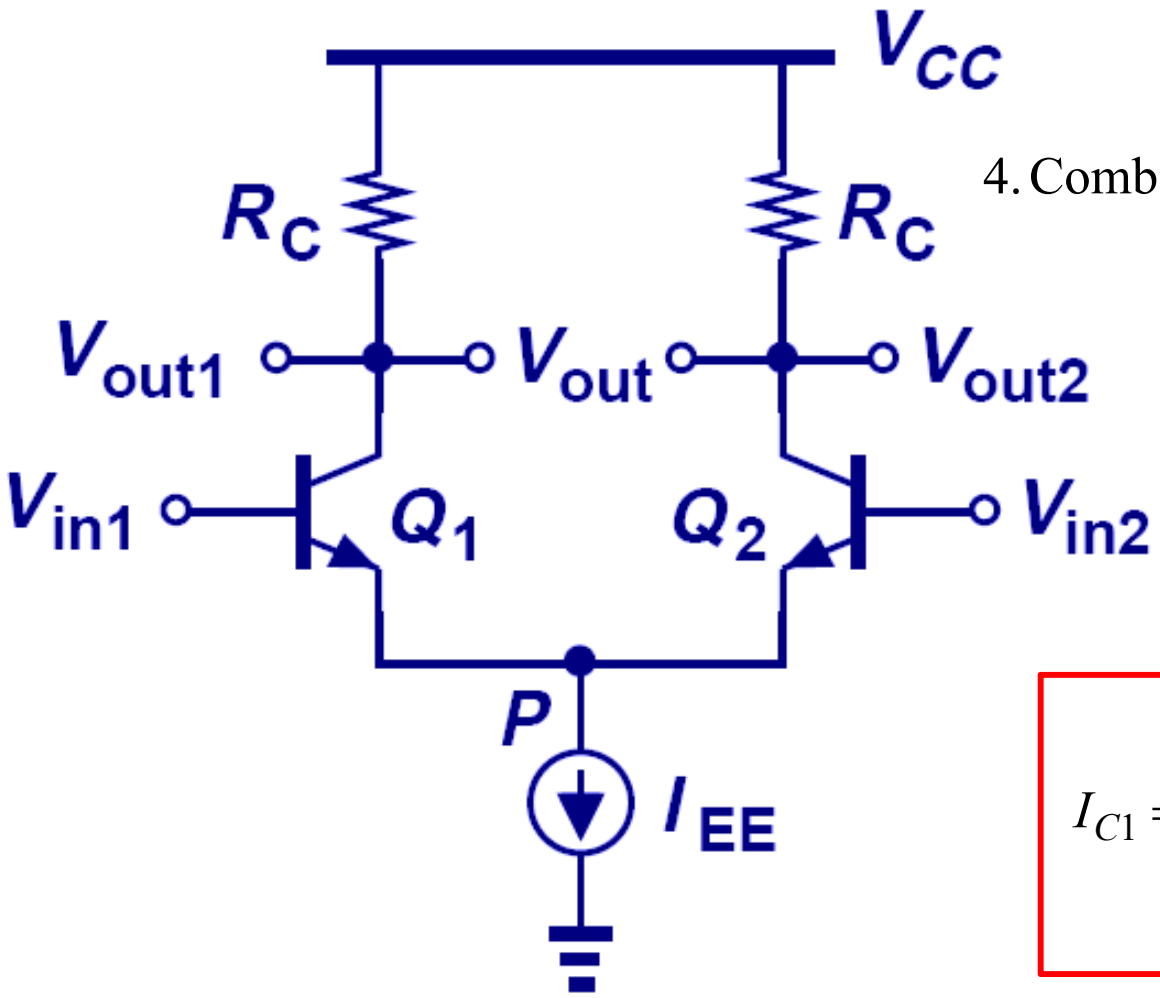
$$V_{in1} - V_{BE1} = V_P = V_{in2} - V_{BE2}$$

$$V_{in1} - V_{in2} = V_{BE1} - V_{BE2}$$

$$= V_T \ln\left(\frac{I_{C1}}{I_S}\right) - V_T \ln\left(\frac{I_{C2}}{I_S}\right)$$

$$= V_T \ln\left(\frac{I_{C1}}{I_{C2}}\right)$$

# Large Signal Analysis




3. Writing a KCL at node P

$$I_{C1} + I_{C2} = I_{EE}$$

4. Combining previous KVL equation with the KCL

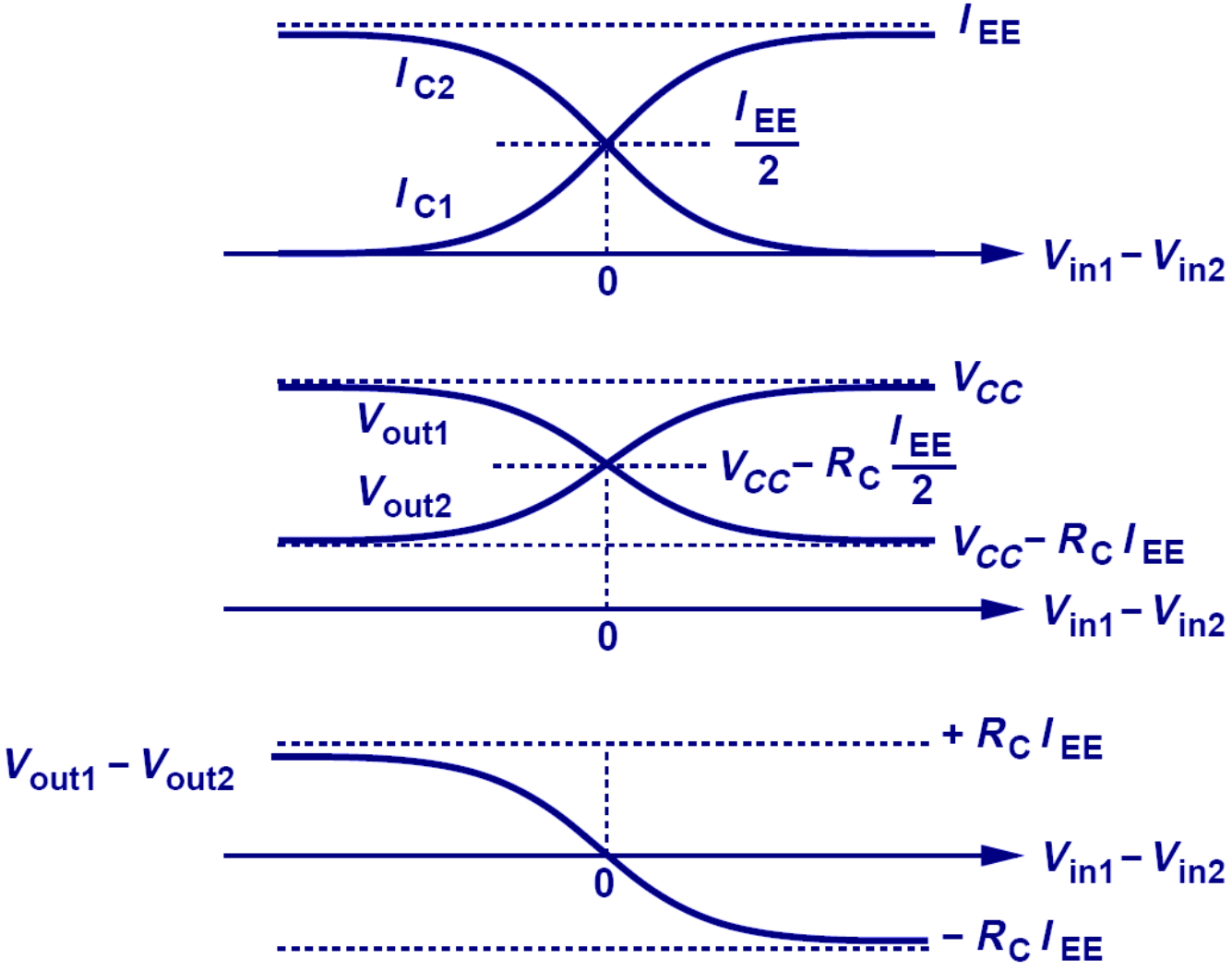
$$I_{C2} \exp\frac{V_{in1} - V_{in2}}{V_T} + I_{C2} = I_{EE}$$

$$I_{C2} = \frac{I_{EE}}{1 + \exp\dfrac{V_{in1} - V_{in2}}{V_T}}$$

5. From circuit symmetry

$$I_{C1} = \frac{I_{EE}}{1 + \exp\dfrac{V_{in2} - V_{in1}}{V_T}} = \frac{I_{EE}\exp\dfrac{V_{in1} - V_{in2}}{V_T}}{1 + \exp\dfrac{V_{in1} - V_{in2}}{V_T}}$$

# Input/Output Characteristics



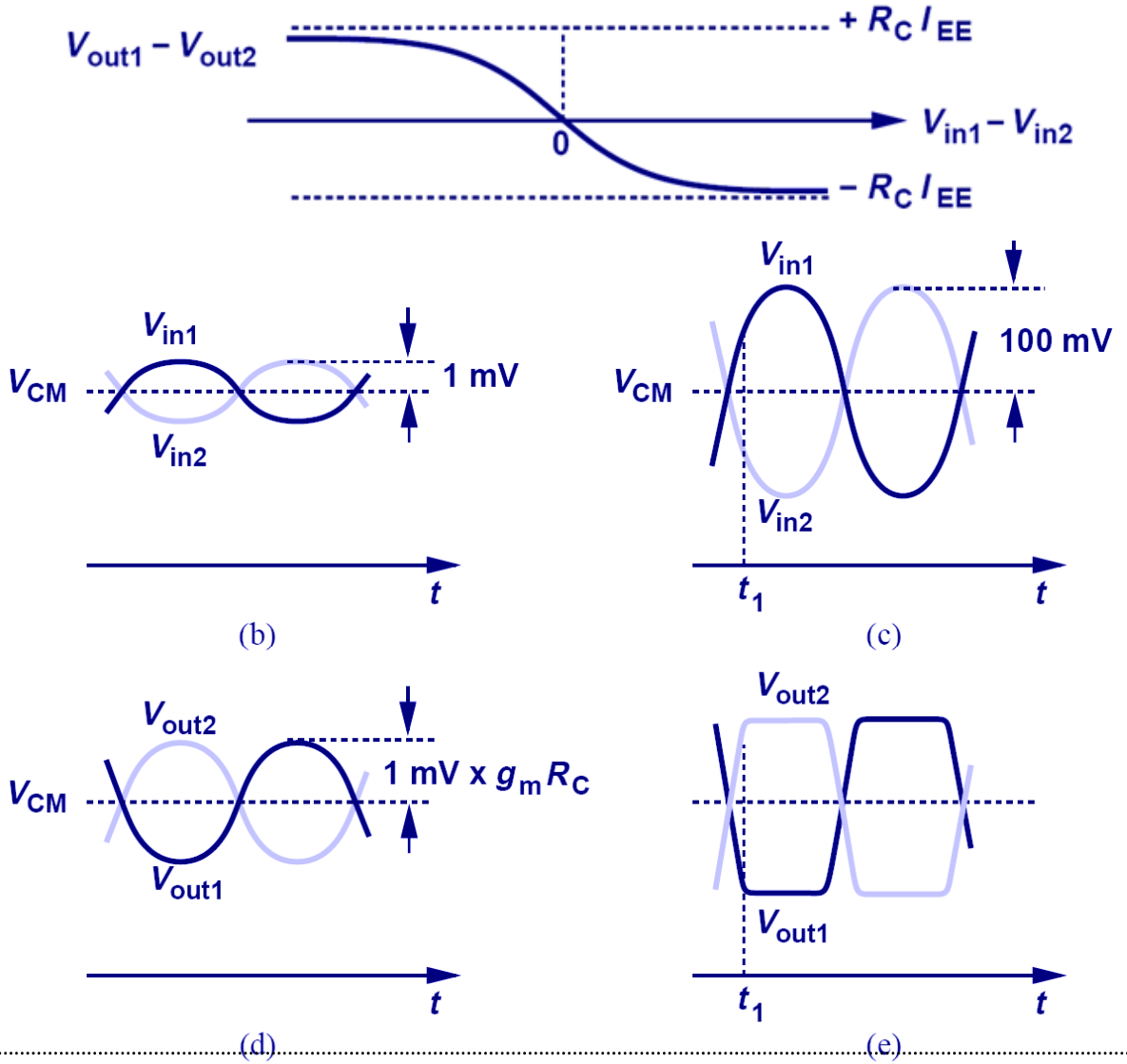

$$I_{C1} = \frac{I_{EE} \exp \frac{V_{in1} - V_{in2}}{V_T}}{1 + \exp \frac{V_{in1} - V_{in2}}{V_T}}$$

$$I_{C2} = \frac{I_{EE}}{1 + \exp \frac{V_{in1} - V_{in2}}{V_T}}$$

$$V_{out1} - V_{out2} = -R_C I_{EE} \tanh \frac{V_{in1} - V_{in2}}{2V_T}$$

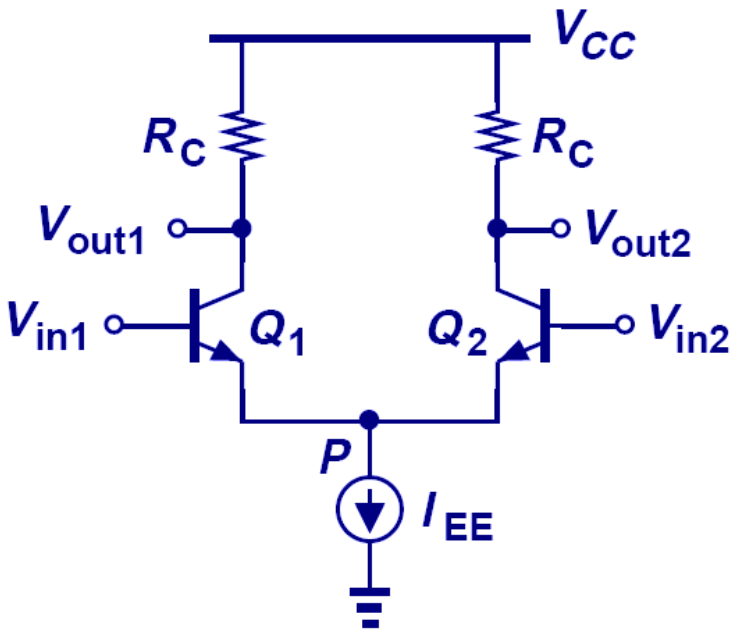
- If $V_{in1}$-$V_{in2}$ ≥ $4V_T$ = 104mV, the majority of the current is steered through $Q_1$

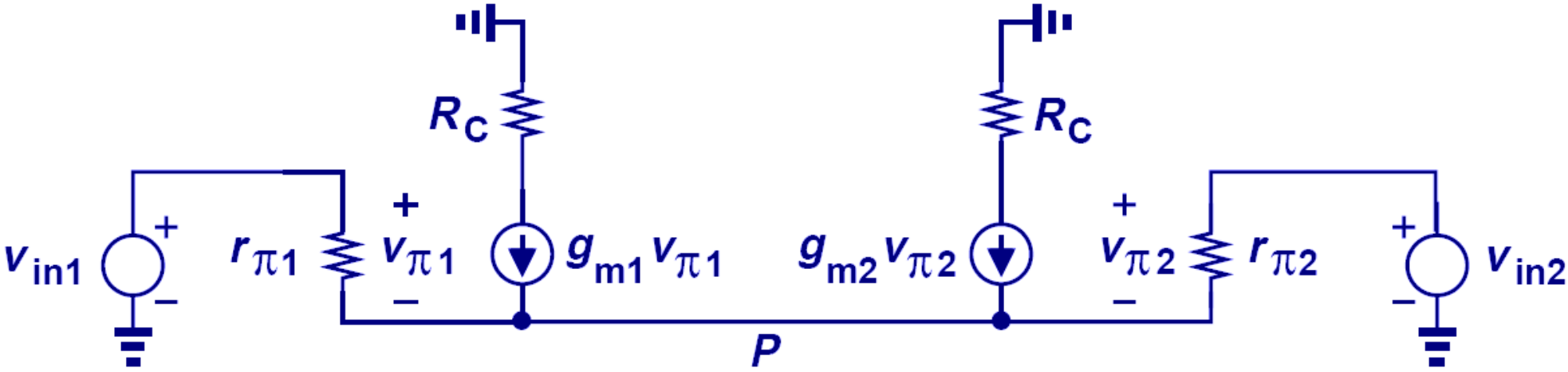
# Linear/Nonlinear Regions




- **The left column operates in linear region, whereas the right column operates in nonlinear region.**

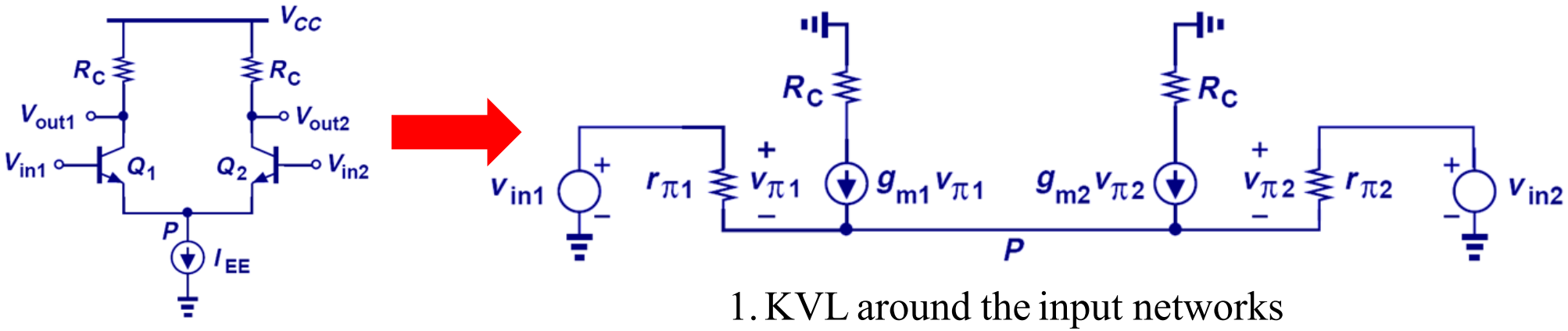
# Small-Signal Model




- We can use the virtual GND concept discussed in Slide 23 to simplify this

# Virtual GND Proof




1. KVL around the input networks

$$v_{in1} - v_{\pi 1} = v_P = v_{in2} - v_{\pi 2}$$

2. KCL at node P

$$\frac{v_{\pi 1}}{r_{\pi 1}} + g_{m1}v_{\pi 1} + \frac{v_{\pi 2}}{r_{\pi 2}} + g_{m2}v_{\pi 2} = 0$$

For small signals $r_{\pi 1} = r_{\pi 2}$ and $g_{m1} = g_{m2}$

$$v_{\pi 1} = -v_{\pi 2}$$

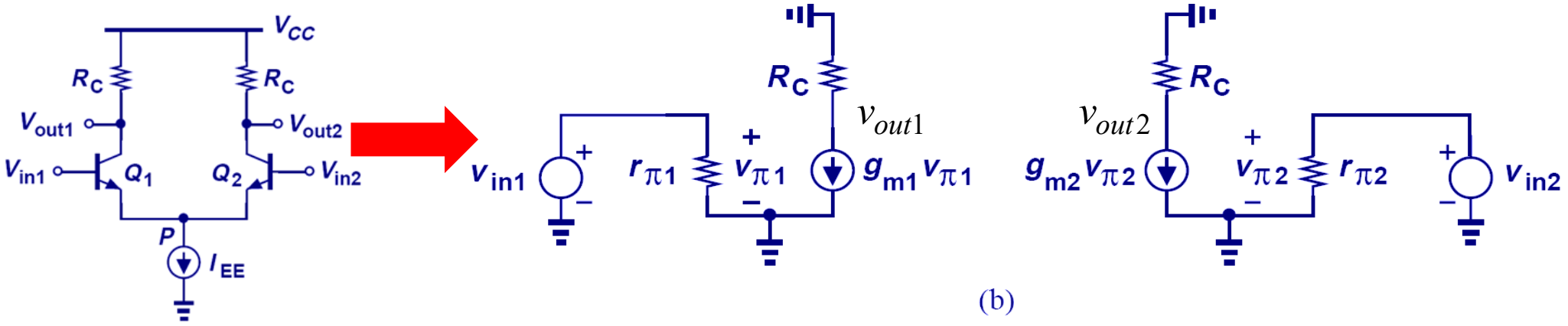
For differential operation $v_{in1} = -v_{in2}$, and using the above KVL

$$2v_{in1} = 2v_{\pi 1}$$

which implies that

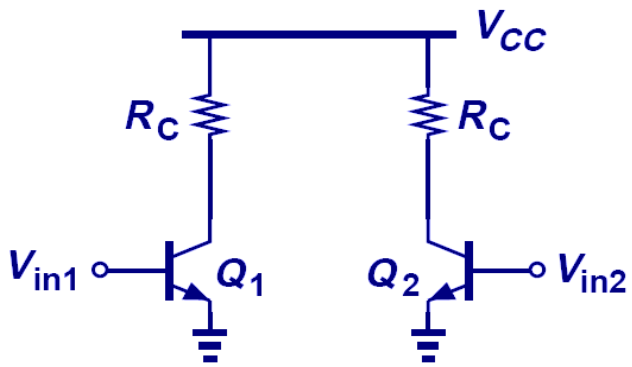
$$v_P = v_{in1} - v_{\pi 1} = 0$$

# Half Circuits




(b)

$$v_{out1} = -g_m R_C v_{in1}$$
$$v_{out2} = -g_m R_C v_{in2}$$

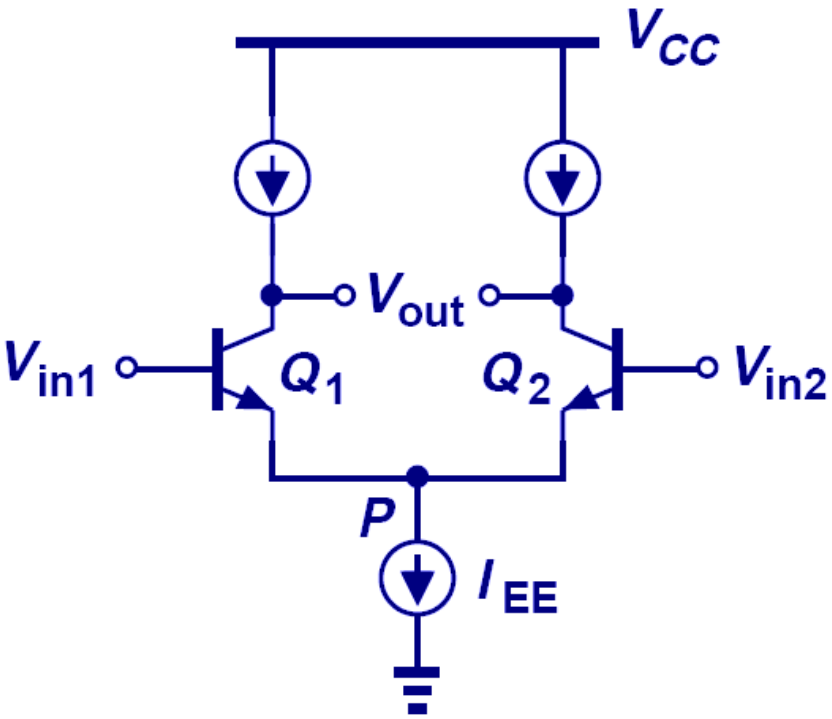



(c)

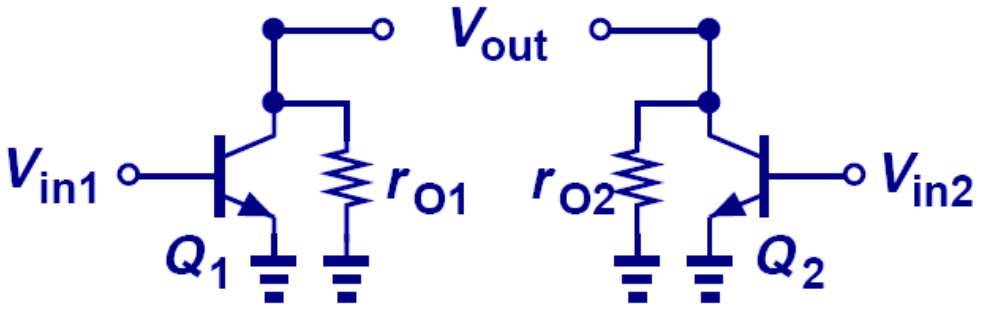
$$\frac{v_{out1} - v_{out2}}{v_{in1} - v_{in2}} = -g_m R_C$$

- Since $V_P$ is grounded, we can treat the differential pair as two CE "half circuits", with half the output swing on either side
- If the circuit is symmetrical, we can just analyze the half-circuit with a virtual ground to get the gain equation

# Example: Differential Gain

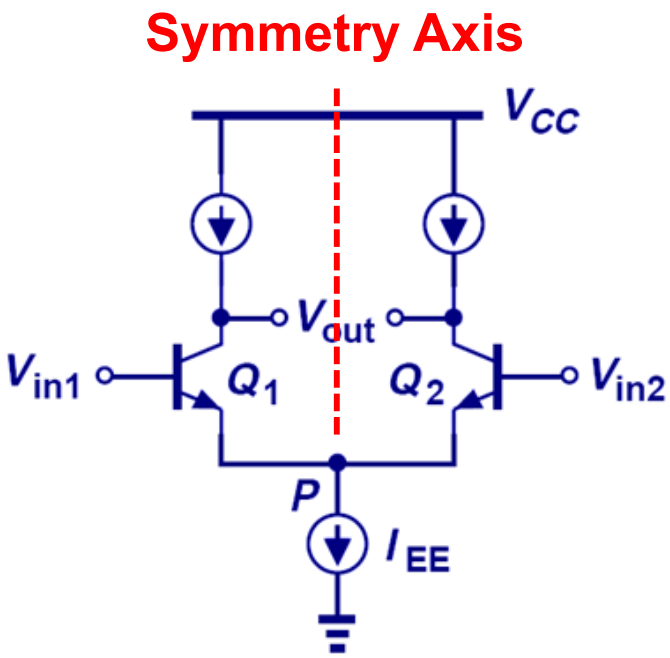


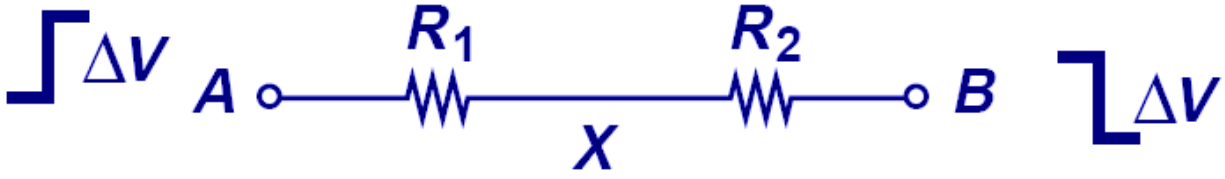

w/ finite $r_o$




$$\frac{v_{out1} - v_{out2}}{v_{in1} - v_{in2}} = -g_m r_O$$

# Extension of Virtual Ground

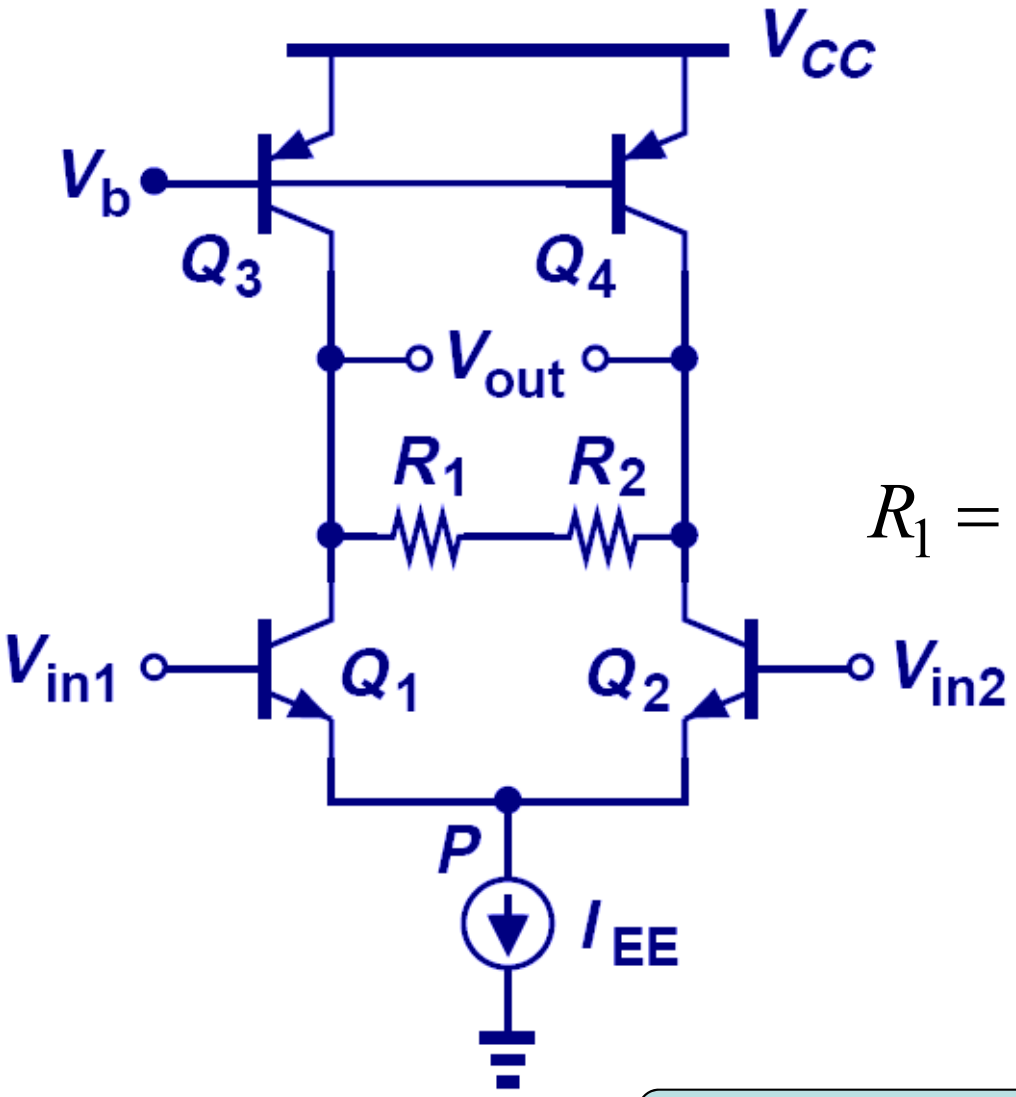


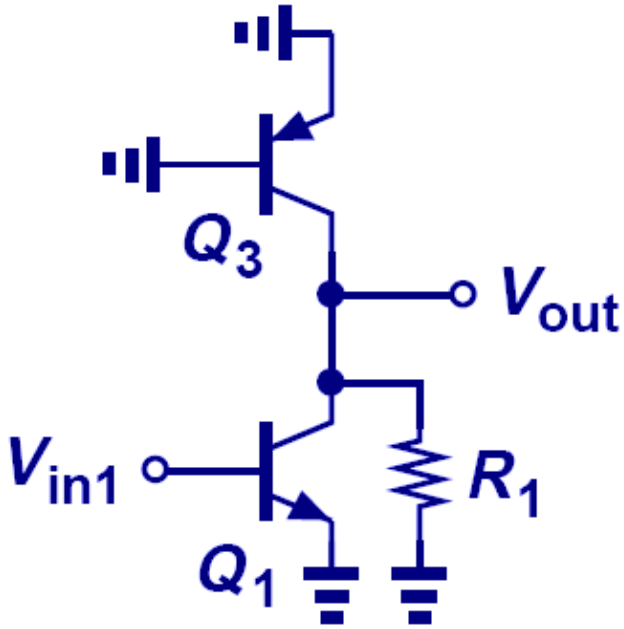

$$V_X = 0$$

- It can be shown that if $R_1 = R_2$, and points A and B go up and down by the same amount respectively, $V_X$ does not move.

# Half Circuit Example I

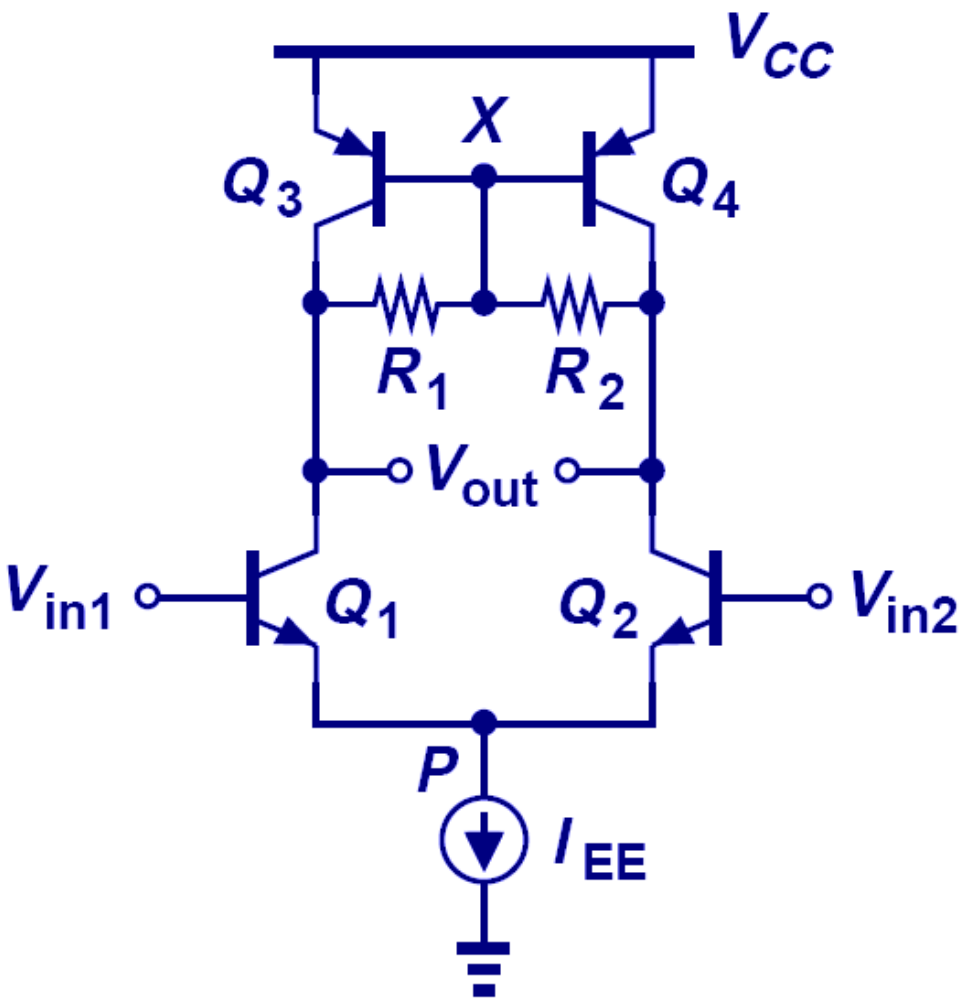


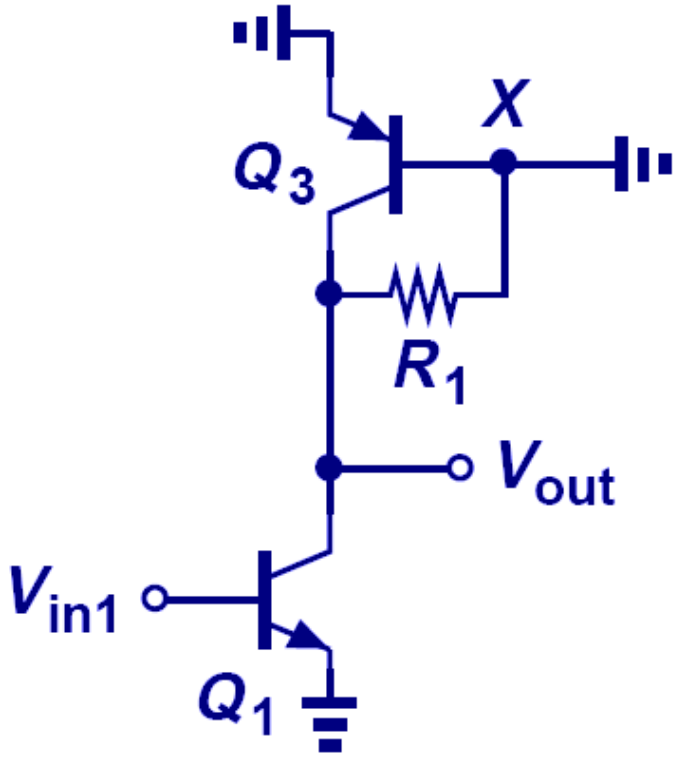

$$R_1 = R_2$$




$$A_v = -g_{m1}\left(r_{O1} \parallel r_{O3} \parallel R_1\right)$$

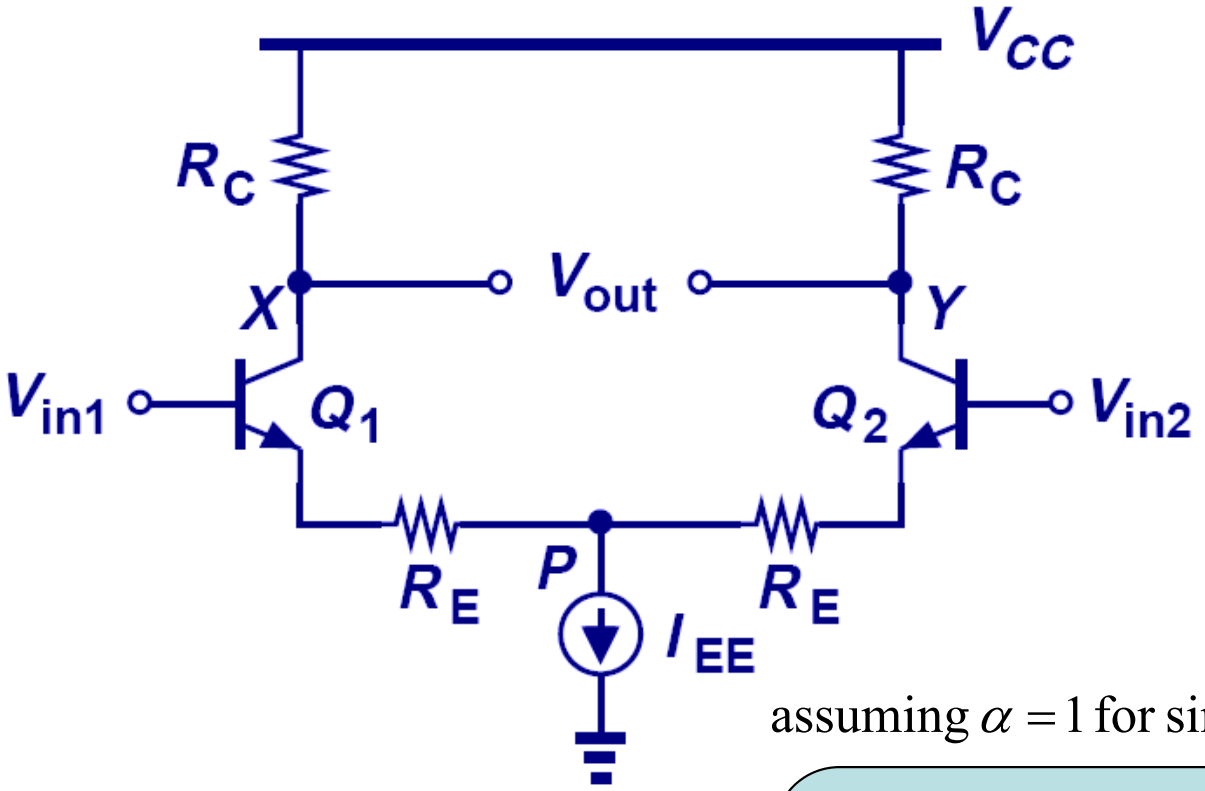
# Half Circuit Example II

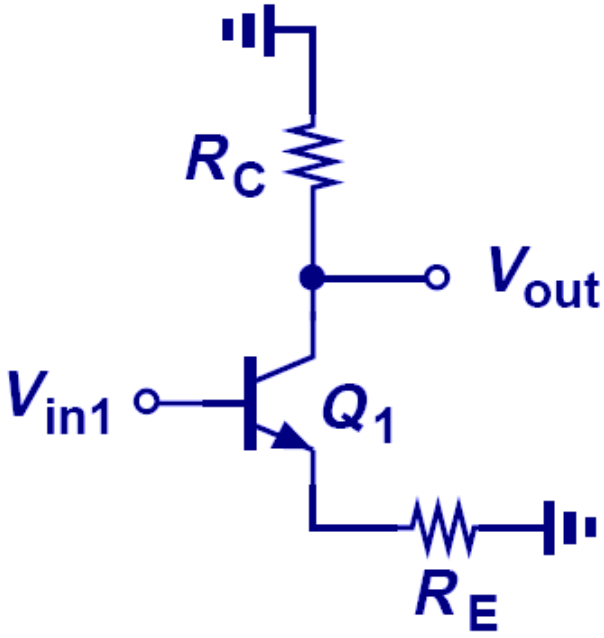



$$A_v = -g_{m1}\left(r_{O1} \parallel r_{O3} \parallel R_1\right)$$

# Half Circuit Example III

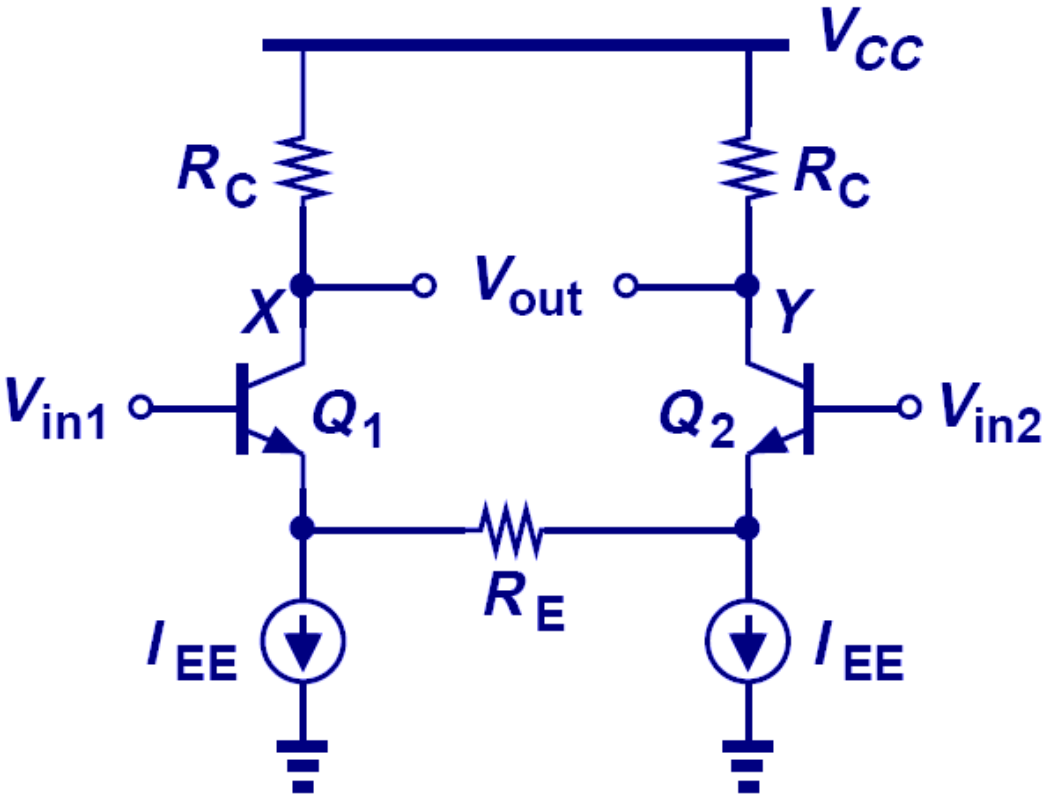


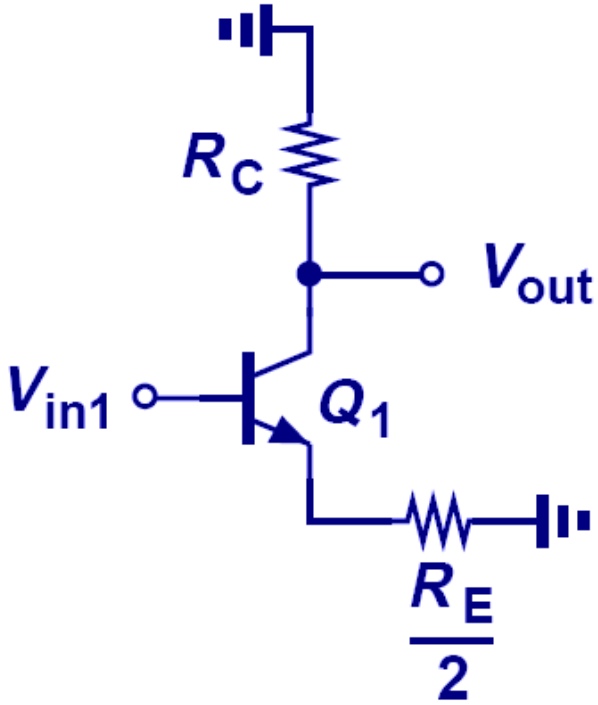




assuming $\alpha = 1$ for simplicity

$$A_v = -\frac{R_C}{R_E + \frac{1}{g_m}}$$

# Half Circuit Example IV

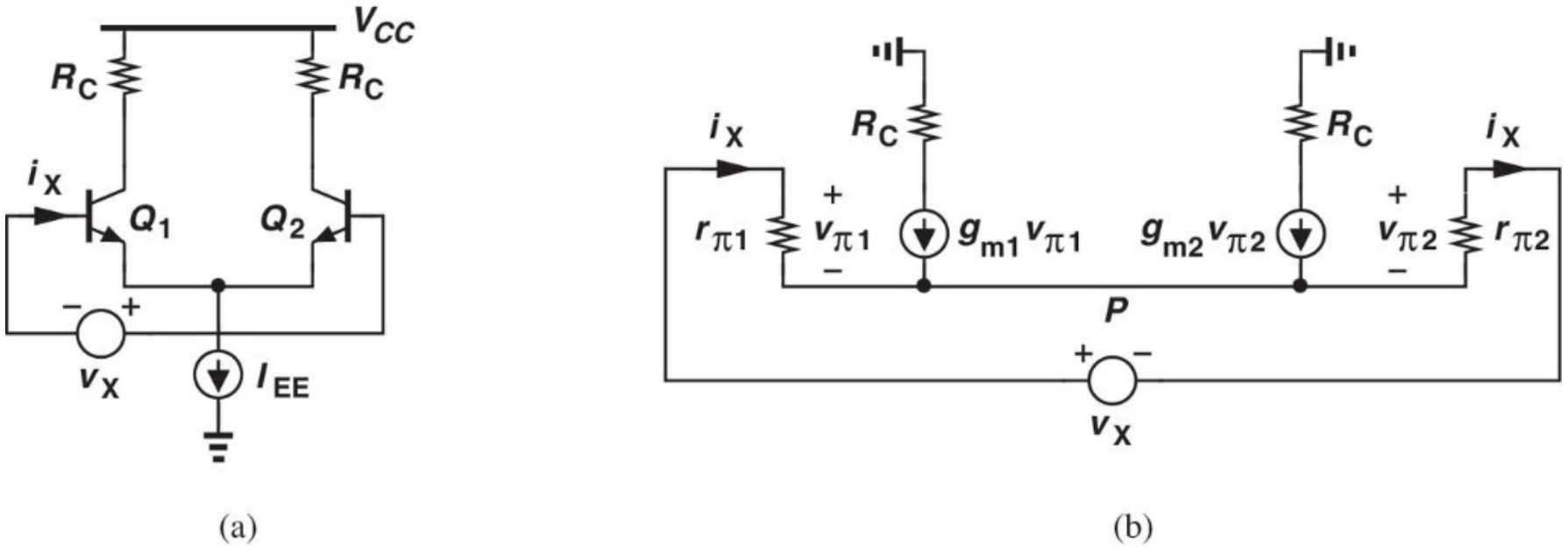



assuming $\alpha = 1$ for simplicity

$$A_v = -\frac{R_C}{\frac{R_E}{2} + \frac{1}{g_m}}$$

# BJT Differential Pair Input Resistance




- In order to obtain the differential input resistance, apply a test differential voltage $v_X$ and find the developed current $i_X$

$$\frac{v_{\pi 1}}{r_{\pi 1}} = i_X = -\frac{v_{\pi 2}}{r_{\pi 2}}$$

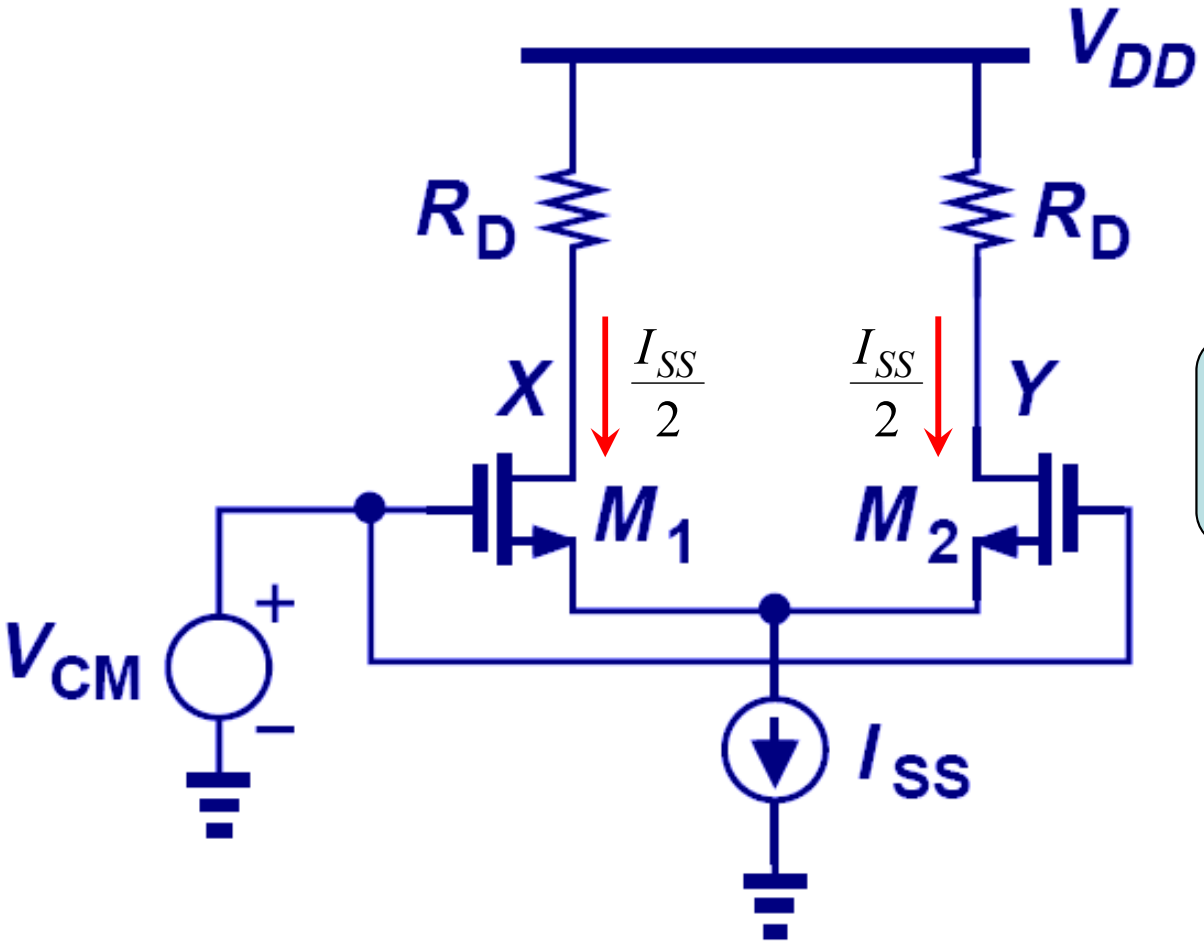
$$v_X = v_{\pi 1} - v_{\pi 2} = 2 r_\pi i_X$$

$$\text{Differential } R_{in} = \frac{v_X}{i_X} = 2 r_\pi$$

# Agenda

- General considerations
- Bipolar differential pair
- MOS differential pair
- Cascode differential amplifiers
- Common-mode rejection
- Differential pair with active load

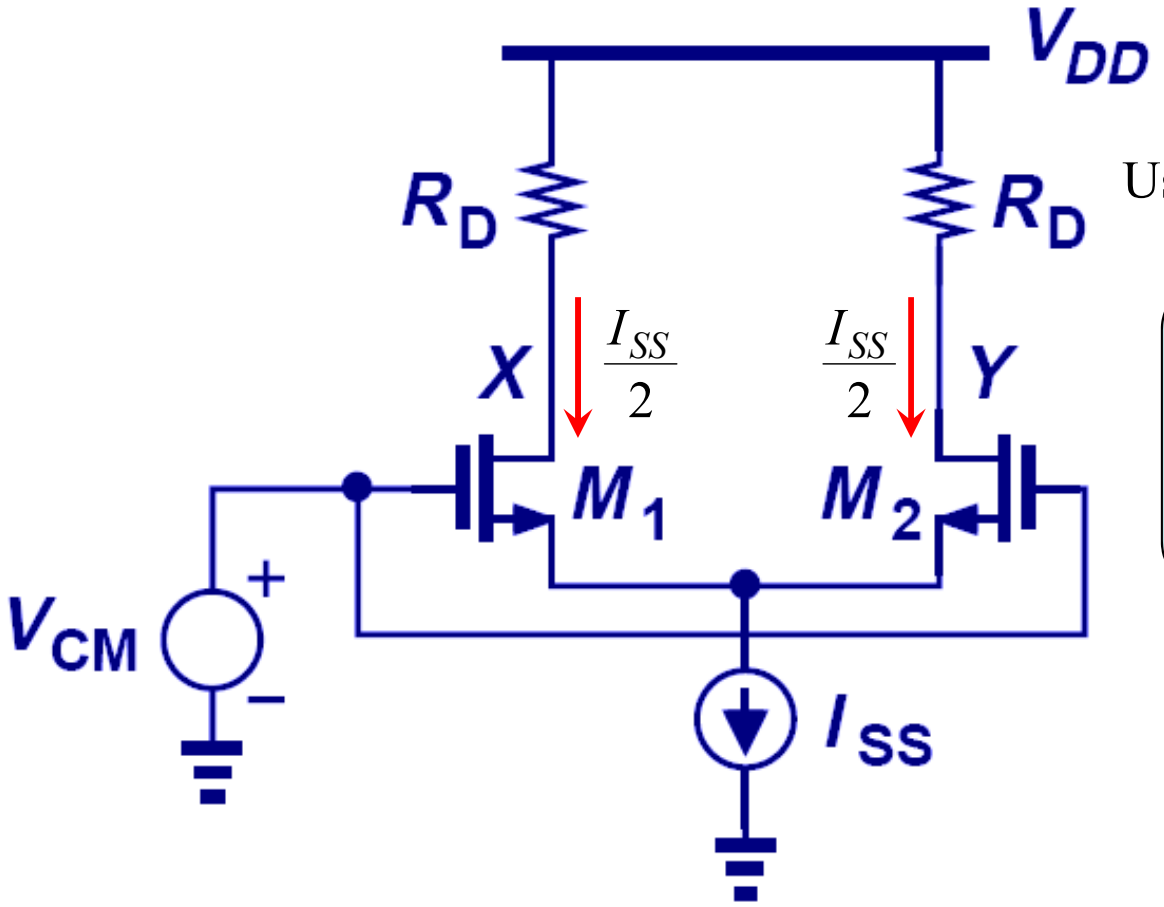
# MOS Differential Pair's Common-Mode Response




$$V_X = V_Y = V_{DD} - R_D \frac{I_{SS}}{2}$$

- Similar to its bipolar counterpart, MOS differential pair produces zero differential output as $V_{CM}$ changes.

# Equilibrium Overdrive Voltage

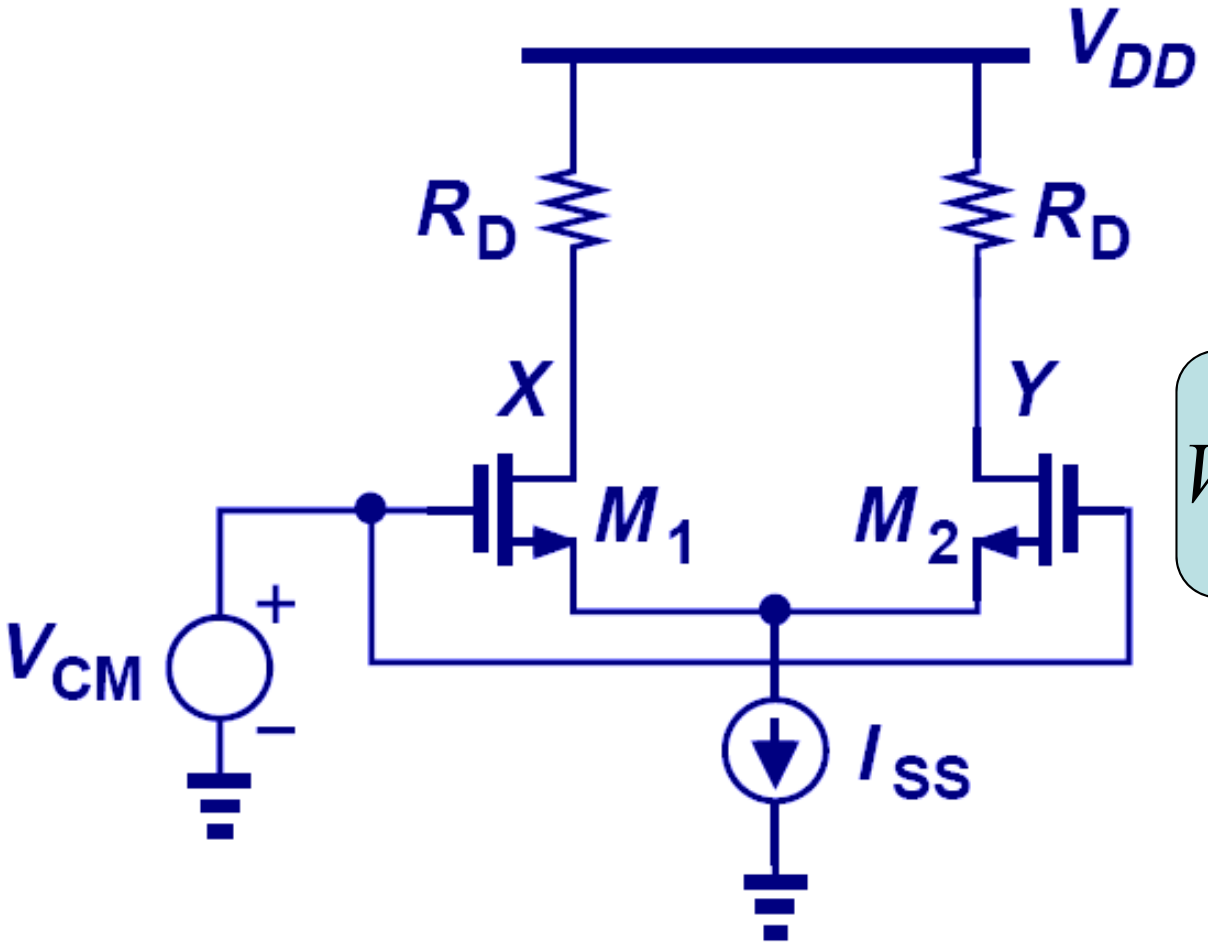



Using Saturation $I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS} - V_{TH})^2$

$$(V_{GS} - V_{TH})_{equil} = \sqrt{\frac{I_{SS}}{\mu_n C_{ox}\frac{W}{L}}}$$

- The equilibrium overdrive voltage is defined as the overdrive voltage seen by $M_1$ and $M_2$ when both carry an $I_{SS}/2$ current
- Larger tail current or smaller W/L results in a larger equilibrium overdrive voltage

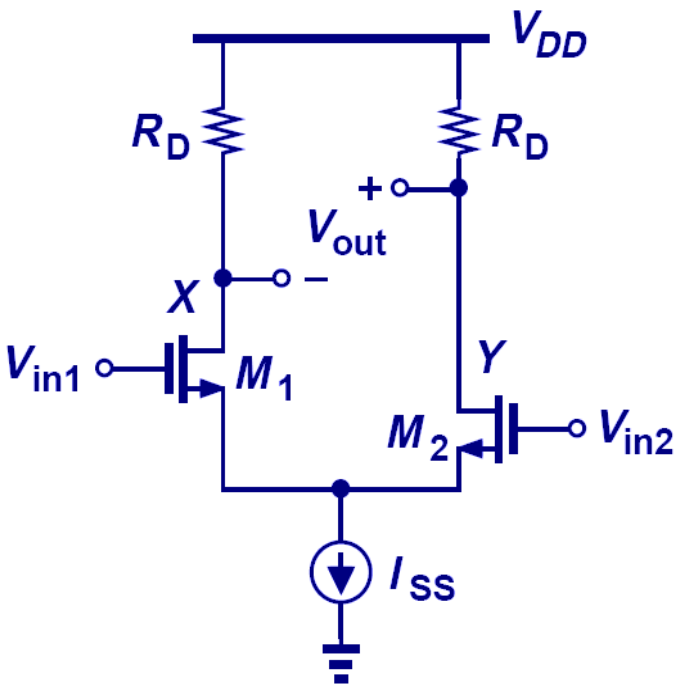
# Minimum Common-mode Output Voltage



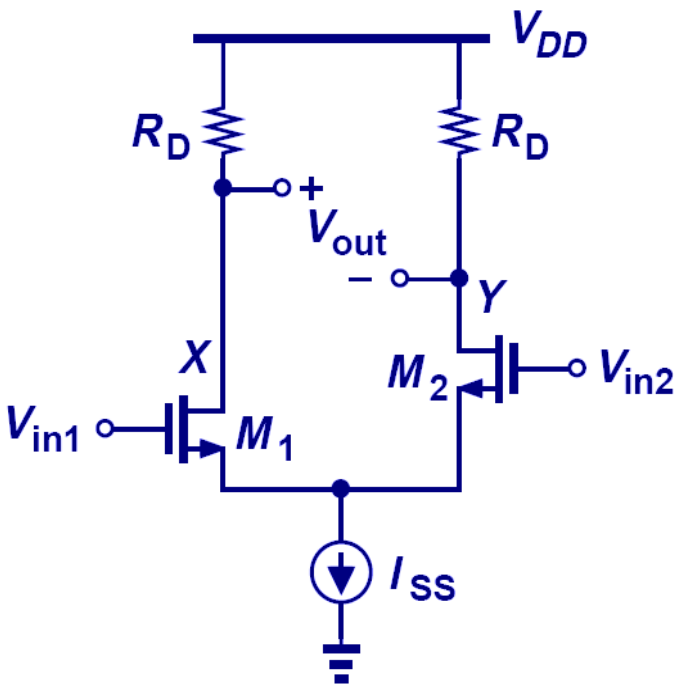

$$V_{DD} - R_D \frac{I_{SS}}{2} > V_{CM} - V_{TH}$$

- In order to maintain $M_1$ and $M_2$ in saturation, the common-mode output voltage cannot fall below the value above.
- This value usually limits voltage gain.

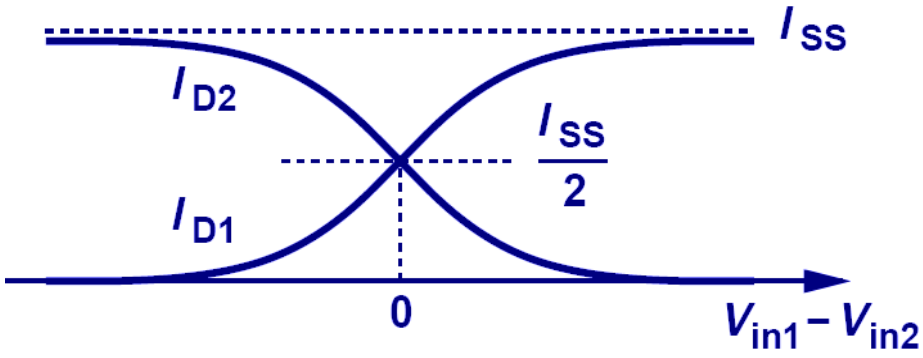
# Differential Response

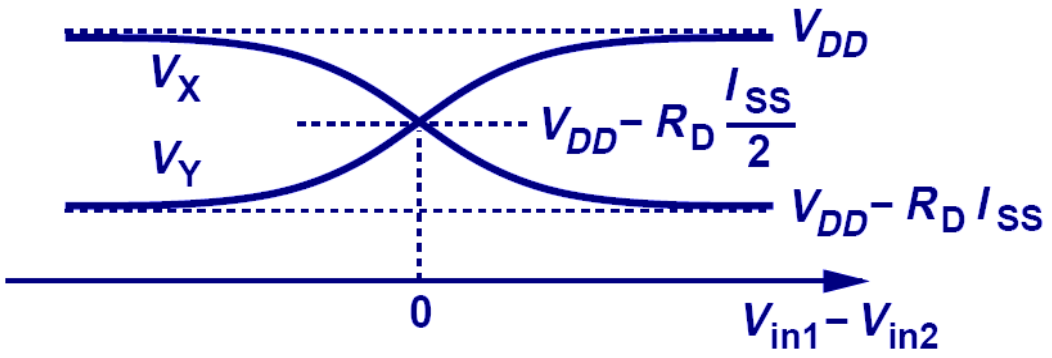



(a)



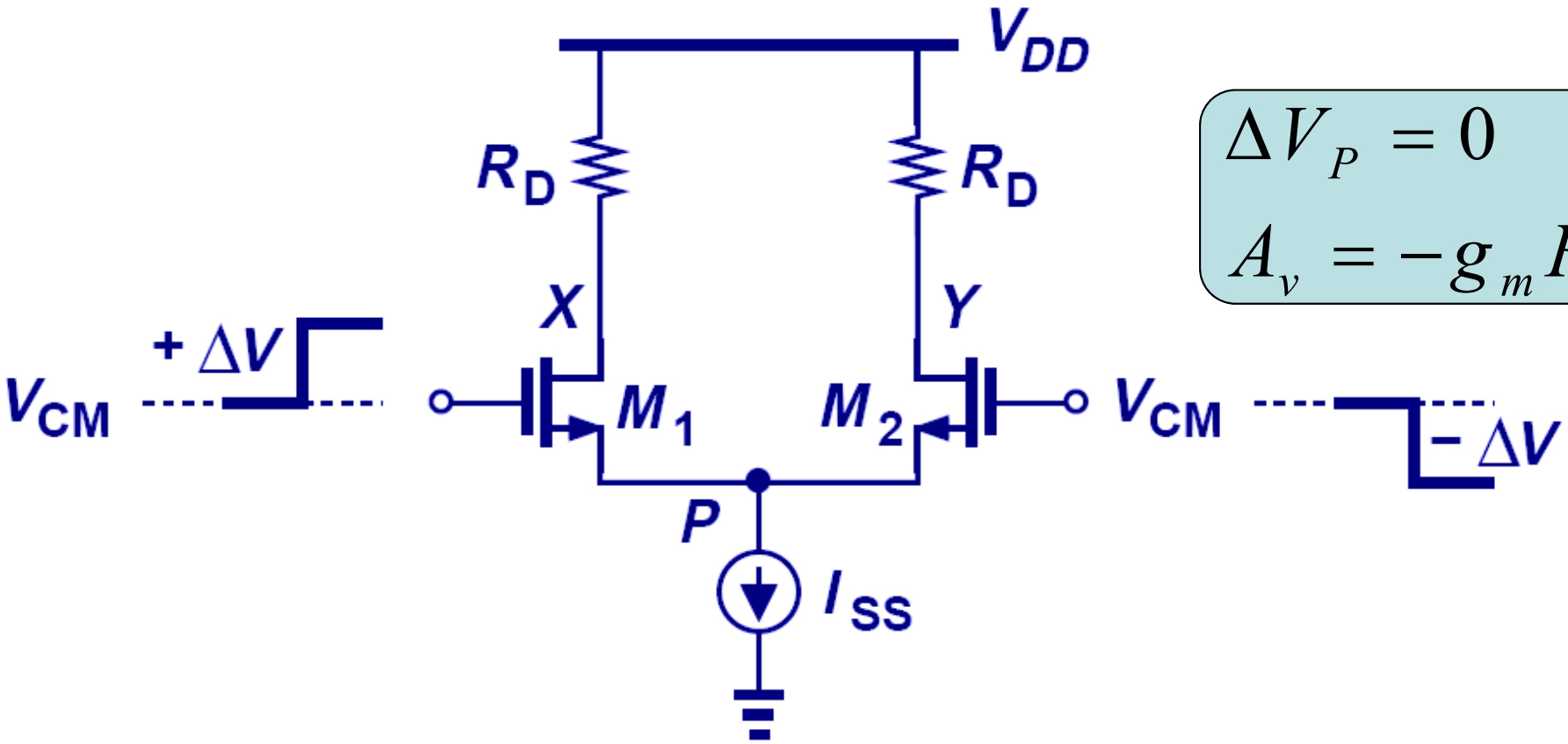

(b)




(c)

# Small-Signal Response

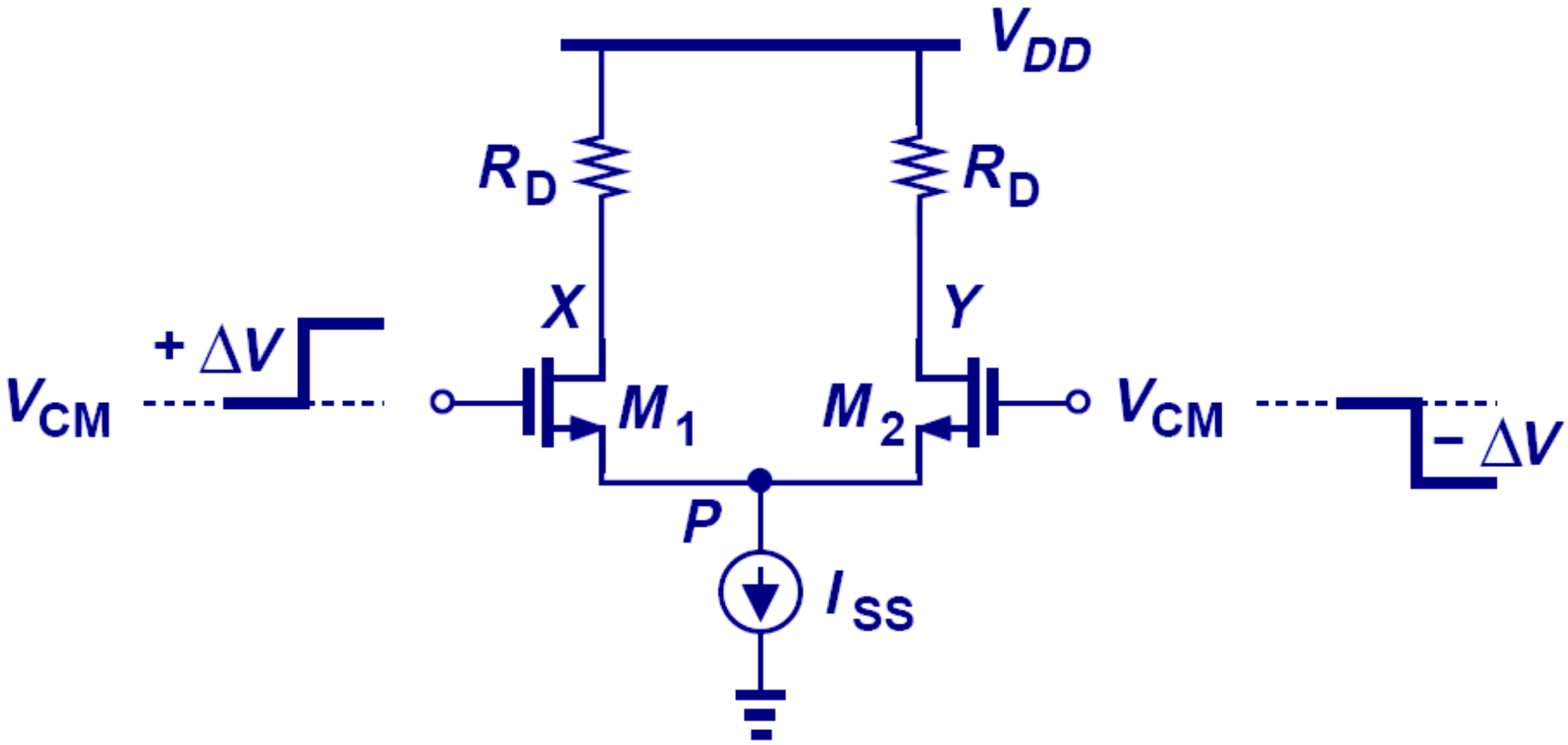



$$\Delta V_P = 0$$

$$A_v = -g_m R_D$$

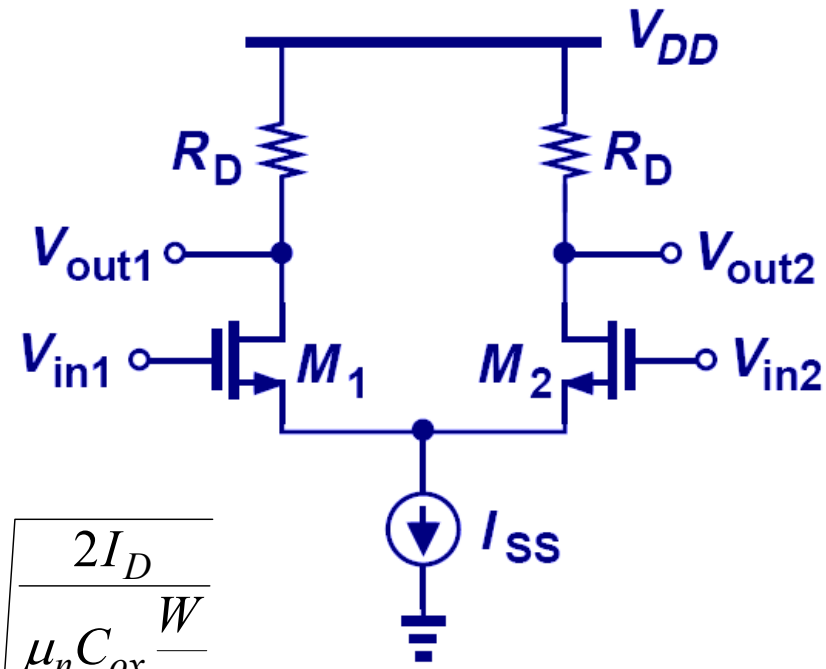
- **Similar to its bipolar counterpart, the MOS differential pair exhibits the same virtual ground node and small signal gain.**

# Power and Gain Tradeoff




- **In order to obtain the source gain as a CS stage, a MOS differential pair must dissipate twice the amount of current (assuming the same MOSFET overdrive voltage). This power and gain tradeoff is also echoed in its bipolar counterpart.**

# MOS Differential Pair's Large-Signal Response




1. Writing a KVL around the input network

$$V_{in1} - V_{GS1} = V_{in2} - V_{GS2}$$

2. Writing a KCL at the tail node

$$I_{D1} + I_{D2} = I_{SS}$$

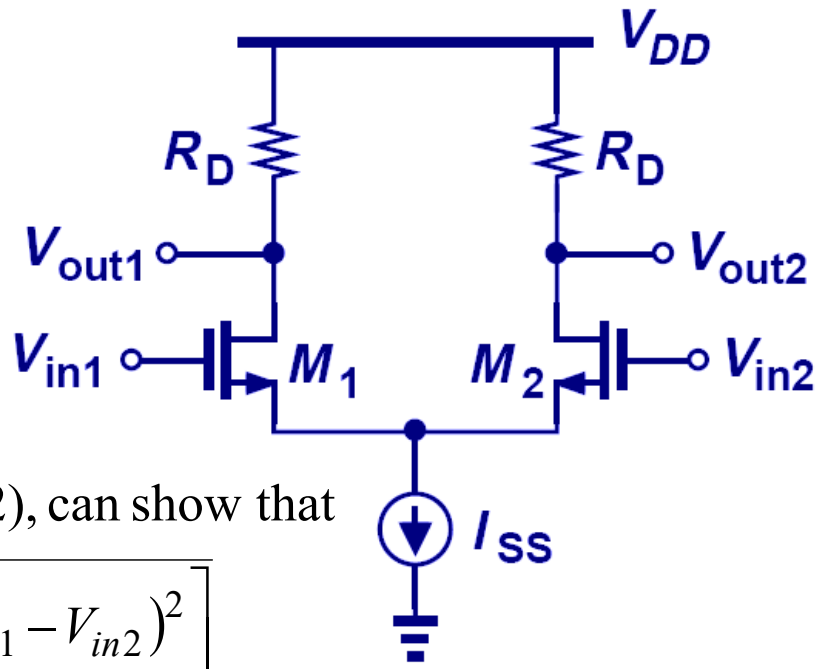
Using $I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS} - V_{TH})^2$ and $V_{GS} = V_{TH} + \sqrt{\frac{2I_D}{\mu_n C_{ox}\frac{W}{L}}}$

$$V_{in1} - V_{in2} = V_{GS1} - V_{GS2} = \sqrt{\frac{2}{\mu_n C_{ox}\frac{W}{L}}}\left(\sqrt{I_{D1}} - \sqrt{I_{D2}}\right)$$

Squaring both sides

$$(V_{in1} - V_{in2})^2 = \frac{2}{\mu_n C_{ox}\frac{W}{L}}\left(I_{D1} + I_{D2} - 2\sqrt{I_{D1}I_{D2}}\right) = \frac{2}{\mu_n C_{ox}\frac{W}{L}}\left(I_{SS} - 2\sqrt{I_{D1}I_{D2}}\right)$$

# MOS Differential Pair's Large-Signal Response




After some algebraic manipulations (see Razavi 10.3.2), can show that

$$I_{D1} = \frac{I_{SS}}{2} + \frac{V_{in1} - V_{in2}}{4}\sqrt{\mu_n C_{ox}\frac{W}{L}\left[4I_{SS} - \mu_n C_{ox}\frac{W}{L}(V_{in1} - V_{in2})^2\right]}$$

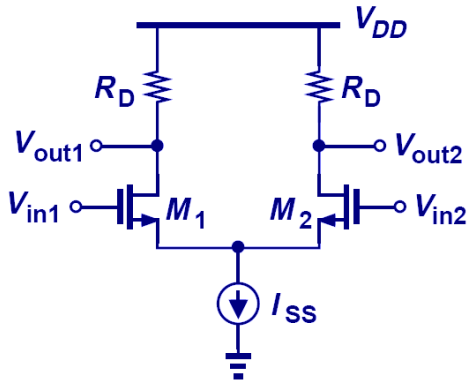
$$I_{D2} = \frac{I_{SS}}{2} + \frac{V_{in2} - V_{in1}}{4}\sqrt{\mu_n C_{ox}\frac{W}{L}\left[4I_{SS} - \mu_n C_{ox}\frac{W}{L}(V_{in2} - V_{in1})^2\right]}$$

$$I_{D1} - I_{D2} = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{in1} - V_{in2})\sqrt{\frac{4I_{SS}}{\mu_n C_{ox}\frac{W}{L}} - (V_{in1} - V_{in2})^2}$$

***Note, this equation is only valid for a certain maximum input differential voltage $V_{in1} - V_{in2}$**

# Maximum Differential Input Voltage

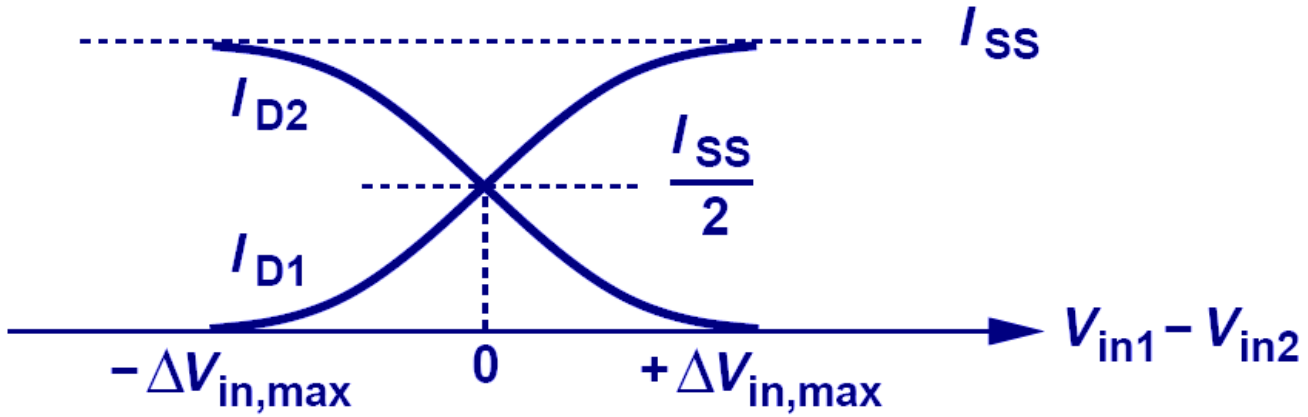
$$I_{D1} - I_{D2} = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{in1} - V_{in2})\sqrt{\frac{4I_{SS}}{\mu_n C_{ox}\frac{W}{L}} - (V_{in1} - V_{in2})^2}$$




The above equation is only valid when both $M_1$ and $M_2$ are on.

This stops when $V_{GS2} = V_{TH}$ and $V_{GS1}$ supports a full $I_{SS}$ value.

$$V_{GS1} = V_{TH} + \sqrt{\frac{2I_{SS}}{\mu_n C_{ox}\frac{W}{L}}}$$

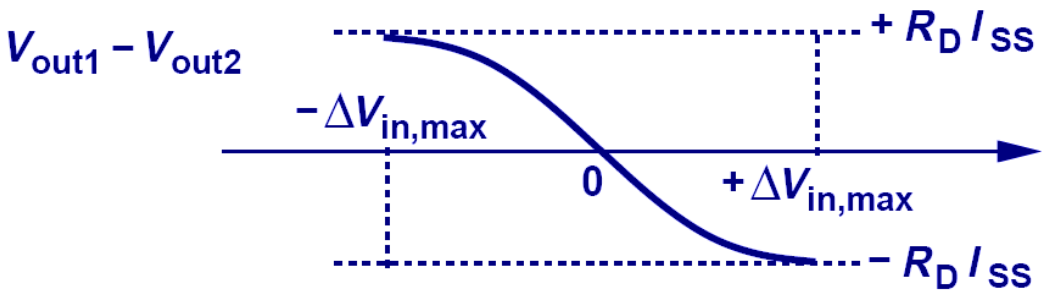



$$|V_{in1} - V_{in2}|_{max} = \sqrt{2}(V_{GS} - V_{TH})_{equil} = \sqrt{\frac{2I_{SS}}{\mu_n C_{ox}\frac{W}{L}}}$$

- **There exists a finite differential input voltage that completely steers the tail current from one transistor to the other. This value is known as the maximum differential input voltage.**

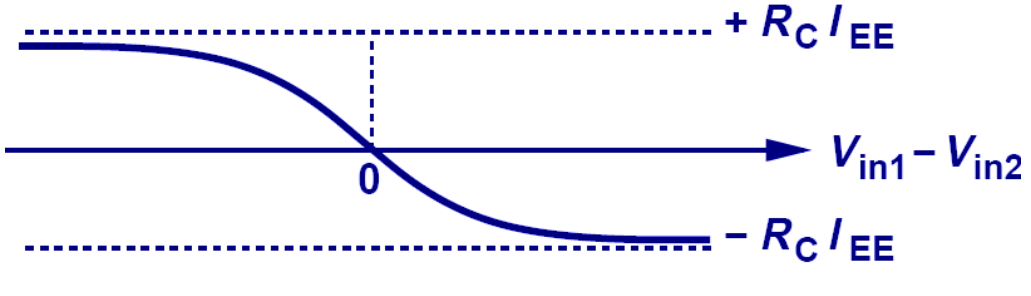
# Contrast Between MOS and Bipolar Differential Pairs

*MOS*




$$V_{out1} - V_{out2} = -R_D \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{in1} - V_{in2}) \sqrt{\frac{4I_{SS}}{\mu_n C_{ox} \frac{W}{L}} - (V_{in1} - V_{in2})^2}$$

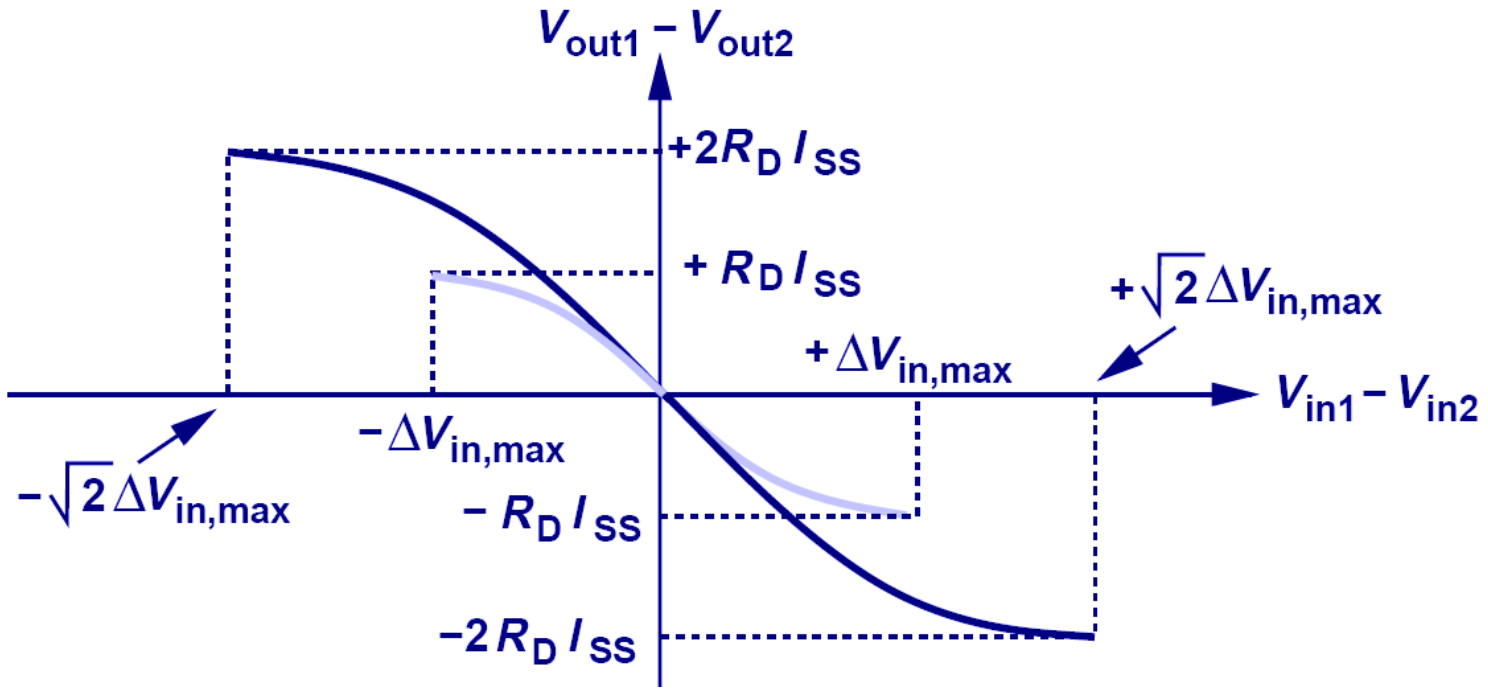
*Bipolar*




$$V_{out1} - V_{out2} = -R_C I_{EE} \tanh\left(\frac{V_{in1} - V_{in2}}{2V_T}\right)$$

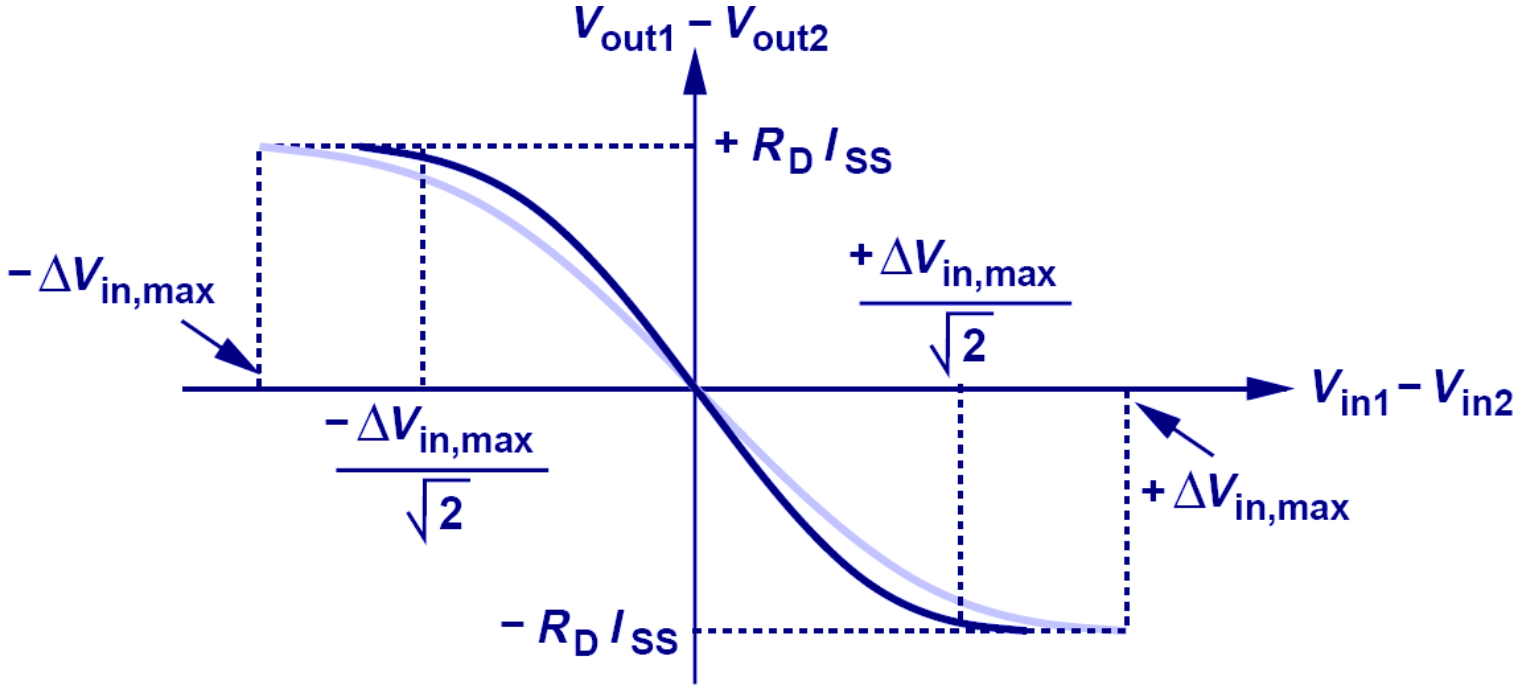
- **In a MOS differential pair, there exists a finite differential input voltage to completely switch the current from one transistor to the other, whereas, in a bipolar pair that voltage is infinite.**

# The effects of Doubling the Tail Current



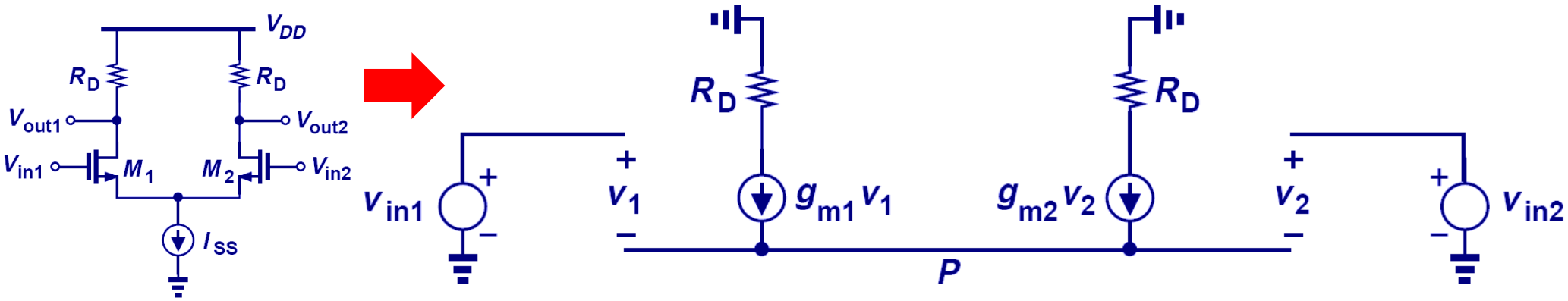

- Since $I_{SS}$ is doubled and W/L is unchanged, the equilibrium overdrive voltage for each transistor must increase by $\sqrt{2}$ to accommodate this change, thus $\Delta V_{in,max}$ increases by $\sqrt{2}$ as well. Moreover, since $I_{SS}$ is doubled, the differential output swing will double.
- Small signal gain also increases by $\sqrt{2}$
- Linear input range increases, assuming RD value is small enough to keep transistors in saturation

# The effects of Doubling W/L




- Since W/L is doubled and the tail current remains unchanged, the equilibrium overdrive voltage will be lowered by $\sqrt{2}$ to accommodate this change, thus $\Delta V_{in,max}$ will be lowered by $\sqrt{2}$ as well. Moreover, the differential output swing will remain unchanged since neither $I_{SS}$ nor $R_D$ has changed
- Small signal gain increases by $\sqrt{2}$
- Linear input range decreases

# Small-Signal Analysis of MOS Differential Pair

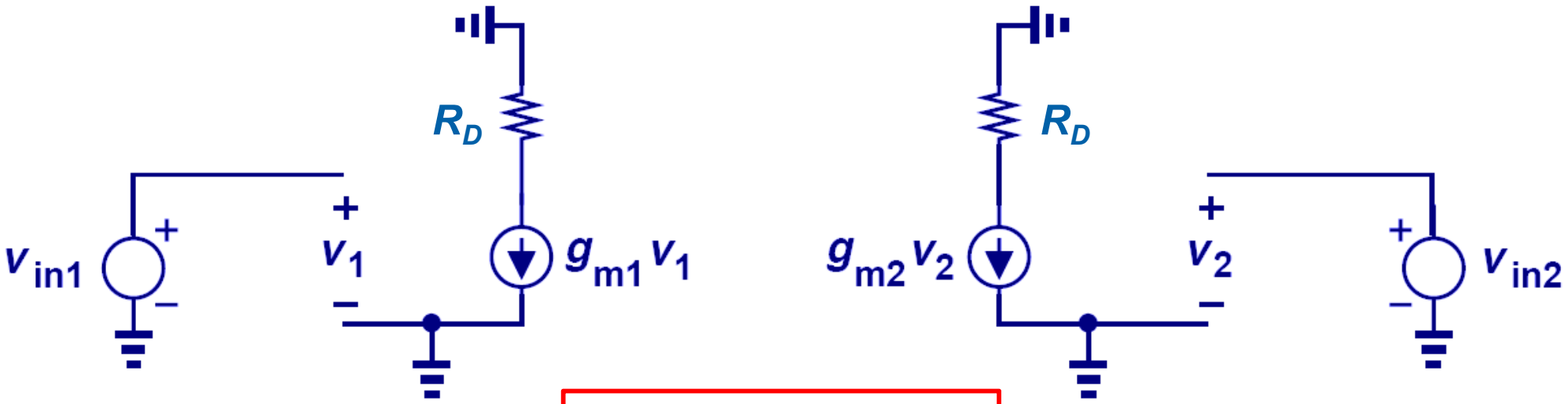



$$I_{D1} - I_{D2} = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{in1} - V_{in2})\sqrt{\frac{4I_{SS}}{\mu_n C_{ox}\frac{W}{L}} - (V_{in1} - V_{in2})^2}$$

$$\approx \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{in1} - V_{in2})\sqrt{\frac{4I_{SS}}{\mu_n C_{ox}\frac{W}{L}}} = \sqrt{\mu_n C_{ox}\frac{W}{L}2\left(\frac{I_{SS}}{2}\right)}(V_{in1} - V_{in2}) = g_m(V_{in1} - V_{in2})$$

- **When the input differential signal is small compared to $4I_{SS}/\mu_n C_{ox}(W/L)$, the output differential current is linearly proportional to it, and small-signal model can be applied.**

# Virtual Ground and Half Circuit




$$v_{out1} = -g_m R_D v_{in1}$$

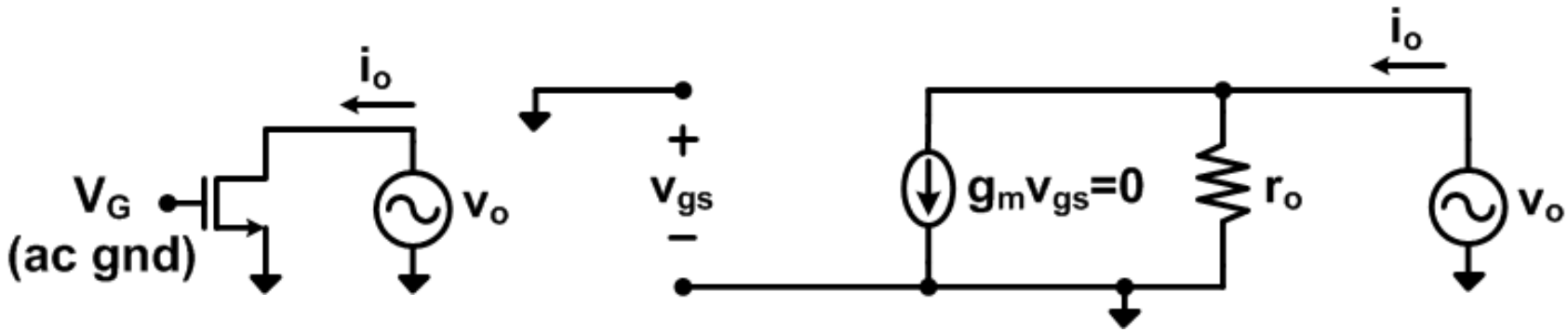
$$v_{out2} = -g_m R_D v_{in2}$$

$$\Delta V_P = 0$$

$$A_v = -g_m R_D$$

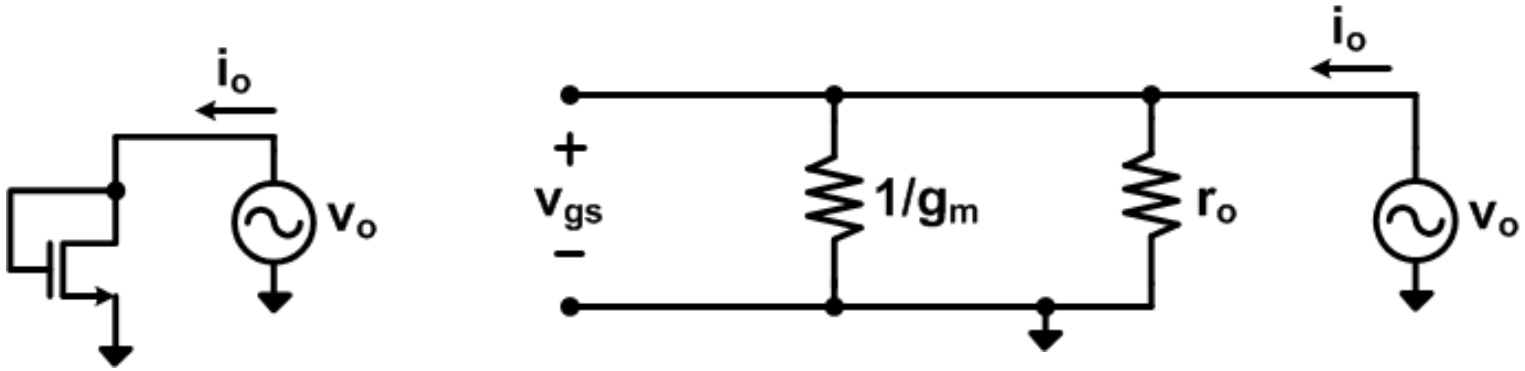
- **Applying the same analysis as the bipolar case, we will arrive at the same conclusion that node P will not move for small input signals and the concept of half circuit can be used to calculate the gain.**

# Small-Signal Impedance: Simple Current Source (Finite $r_o$)



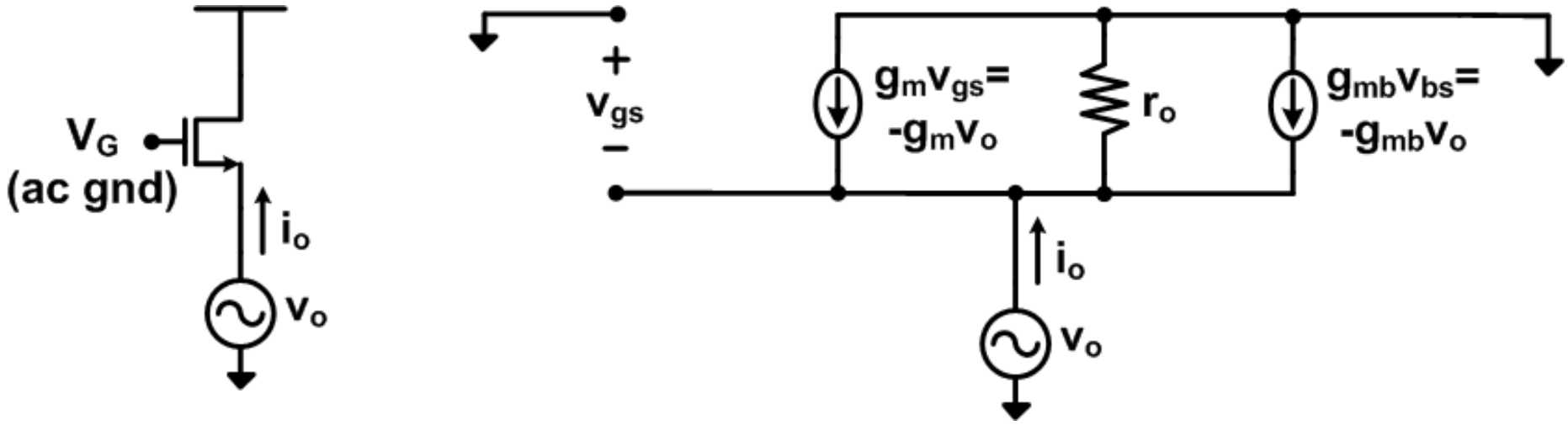

$$r_{out} = \frac{1}{g_o}$$

# Small-Signal Impedance: "Diode" Load (Finite $r_o$)




$$r_{out} = \frac{1}{g_m} \Big\| r_o = \frac{1}{g_m + g_o} \approx \frac{1}{g_m}$$

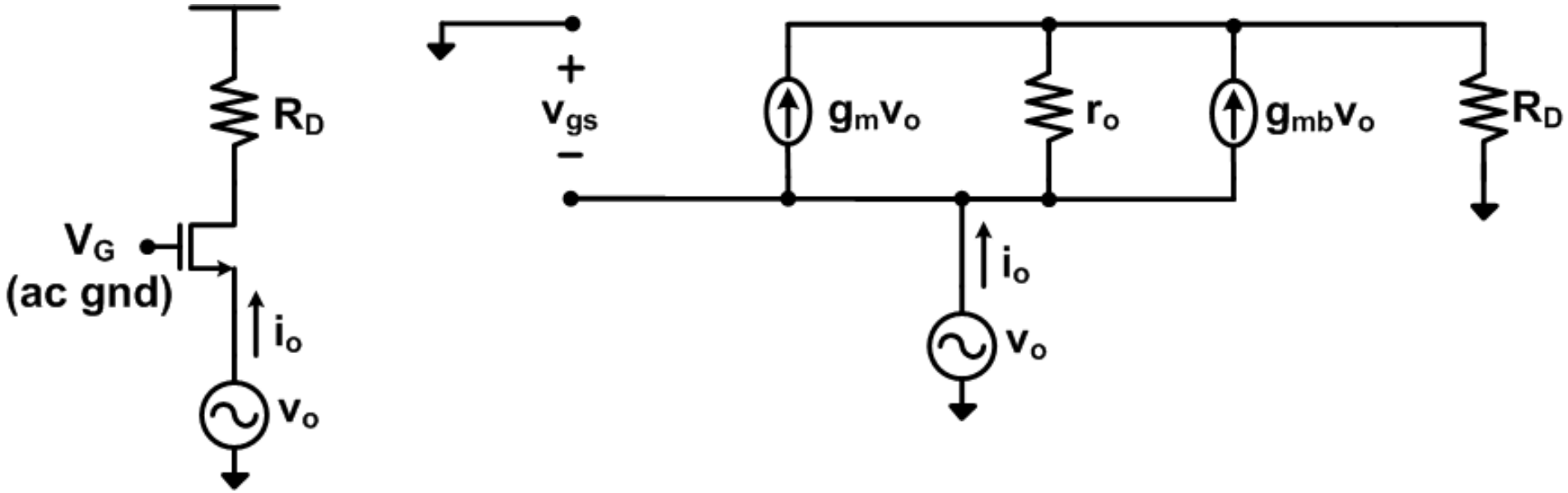
# Small-Signal Impedance: Looking Into Source (Finite $r_o$ and $g_{mb}$)




$$i_o = (g_m + g_{mb})v_o + \frac{v_o}{r_o} = (g_m + g_{mb} + g_o)v_o$$

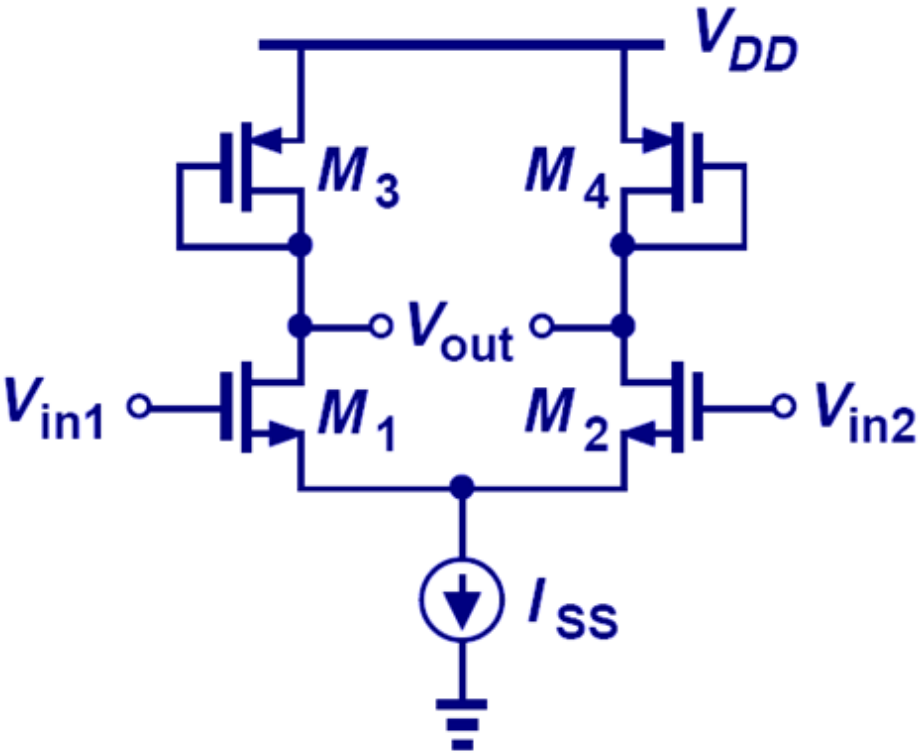
$$r_{out} = \frac{1}{g_m + g_{mb} + g_o} = \frac{1}{g_m} \left\| \frac{1}{g_{mb}} \right\| r_o \approx \frac{1}{g_m}$$

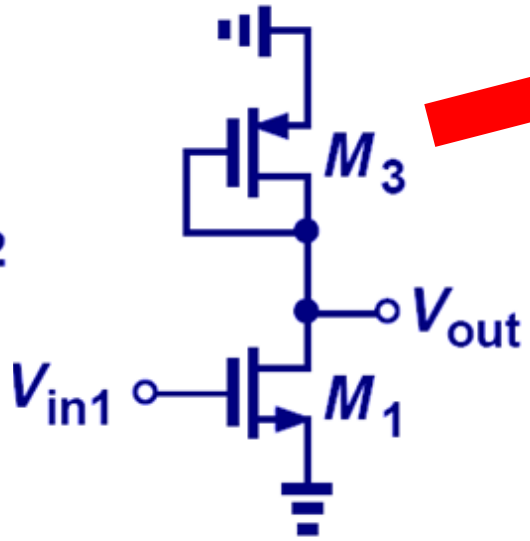
# Small-Signal Impedance: Looking Into Source w/ $R_D$ ($r_o$ and $g_{mb}$)

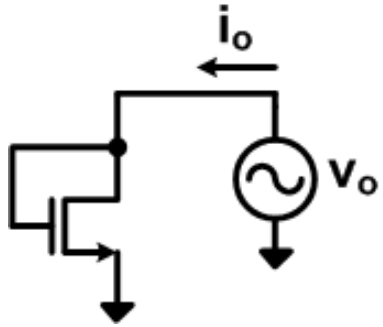



$$r_{out} = \frac{1}{g_m + g_{mb} + g_o}\left(1 + \frac{R_D}{r_o}\right)$$

# MOS Differential Pair Half Circuit Example I



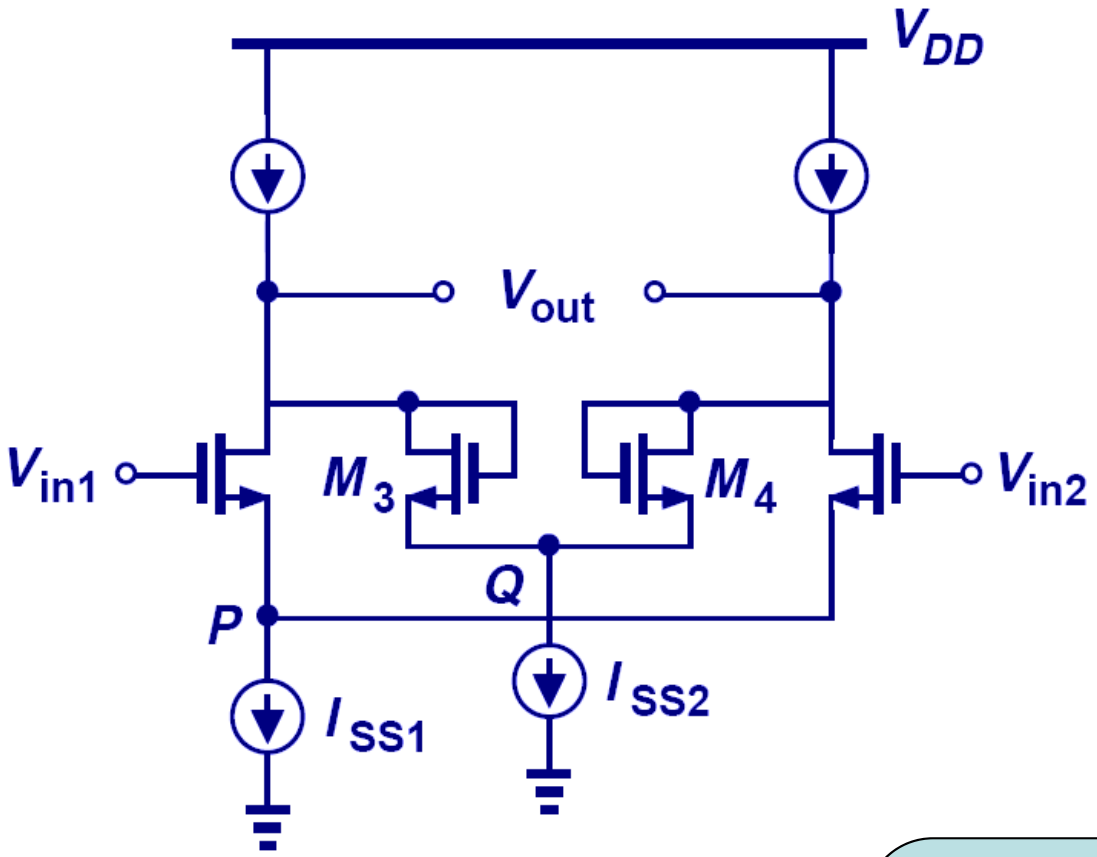



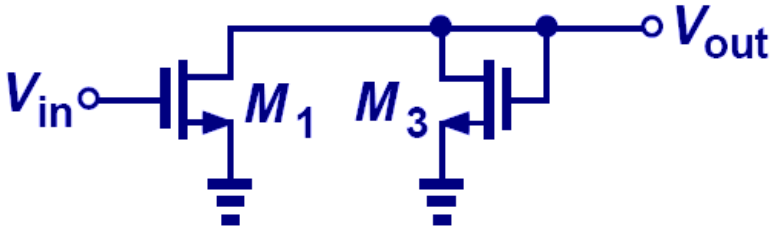

$$r_{out} = \frac{1}{g_m} \Big\| r_o \approx \frac{1}{g_m}$$

$$\lambda \neq 0$$

$$A_v = -g_{m1}\left(\frac{1}{g_{m3}} \| r_{O3} \| r_{O1}\right) \approx -\frac{g_{m1}}{g_{m3}}$$

# MOS Differential Pair Half Circuit Example II

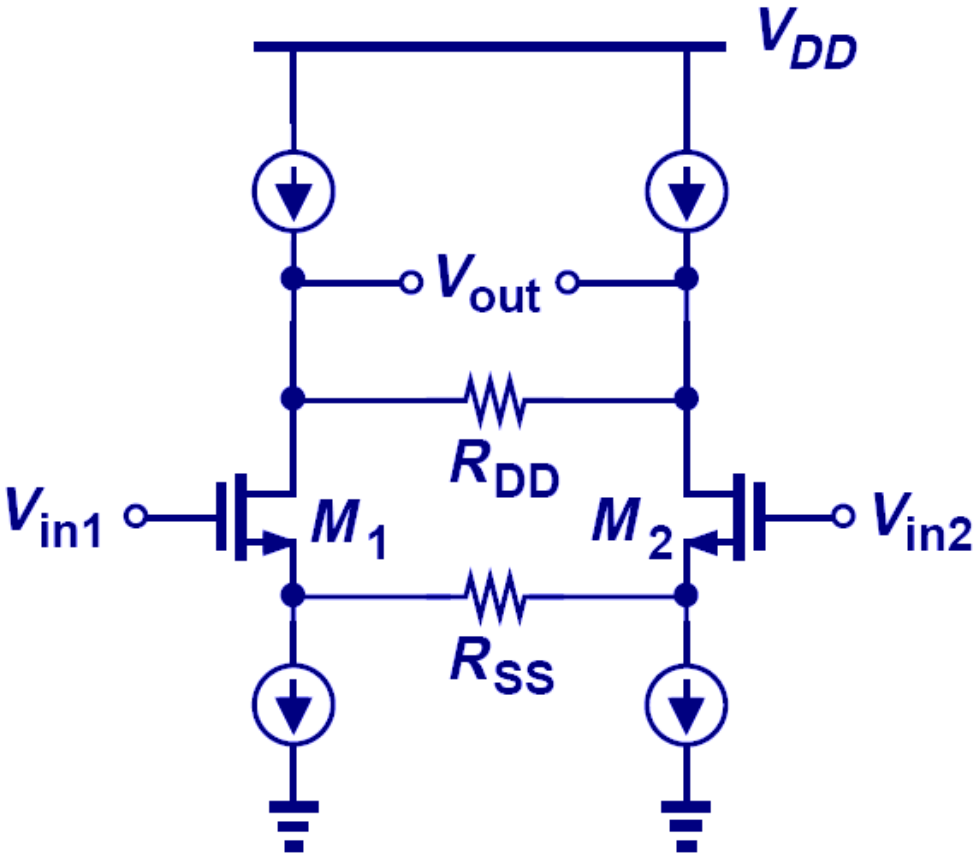


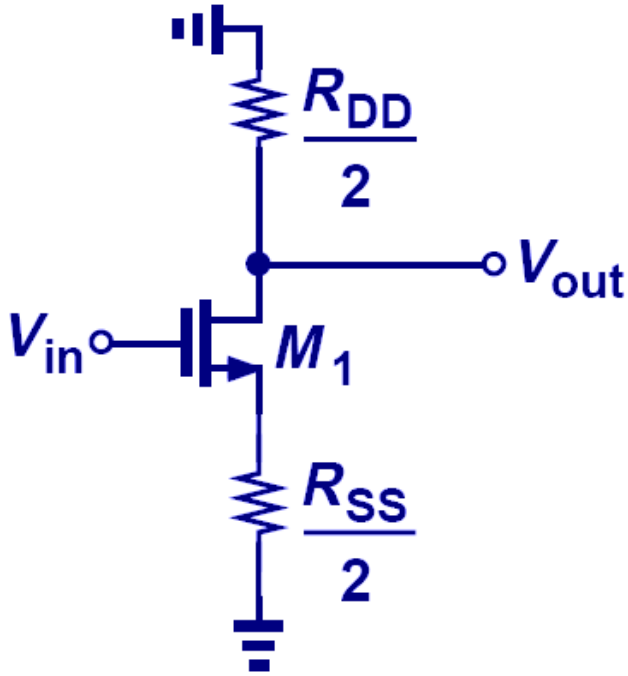




$$\lambda = 0$$

$$A_v = -\frac{g_{m1}}{g_{m3}}$$

# MOS Differential Pair Half Circuit Example III



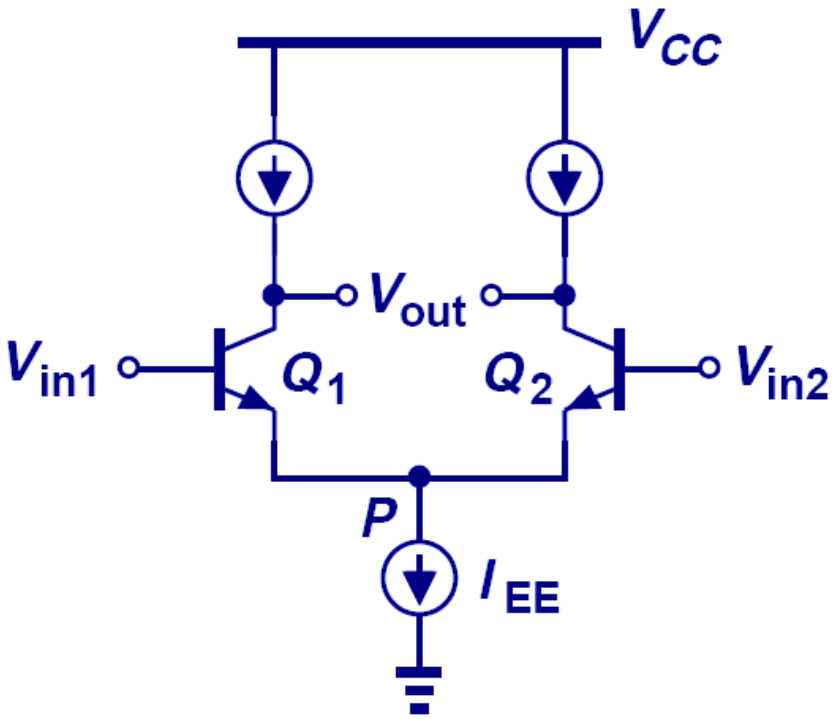

$$\lambda = 0$$

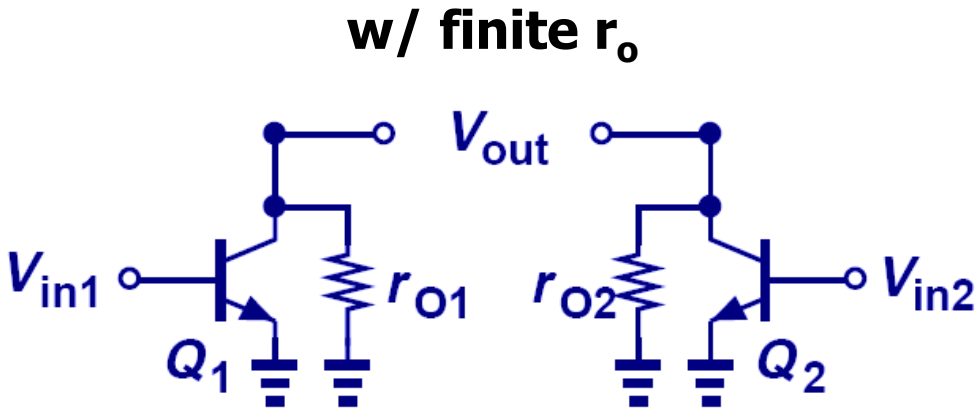
$$A_v = -\frac{R_{DD}/2}{R_{SS}/2 + 1/g_m}$$

# Agenda

- General considerations
- Bipolar differential pair
- MOS differential pair
- Cascode differential amplifiers
- Common-mode rejection
- Differential pair with active load

# Maximum Differential Amplifier Gain

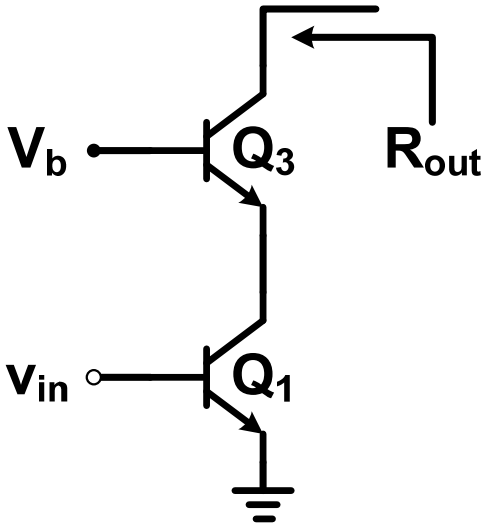


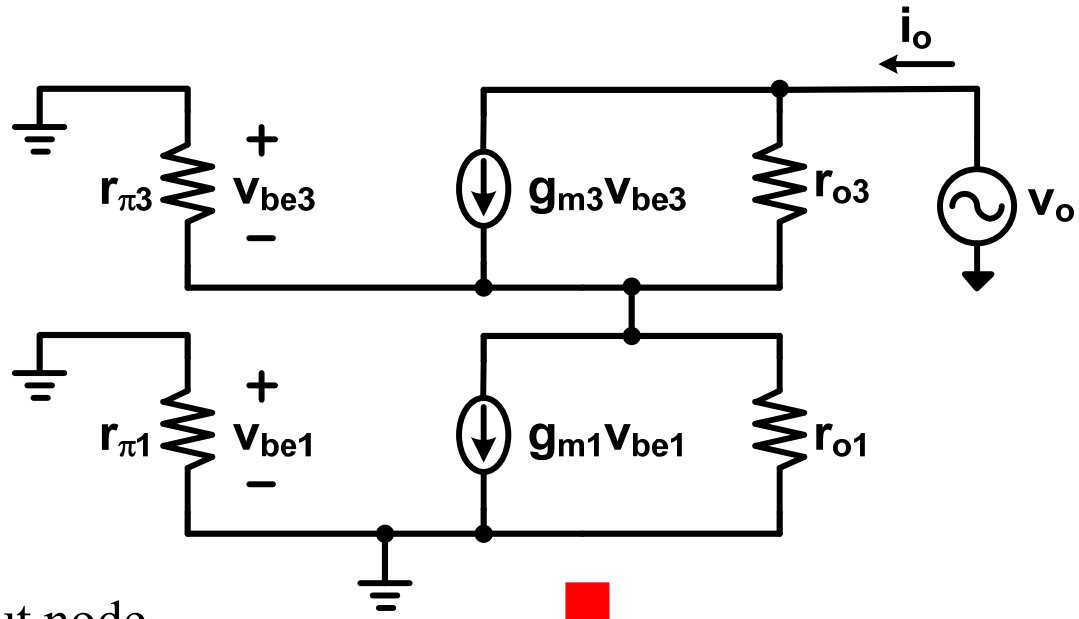




$$\frac{v_{out1} - v_{out2}}{v_{in1} - v_{in2}} = -g_m r_O$$

- With ideal current source loads, the differential gain is limited by the intrinsic transistor gain ($g_m r_o$)
- How to increase the gain further?
  - Use a topology which boosts the output resistance

# Bipolar Cascode Topology



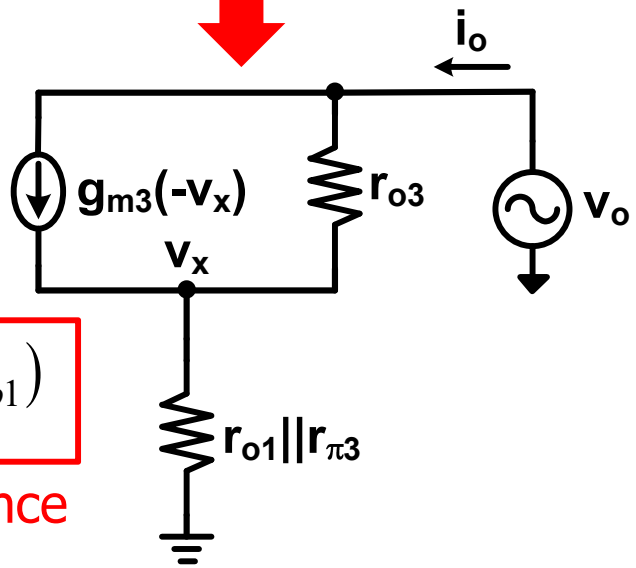




$$v_x = i_o\left(r_{\pi 3} \| r_{o1}\right)$$

Writing a KCL at the output node

$$-i_o + g_{m3}\left(-v_x\right) + \frac{v_o - v_x}{r_{o3}} = 0$$

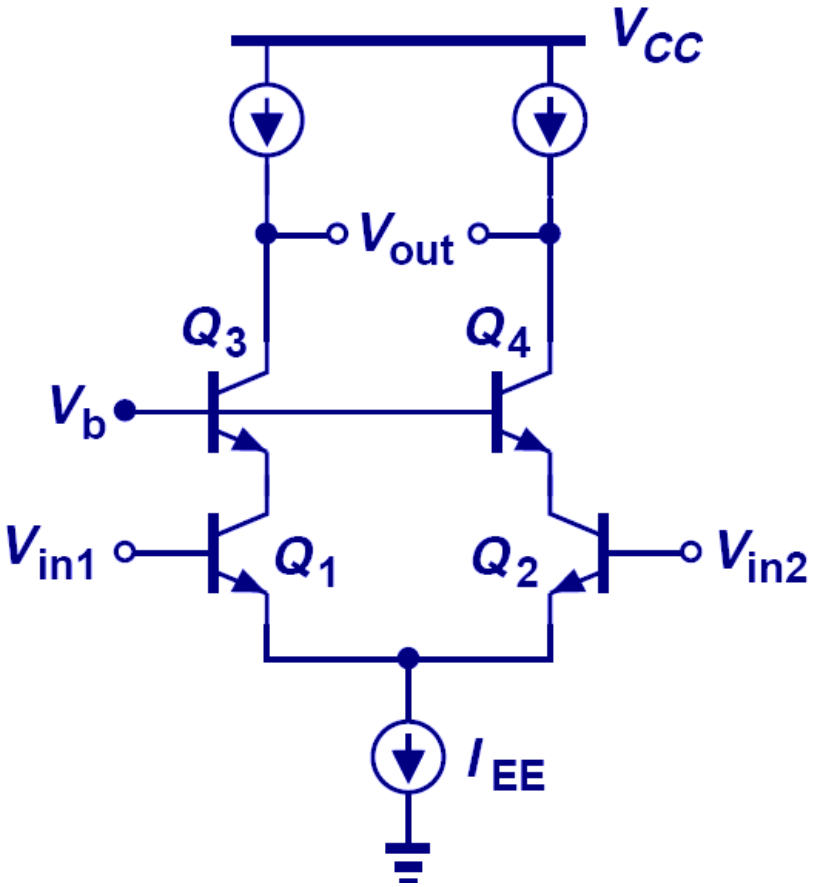
$$-i_o - g_{m3} i_o \left(r_{\pi 3} \| r_{o1}\right) - \frac{i_o\left(r_{\pi 3} \| r_{o1}\right)}{r_{o3}} = -\frac{v_o}{r_{o3}}$$




$$R_{out} = \frac{v_o}{i_o} = r_{o3} + r_{\pi 3} \| r_{o1} + g_{m3} r_{o3}\left(r_{\pi 3} \| r_{o1}\right) \approx g_{m3} r_{o3}\left(r_{\pi 3} \| r_{o1}\right)$$

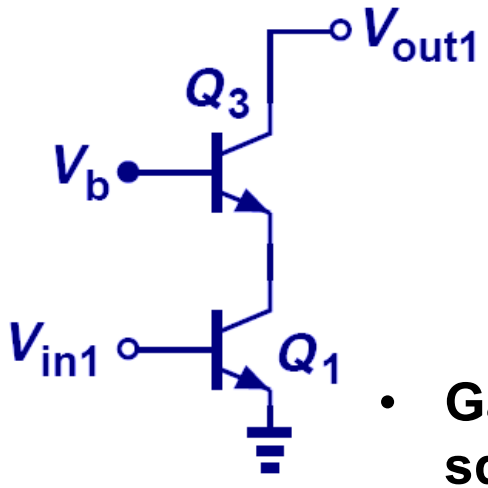
The dominant term is the bottom effective resistance boosted by the gain of the top transistor ($g_{m3}r_{o3}$)

# Bipolar Cascode Differential Pair




**Cascode Output Resistance**

$$R_{out} = r_{o3} + r_{o1} \| r_{\pi 3} + g_{m3} r_{o3} \left( r_{o1} \| r_{\pi 3} \right)$$
$$\approx g_{m3} r_{o3} \left( r_{o1} \| r_{\pi 3} \right)$$

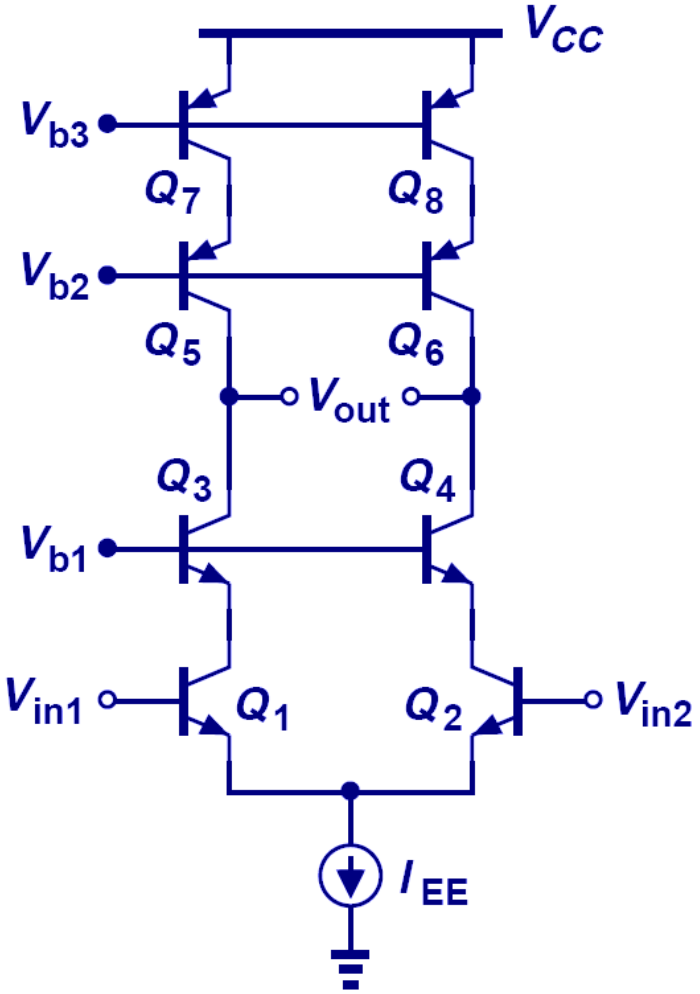


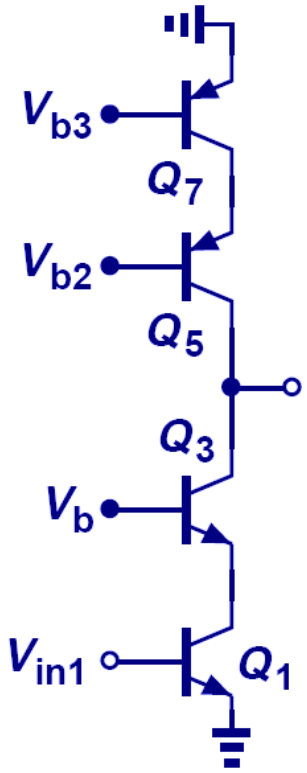

$$A_v = -g_{m1} \left[ r_{o3} + r_{o1} \| r_{\pi 3} + g_{m3} r_{o3} \left( r_{o1} \| r_{\pi 3} \right) \right]$$
$$\approx -g_{m1} g_{m3} r_{o3} \left( r_{o1} \| r_{\pi 3} \right)$$

Slight approximation here. More when we study Cascodes in detail.

- **Gain is roughly squared relative to the simple differential pair**
- **Trade-off is reduced output voltage swing range**

# Bipolar Telescopic Cascode

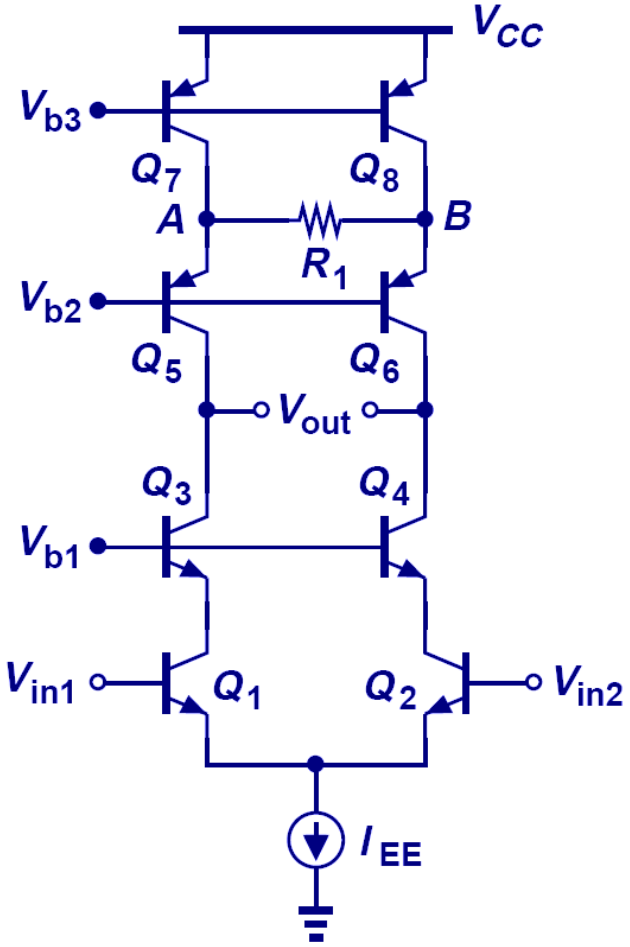


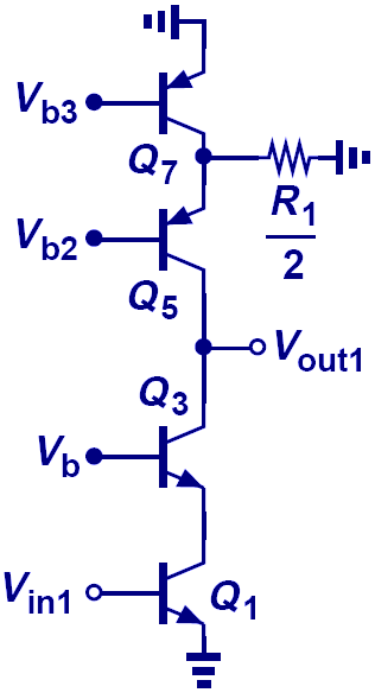




$$A_v = -g_{m1}\left[\left(r_{o3} + r_{o1}\|r_{\pi 3} + g_{m3}r_{o3}\left(r_{o1}\|r_{\pi 3}\right)\right)\|\left(r_{o5} + r_{o7}\|r_{\pi 5} + g_{m5}r_{o5}\left(r_{o7}\|r_{\pi 5}\right)\right)\right]$$

$$\approx -g_{m1}\left[\left(g_{m3}r_{o3}\left(r_{o1}\|r_{\pi 3}\right)\right)\|\left(g_{m5}r_{o5}\left(r_{o7}\|r_{\pi 5}\right)\right)\right]$$

# Example: Bipolar Telescopic Parasitic Resistance

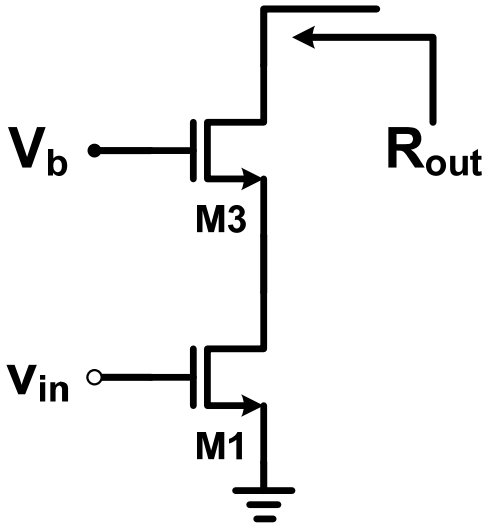


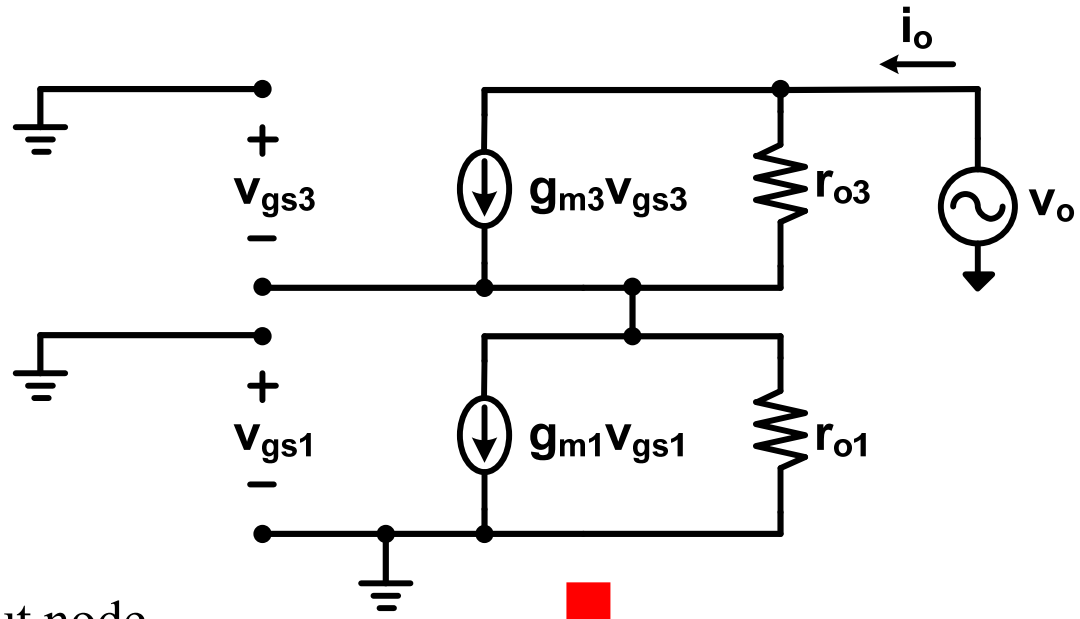




$$R_{op} = r_{O5}\left[1 + g_{m5}\left(r_{O7} \parallel r_{\pi 5} \parallel \frac{R_1}{2}\right)\right] + r_{O7} \parallel r_{\pi 5} \parallel \frac{R_1}{2} \approx g_{m5} r_{O5}\left(r_{O7} \parallel r_{\pi 5} \parallel \frac{R_1}{2}\right)$$

$$A_v = -g_{m1}\left[g_{m3} r_{O3}\left(r_{O1} \parallel r_{\pi 3}\right)\right] \parallel R_{op}$$

# MOS Cascode Topology



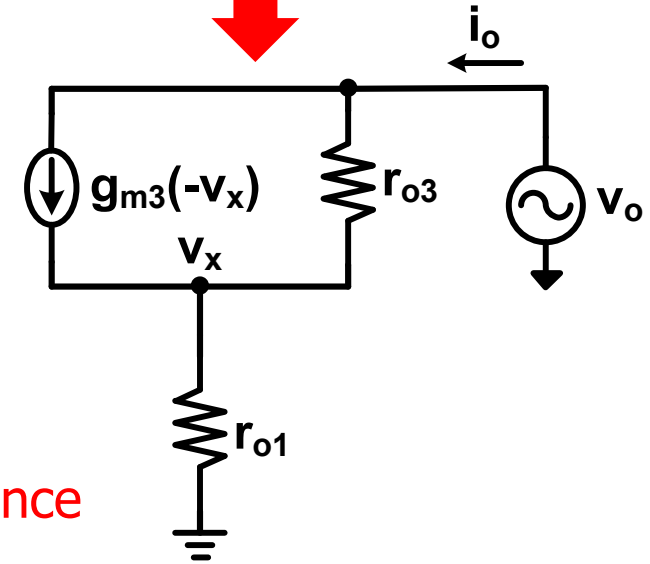

$$v_x = i_o r_{o1}$$

Writing a KCL at the output node

$$-i_o + g_{m3}(-v_x) + \frac{v_o - v_x}{r_{o3}} = 0$$

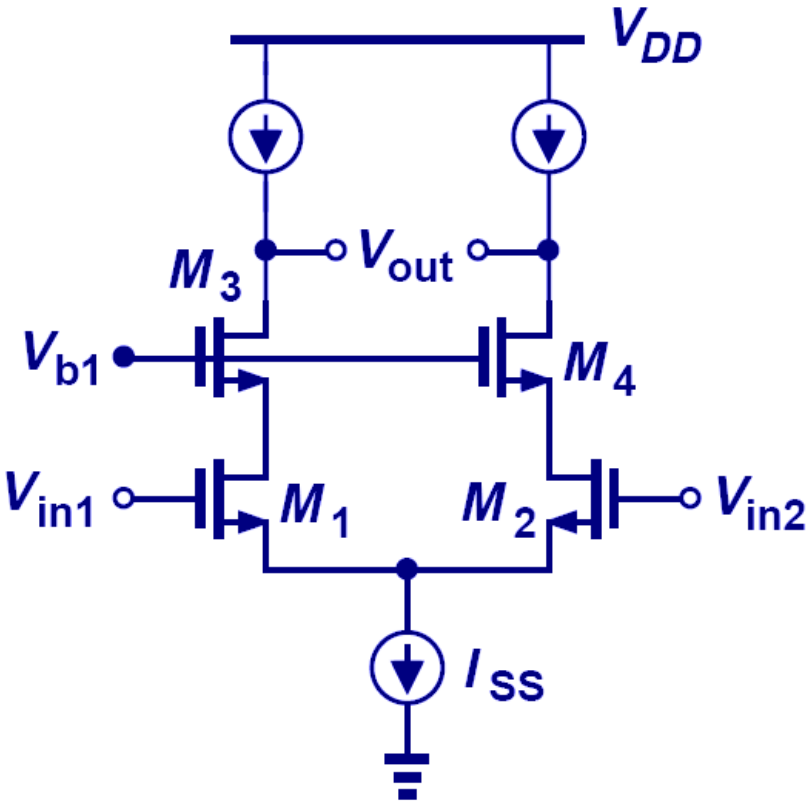
$$-i_o - g_{m3} i_o r_{o1} - \frac{i_o r_{o1}}{r_{o3}} = -\frac{v_o}{r_{o3}}$$

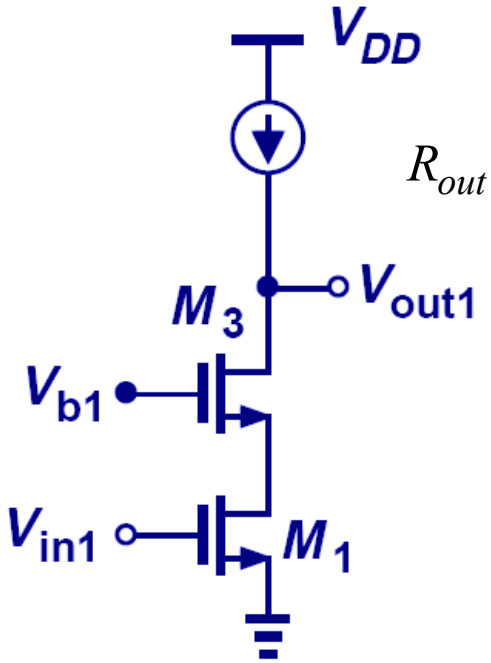
$$R_{out} = \frac{v_o}{i_o} = r_{o3} + r_{o1} + g_{m3} r_{o3} r_{o1} \approx g_{m3} r_{o3} r_{o1}$$




The dominant term is the bottom effective resistance boosted by the gain of the top transistor ($g_{m3}r_{o3}$)

# MOS Cascode Differential Pair



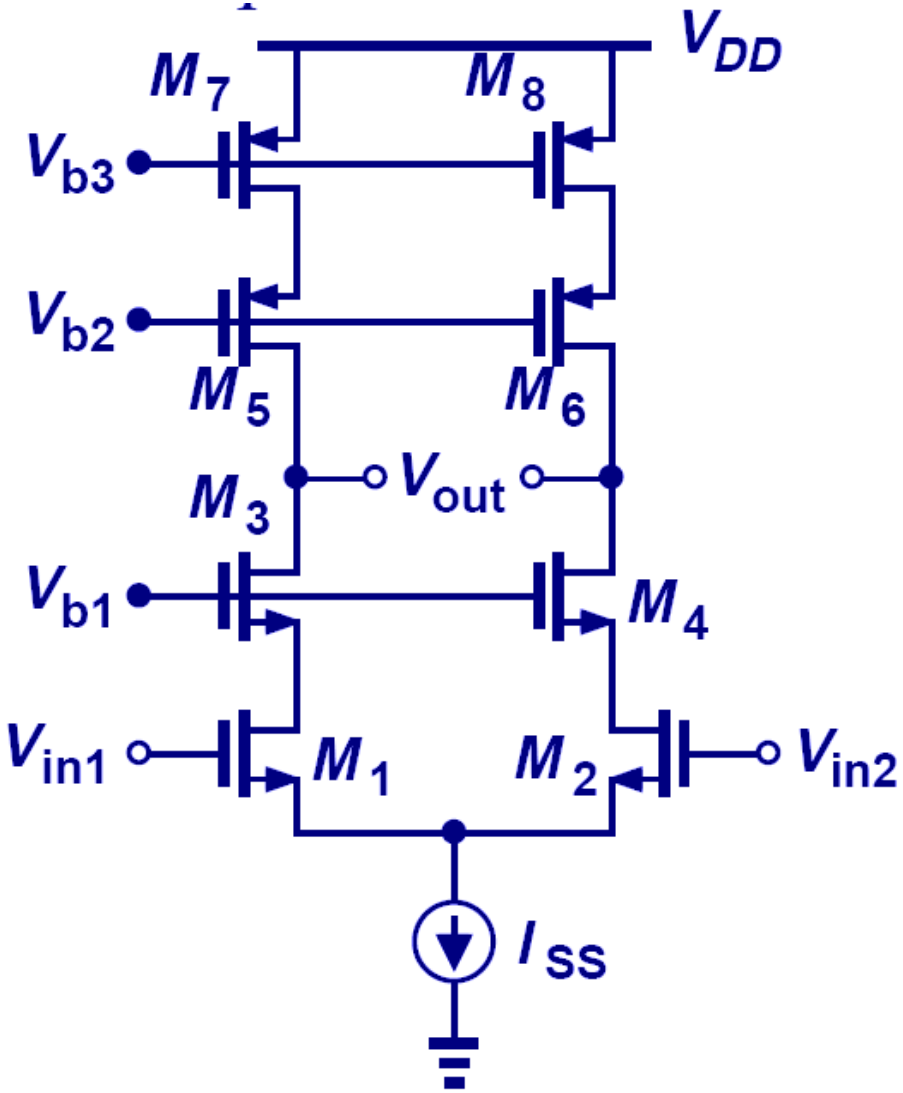

**Cascode Output Resistance**

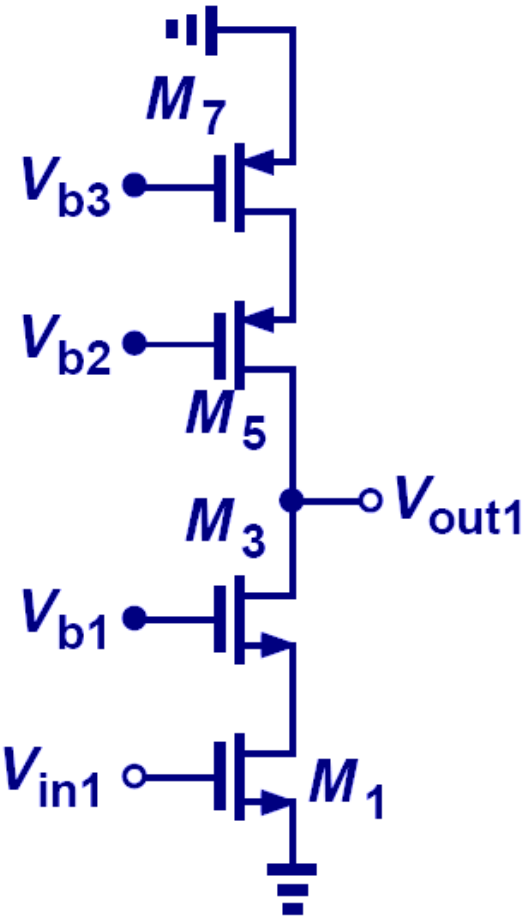
$$R_{out} = r_{o3} + r_{o1} + g_{m3} r_{o3} r_{o1}$$
$$\approx g_{m3} r_{o3} r_{o1}$$

$$A_v = -g_{m1}\left[r_{o3} + r_{o1} + g_{m3} r_{o3} r_{o1}\right]$$
$$\approx -g_{m1} g_{m3} r_{o3} r_{o1}$$

- **Gain is roughly squared relative to the simple differential pair**
- **Trade-off is reduced output voltage swing range**

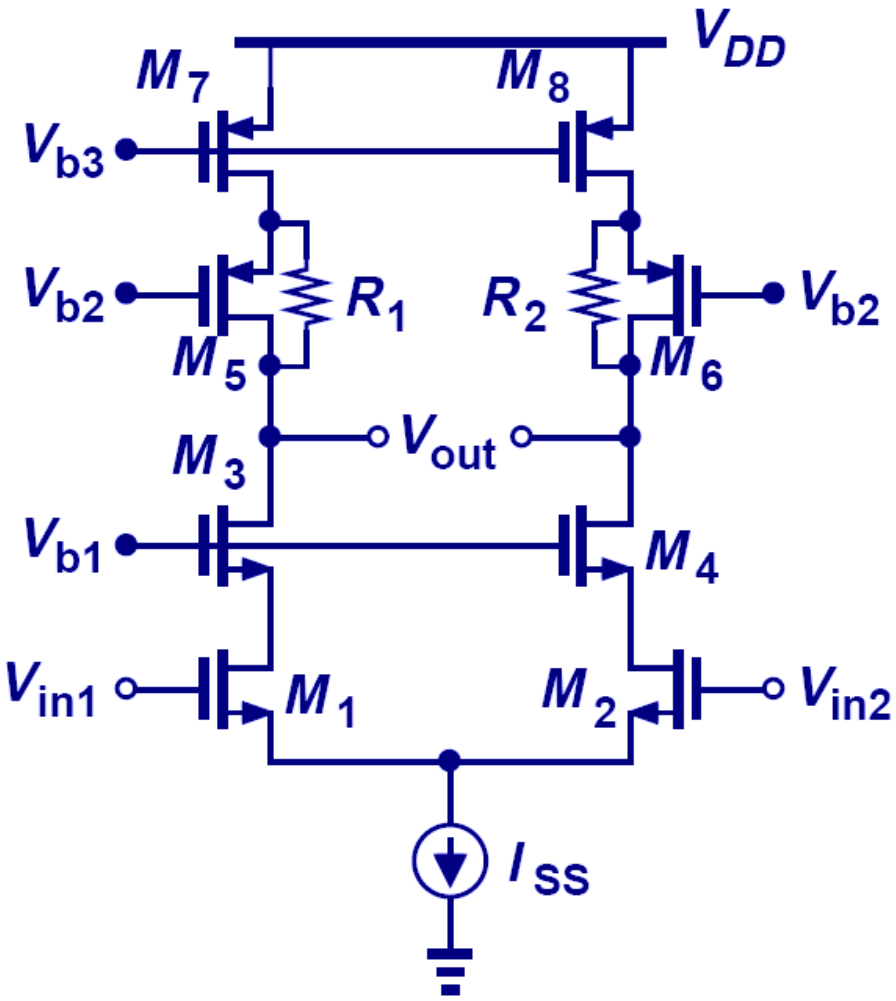
# MOS Telescopic Cascode

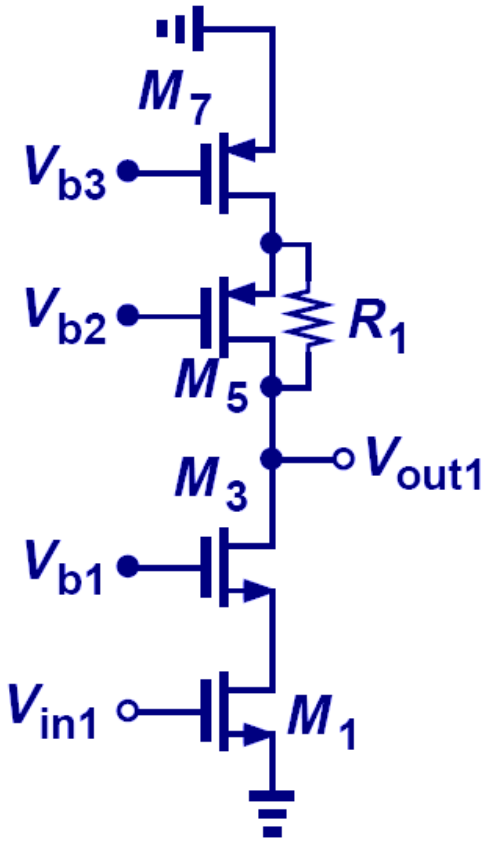



$$A_v \approx -g_{m1}\left[\left(g_{m3}r_{O3}r_{O1}\right) \| \left(g_{m5}r_{O5}r_{O7}\right)\right]$$

# Example: MOS Telescopic Parasitic Resistance



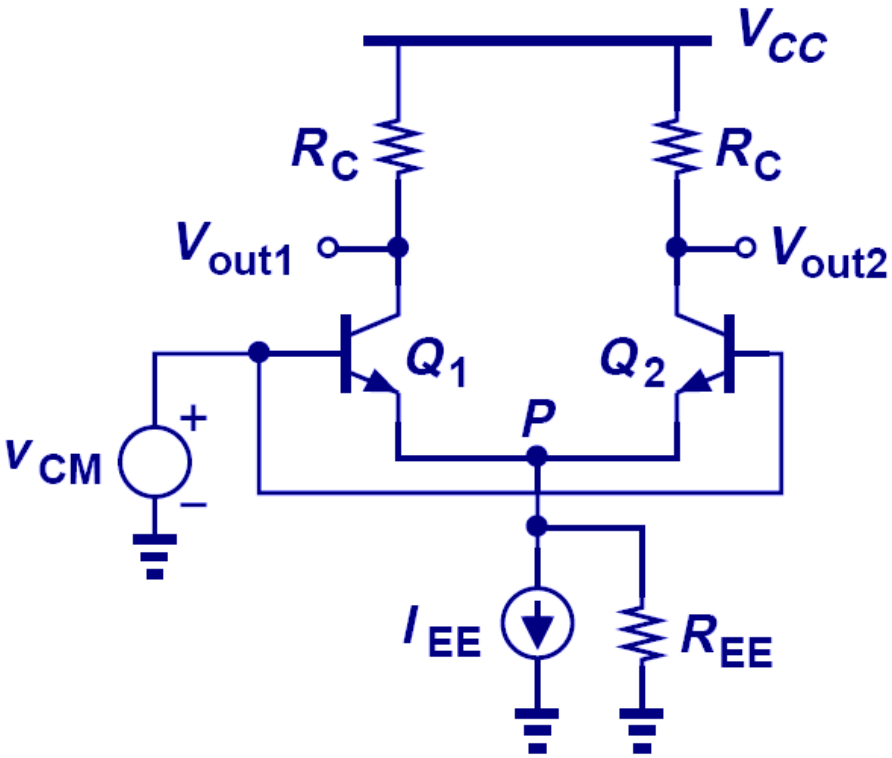

$$R_{op} = r_{o5}\|R_1 + r_{o7} + g_{m5}\left(r_{o5}\|R_1\right)r_{o7} \approx g_{m5}\left(r_{o5}\|R_1\right)r_{o7}$$

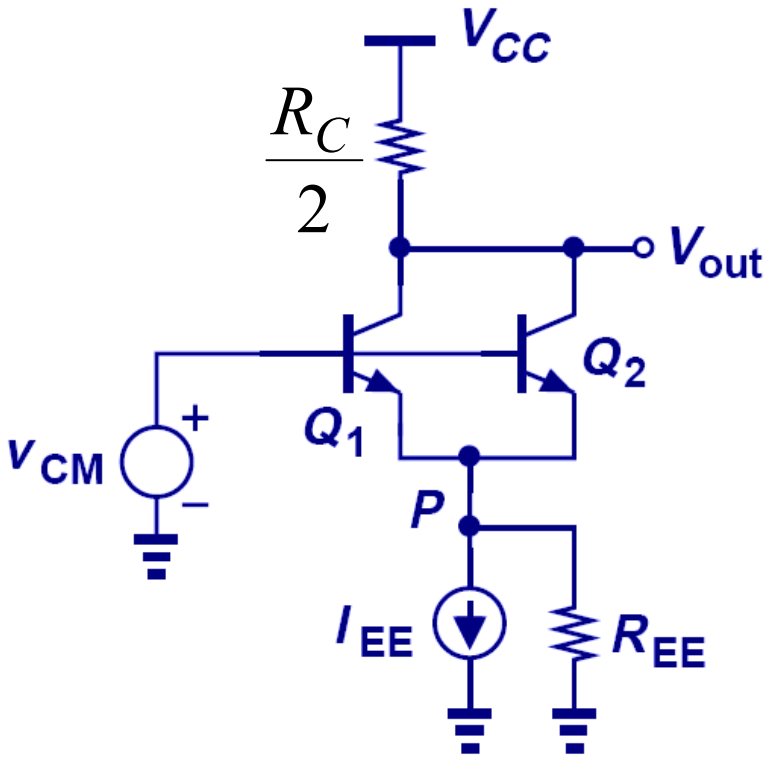
$$A_v \approx -g_{m1}\left[g_{m3}r_{o3}r_{o1}\|g_{m5}\left(r_{o5}\|R_1\right)r_{o7}\right]$$

# Agenda

- General considerations
- Bipolar differential pair
- MOS differential pair
- Cascode differential amplifiers
- Common-mode rejection
- Differential pair with active load

# Effect of Finite Tail Impedance



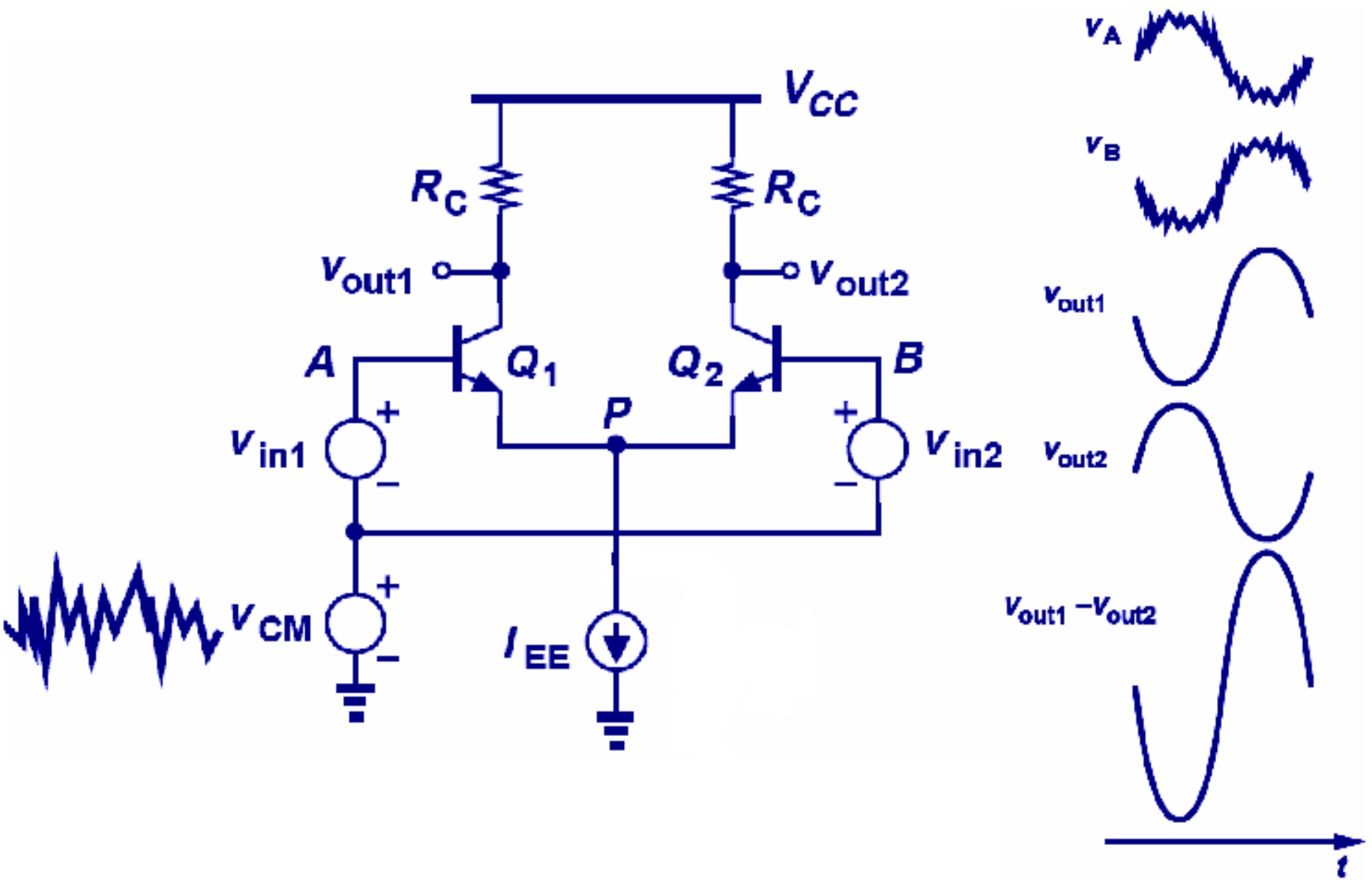




Assuming $\alpha$=1

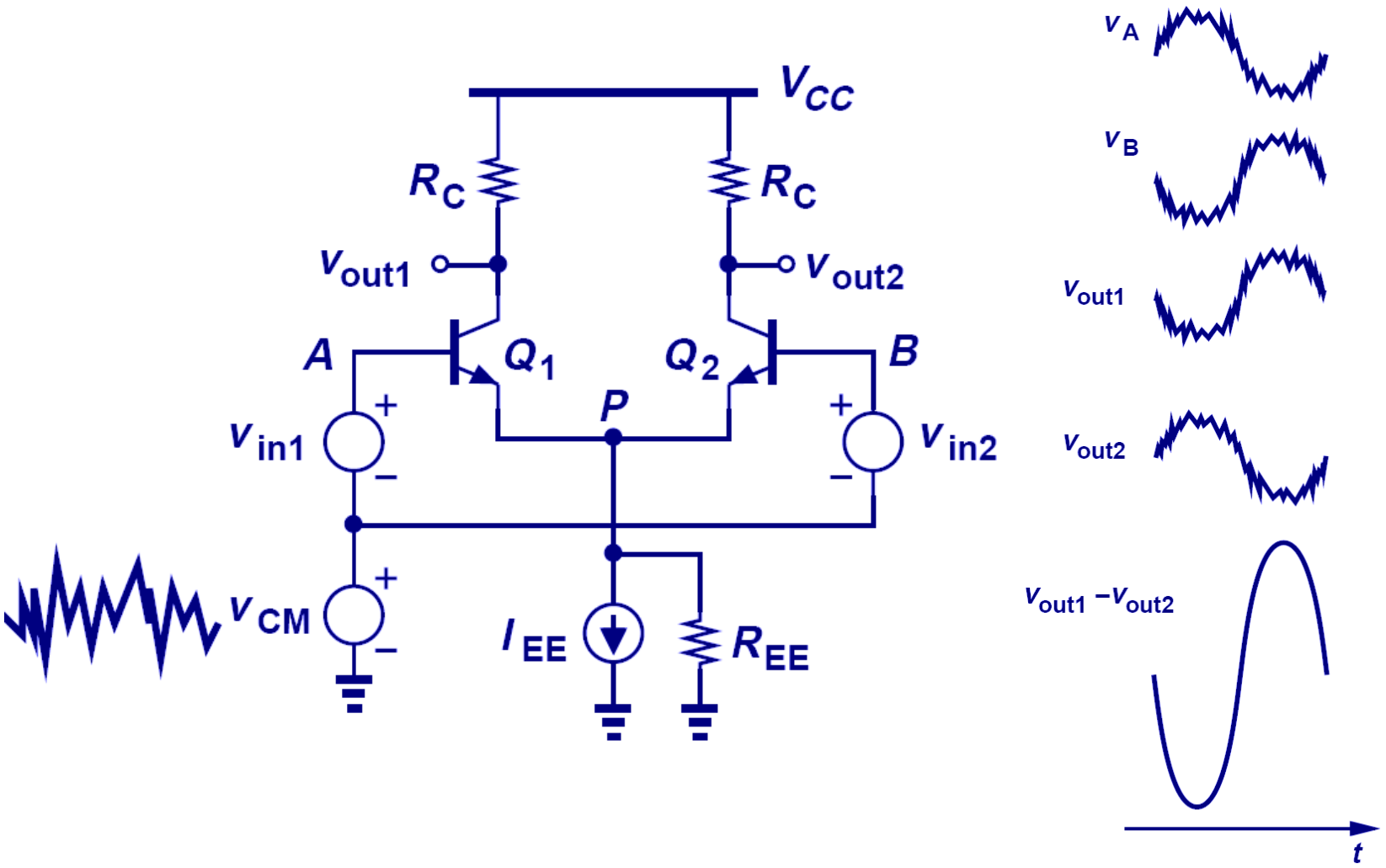
$$\frac{\Delta V_{out,CM}}{\Delta V_{in,CM}} = -\frac{R_C/2}{R_{EE}+1/2g_m}$$

- **If the tail current source is not ideal, then when a input CM voltage is applied, the currents in $Q_1$ and $Q_2$ and hence output CM voltage will change.**

# Input CM Noise with Ideal Tail Current

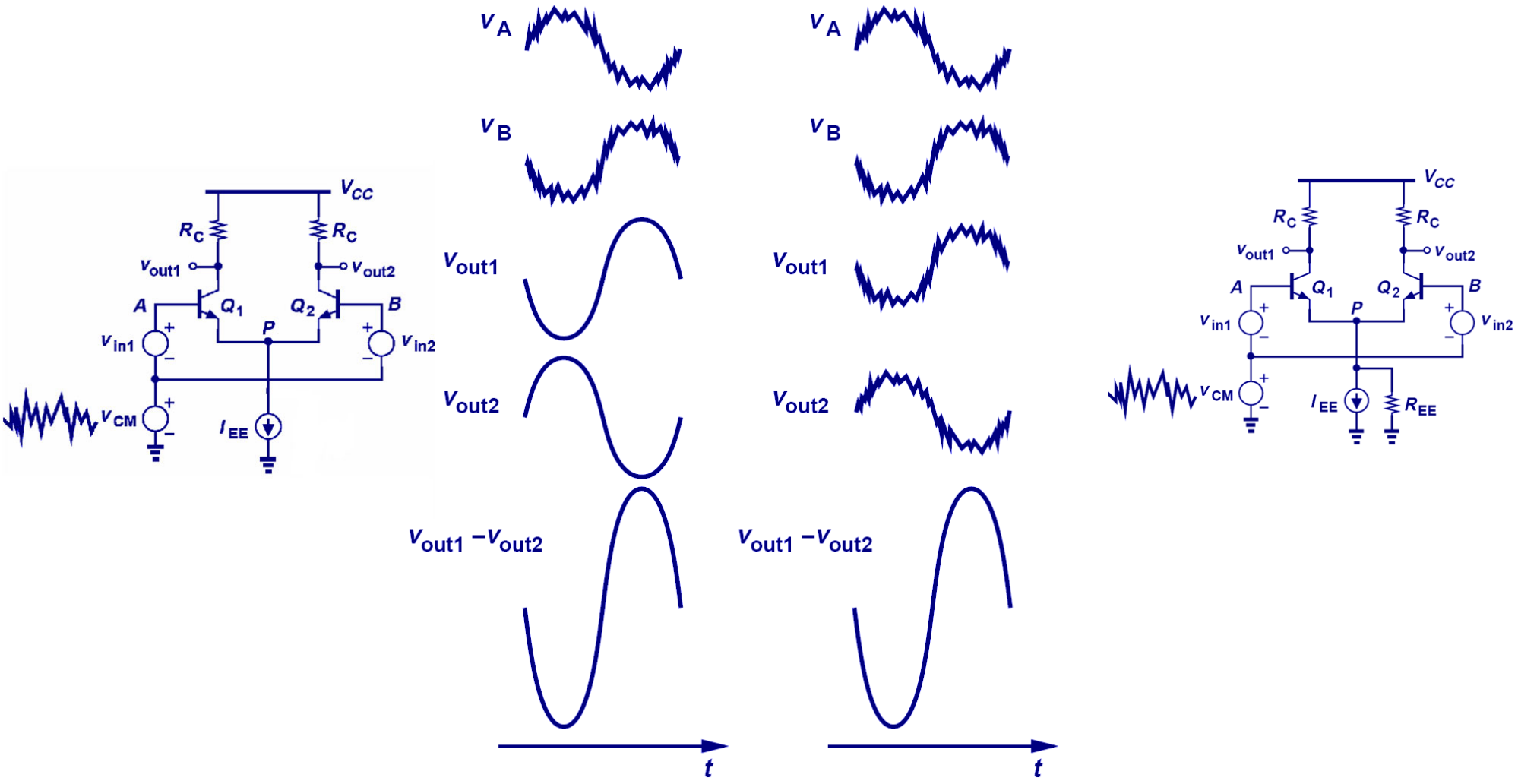


# Input CM Noise with Non-ideal Tail Current



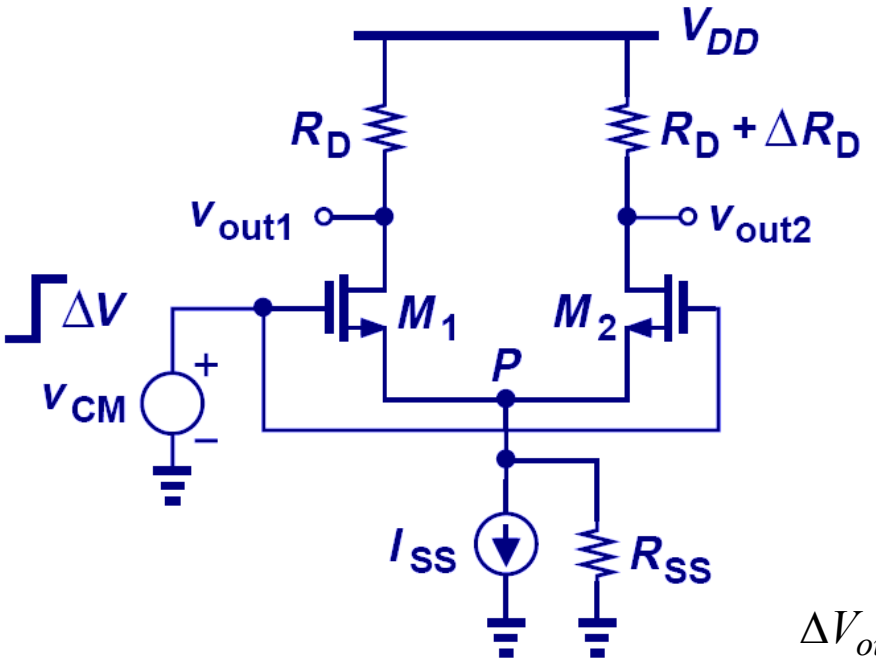

- Common-mode noise is now transferred to the single-ended outputs
- However, output differential signal is still ideally unaffected by common-mode noise

# Comparison




- **As it can be seen, the differential output voltages for both cases are the same. So for small input CM noise, the differential pair is not affected.**

# CM to DM Conversion, $A_{CM\text{-}DM}$




Assuming high $r_o$ in the diff. pair transistors

$$\Delta I_{D1} = \Delta I_{D2} = \Delta I_D \quad \text{and} \quad \Delta V_{GS1} = \Delta V_{GS2} = \Delta V_{GS}$$

A net current of $2\Delta I_D$ will flow through $R_{SS}$

$$\Delta V_{CM} = \Delta V_{GS} + 2\Delta I_D R_{SS}$$

$$\Delta V_{CM} = \Delta I_D \left( \frac{1}{g_m} + 2R_{SS} \right)$$

$$\Delta I_D = \frac{\Delta V_{CM}}{\frac{1}{g_m} + 2R_{SS}}$$

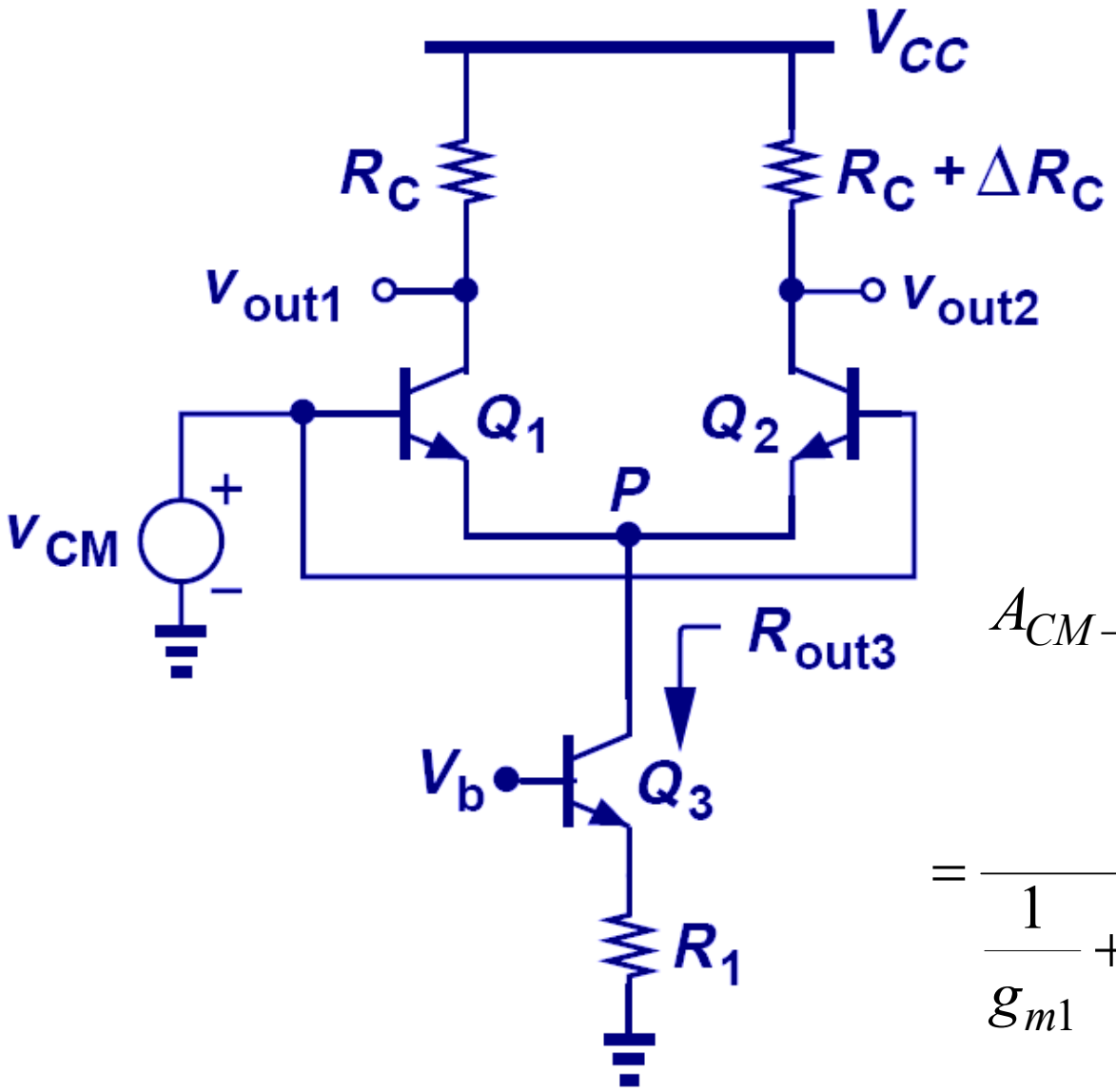
$$\Delta V_{out} = \Delta V_{out1} - \Delta V_{out2} = \Delta I_D R_D - \Delta I_D (R_D + \Delta R_D) = -\Delta I_D \Delta R_D$$

$$\Delta V_{out} = -\frac{\Delta V_{CM}}{\frac{1}{g_m} + 2R_{SS}} \Delta R_D$$

$$\left| \frac{\Delta V_{out}}{\Delta V_{CM}} \right| = \frac{\Delta R_D}{\frac{1}{g_m} + 2R_{SS}}$$

- **If finite tail impedance and asymmetry are both present, then the differential output signal will contain a portion of input common-mode signal.**

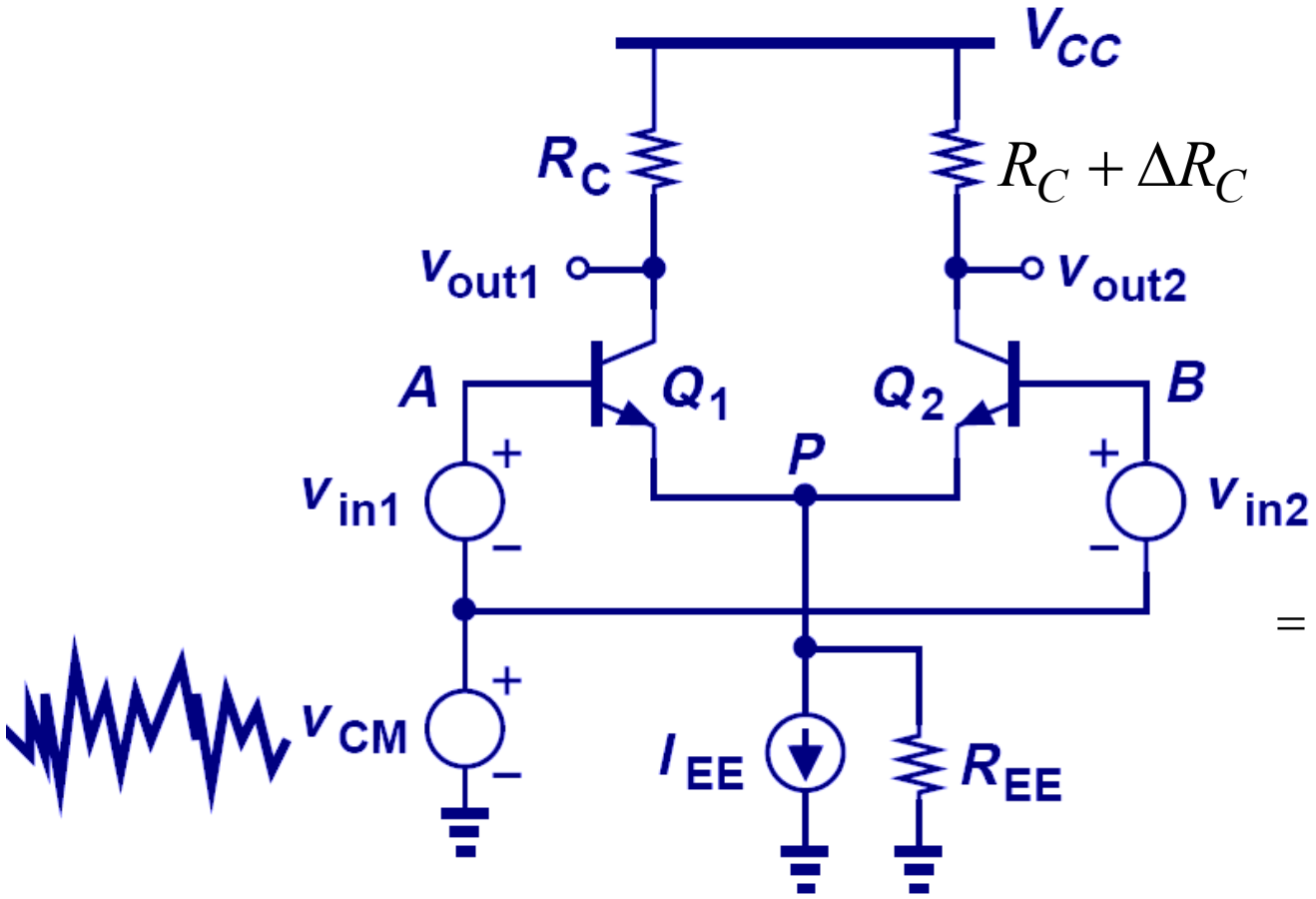
# Example: $A_{CM-DM}$




$$A_{CM-DM} = \left|\frac{\Delta V_{out}}{\Delta V_{CM}}\right| = \frac{\Delta R_C}{\dfrac{1}{g_{m1}} + 2R_{out3}}$$

$$= \frac{\Delta R_C}{\dfrac{1}{g_{m1}} + 2\left[r_{o3} + R_1 \| r_{\pi 3} + g_{m3} r_{o3}\left(R_1 \| r_{\pi 3}\right)\right]}$$

# CMRR




$$CMRR = \frac{A_{DM}}{A_{CM-DM}}$$

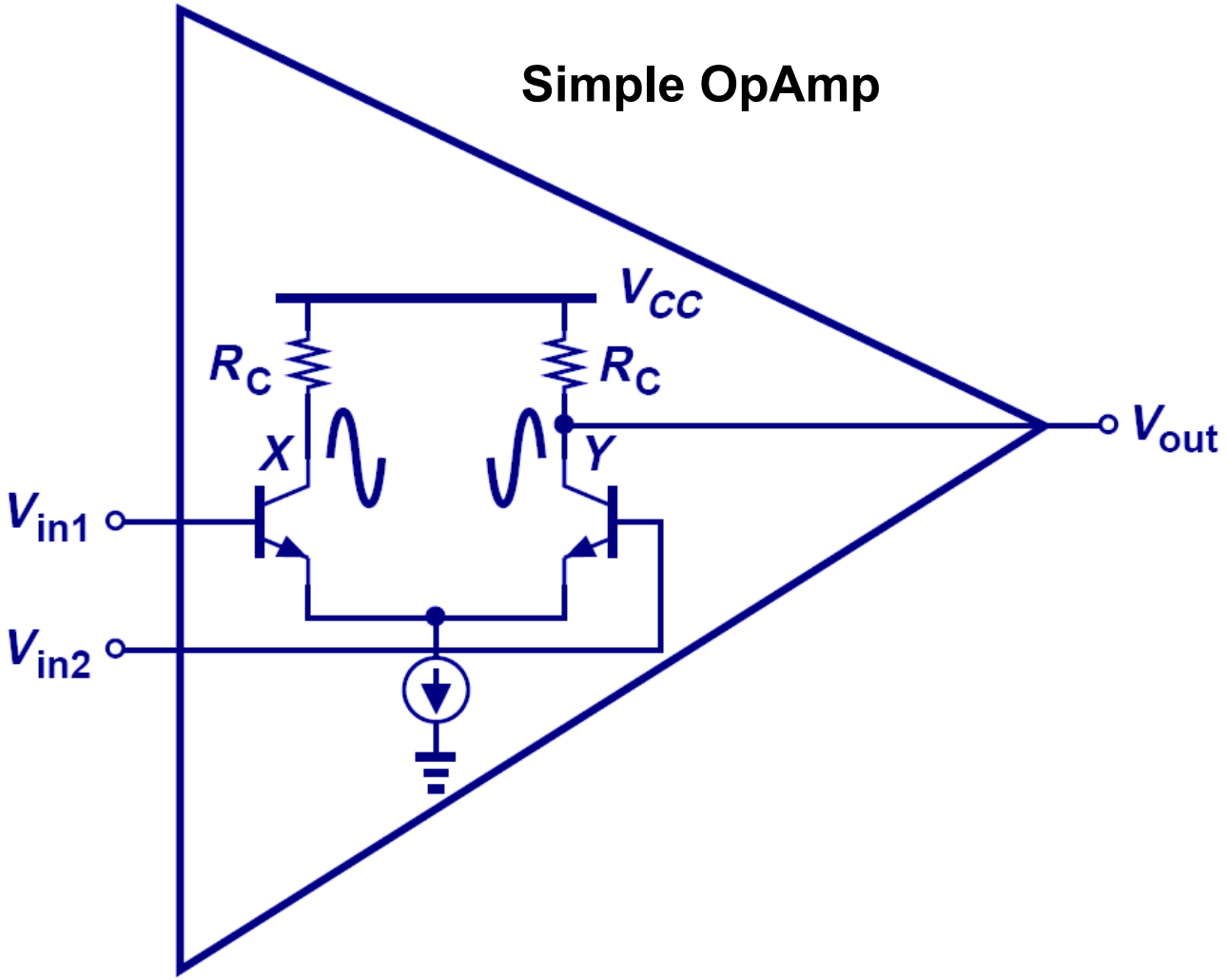
$$= \frac{g_m R_C}{\left(\frac{\Delta R_C}{\frac{1}{g_m} + 2R_{EE}}\right)} = \frac{R_C + 2g_m R_C R_{EE}}{\Delta R_C}$$

- **CMRR defines the ratio of wanted amplified differential input signal to unwanted converted input common-mode noise that appears at the output.**

# Agenda

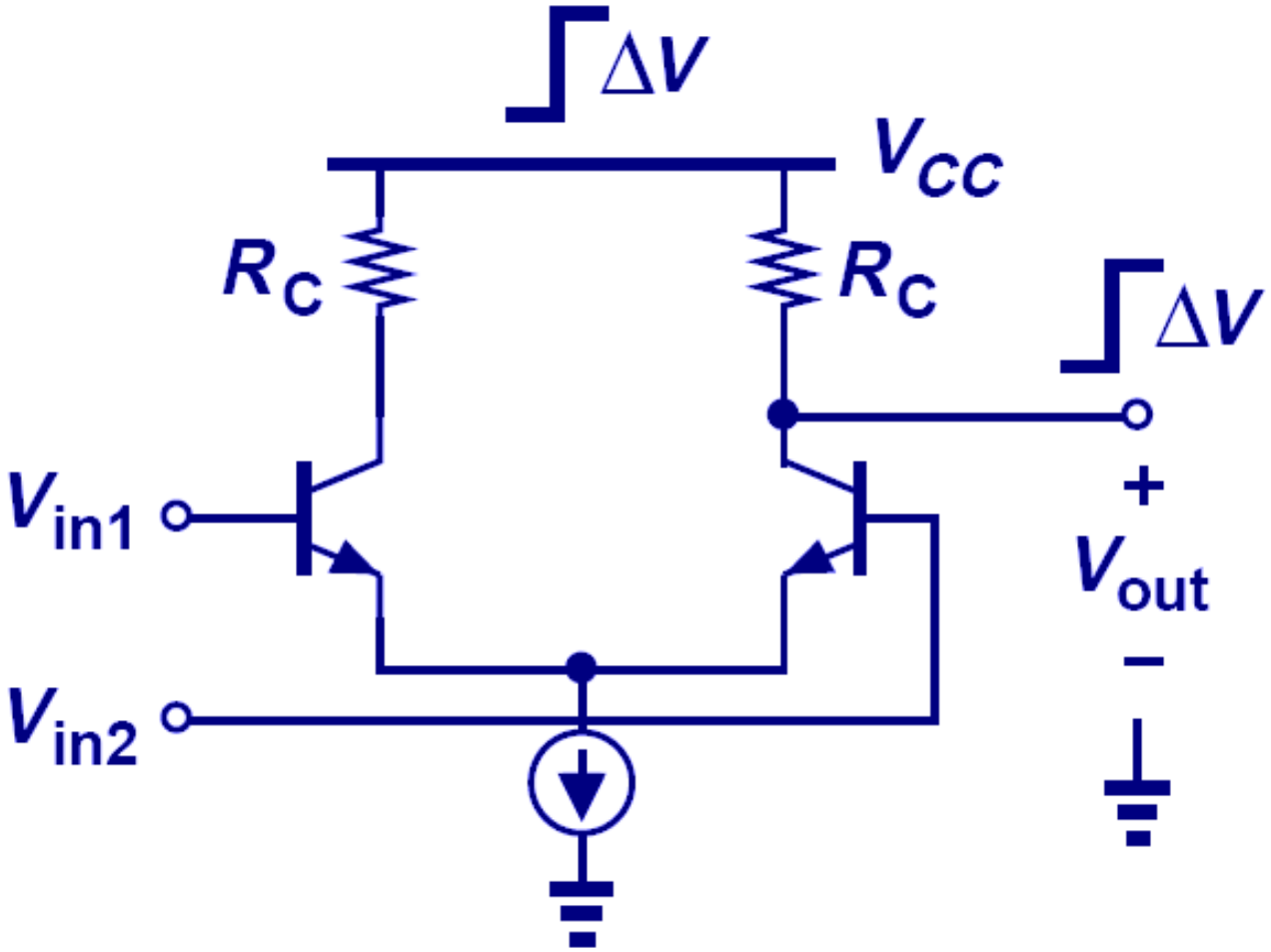
- General considerations
- Bipolar differential pair
- MOS differential pair
- Cascode differential amplifiers
- Common-mode rejection
- Differential pair with active load

# Differential to Single-ended Conversion



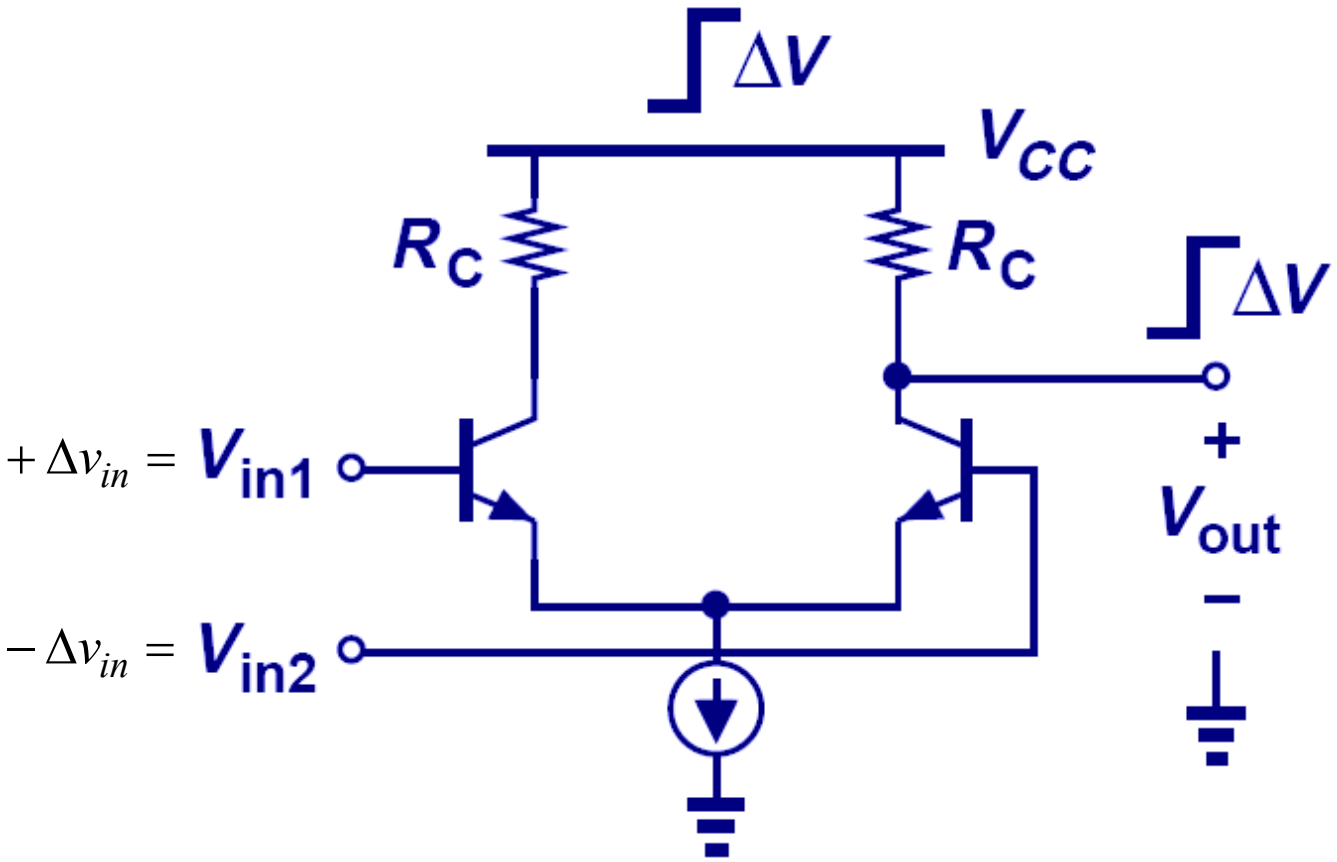

- **Many circuits require a differential to single-ended conversion, however, the above topology is not very good.**

# Supply Noise Corruption




- **The most critical drawback of this topology is supply noise corruption, since no common-mode cancellation mechanism exists. Also, we lose half of the signal.**

# Gain Reduction




$$v_{in1} = +\Delta v_{in}$$

$$v_{in2} = -\Delta v_{in}$$

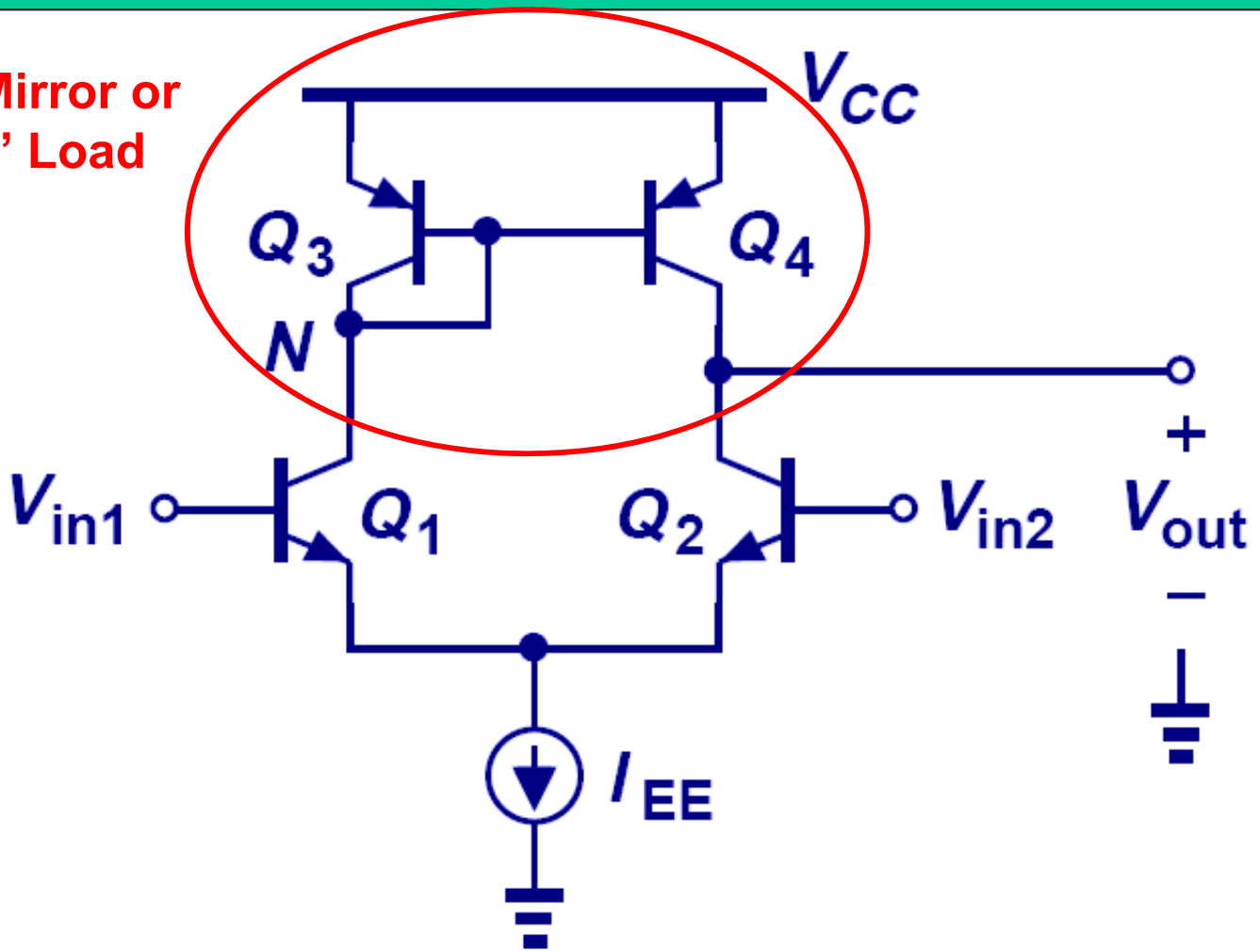
$$v_{out} = -g_m(-\Delta v_{in})R_C$$

$$\frac{v_{out}}{v_{in1} - v_{in2}} = \frac{g_m R_C \Delta v_{in}}{2\Delta v_{in}} = \frac{g_m R_C}{2}$$

- **The most critical drawback of this topology is supply noise corruption, since no common-mode cancellation mechanism exists. Also, we lose half of the signal.**

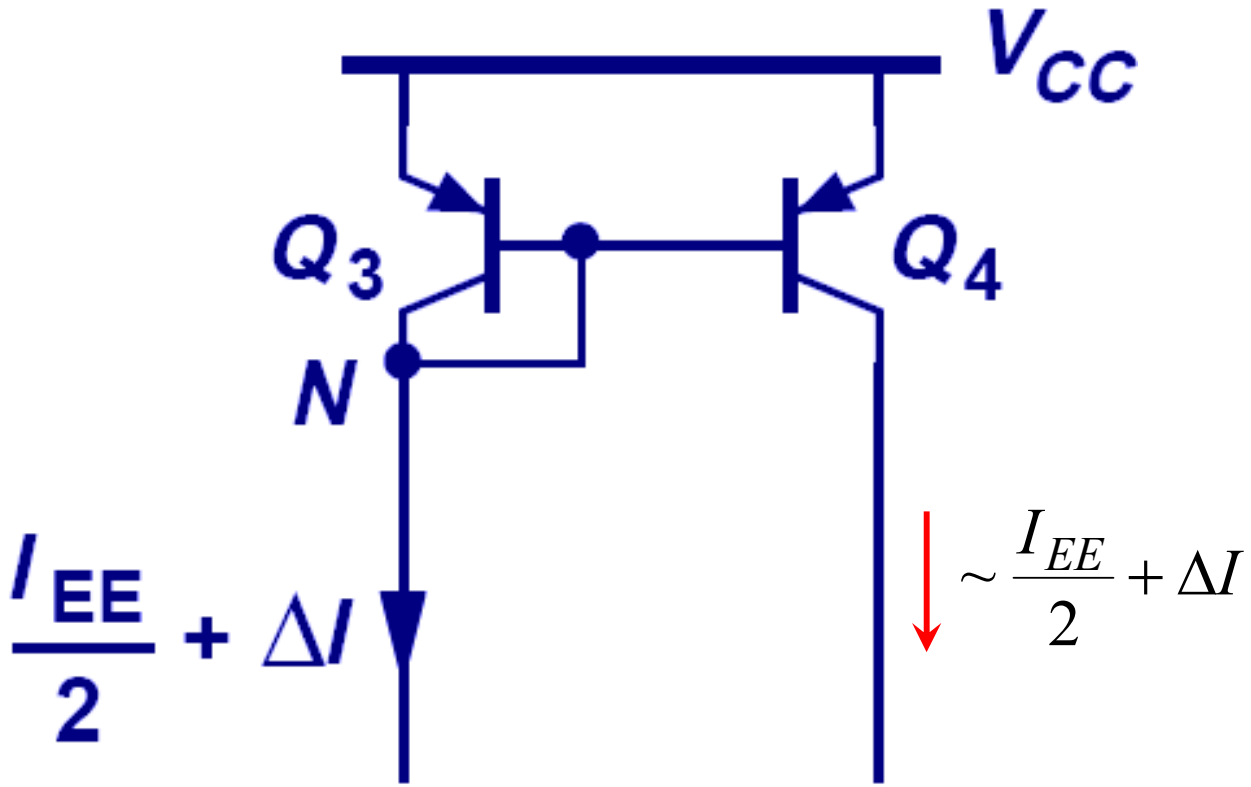
# Better Alternative

Current Mirror or "Active" Load



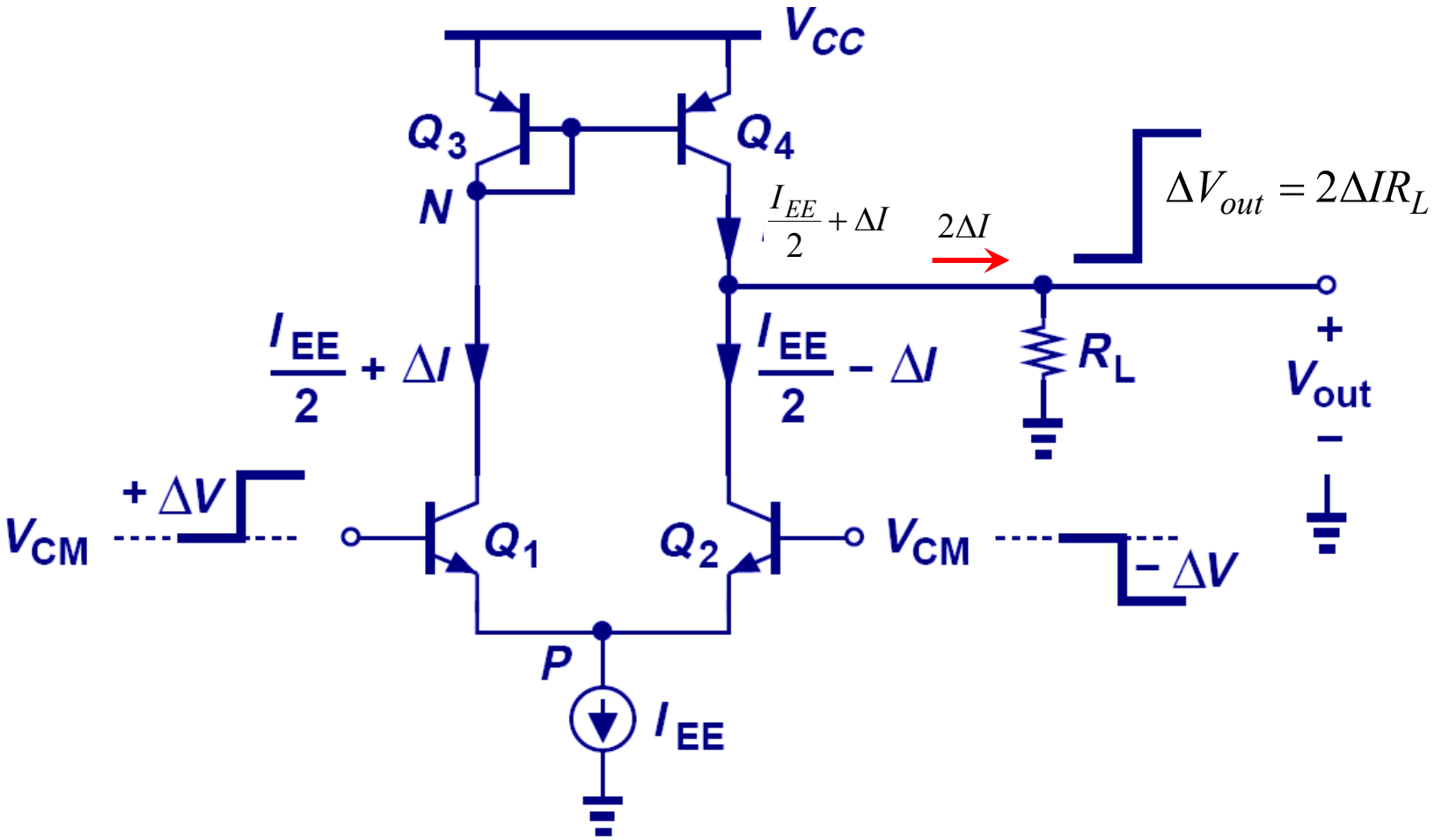

- This circuit topology performs differential to single-ended conversion with no loss of gain.

# Active Load



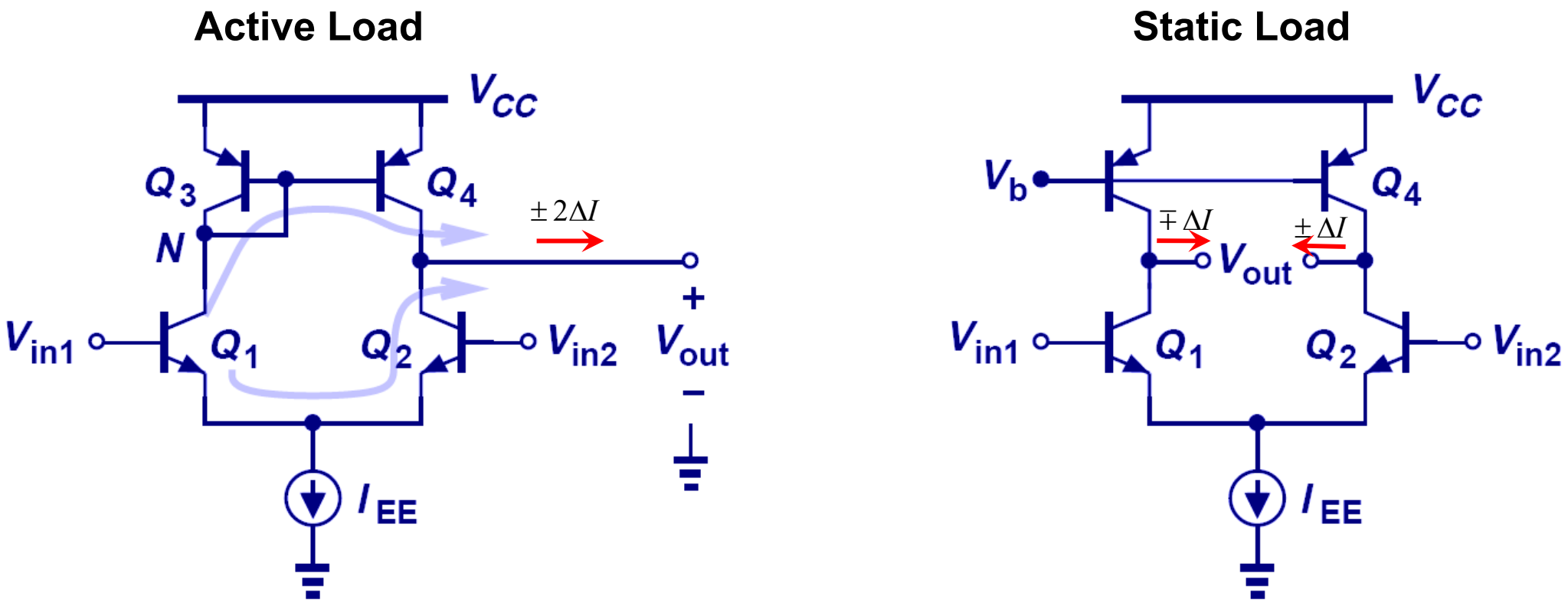

- With current mirror used as the load, the signal current produced by the $Q_1$ can be replicated onto $Q_4$.
- This type of load is different from the conventional "static load" and is known as an "active load".

# Differential Pair with Active Load



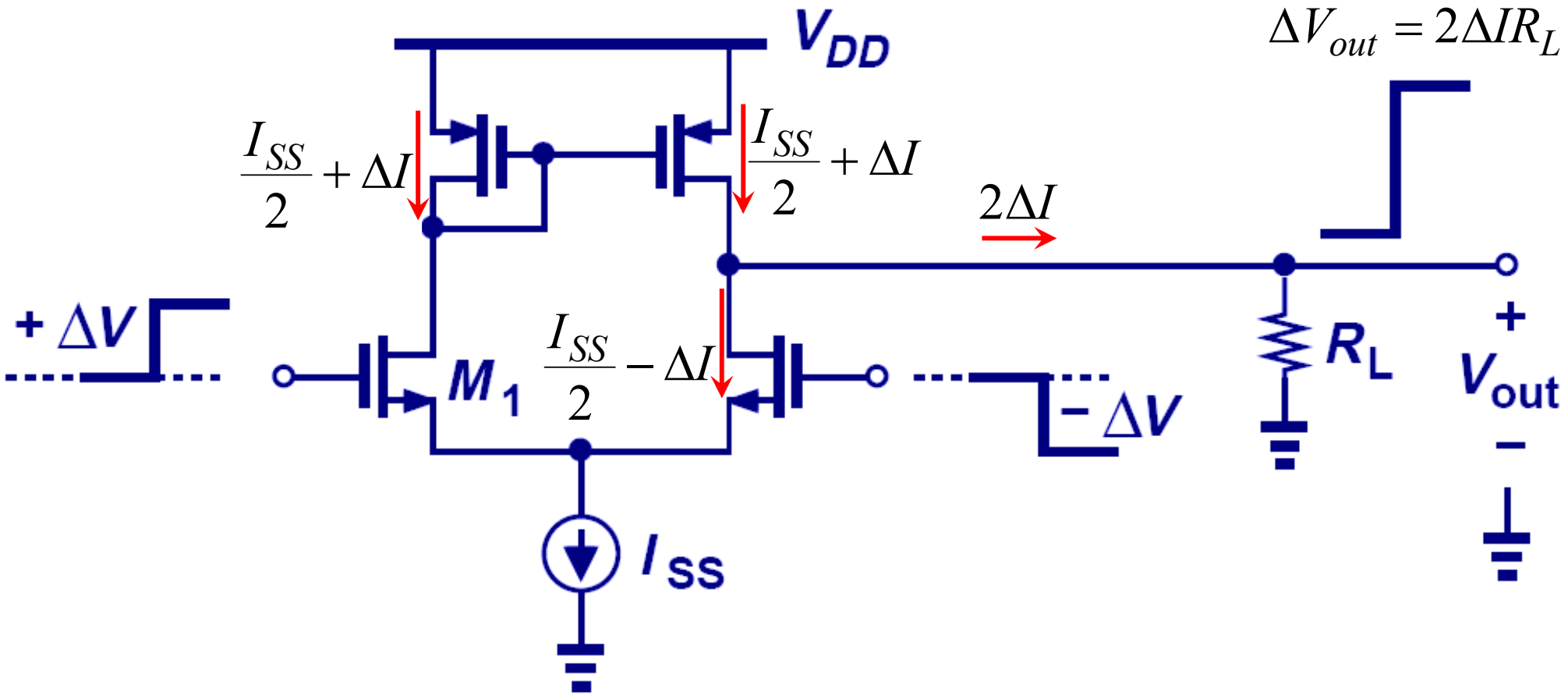

- **The input differential pair decreases the current drawn from $R_L$ by $\Delta I$ and the active load pushes an extra $\Delta I$ into $R_L$ by current mirror action; these effects enhance each other.**

# Active Load vs. Static Load



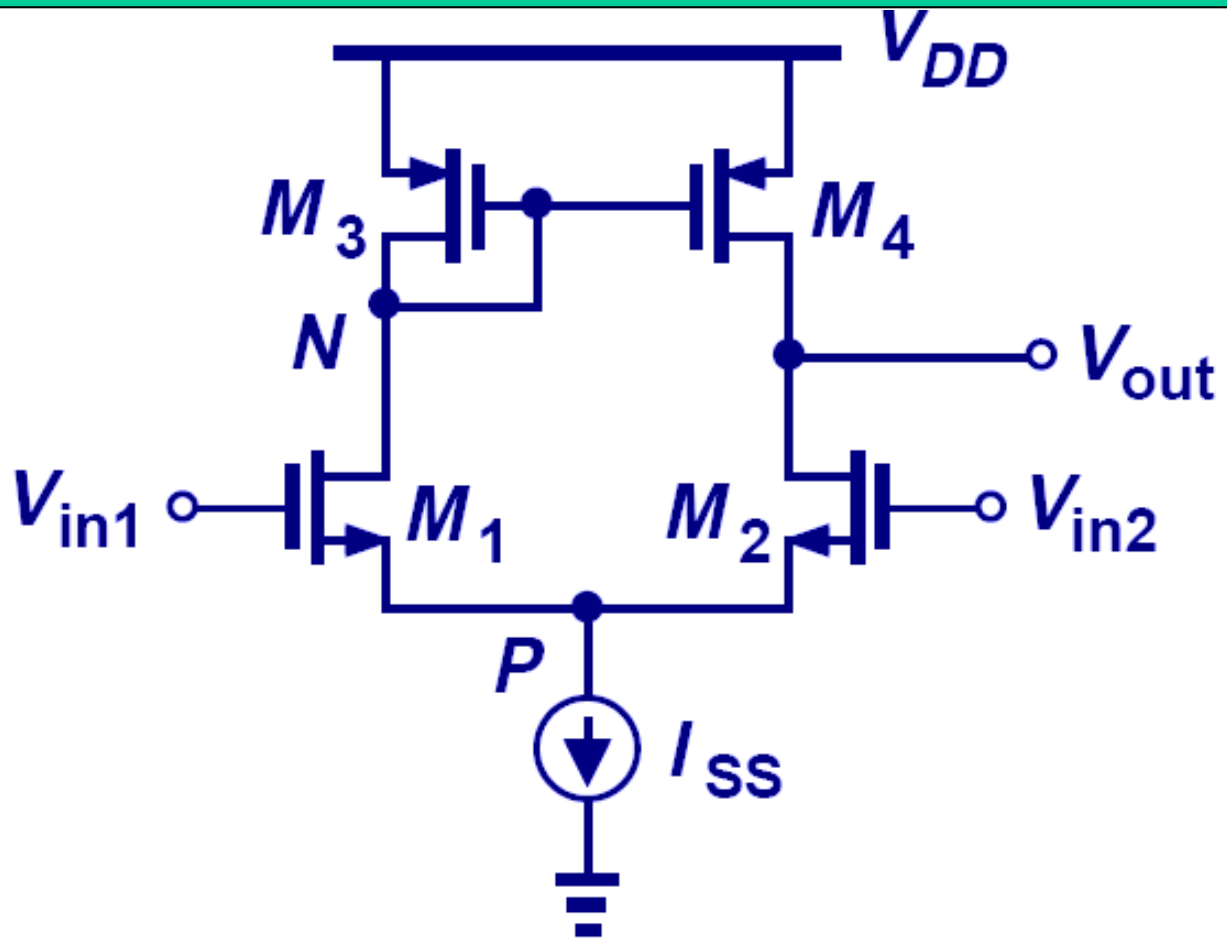

- **The load on the left responds to the input signal and enhances the single-ended output, whereas the load on the right does not.**

# MOS Differential Pair with Active Load



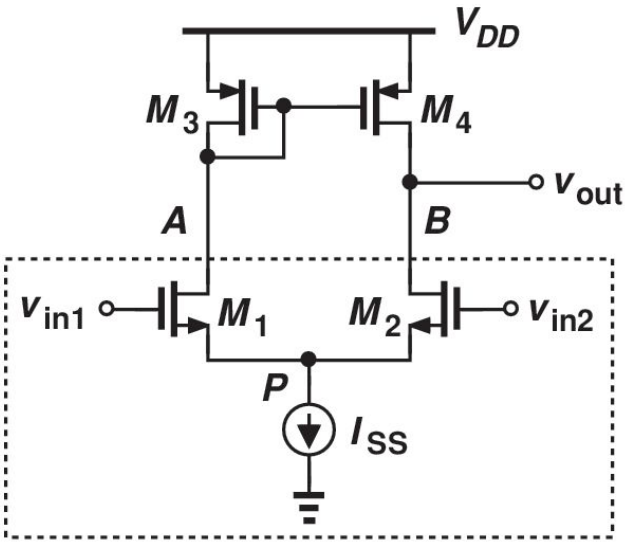

- **Similar to its bipolar counterpart, MOS differential pair can also use active load to enhance its single-ended output.**

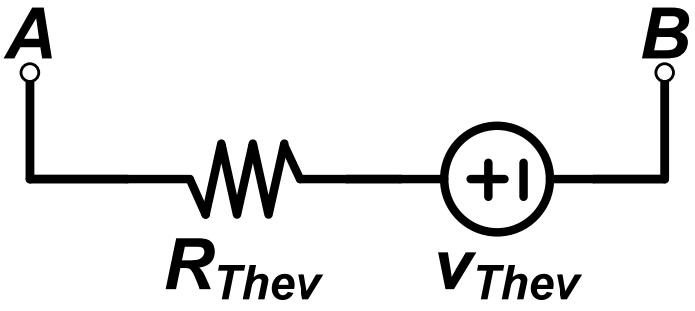
# Asymmetric Differential Pair

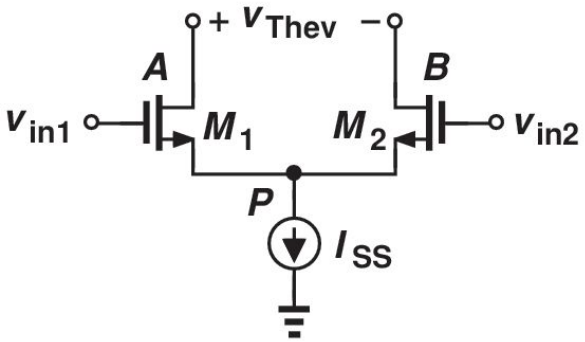



- **Because of the vastly different resistance magnitude at the drains of $M_1$ and $M_2$, the voltage swings at these two nodes are different and therefore node P cannot be viewed as a virtual ground.**

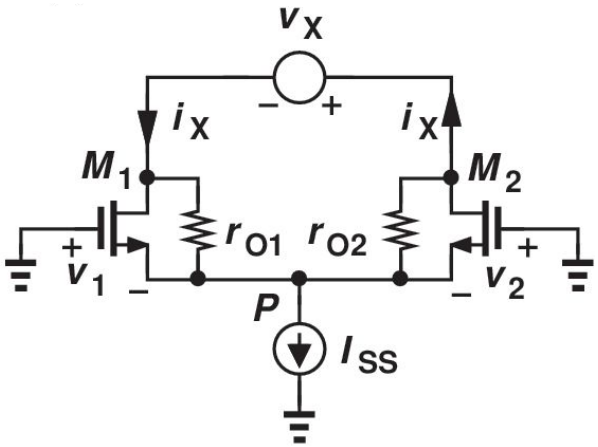
# Thevenin Equivalent of the Input Pair



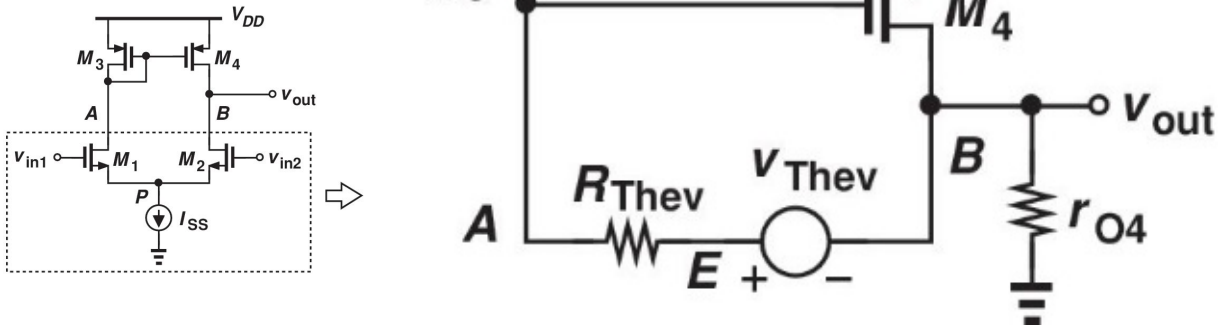

To Find $R_{Thev}$




$$v_{Thev} = -g_{mN} r_{oN} (v_{in1} - v_{in2})$$

$$R_{Thev} = 2r_{oN}$$

# Simplified Differential Pair with Active Load




$v_A$ can be viewed as a divided version of $v_E$

$$v_A = \frac{\dfrac{1}{g_{m3}} \Big\| r_{o3}}{\dfrac{1}{g_{m3}} \Big\| r_{o3} + R_{Thev}} (v_{out} + v_{Thev})$$

Writing a KCL at the output node

$$g_{m4} v_A + \frac{v_{out}}{r_{o4}} + \frac{v_{out} + v_{Thev}}{\dfrac{1}{g_{m3}} \Big\| r_{o3} + R_{Thev}} = 0$$

$$\left( g_{m4} \frac{\dfrac{1}{g_{m3}} \Big\| r_{o3}}{\dfrac{1}{g_{m3}} \Big\| r_{o3} + R_{Thev}} + \frac{1}{\dfrac{1}{g_{m3}} \Big\| r_{o3} + R_{Thev}} \right) (v_{out} + v_{Thev}) + \frac{v_{out}}{r_{o4}} = 0$$

since $1/g_{m3} << r_{o3}$ and $1/g_{m3} << R_{Thev}$ and $g_{m3} = g_{m4} = g_{mP}$ and $r_{o3} = r_{o4} = r_{oP}$

$$\frac{2}{R_{Thev}} (v_{out} + v_{Thev}) + \frac{v_{out}}{r_{oP}} = 0$$

$$\frac{v_{out}}{v_{in1} - v_{in2}} = g_{mN} (r_{oN} \| r_{oP})$$

$$\boxed{\frac{v_{out}}{v_{in1} - v_{in2}} = g_{mN} (r_{ON} \| r_{OP})}$$

# Next Time

- Cascode Stages & Current Mirrors
  - Razavi Chapter 9