ECEN326: Electronic Circuits
Fall 2015

Lecture 4: Cascode Stages and Current Mirrors

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Announcements

• HW3 due 10/7

• Exam 1 10/12
  • 9:10-10:10 (10 extra minutes)
  • Closed book w/ one standard note sheet
  • 8.5”x11” front & back
  • Bring your calculator
  • Covers through half of Lecture 4 (cascode material)
  • Sample Exam1 posted on website

• Reading
  • Razavi Chapter 9
Agenda

• Differential Amplifier (Lab 4) Simulation Tips

• Cascode Stages

• Current Mirrors
Simulating Differential Amplifiers

- To simulate differential amplifiers, I like to use voltage-controlled voltage sources (VCVS or “E” elements) to generate the differential input signal and combine the differential output into a single-ended signal.

Note: This example doesn’t meet the Lab 4 gain spec.

Single-ended input source

DC voltage source to set input DC level

2 VCVS to generate differential or common-mode inputs
VCVS or E Elements

Out_p – Out_n = Gain*(In_p – In_n)
Simulating Differential Gain

- Set Inputs E1 Gain=0.5 and E2 Gain=-0.5, Output E3 Gain=1
- With input source AC=1, simply plot the output of E3 (Vo) to get the differential AC gain
Simulating Differential Gain

- $A_{dm} = 30.7 \text{ V/V} = 29.7 \text{dB}$
Simulating Differential $R_{\text{ind}}$

- The differential input resistance is equivalent to the differential input ($V_i$) divided by the input current, where $I$ use the base current of Q1 or $I_B(Q1)$
- $R_{\text{ind}} = 25.5\,k\Omega$
Simulating THD

- Set input source to Differential Output Amplitude/A_{dm}
  - For Lab 4, that is 5V/A_{dm}
  - In this example I set the differential input VAMPL = 5V/30.7 = 163mV

Note that the even-order harmonics (HD2, HD4, ...) are very small (ideally zero)

A nice property of ideal differential amplifiers is that they reject even-order harmonics
Simulating Common-Mode Gain

- Set Inputs E1 Gain=1 and E2 Gain=1, Output E3 Gain=1
- With input source AC=1, plot one of the single-ended outputs (Vo1 or Vo2) to get the common-mode gain
Simulating Common-Mode Gain

- $A_{cm} = -57.5\text{dB at 1kHz}$
CMRR Definitions

- CMRR is the ratio of the differential-mode gain ($A_{DM}$) over the common-mode to differential conversion gain ($A_{CM-DM}$)

\[
CMRR = \frac{A_{DM}}{A_{CM-DM}}
\]

- However, this can be hard to simulate without introducing variations in the circuit, as $A_{CM-DM}$ will be zero without variations.

- Thus, the lab uses an alternative CMRR definition which is the ratio of the differential-mode gain ($A_{DM}$) over the common-mode gain ($A_{CM}$), which is also a useful figure of merit.

\[
CMRR_{lab} = \frac{A_{DM}}{A_{CM}}
\]

- Using the previous simulation data, the $CMRR_{lab}$ would be $29.7\text{dB} - (-57.5\text{db}) = 87.2\text{dB}$
Agenda

- Differential Amplifier (Lab 4) Simulation Tips
- Cascode Stages
- Current Mirrors
Boosted Output Impedances

\[ R_{out1} = [1 + g_m (R_E \parallel r_\pi)] r_O + R_E \parallel r_\pi \]
\[ R_{out2} = (1 + g_m R_S) r_O + R_S \]
Bipolar Cascode Stage

\[ R_{out} = \left[ 1 + g_m \left( r_{O2} \parallel r_{\pi 1} \right) \right] r_{O1} + r_{O2} \parallel r_{\pi 1} \]

\[ R_{out} \approx g_{m1} r_{O1} \left( r_{O2} \parallel r_{\pi 1} \right) \]
The maximum output impedance of a bipolar cascode is bounded by the ever-present $r_\pi$ between emitter and ground of $Q_1$. 

$$R_{out,\text{max}} \approx g_{m1} r_{O1} r_{\pi1}$$

$$R_{out,\text{max}} \approx \beta_1 r_{O1}$$
Example: Trying to double Output Impedance using $R_E$

Relative to a simple bottom Q2 cascode, let's try and double this by adding an additional $R_E$

$$R_{out} \approx g_{m1}r_{o1}(r_{o2}||r_{\pi1})$$

$$R_{outA} = r_{o2} + R_E || r_{\pi2} + g_{m2}r_{o2}(R_E || r_{\pi2}) \approx g_{m2}r_{o2}(R_E || r_{\pi2})$$

In order to roughly double $R_{out}$ we need

$$R_{outA} || r_{\pi1} = 2(r_{o2}||r_{\pi1})$$

After some algebra, we find that

$$R_{outA} = \frac{2r_{o2}r_{\pi1}}{r_{\pi1} - r_{o2}}$$

Typically $r_{\pi}$ is smaller than $r_O$, so in general it is impossible to double the output impedance by degenerating Q2 with a resistor.
PNP Cascode Stage

\[ R_{out} = \left[1 + g_m (r_{O2} \parallel r_{\pi1})\right] r_{O1} + r_{O2} \parallel r_{\pi1} \]

\[ R_{out} \approx g_{m1} r_{O1} \left( r_{O2} \parallel r_{\pi1} \right) \]
Another Interpretation of Bipolar Cascode

- Instead of treating cascode as Q₂ degenerating Q₁, we can also think of it as Q₁ stacking on top of Q₂ (current source) to boost Q₂’s output impedance.

\[ R_{\text{out}} \approx g_m \frac{r_0}{1} \left( r_{o2} \parallel r_{\pi1} \right) \]
False Cascodes

When the emitter of $Q_1$ is connected to the emitter of $Q_2$, it’s no longer a cascode since $Q_2$ becomes a diode-connected device instead of a current source.

$$R_{out} = \left[ 1 + g_{m1} \left( \frac{1}{g_{m2}} \parallel r_{O2} \parallel r_{\pi2} \parallel r_{\pi1} \right) \right] r_{O1} + \frac{1}{g_{m2}} \parallel r_{O2} \parallel r_{\pi2} \parallel r_{\pi1}$$

$$R_{out} \approx \left( 1 + \frac{g_{m1}}{g_{m2}} \right) r_{O1} + \frac{1}{g_{m2}} \approx 2r_{O1}$$
MOS Cascode Stage

\[ R_{\text{out}} = (1 + g_{m1} r_{O2}) r_{O1} + r_{O2} \]

\[ R_{\text{out}} \approx g_{m1} r_{O1} r_{O2} \]
Another Interpretation of MOS Cascode

- Similar to its bipolar counterpart, MOS cascode can be thought of as stacking a transistor on top of a current source.
- Unlike bipolar cascode, the output impedance is not limited by $\beta$. 

$R_{out} \approx g_{m1} r_{o1} r_{o2}$
PMOS Cascode Stage

\[ R_{out} = \left(1 + g_{m1}r_{O2}\right)r_{O1} + r_{O2} \]

\[ R_{out} \approx g_{m1}r_{O1}r_{O2} \]
Example: Parasitic Resistance

\[ R_{out} = (1 + g_m r_{O2})(r_{O1} \parallel R_P) + r_{O2} \]

- \( R_P \) will lower the output impedance, since its parallel combination with \( r_{O1} \) will always be lower than \( r_{O1} \).
The short-circuit transconductance of a circuit measures its strength in converting input voltage to output current.

Note, in Lecture 2 we defined $G_m$ with $i_{out}$ flowing out of the circuit.

- Either convention is OK, as long as the appropriate $A_v$ expression is used.
Transconductance Example

\[ G_m = g_{m1} \]
Derivation of Voltage Gain

By representing a linear circuit with its Norton equivalent, the relationship between $V_{out}$ and $V_{in}$ can be expressed by the product of $G_m$ and $R_{out}$.

$$v_{out} = -i_{out}R_{out} = -G_m v_{in} R_{out}$$

$$v_{out} / v_{in} = -G_m R_{out}$$

Note: If you define $G_m$ with $i_{sc}$ flowing outward, then $A_v = G_m R_{out}$.
Example: Voltage Gain

\[ A_v = -g_{m1}r_{O1} \]
Since the output impedance of bipolar cascode is higher than that of the CE stage, we would expect its voltage gain to be higher as well.
Voltage Gain of Bipolar Cascode Amplifier

Since $r_O$ is much larger than $1/g_m$, most of $I_{C,Q1}$ flows into the diode-connected $Q_2$. Using $R_{out}$ as before, $A_v$ is easily calculated.

\[
G_m \approx g_{m1}
\]

\[
A_v \approx -g_{m1}r_{O2}g_{m2}(r_{O1} \parallel r_{\pi2})
\]
Practical Cascode Stage

Since no current source can be ideal, the output impedance drops.

\[ R_{out} \approx r_{O3} \parallel g_{m2} r_{O2} \left( r_{O1} \parallel r_{\pi2} \right) \]
In order to preserve the high output impedance, a cascode PNP current source is used.

\[ R_{out} \approx g_m r_o (r_o \parallel r_{\pi}) \parallel g_m r_{o2} (r_o \parallel r_{\pi}) \]
MOS Cascode Amplifier

\[ A_v = -G_m R_{out} \]
\[ A_v \approx -g_{m1} \left[ (1 + g_{m2}r_{O2})r_{O1} + r_{O2} \right] \]
\[ A_v \approx -g_{m1}g_{m2}r_{O2}r_{O1} \]
Improved MOS Cascode Amplifier

Similar to its bipolar counterpart, the output impedance of a MOS cascode amplifier can be improved by using a PMOS cascode current source.

\[ R_{on} \approx g_{m2}r_{O2}r_{O1} \]
\[ R_{op} \approx g_{m3}r_{O3}r_{O4} \]
\[ R_{out} = R_{on} \parallel R_{op} \]
Agenda

• Differential Amplifier (Lab 4) Simulation Tips

• Cascode Stages

• Current Mirrors
Since $V_T$, $I_S$, $\mu_n$, and $V_{TH}$ all depend on temperature, $I_1$ for both bipolar and MOS depends on temperature and supply.
The motivation behind a current mirror is to sense the current from a “golden current source” and duplicate this “golden current” to other locations.
Neglecting base current for now (assuming high $\beta$), from the $I_C$ expression

$$I_C = I_S \left( e^{\frac{V_{BE}}{V_T}} - 1 \right) \approx I_S e^{\frac{V_{BE}}{V_T}}$$

the voltage produced by the diode connected transistor is

$$V_1 = V_T \ln \left( \frac{I_{REF}}{I_{S,REF}} \right)$$

this voltage forms the $V_{BE}$ of the output current source to produce

$$I_{copy} = I_S 1 e^{\frac{V_T}{V_T}} = \frac{I_{S1}}{I_{S,REF}} I_{REF}$$

- The diode-connected $Q_{REF}$ produces an output voltage $V_1$ that forces $I_{copy1} = I_{REF}$, if $Q_1 = Q_{REF}$. 

CH 9 Cascode Stages and Current Mirrors
Multiple copies of $I_{REF}$ can be generated at different locations by simply applying the idea of current mirror to more transistors.

Neglecting $I_B$

\[ I_{copy,j} = \frac{I_{S,j}}{I_{S,REF}} I_{REF} \]
By scaling the emitter area of $Q_j$ $n$ times with respect to $Q_{REF}$, $I_{copy,j}$ is also $n$ times larger than $I_{REF}$. This is equivalent to placing $n$ unit-size transistors in parallel.

Neglecting $I_B$, $I_{copy,j} = nI_{REF}$
Example: Scaled Current

Neglecting $I_B$
Fractional Scaling

A fraction of $I_{REF}$ can be created on $Q_1$ by scaling up the emitter area of $Q_{REF}$.

Neglecting $I_B$

$$I_{copy} = \frac{1}{3} I_{REF}$$

A fraction of $I_{REF}$ can be created on $Q_1$ by scaling up the emitter area of $Q_{REF}$. 
Example: Different Mirroring Ratio

Using the idea of current scaling and fractional scaling, $I_{\text{copy2}}$ is $0.5\,\text{mA}$ and $I_{\text{copy1}}$ is $0.05\,\text{mA}$ respectively. All coming from a source of $0.2\,\text{mA}$. Neglecting $I_B$.
Mirroring Error Due to Base Currents

\[ I_{B1} = \frac{I_{\text{copy}}}{\beta} \]

\[ I_{B,\text{REF}} = \frac{I_{\text{copy}}}{n\beta} \]

From a KCL at the base/collector of \( Q_{\text{REF}} \)

\[ I_{\text{REF}} = \frac{I_{\text{copy}}}{n} + \frac{I_{\text{copy}}}{n\beta} + \frac{I_{\text{copy}}}{\beta} \]

\[ I_{\text{copy}} = \frac{nI_{\text{REF}}}{1 + \frac{1}{\beta}(n+1)} \]
Improved Mirroring Accuracy

From a KCL at the base of $Q_1$ and $Q_{REF}$

$$I_{E,F} \approx I_{C,F} = \frac{I_{copy}}{\beta} \left(1 + \frac{1}{n}\right)$$

$$I_{B,F} = \frac{I_{copy}}{\beta^2} \left(1 + \frac{1}{n}\right)$$

From a KCL at the collector of $Q_{REF}$

$$I_{REF} = I_{B,F} + I_{C,REF} = \frac{I_{copy}}{\beta^2} \left(1 + \frac{1}{n}\right) + \frac{I_{copy}}{n}$$

$$I_{copy} = \frac{nI_{REF}}{1 + \frac{1}{\beta^2(n+1)}}$$

Because of $Q_F$, the base currents of $Q_{REF}$ and $Q_1$ are mostly supplied by $Q_F$ rather than $I_{REF}$. Mirroring error is reduced $\beta$ times.

$Q_F$ is often called a “$\beta$ helper”
Example: Different Mirroring Ratio Accuracy

The key to finding the copied currents is to first compute the total current copied using

\[
I_{\text{copy,total}} = \frac{n_{\text{total}}I_{\text{REF}}}{1 + \frac{1}{\beta^2}(n_{\text{total}} + 1)} = \frac{\left(\frac{11}{4}\right)I_{\text{REF}}}{1 + \frac{1}{\beta^2}\left(\frac{11}{4} + 1\right)} = \frac{11I_{\text{REF}}}{4 + \frac{15}{\beta^2}}
\]

Then scale the individual output currents

\[
I_{\text{copy1}} = \left(\frac{1}{11}\right)I_{\text{copy,total}} = \frac{I_{\text{REF}}}{4 + \frac{15}{\beta^2}}
\]

\[
I_{\text{copy2}} = \left(\frac{10}{11}\right)I_{\text{copy,total}} = \frac{10I_{\text{REF}}}{4 + \frac{15}{\beta^2}}
\]
PNP current mirror is used as a current source load to an NPN amplifier stage.

But what if we only have 1 ideal reference current that flows from $V_{CC}$, as in all the previous NPN current mirror examples?
Generation of $I_{REF}$ for PNP Current Mirror
Example: Current Mirror with Discrete Devices

- Let $Q_{\text{REF}}$ and $Q_1$ be discrete NPN devices. $I_{\text{REF}}$ and $I_{\text{copy1}}$ can vary in large magnitude due to $I_s$ mismatch.
- Thus, current mirrors may not be used that often in discrete (board-level) design, but are pervasive in integrated circuit (IC) design.
MOS Current Mirror

From the saturation current equation

\[ I_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS} - V_{TH,n})^2 \]

the voltage produced by the diode connected transistor is

\[ V_X = \sqrt{\frac{2I_{REF}}{\mu_n C_{ox} (\frac{W}{L})_{REF}}} + V_{TH,n} \]

this voltage forms the \( V_{GS} \) of the output current source to produce

\[ I_{copy} = \frac{\mu_n C_{ox}}{2} \left( \frac{W}{L} \right)_1 \left( \sqrt{\frac{2I_{REF}}{\mu_n C_{ox} (\frac{W}{L})_{REF}}} + V_{TH,n} - V_{TH,n} \right)^2 = \left( \frac{W}{L} \right)_1 I_{REF} \]

(c)

\[ I_{copy} = \frac{W}{L} \left( \frac{W}{L} \right)_{REF} I_{REF} \]
Example: Current Scaling

Similar to their bipolar counterpart, MOS current mirrors can also scale $I_{\text{REF}}$ up or down ($I_1 = 0.2\text{mA}$, $I_2 = 0.5\text{mA}$).
The idea of combining NMOS and PMOS to produce CMOS current mirror is shown above.
Next Time

- Frequency response
  - Razavi Chapter 11