ECEN326: Electronic Circuits
Spring 2022

Lecture 4: Cascode Stages and Current Mirrors

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Announcements

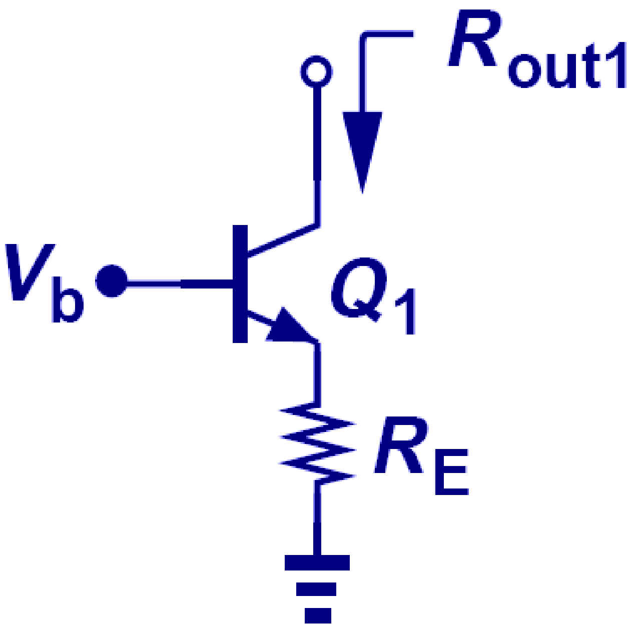
- HW4 due Mar 8

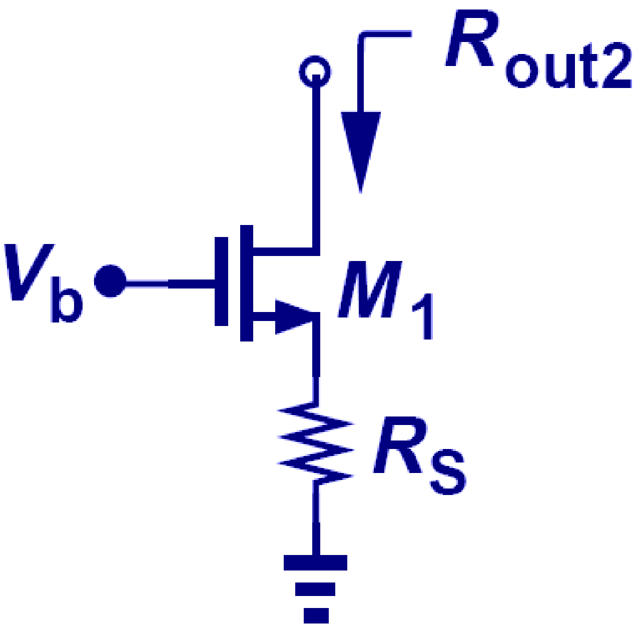
- Reading
    - Razavi Chapter 9

Agenda

- Cascode Stages
- Current Mirrors

Boosted Output Impedances

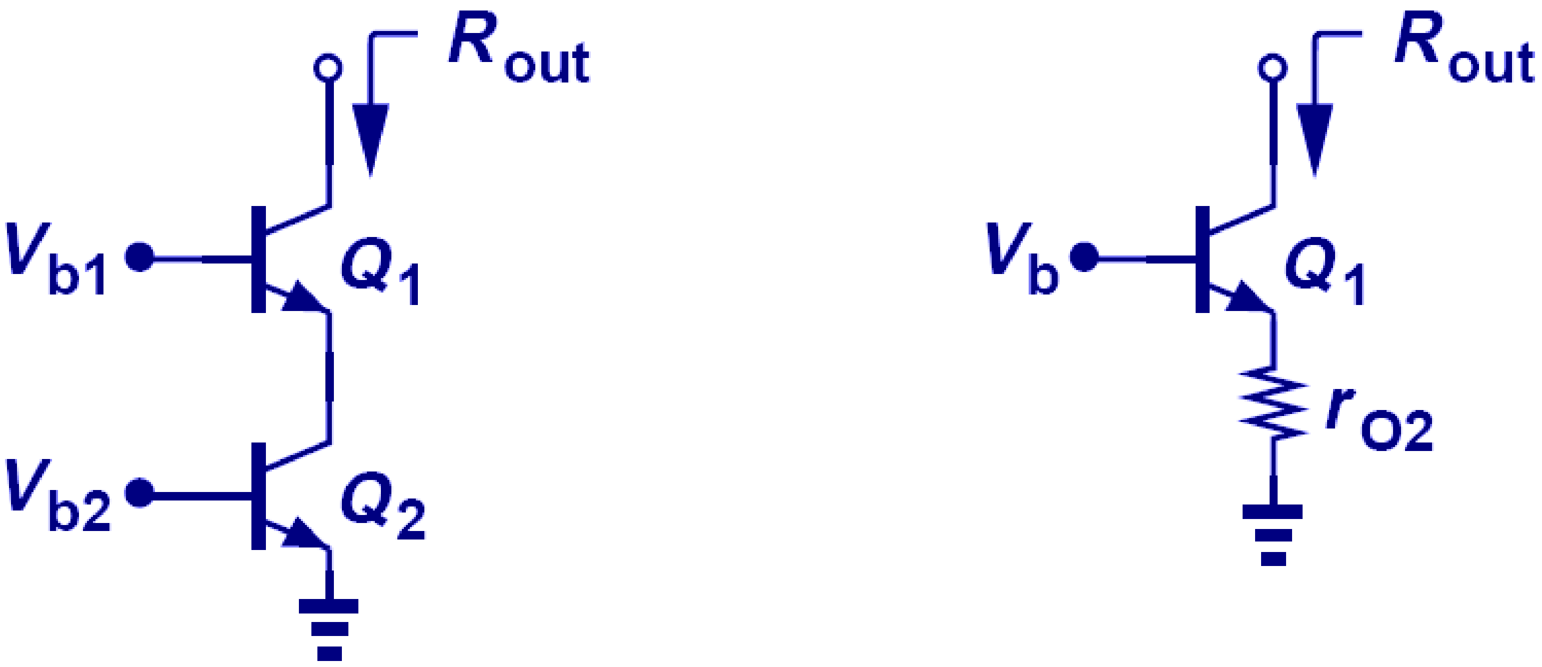




$$R_{out1} = \left[1 + g_m\left(R_E \parallel r_\pi\right)\right] r_O + R_E \parallel r_\pi$$

$$R_{out2} = \left(1 + g_m R_S\right) r_O + R_S$$

Bipolar Cascode Stage

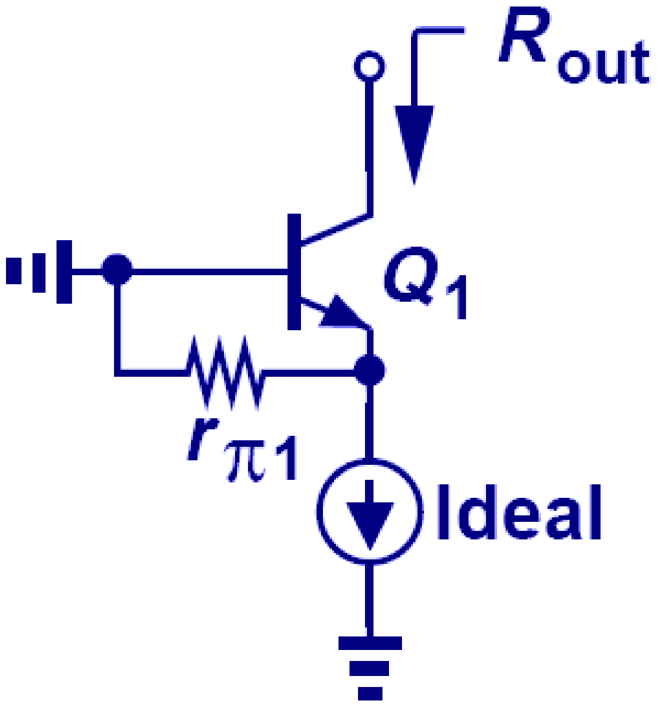


(a) (b)

$$R_{out} = [1 + g_m (r_{O2} \| r_{\pi 1})] r_{O1} + r_{O2} \| r_{\pi 1}$$

$$R_{out} \approx g_{m1} r_{O1} \left(r_{O2} \| r_{\pi 1} \right)$$

Maximum Bipolar Cascode Output Impedance



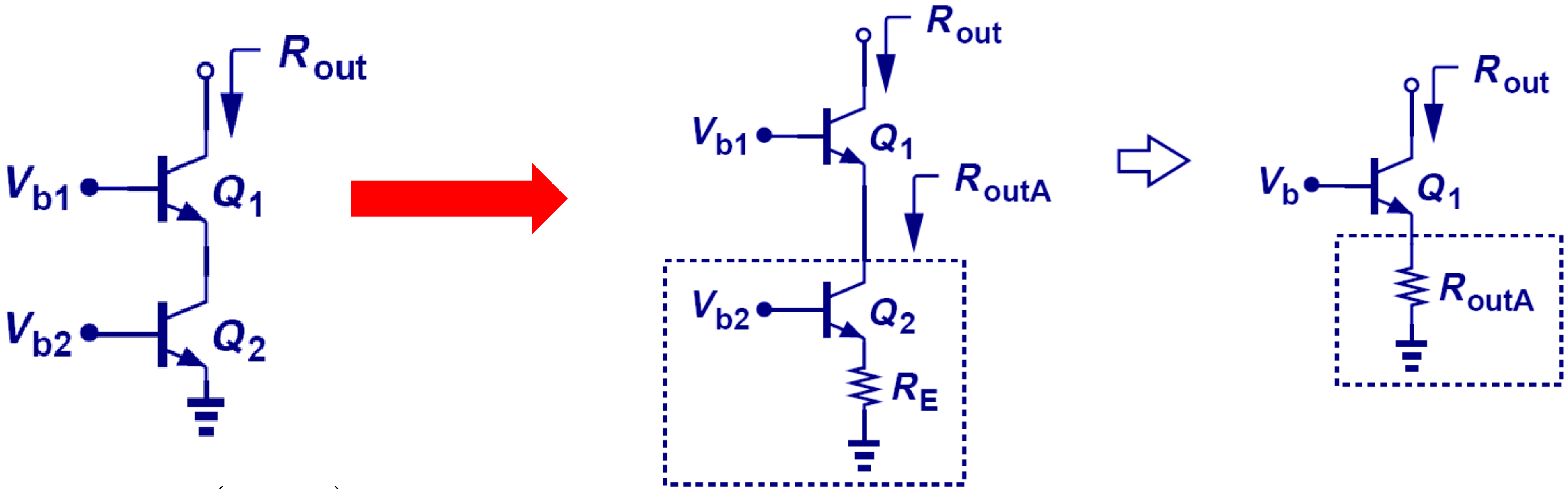
$$R_{out,\max} \approx g_{m1} r_{O1} r_{\pi 1}$$

$$R_{out,\max} \approx \beta_1 r_{O1}$$

- **The maximum output impedance of a bipolar cascode is bounded by the ever-present r_π between emitter and ground of Q_1.**

Example: Trying to Double Output Impedance using R_E

Relative to a simple bottom Q2 cascode, lets try and double this by adding an additional R_E



$$R_{out} \approx g_{m1} r_{o1} \left(r_{o2} \| r_{\pi 1} \right)$$

$$R_{outA} = r_{o2} + R_E \| r_{\pi 2} + g_{m2} r_{o2} \left(R_E \| r_{\pi 2} \right) \approx g_{m2} r_{o2} \left(R_E \| r_{\pi 2} \right)$$

$$R_{out} \approx g_{m1} r_{o1} \left(R_{outA} \| r_{\pi 1} \right)$$

In order to roughly double R_{out} we need

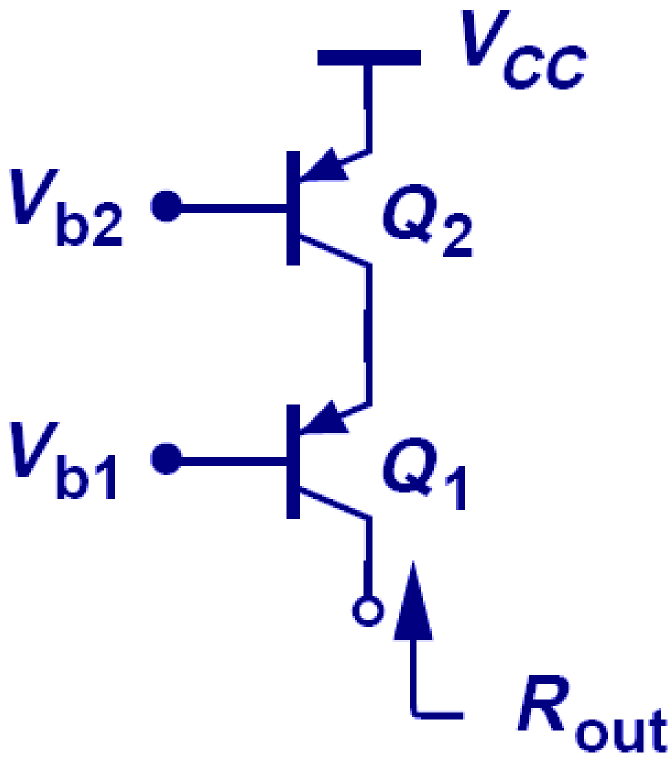
$$R_{outA} \| r_{\pi 1} = 2 \left(r_{o2} \| r_{\pi 1} \right)$$

After some algebra, we find that

$$R_{outA} = \frac{2 r_{o2} r_{\pi 1}}{r_{\pi 1} - r_{o2}}$$

- ➢ **Typically r_π is smaller than r_O, so in general it is impossible to double the output impedance by degenerating Q_2 with a resistor.**

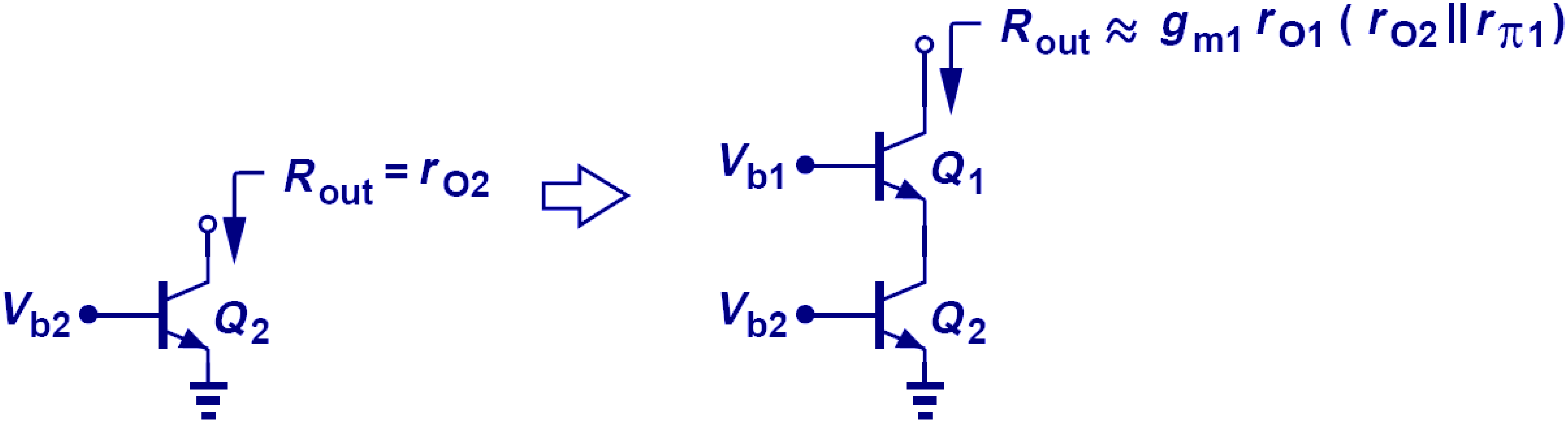
PNP Cascode Stage



$$R_{out} = [1 + g_m (r_{O2} \| r_{\pi 1})] r_{O1} + r_{O2} \| r_{\pi 1}$$

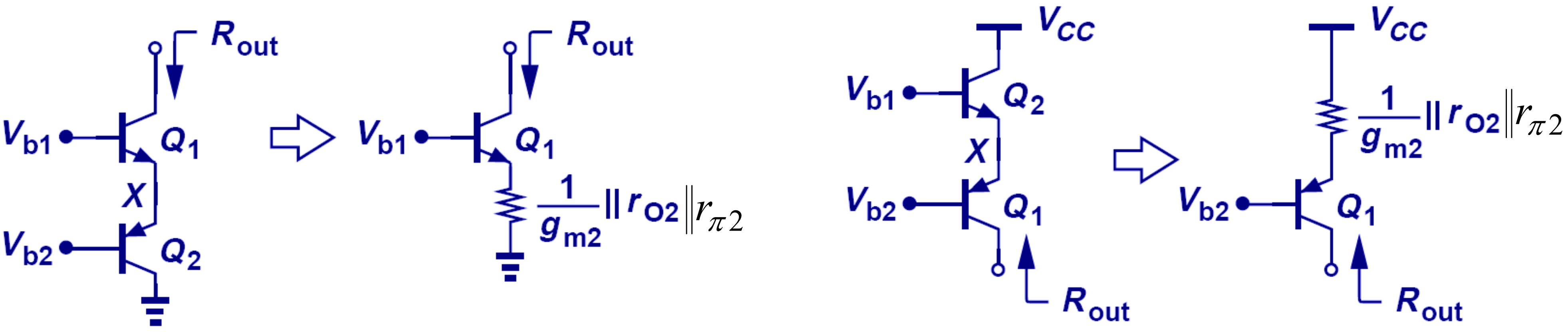
$$R_{out} \approx g_{m1} r_{O1} (r_{O2} \| r_{\pi 1})$$

Another Interpretation of Bipolar Cascode



- **Instead of treating cascode as Q_2 degenerating Q_1, we can also think of it as Q_1 stacking on top of Q_2 (current source) to boost Q_2's output impedance.**

False Cascodes



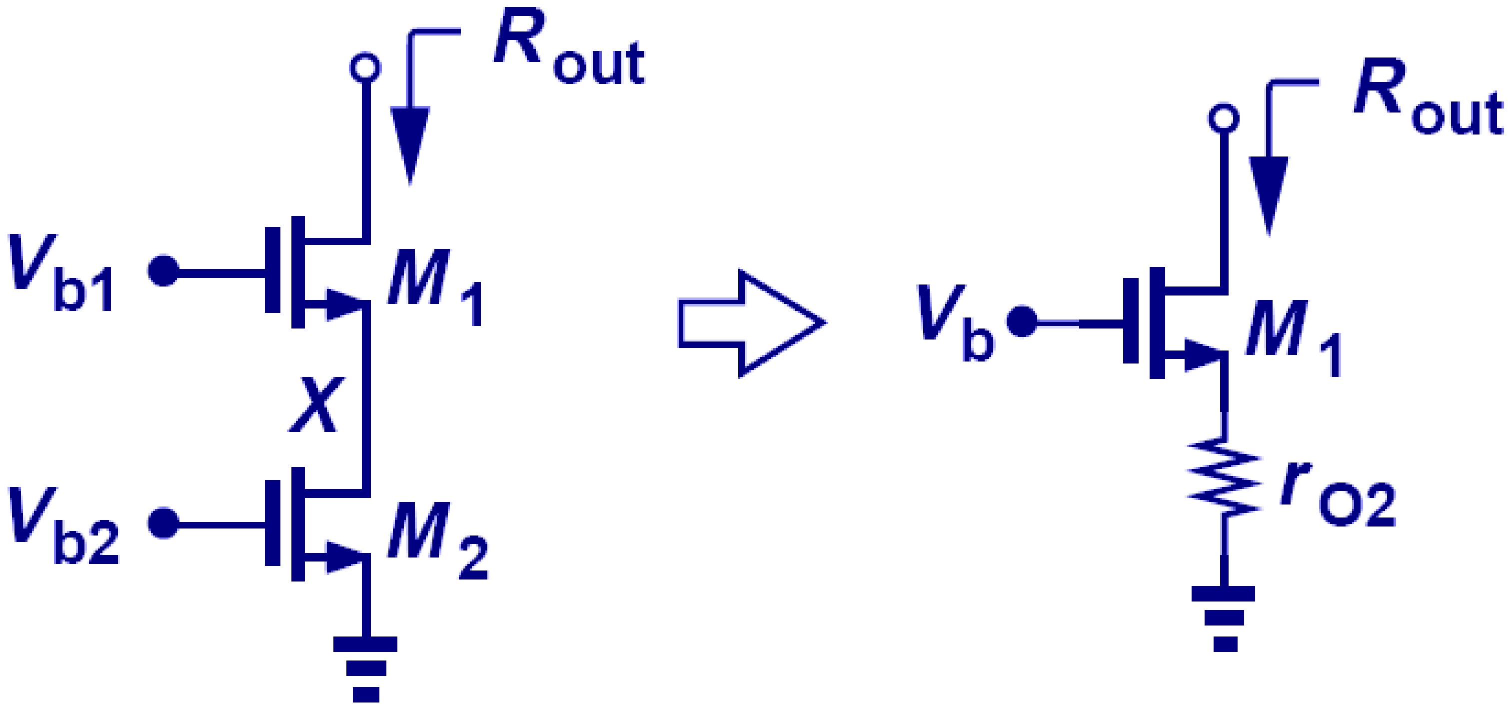
(a) (b)

$$R_{out} = \left[1 + g_{m1}\left(\frac{1}{g_{m2}} \| r_{O2} \| r_{\pi 2} \| r_{\pi 1}\right)\right] r_{O1} + \frac{1}{g_{m2}} \| r_{O2} \| r_{\pi 2} \| r_{\pi 1}$$

$$R_{out} \approx \left(1 + \frac{g_{m1}}{g_{m2}}\right) r_{O1} + \frac{1}{g_{m2}} \approx 2 r_{O1}$$

- **When the emitter of Q_1 is connected to the emitter of Q_2, it's no longer a cascode since Q_2 becomes a diode-connected device instead of a current source.**

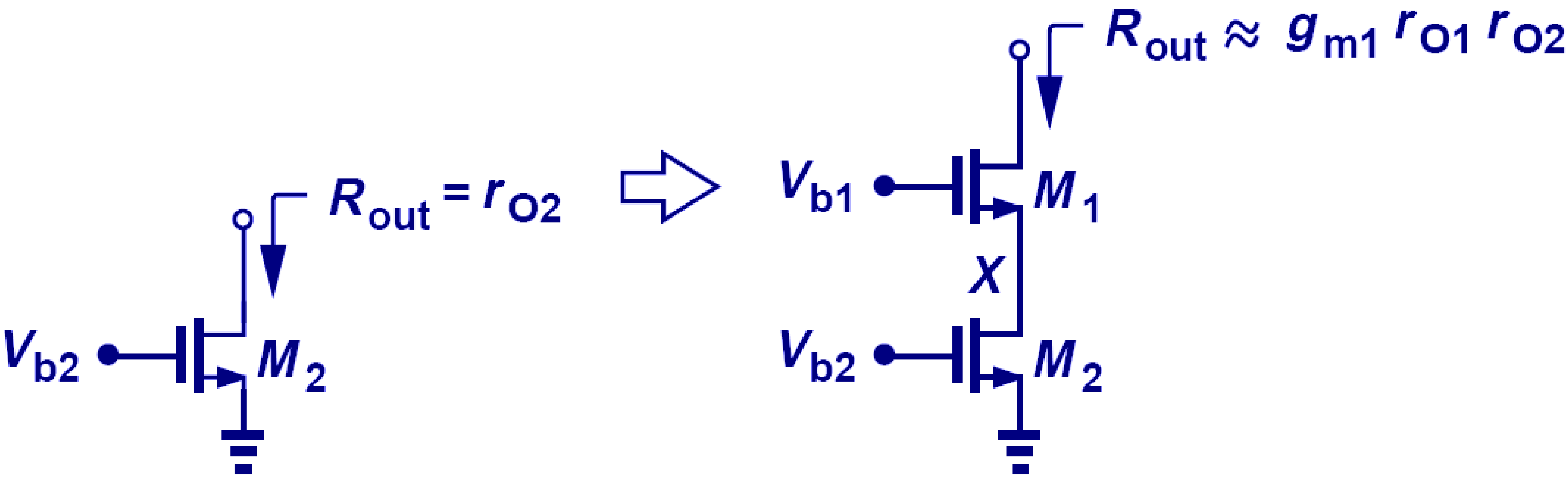
MOS Cascode Stage



$$R_{out} = (1 + g_{m1} r_{O2}) r_{O1} + r_{O2}$$

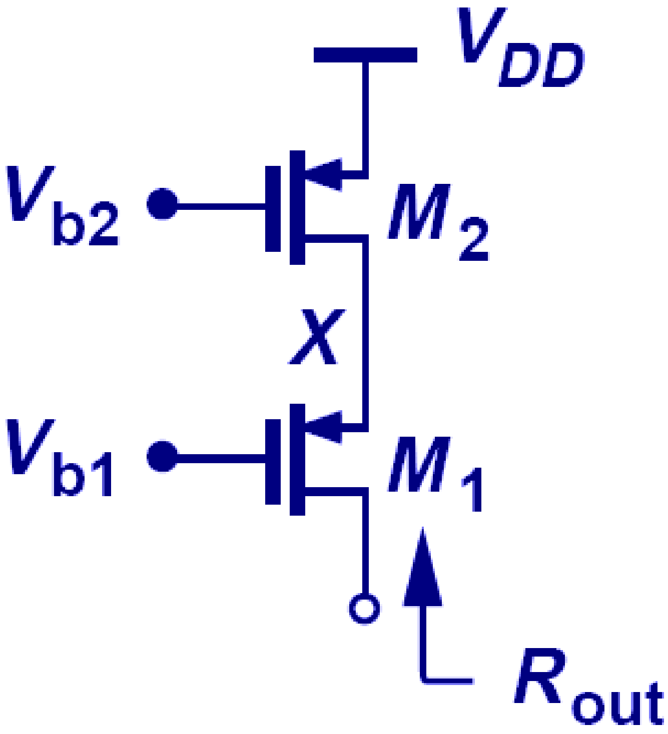
$$R_{out} \approx g_{m1} r_{O1} r_{O2}$$

Another Interpretation of MOS Cascode



- Similar to its bipolar counterpart, MOS cascode can be thought of as stacking a transistor on top of a current source.
- Unlike bipolar cascode, the output impedance is not limited by β.

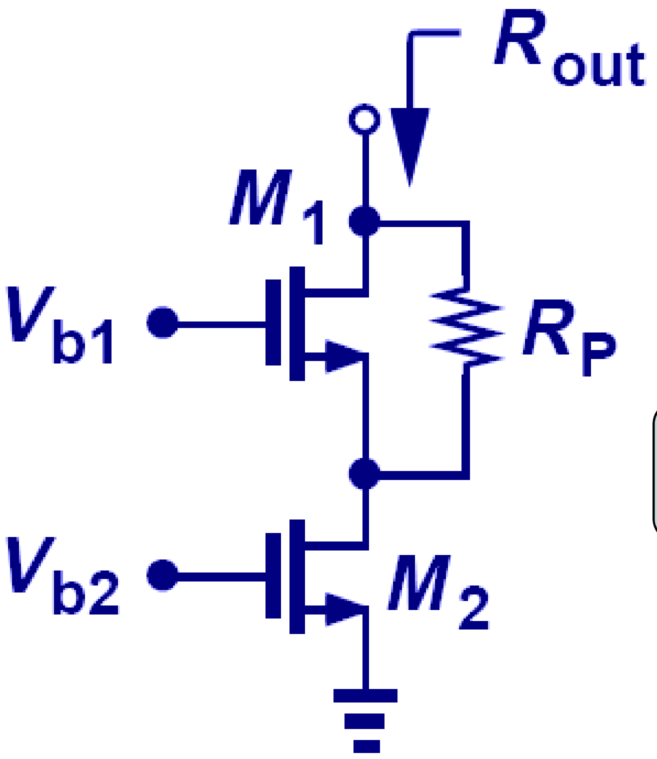
PMOS Cascode Stage



$$R_{out} = (1 + g_{m1} r_{O2}) r_{O1} + r_{O2}$$

$$R_{out} \approx g_{m1} r_{O1} r_{O2}$$

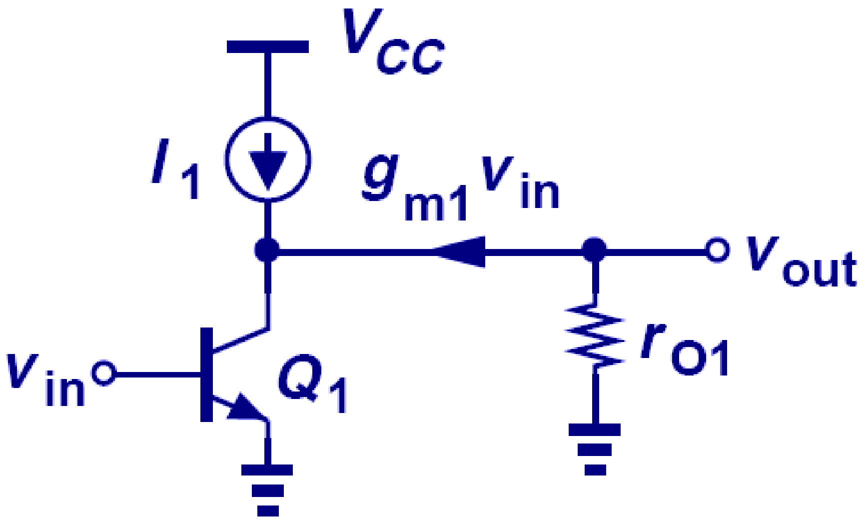
Example: Parasitic Resistance



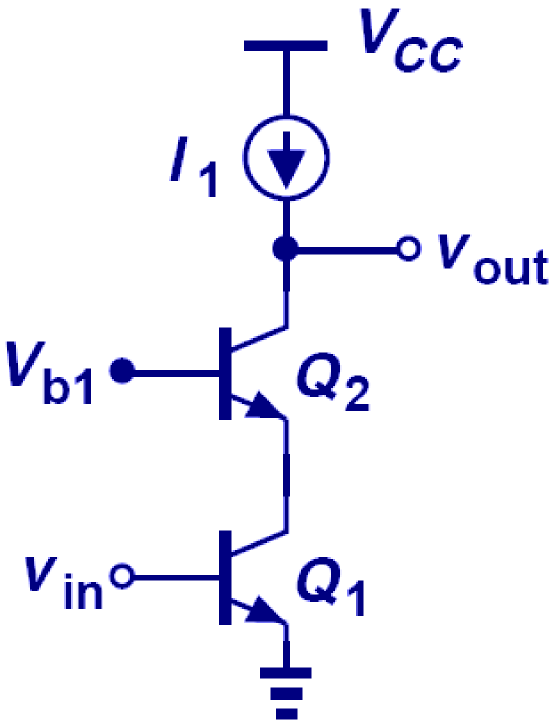
$$R_{out} = (1 + g_{m1} r_{O2})(r_{O1} \| R_P) + r_{O2}$$

- R_P will lower the output impedance, since its parallel combination with r_{O1} will always be lower than r_{O1}.

Comparison between Bipolar Cascode and CE Stage



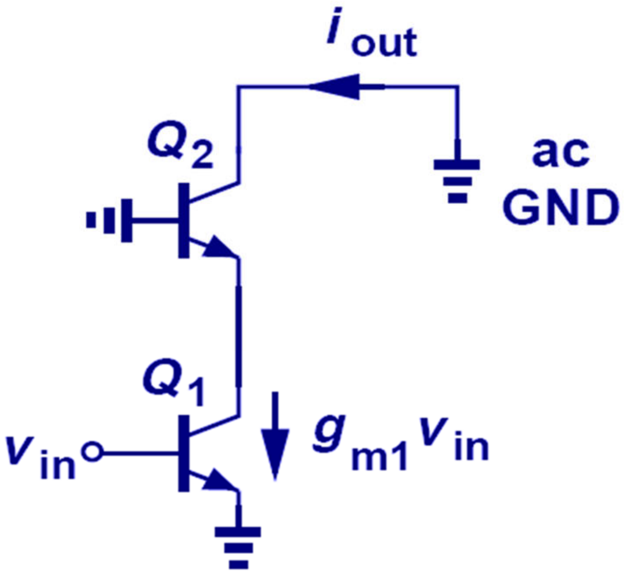
(a)



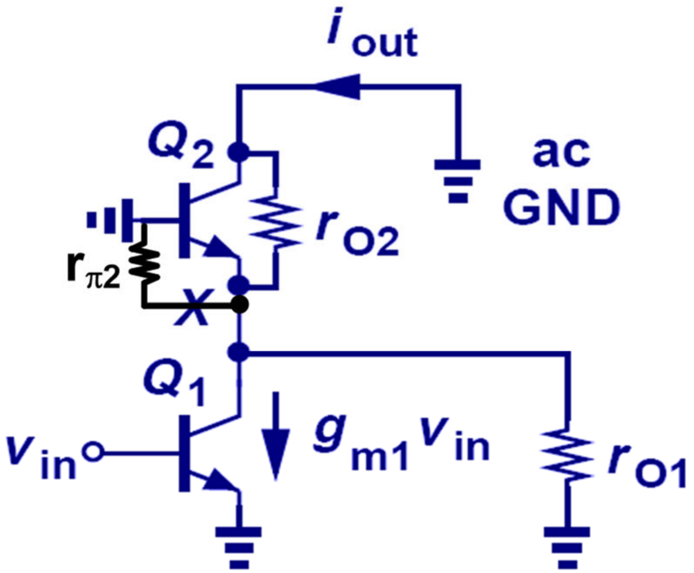
(b)

- Since the output impedance of bipolar cascode is higher than that of the CE stage, we would expect its voltage gain to be higher as well.

Voltage Gain of Bipolar Cascode Amplifier



(a)



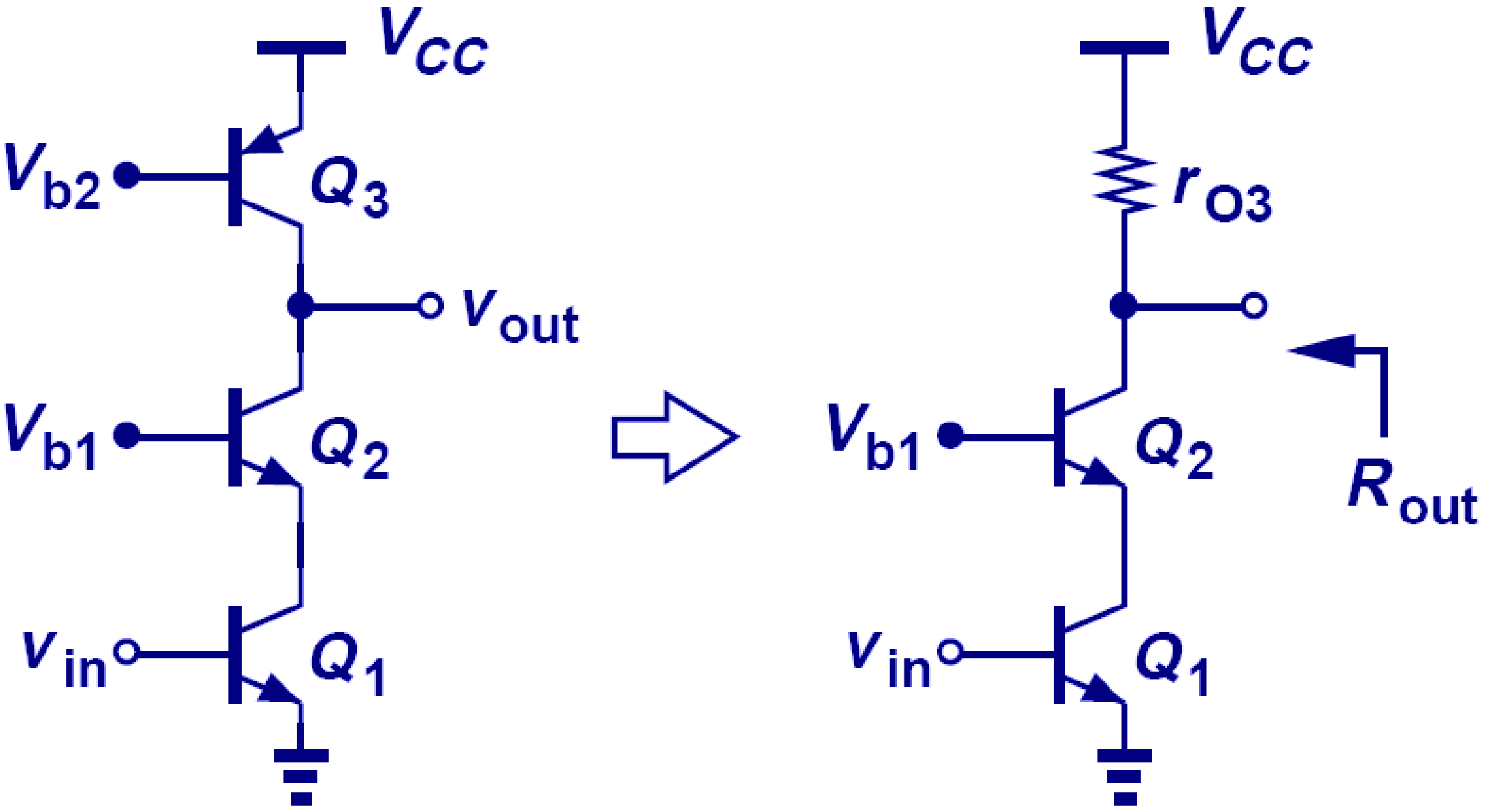
(b)

$$G_m \approx g_{m1}$$

$$A_v \approx -g_{m1} r_{O2} g_{m2} (r_{O1} \| r_{\pi 2})$$

- **Since r_O is much larger than $1/g_m$, most of $I_{C,Q1}$ flows into the diode-connected Q_2. Using R_{out} as before, A_V is easily calculated.**

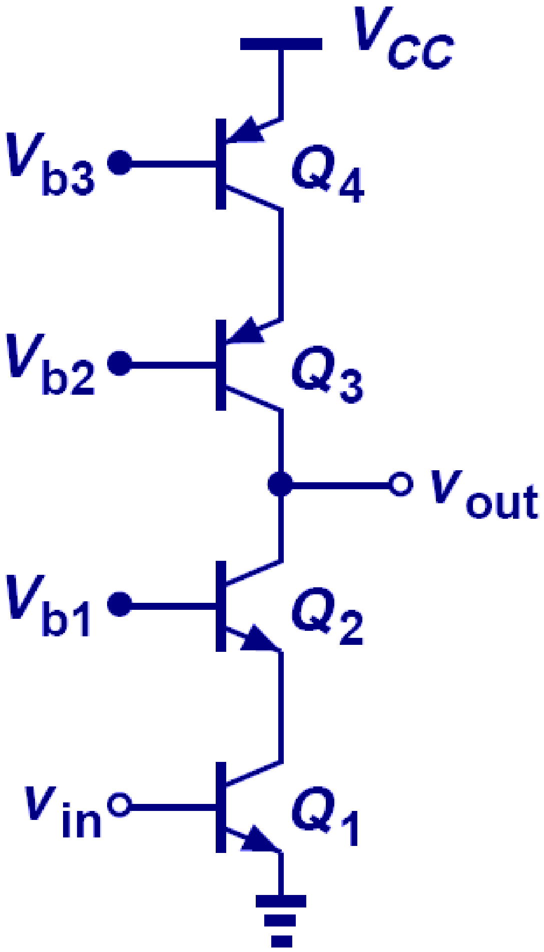
Practical Cascode Stage



$$R_{out} \approx r_{O3} \| g_{m2} r_{O2} (r_{O1} \| r_{\pi 2})$$

- **Since no current source can be ideal, the output impedance drops.**

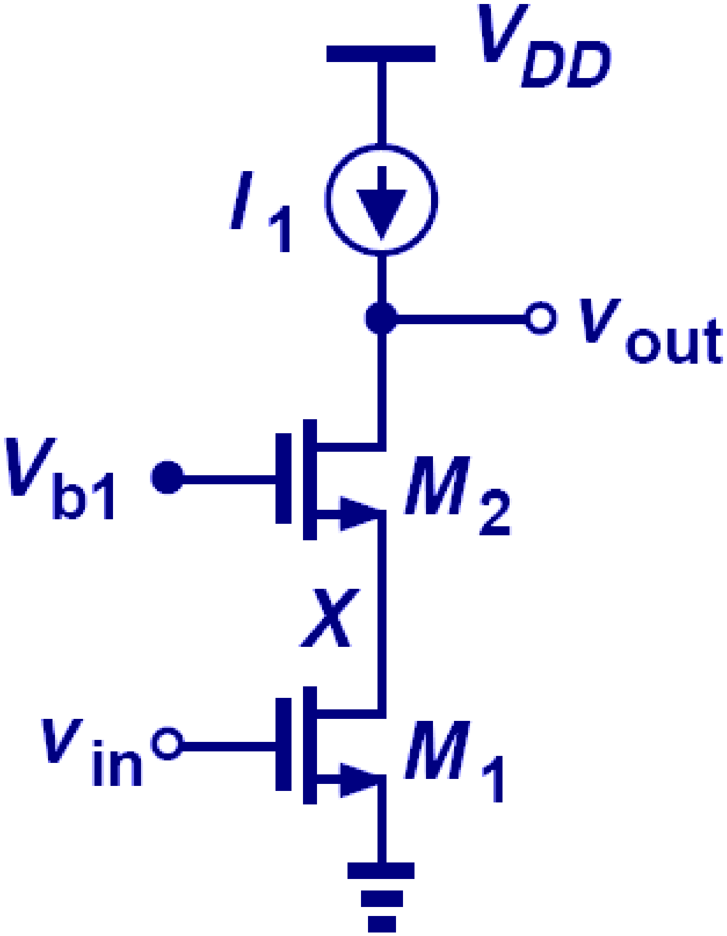
Improved Cascode Stage



$$R_{out} \approx g_{m3} r_{O3} (r_{O4} \| r_{\pi 3}) \| g_{m2} r_{O2} (r_{O1} \| r_{\pi 2})$$

- **In order to preserve the high output impedance, a cascode PNP current source is used.**

MOS Cascode Amplifier

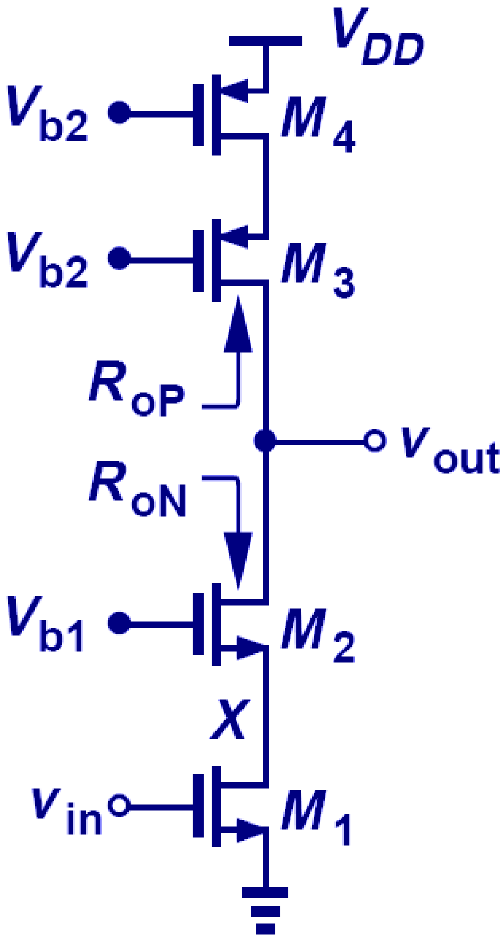


$$A_v = -G_m R_{out}$$

$$A_v \approx -g_{m1}\left[(1+g_{m2}r_{O2})r_{O1}+r_{O2}\right]$$

$$A_v \approx -g_{m1}g_{m2}r_{O2}r_{O1}$$

Improved MOS Cascode Amplifier



$$R_{on} \approx g_{m2} r_{O2} r_{O1}$$

$$R_{op} \approx g_{m3} r_{O3} r_{O4}$$

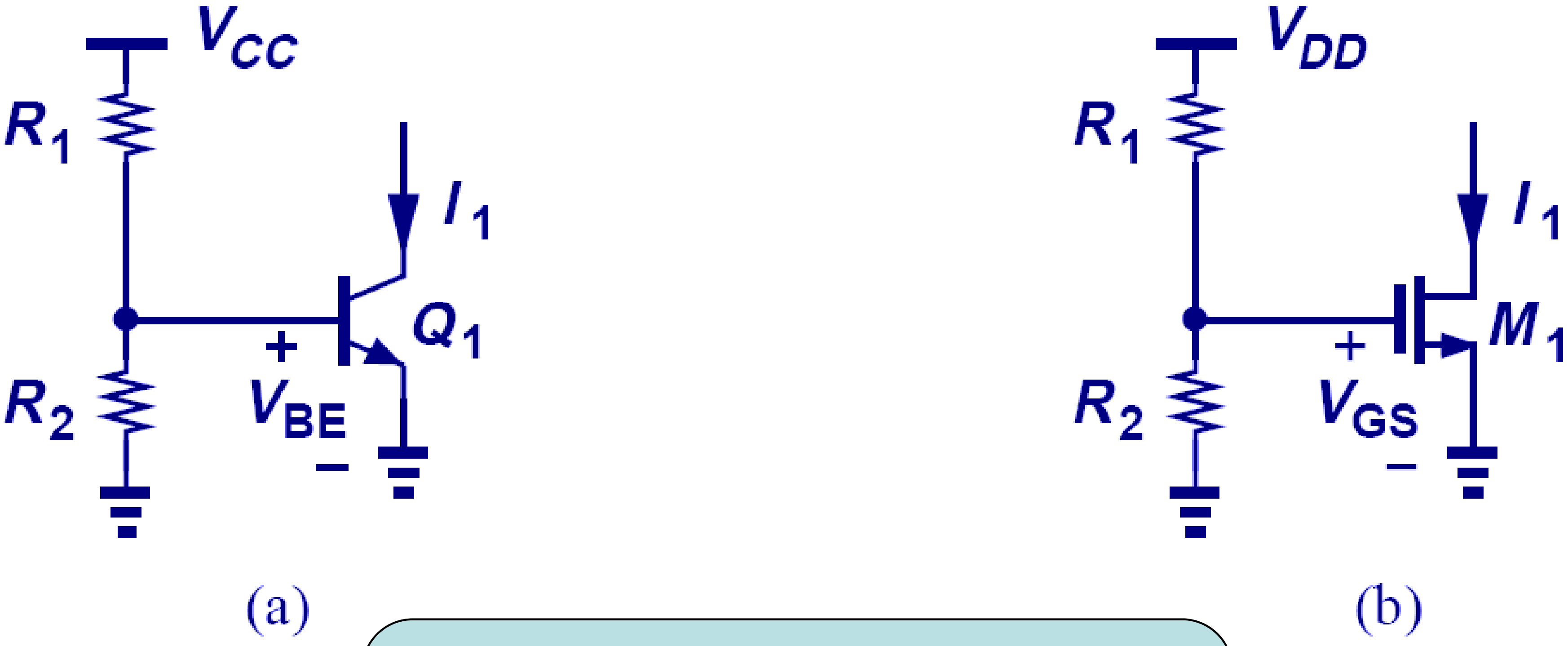
$$R_{out} = R_{on} \parallel R_{op}$$

- **Similar to its bipolar counterpart, the output impedance of a MOS cascode amplifier can be improved by using a PMOS cascode current source.**

Agenda

- Cascode Stages
- Current Mirrors
  - BJT Current Mirror Basics
  - MOS Current Mirrors Basics

Temperature and Supply Dependence of Bias Current



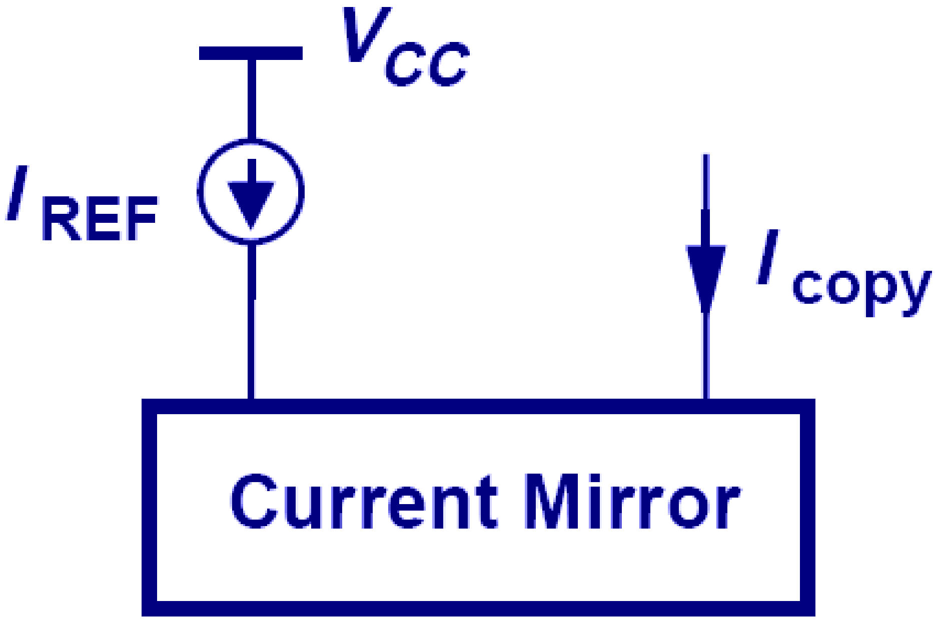
$$V_{BE} = V_T \ln(I_1/I_S) \approx R_2 V_{CC}/(R_1 + R_2)$$

$$I_1 = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(\frac{R_2}{R_1 + R_2}V_{DD} - V_{TH}\right)^2$$

Neglecting I_B

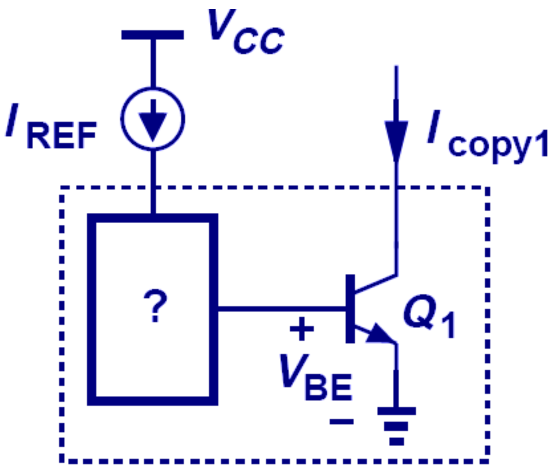
- Since V_T, I_S, μ_n, and V_{TH} all depend on temperature, I_1 for both bipolar and MOS depends on temperature and supply.

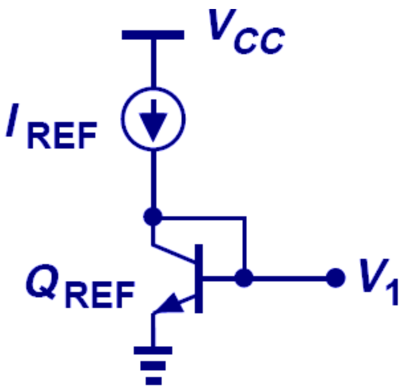
Concept of Current Mirror

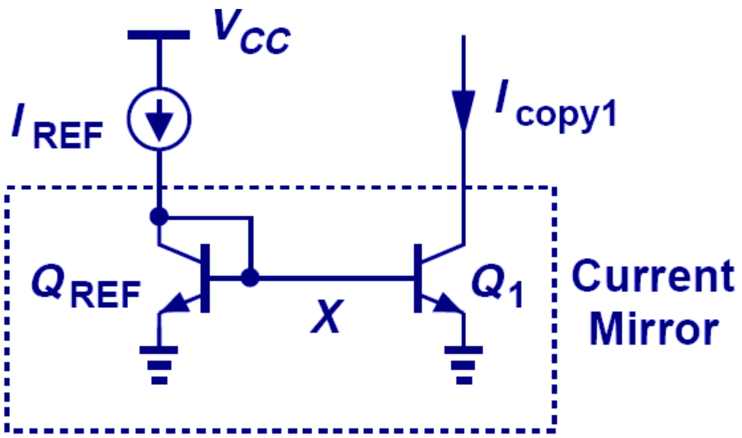


- The motivation behind a current mirror is to sense the current from a “golden current source” and duplicate this “golden current” to other locations.

Bipolar Current Mirror Circuitry







Neglecting base current for now (assuming high β),

from the I_C expression

$$I_C = I_S\left(e^{\frac{V_{BE}}{V_T}} - 1\right) \approx I_S e^{\frac{V_{BE}}{V_T}}$$

the voltage produced by the diode connected transistor is

$$V_1 = V_T \ln\left(\frac{I_{REF}}{I_{S,REF}}\right)$$

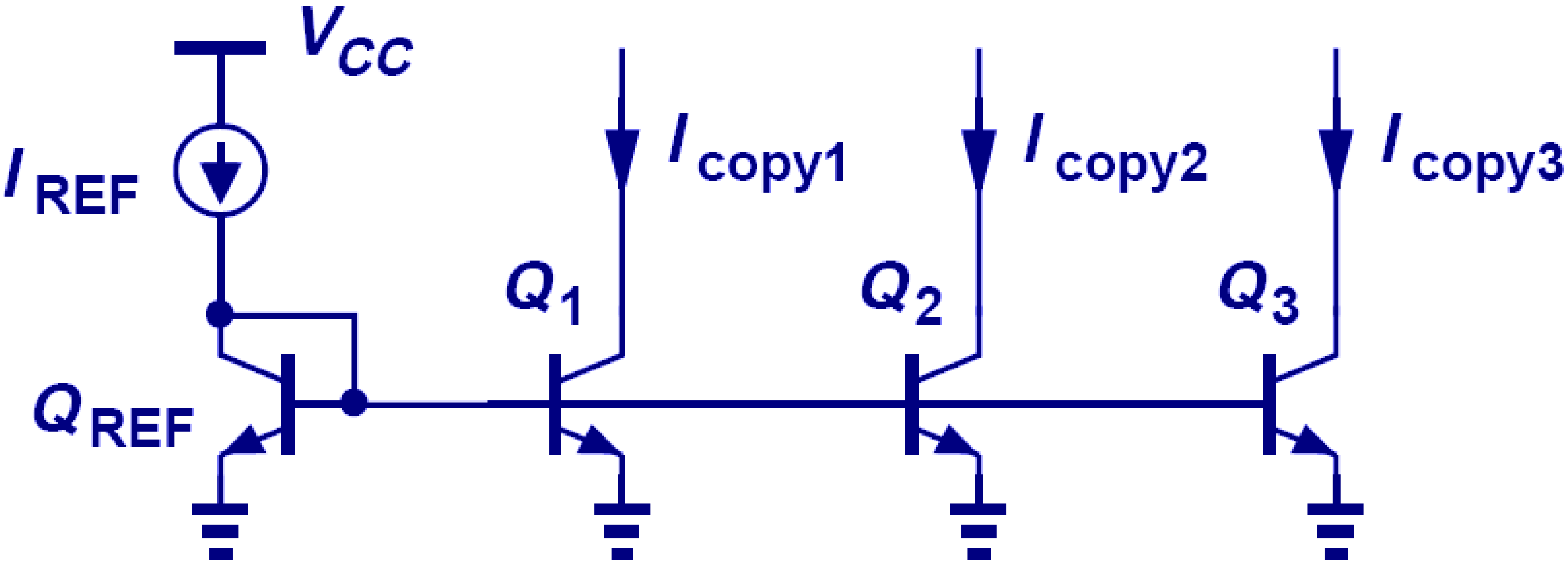
this voltage forms the V_{BE} of the output current source to produce

$$I_{copy} = I_{S1} e^{\frac{V_T \ln\left(\frac{I_{REF}}{I_{S,REF}}\right)}{V_T}} = \frac{I_{S1}}{I_{S,REF}} I_{REF}$$

$$I_{copy} = \frac{I_{S1}}{I_{S,REF}} I_{REF}$$

- **The diode-connected Q_{REF} produces an output voltage V_1 that forces $I_{copy1} = I_{REF}$, if $Q_1 = Q_{REF}$.**

Multiple Copies of I_{REF}

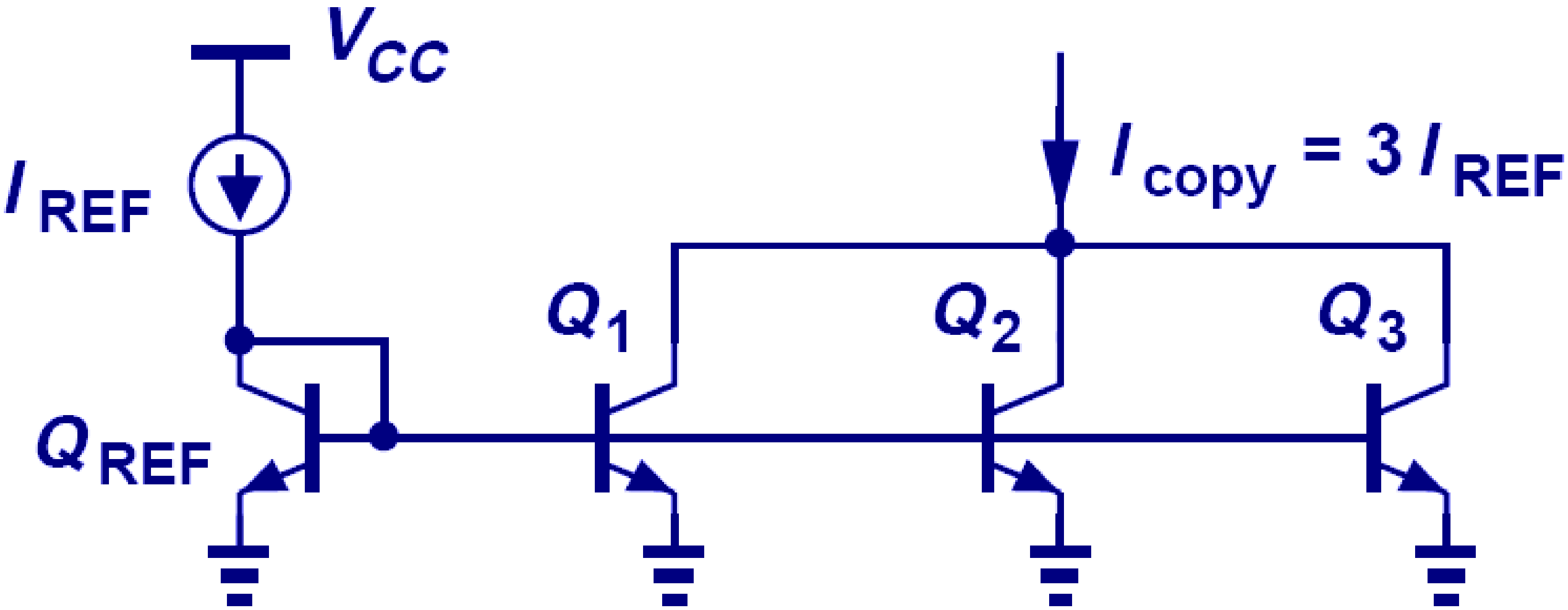


Neglecting I_B

$$I_{copy,j} = \frac{I_{S,j}}{I_{S,REF}} I_{REF}$$

- Multiple copies of I_{REF} can be generated at different locations by simply applying the idea of current mirror to more transistors.

Current Scaling

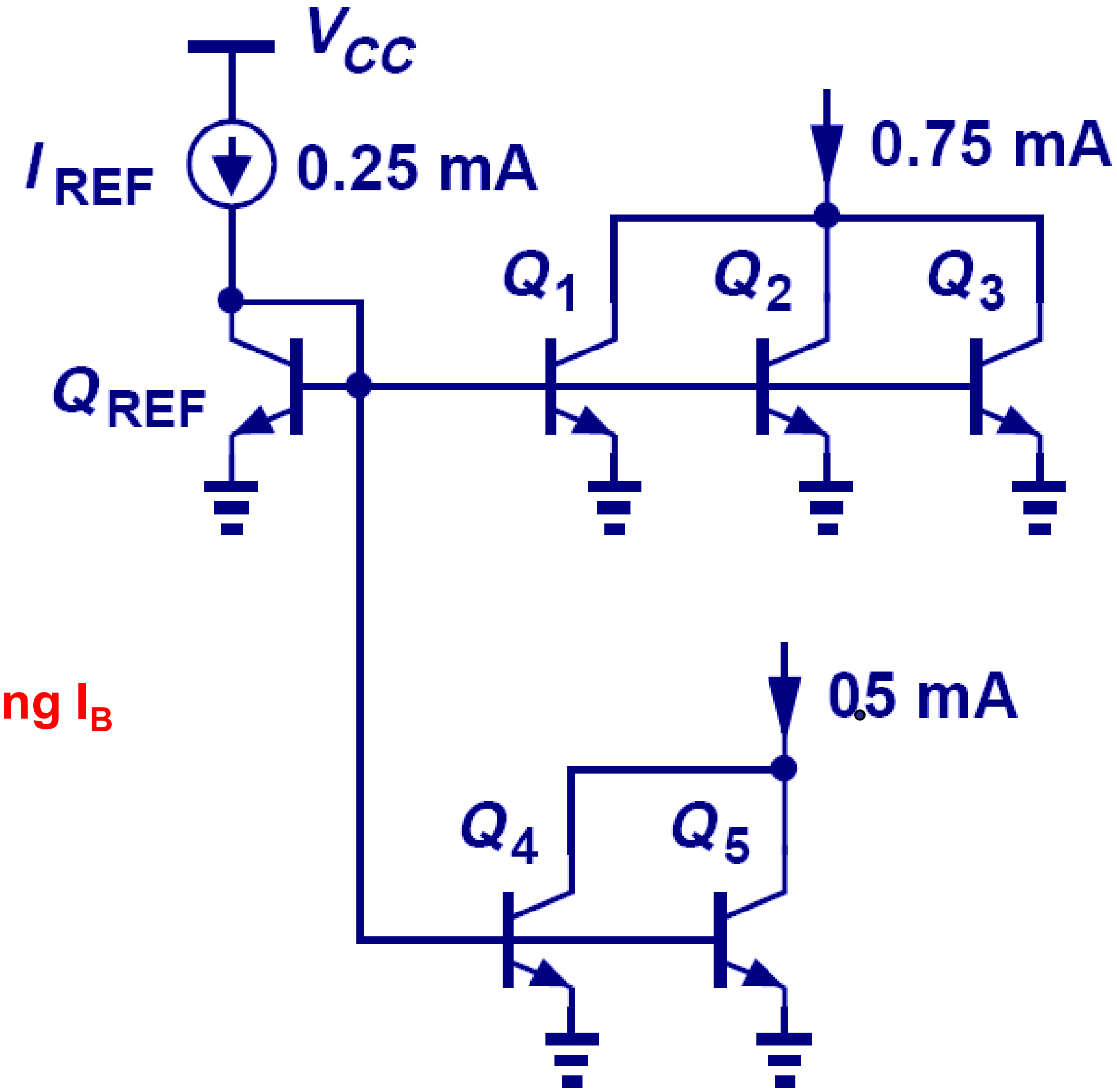


Neglecting I_B

$$I_{copy,j} = nI_{REF}$$

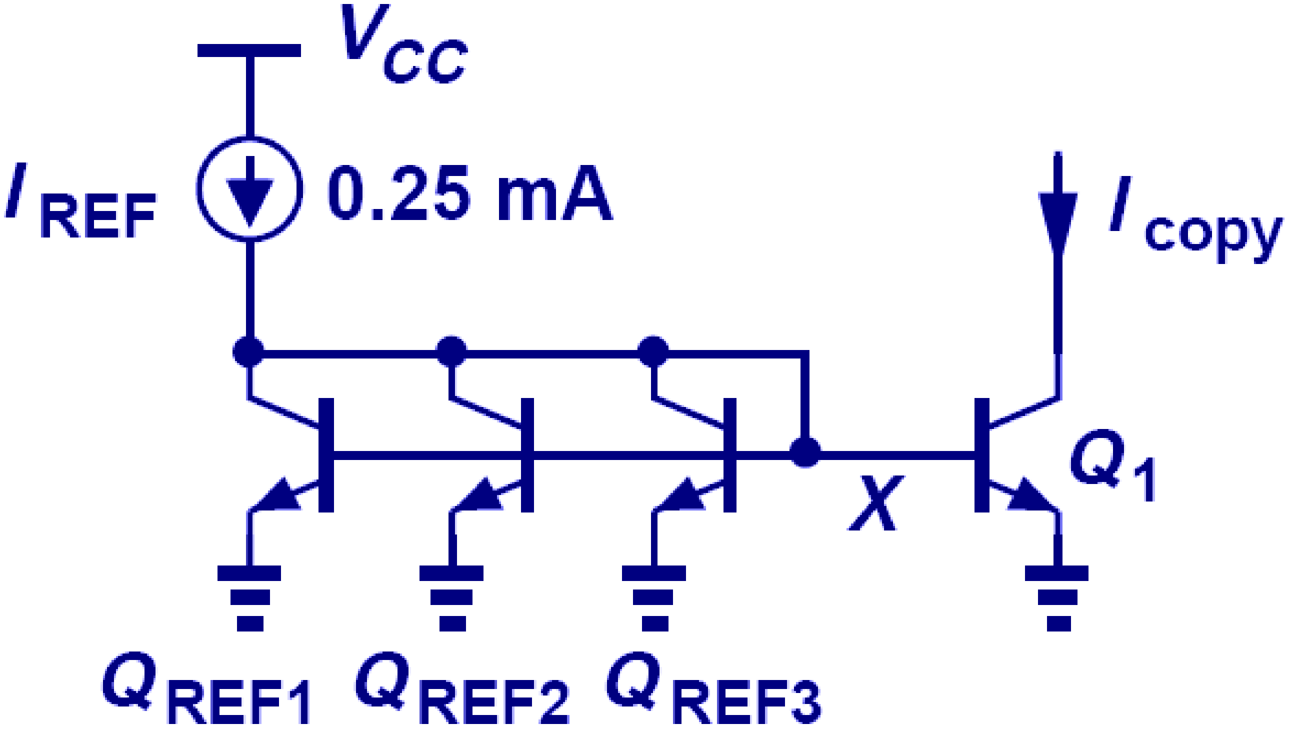
- By scaling the emitter area of Q_j n times with respect to Q_{REF}, $I_{copy,j}$ is also n times larger than I_{REF}. This is equivalent to placing n unit-size transistors in parallel.

Example: Scaled Current



Neglecting I_B

Fractional Scaling

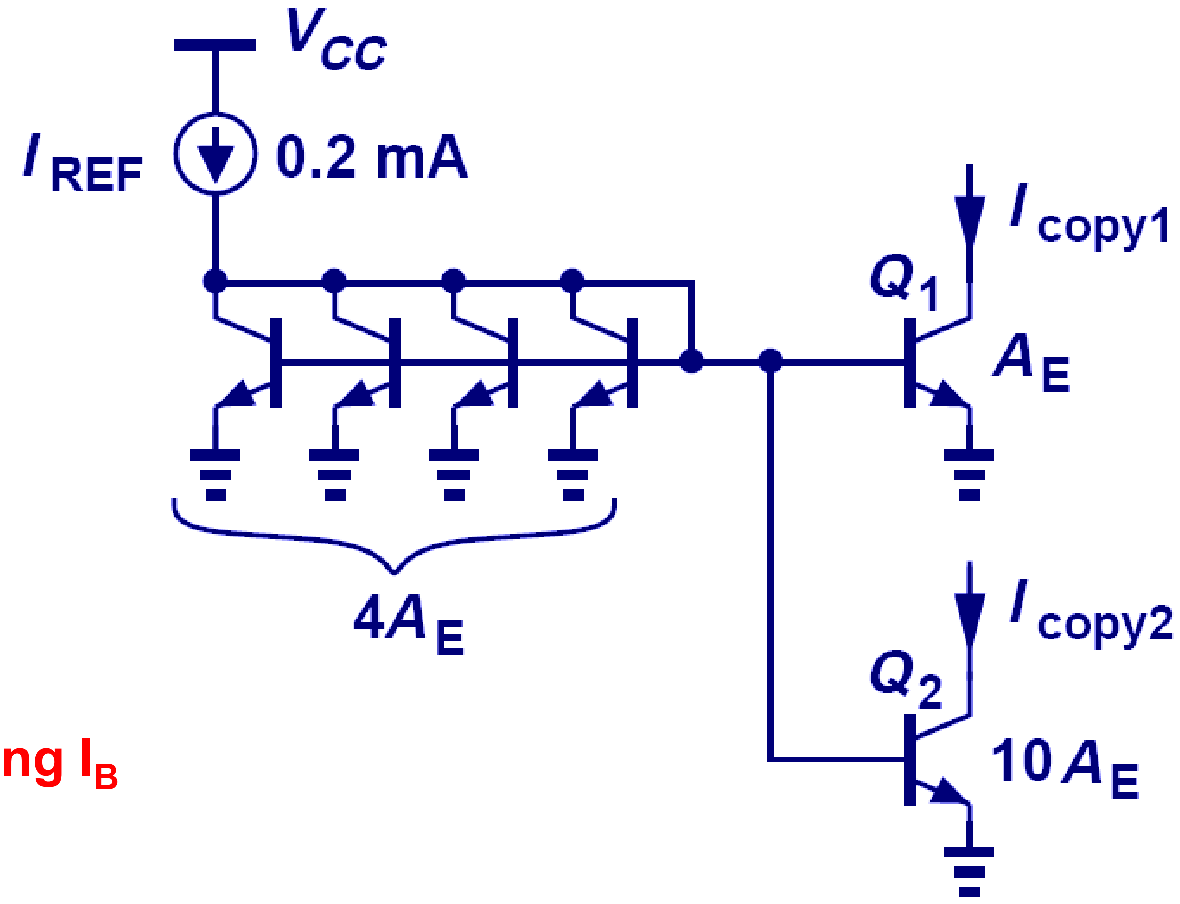


Neglecting I_B

$$I_{copy} = \frac{1}{3} I_{REF}$$

- A fraction of I_{REF} can be created on Q_1 by scaling up the emitter area of Q_{REF}.

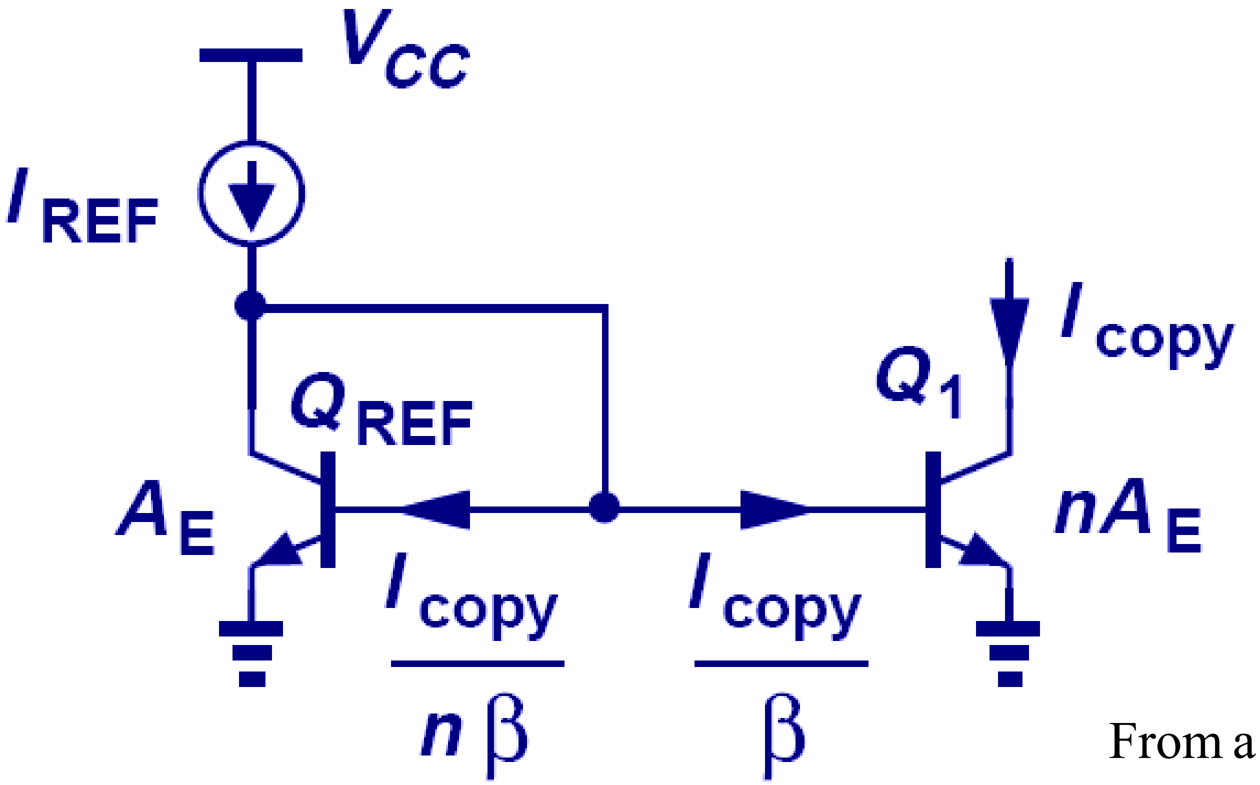
Example: Different Mirroring Ratio



Neglecting I_B

- Using the idea of current scaling and fractional scaling, I_{copy2} is 0.5mA and I_{copy1} is 0.05mA respectively. All coming from a source of 0.2mA.

Mirroring Error Due to Base Currents



$$I_{B1}=\frac{I_{copy}}{\beta}$$

$$I_{B,REF}=\frac{I_{copy}}{n\beta}$$

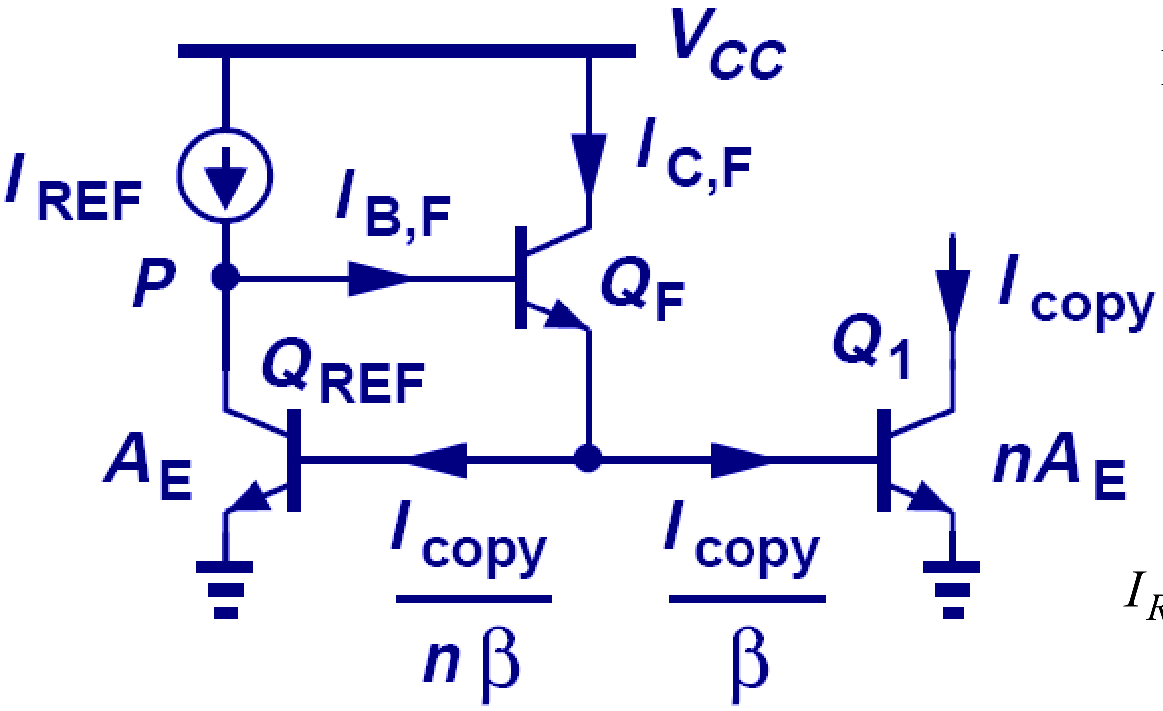
From a KCL at the base/collector of Q_{REF}

$$I_{REF}=\frac{I_{copy}}{n}+\frac{I_{copy}}{n\beta}+\frac{I_{copy}}{\beta}$$

$$I_{copy}=\frac{nI_{REF}}{1+\frac{1}{\beta}(n+1)}$$

$$\boxed{I_{copy}=\frac{nI_{REF}}{1+\frac{1}{\beta}(n+1)}}$$

Improved Mirroring Accuracy



From a KCL at the base of Q_1 and Q_{REF}

$$I_{E,F} \approx I_{C,F} = \frac{I_{copy}}{\beta}\left(1+\frac{1}{n}\right)$$

$$I_{B,F} = \frac{I_{copy}}{\beta^2}\left(1+\frac{1}{n}\right)$$

From a KCL at the collector of Q_{REF}

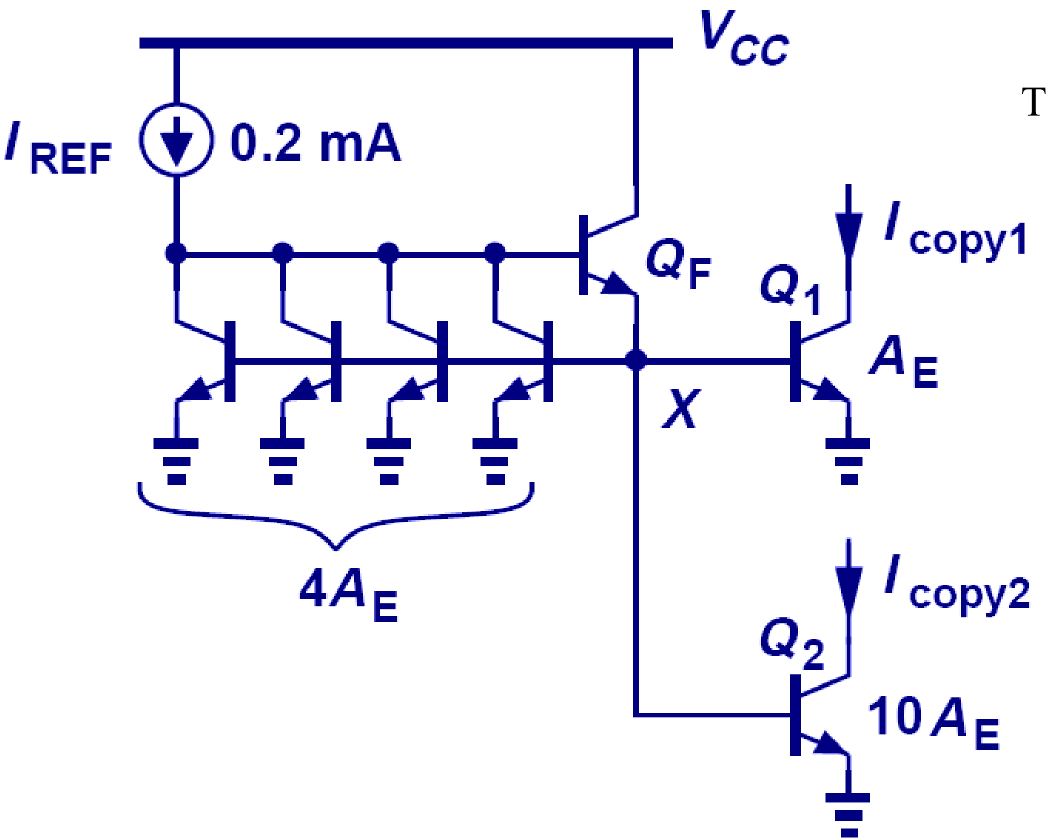
$$I_{REF} = I_{B,F} + I_{C,REF} = \frac{I_{copy}}{\beta^2}\left(1+\frac{1}{n}\right) + \frac{I_{copy}}{n}$$

$$I_{copy} = \frac{nI_{REF}}{1+\frac{1}{\beta^2}(n+1)}$$

$$\boxed{I_{copy} = \frac{nI_{REF}}{1+\frac{1}{\beta^2}(n+1)}}$$

- **Because of Q_F, the base currents of Q_{REF} and Q_1 are mostly supplied by Q_F rather than I_{REF}. Mirroring error is reduced β times.**
- **Q_F is often called a "β helper"**

Example: Different Mirroring Ratio Accuracy



$$n_{total} = \frac{A_E}{4A_E} + \frac{10A_E}{4A_E} = \frac{11}{4}$$

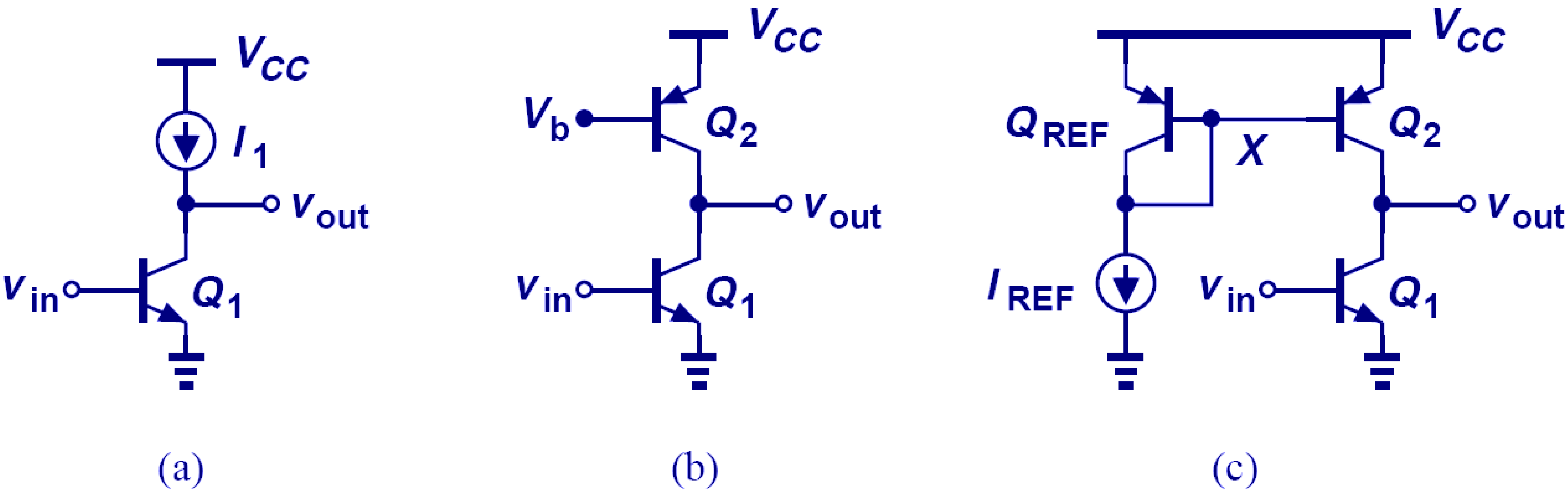
The key to finding the copied currents is to first compute the total current copied using

$$I_{copy,total} = \frac{n_{total} I_{REF}}{1 + \frac{1}{\beta^2}\left(n_{total} + 1\right)} = \frac{\left(\frac{11}{4}\right) I_{REF}}{1 + \frac{1}{\beta^2}\left(\frac{11}{4} + 1\right)} = \frac{11 I_{REF}}{4 + \frac{15}{\beta^2}}$$

Then scale the individual output currents

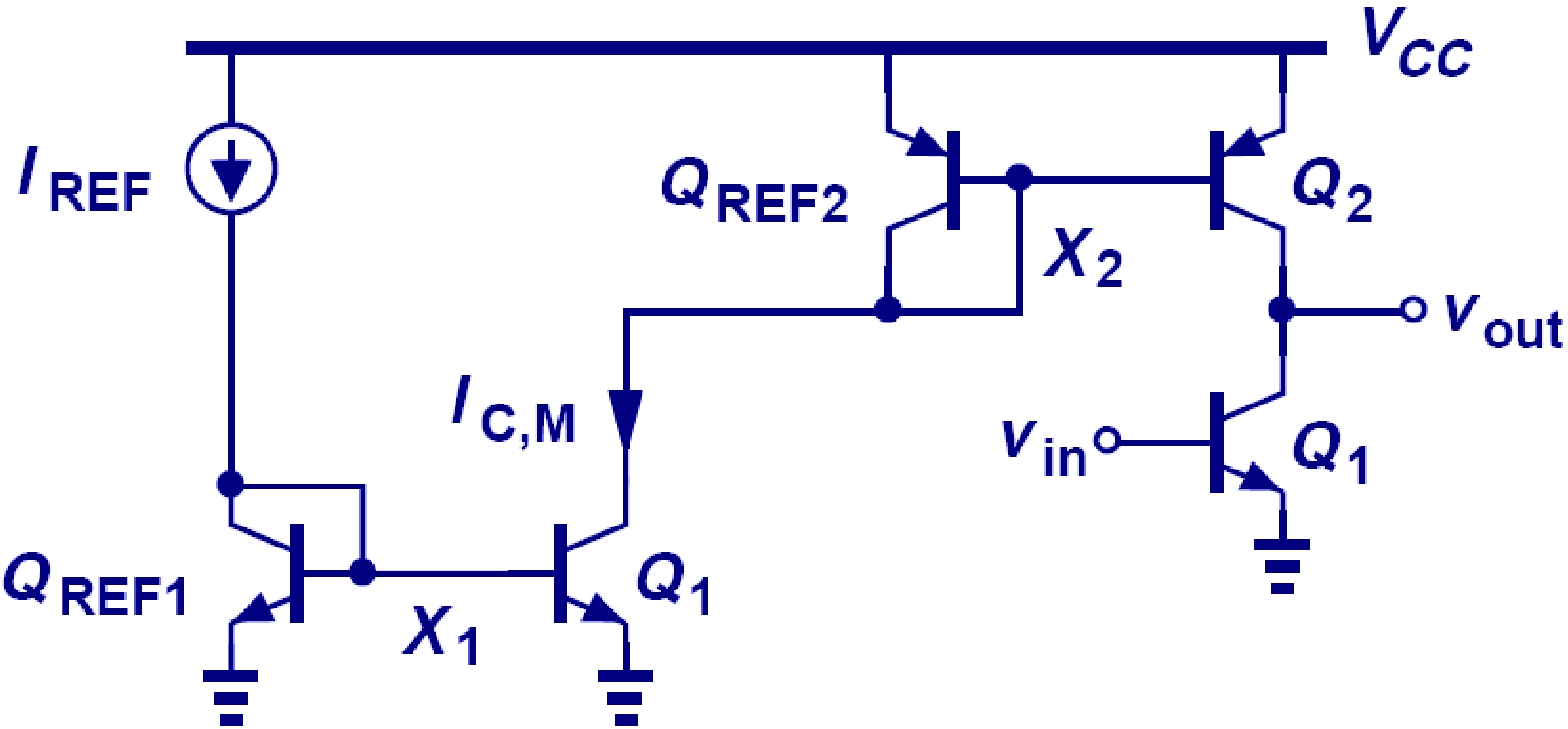
$$\boxed{\begin{aligned} I_{copy1} &= \left(\frac{1}{11}\right) I_{copy,total} = \frac{I_{REF}}{4 + \frac{15}{\beta^2}} \\ I_{copy2} &= \left(\frac{10}{11}\right) I_{copy,total} = \frac{10 I_{REF}}{4 + \frac{15}{\beta^2}} \end{aligned}}$$

PNP Current Mirror

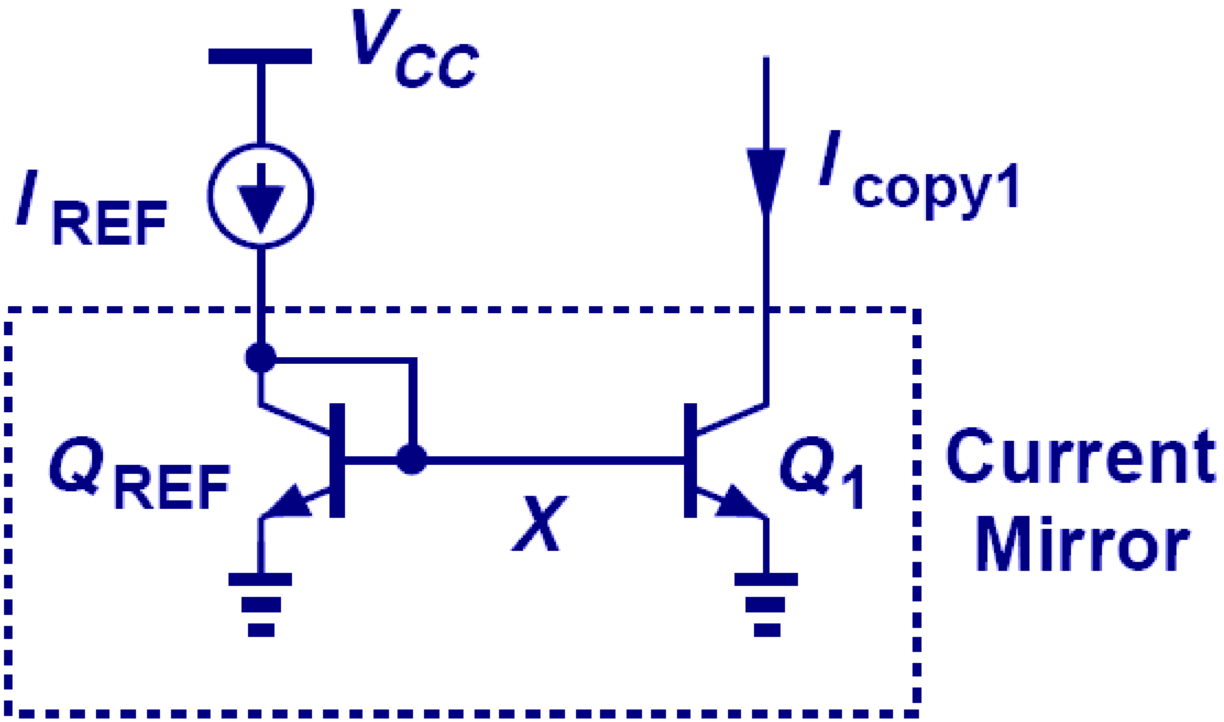


- **PNP current mirror is used as a current source load to an NPN amplifier stage.**
- **But what if we only have 1 ideal reference current that flows from V_{CC}, as in all the previous NPN current mirror examples?**

Generation of I_{REF} for PNP Current Mirror



Example: Current Mirror with Discrete Devices



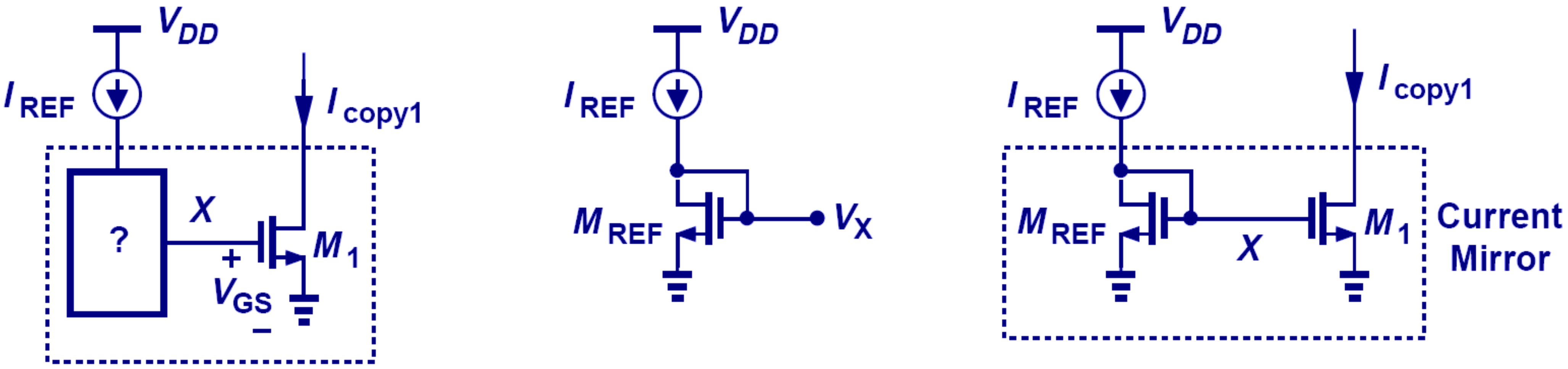
- Let Q_{REF} and Q_1 be discrete NPN devices. I_{REF} and I_{copy1} can vary in large magnitude due to I_S mismatch.
- Thus, current mirrors may not be used that often in discrete (board-level) design, but are pervasive in integrated circuit (IC) design

Agenda

- Cascode Stages

- Current Mirrors
  - BJT Current Mirror Basics
  - MOS Current Mirrors Basics

MOS Current Mirror



(c)

From the saturation current equation

$$I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}\left(V_{GS} - V_{TH,n}\right)^2$$

the voltage produced by the diode connected transistor is

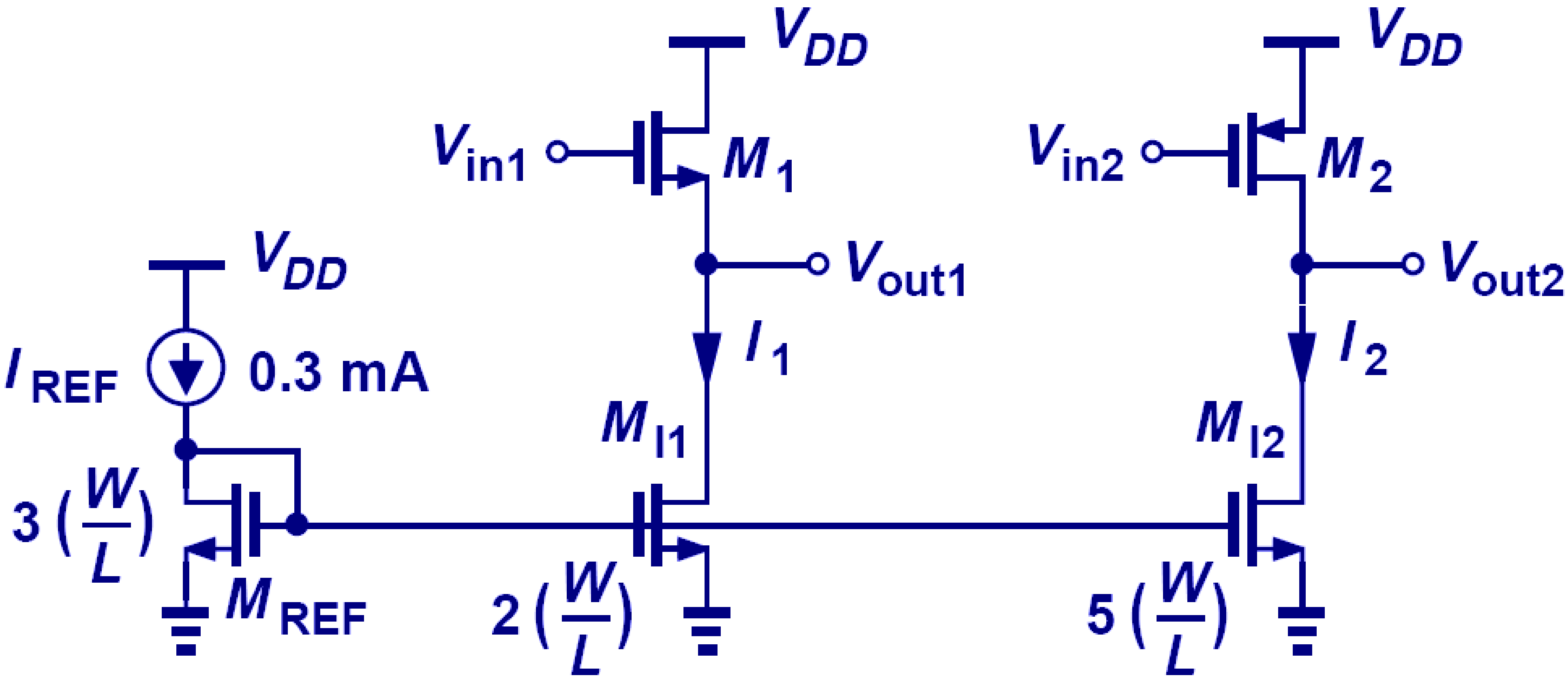
$$V_X = \sqrt{\frac{2I_{REF}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_{REF}}} + V_{TH,n}$$

this voltage forms the V_{GS} of the output current source to produce

$$I_{copy} = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)_1\left(\sqrt{\frac{2I_{REF}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_{REF}}} + V_{TH,n} - V_{TH,n}\right)^2 = \frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_{REF}} I_{REF}$$

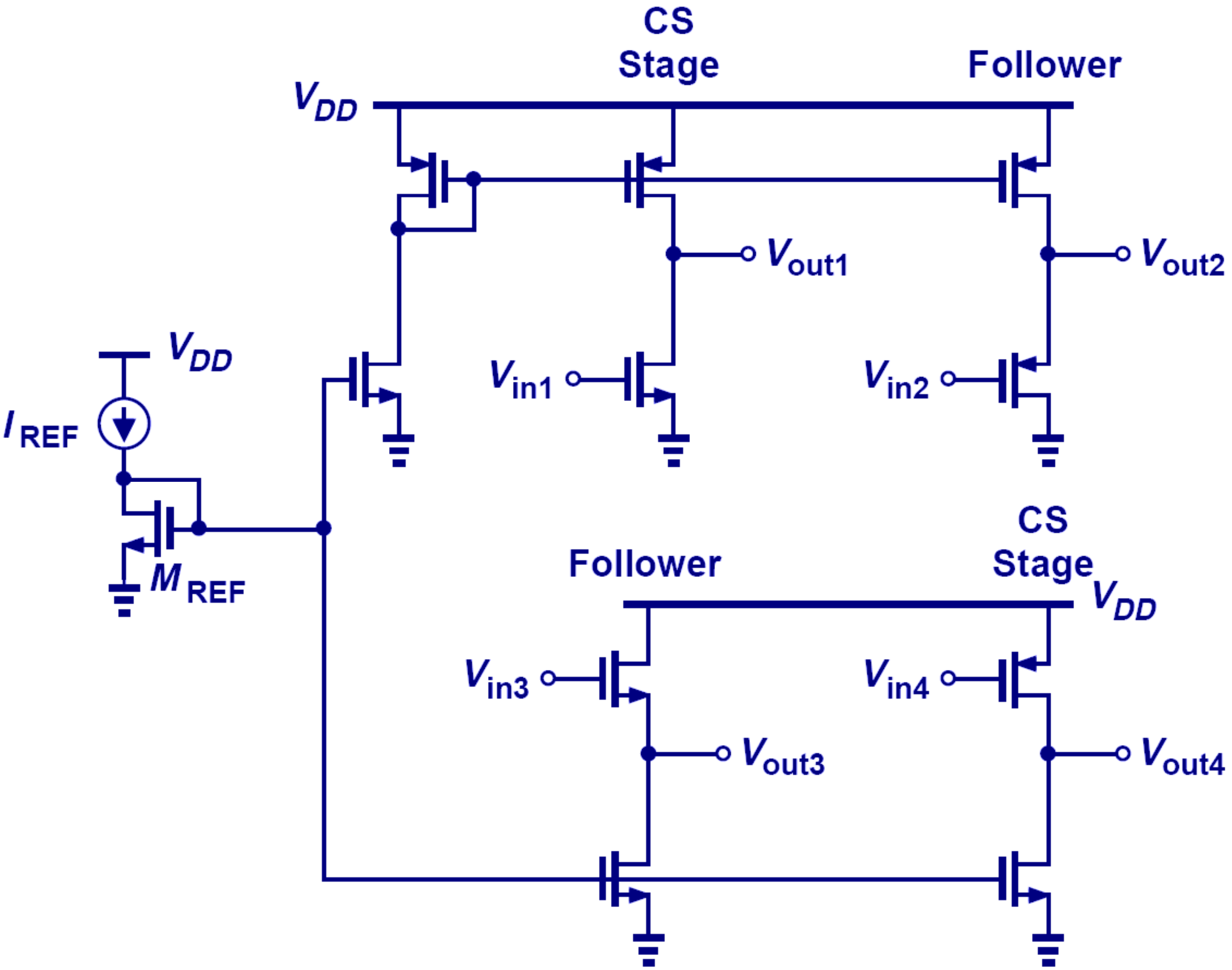
$$\boxed{I_{copy} = \frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_{REF}} I_{REF}}$$

Example: Current Scaling



- **Similar to their bipolar counterpart, MOS current mirrors can also scale I_{REF} up or down ($I_1 = 0.2mA$, $I_2 = 0.5mA$).**

CMOS Current Mirror



- **The idea of combining NMOS and PMOS to produce CMOS current mirror is shown above.**

Next Time

- Operational Transconductance Amplifiers
  - Lab 7