

ECEN326: Electronic Circuits

Fall 2022

Lecture 6: Frequency Response



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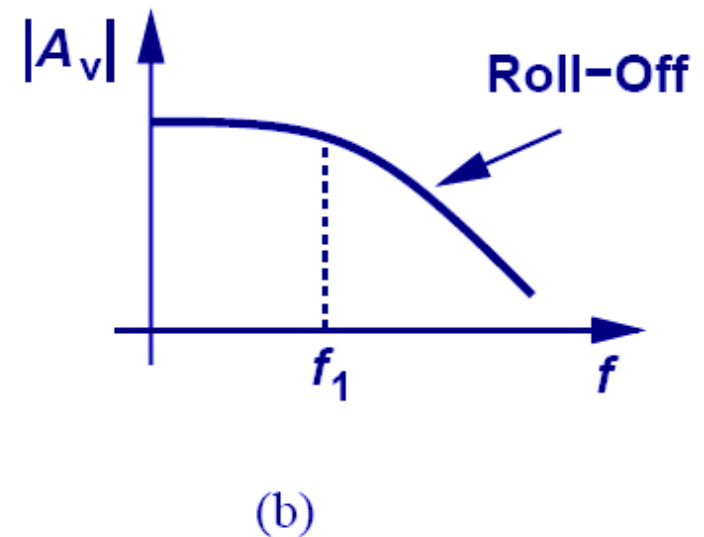
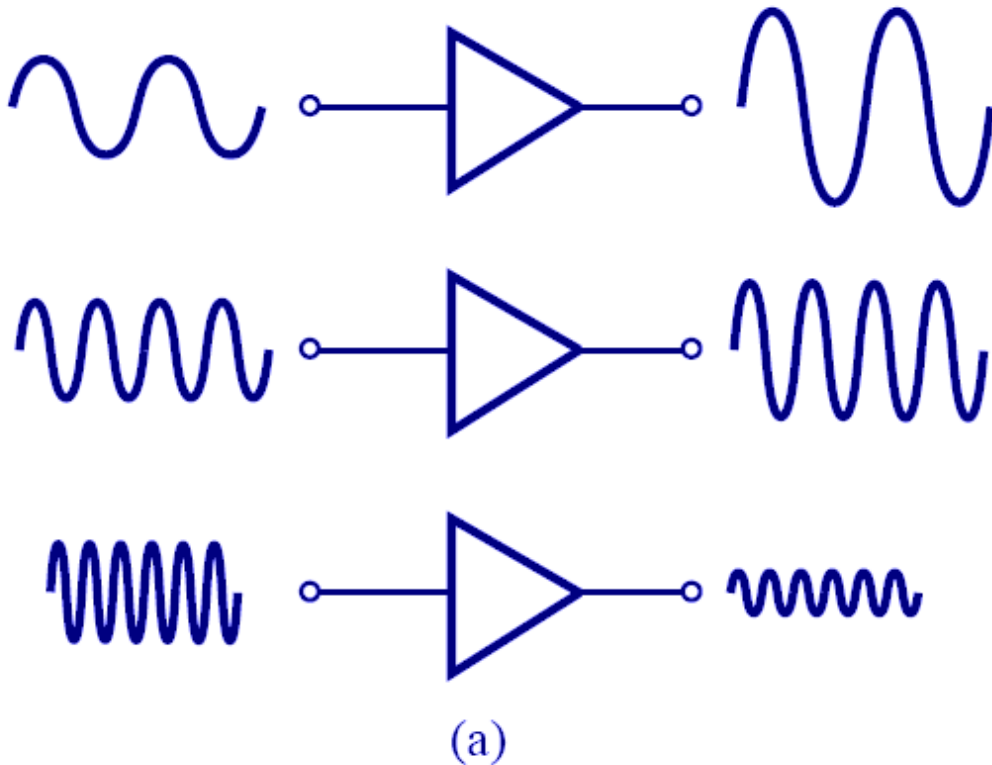
Announcements

- HW5 Due Mar 29
- Exam 2 Mar 31
 - 9:35 – 11:00 (10 extra minutes)
 - Closed book w/ one standard note sheet
 - 8.5"x11" front & back
 - Bring your calculator
 - Emphasis will be on Lectures 4-6
 - Sample Exam2s posted on website
- Reading
 - Razavi Chapter 11

Agenda

- Frequency Response Concepts
- High-Frequency Models of Transistors
- Frequency Response Analysis Procedure
- CE and CS Stages
- CB and CG Stages
- CC and CD (Follower) Stages
- Cascode Stages
- Differential Pairs
- Additional Examples

High Frequency Roll-off of Amplifier



- As frequency of operation increases, the amplifier gain decreases
- This lecture analyzes this frequency response issue

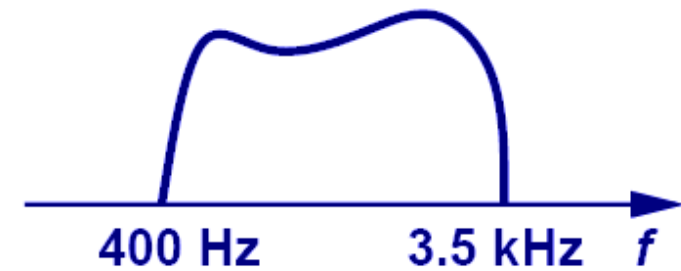
Example: Human Voice I

Natural Voice



(a)

Telephone System

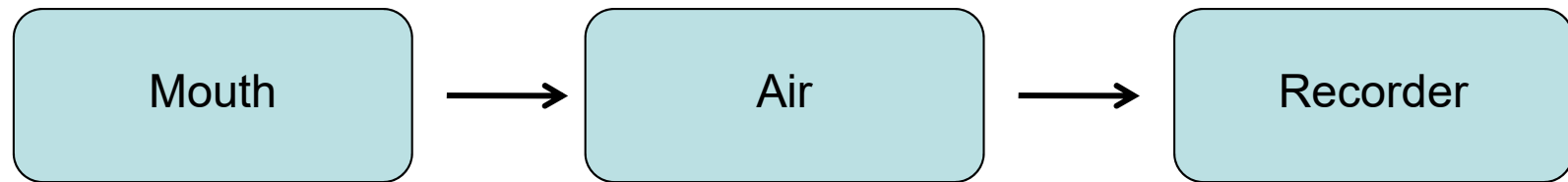


(b)

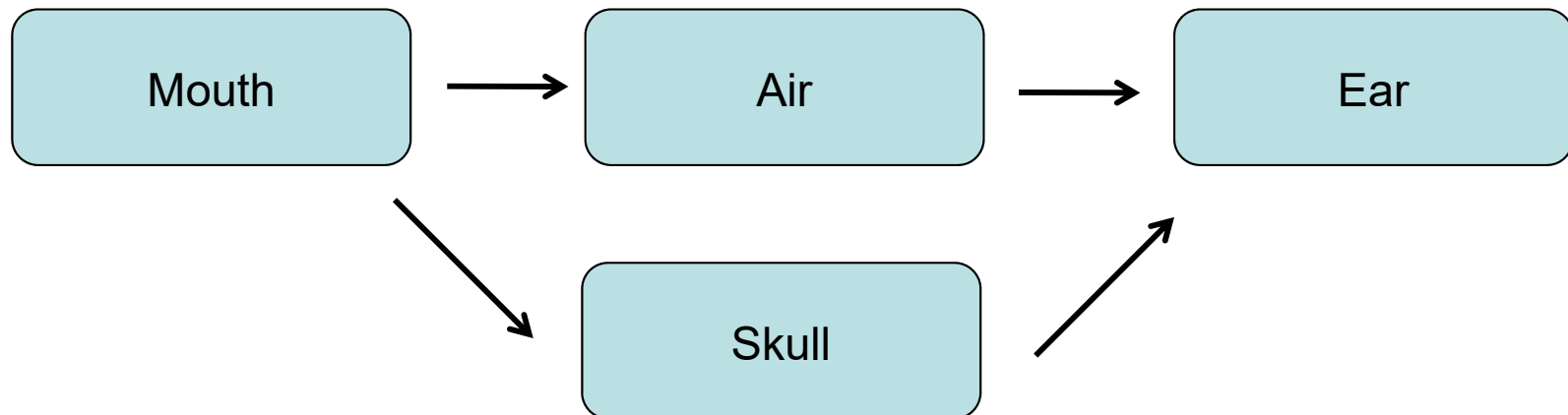
- Natural human voice spans a frequency range from 20Hz to 20KHz, however conventional telephone system passes frequencies from 400Hz to 3.5KHz. Therefore phone conversation differs from face-to-face conversation.

Example: Human Voice II

Path traveled by the human voice to the voice recorder

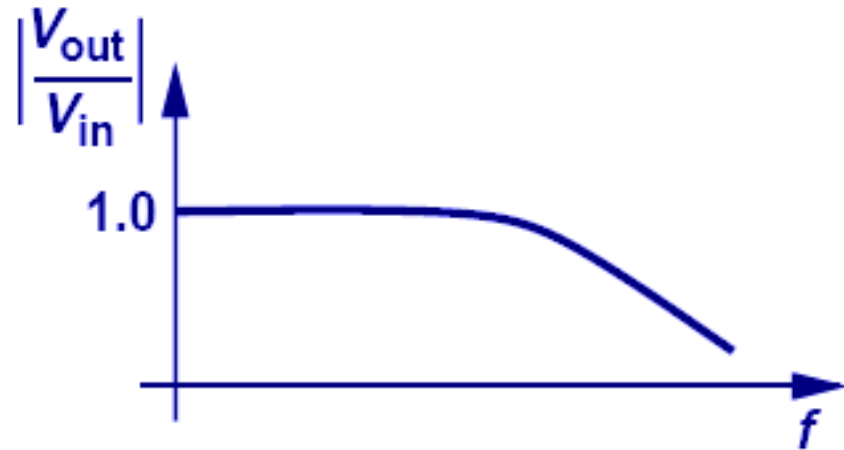
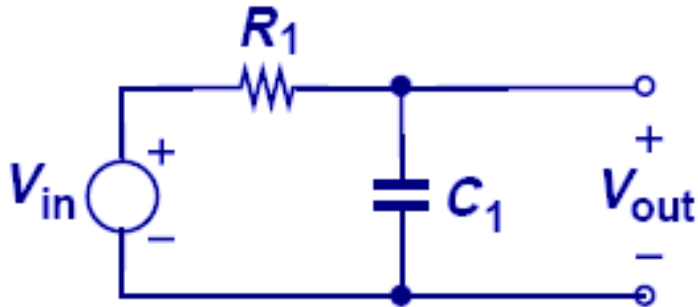


Path traveled by the human voice to the human ear



➤ **Since the paths are different, the results will also be different.**

Gain Roll-off: Simple Low-pass Filter



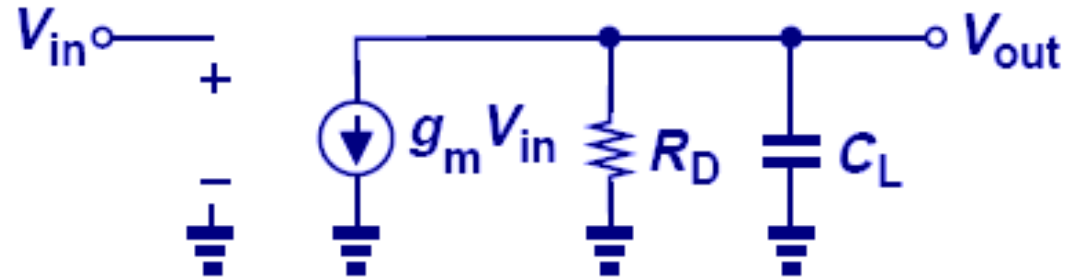
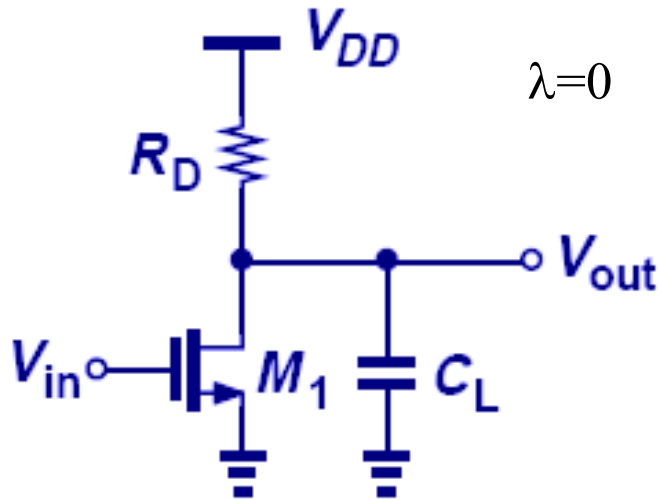
$$V_o(s) = \frac{Z_C}{Z_R + Z_C} V_{in}(s) = \frac{\frac{1}{sC}}{R + \frac{1}{sC}} V_{in}(s) = \frac{1}{1 + sRC} V_{in}(s) \quad \rightarrow \quad H(s) = \frac{V_o(s)}{V_{in}(s)} = \frac{1}{1 + sRC}$$

for sinusoidal steady - state response $s = j\omega$

$$H(j\omega) = \frac{1}{1 + j\omega RC}$$

- In this simple example, as frequency increases the impedance of C_1 decreases and the voltage divider consists of C_1 and R_1 attenuates V_{in} to a greater extent at the output.

Gain Roll-off: Common Source



$$V_{out} = -g_m V_{in} \left(R_D \parallel \frac{1}{C_L s} \right)$$

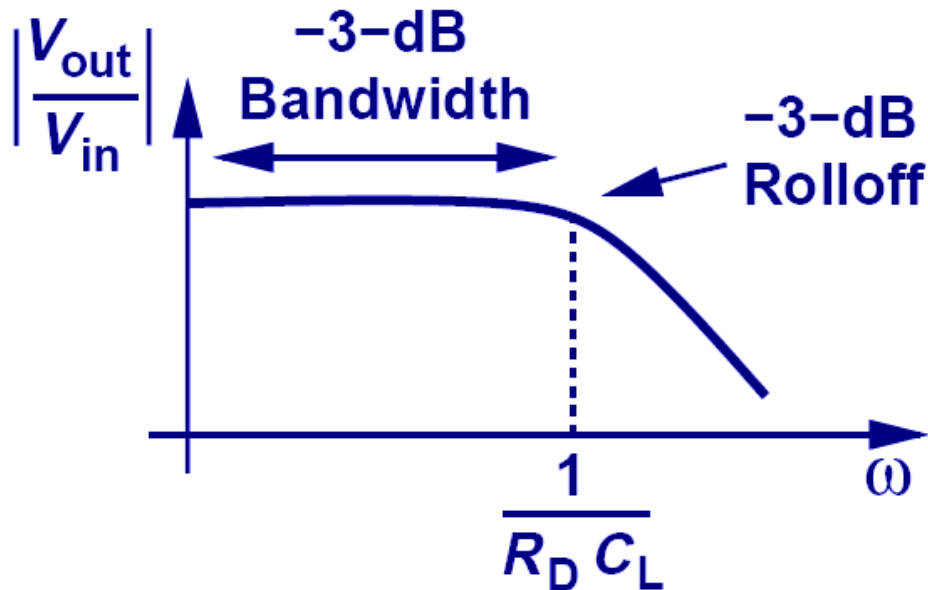
$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{-g_m R_D}{1 + s R_D C_L}$$

This circuit has a pole at

$$|\omega_p| = \frac{1}{R_D C_L}$$

- The capacitive load, C_L , is the culprit for gain roll-off since at high frequency, it will “steal” away some signal current and shunt it to ground.

Frequency Response of the CS Stage



$$\left| \frac{V_{out}}{V_{in}} \right| = \frac{g_m R_D}{\sqrt{R_D^2 C_L^2 \omega^2 + 1}}$$

Recall the Power is proportional to (Voltage)²

To find the half - power (-3dB) point relative to the low - frequency gain

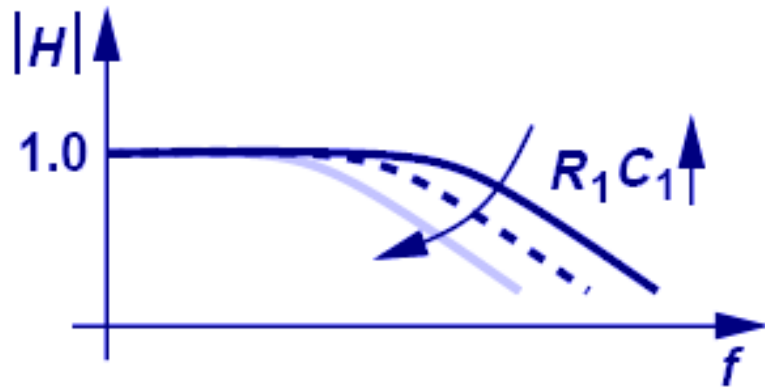
$$\left| \frac{V_{out}}{V_{in}} \right|^2 = \frac{(g_m R_D)^2}{(R_D C_L \omega)^2 + 1} = \frac{(g_m R_D)^2}{2}$$

Solving for ω

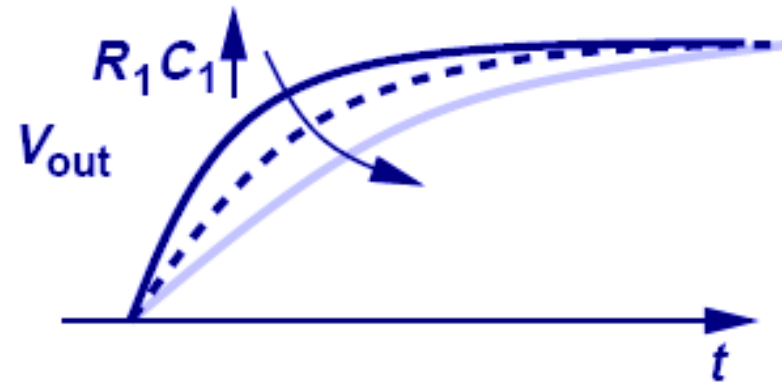
$$\omega = \frac{1}{R_D C_L}$$

- At low frequency, the capacitor is effectively open and the gain is flat. As frequency increases, the capacitor tends to a short and the gain starts to decrease.
- A special frequency is $\omega = 1/(R_D C_L)$, where the gain drops by 3dB (half-power). In this single-pole circuit, this is also the pole frequency.

Example: Relationship between Frequency Response and Step Response



(a)



(b)

$$\left| H(s = j\omega) \right| = \frac{1}{\sqrt{R_1^2 C_1^2 \omega^2 + 1}}$$

$$V_{out}(t) = V_0 \left(1 - \exp\left(\frac{-t}{R_1 C_1}\right) \right) u(t)$$

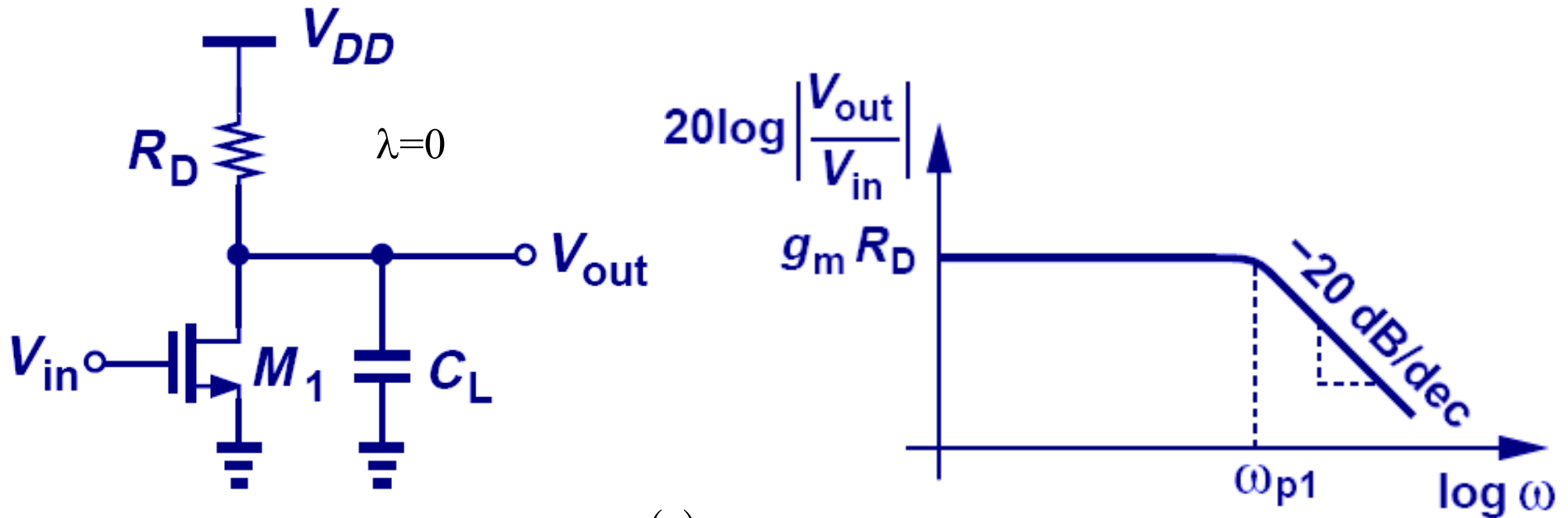
➤ The relationship is such that as $R_1 C_1$ increases, the bandwidth *drops* and the step response becomes *slower*.

Bode Plot

$$H(s) = A_0 \frac{\left(1 + \frac{s}{\omega_{z1}}\right) \left(1 + \frac{s}{\omega_{z2}}\right) \dots}{\left(1 + \frac{s}{\omega_{p1}}\right) \left(1 + \frac{s}{\omega_{p2}}\right) \dots}$$

- When we hit a zero, ω_{zj} , the Bode magnitude rises with a slope of +20dB/dec.
- When we hit a pole, ω_{pj} , the Bode magnitude falls with a slope of -20dB/dec

Example: Bode Plot



$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{-g_m R_D}{1 + s R_D C_L}$$

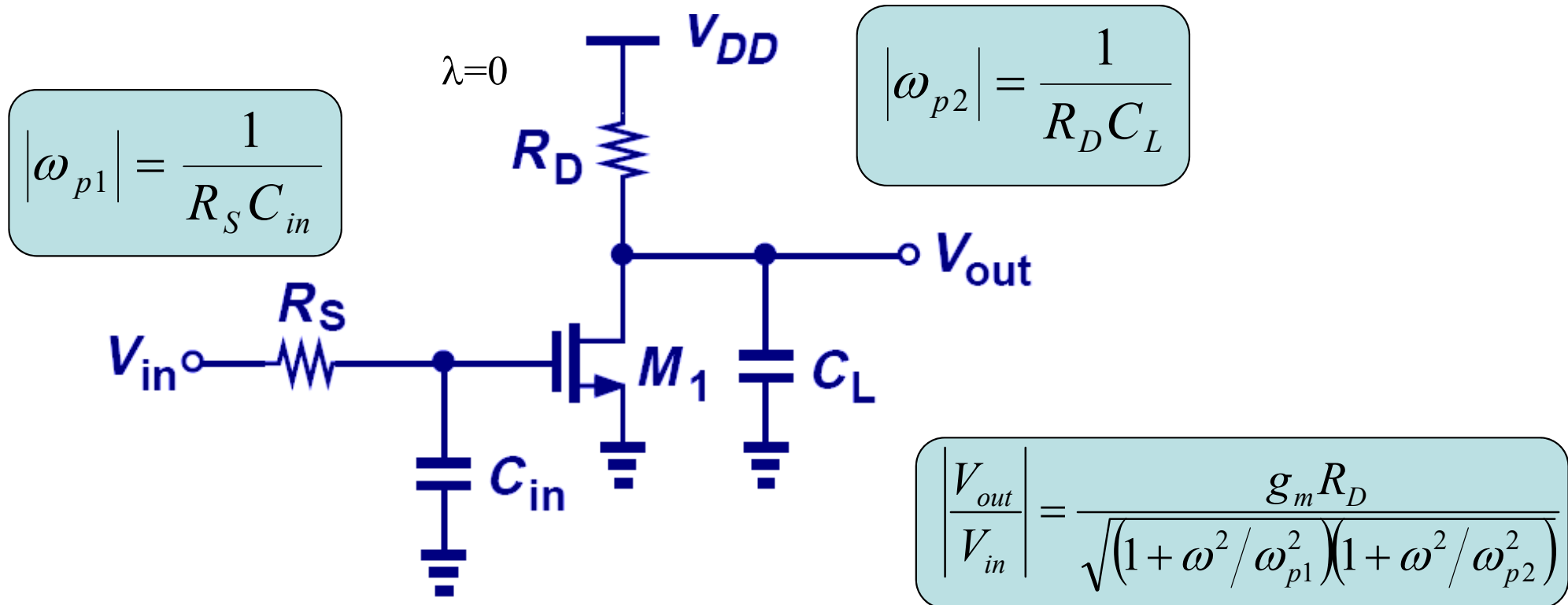
This circuit has a pole at

$$|\omega_p| = \frac{1}{R_D C_L}$$

- The circuit only has one pole (no zero) at $1/(R_D C_L)$, so the slope drops from 0 to -20 dB/dec as we pass ω_{p1} .

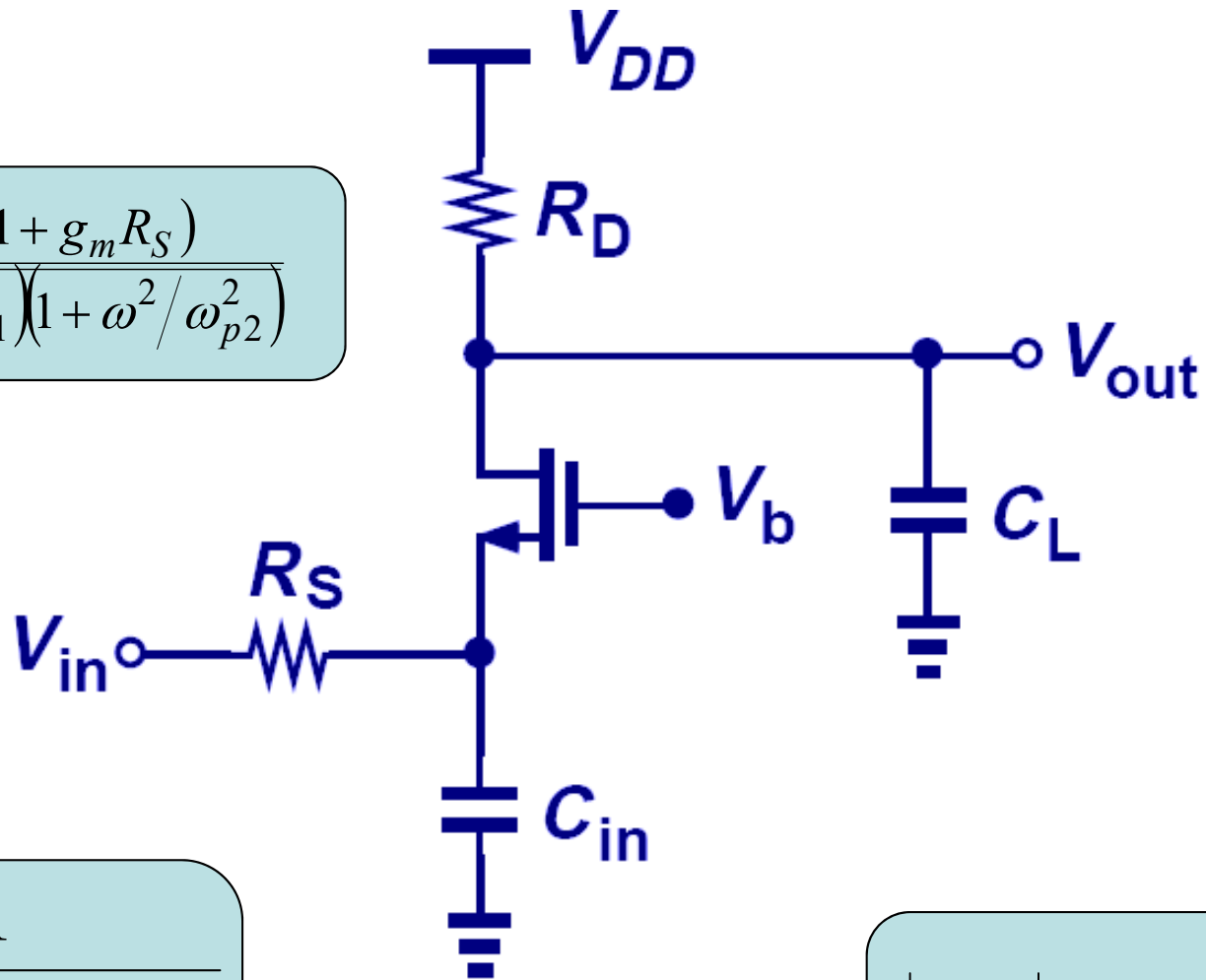
Pole Identification Example I

- Circuit transfer functions can be well approximated by considering that if a node in the signal path has a small-signal resistance R_j and capacitance C_j in parallel to an AC ground, then it contributes a pole of magnitude $(R_j C_j)^{-1}$



Pole Identification Example II

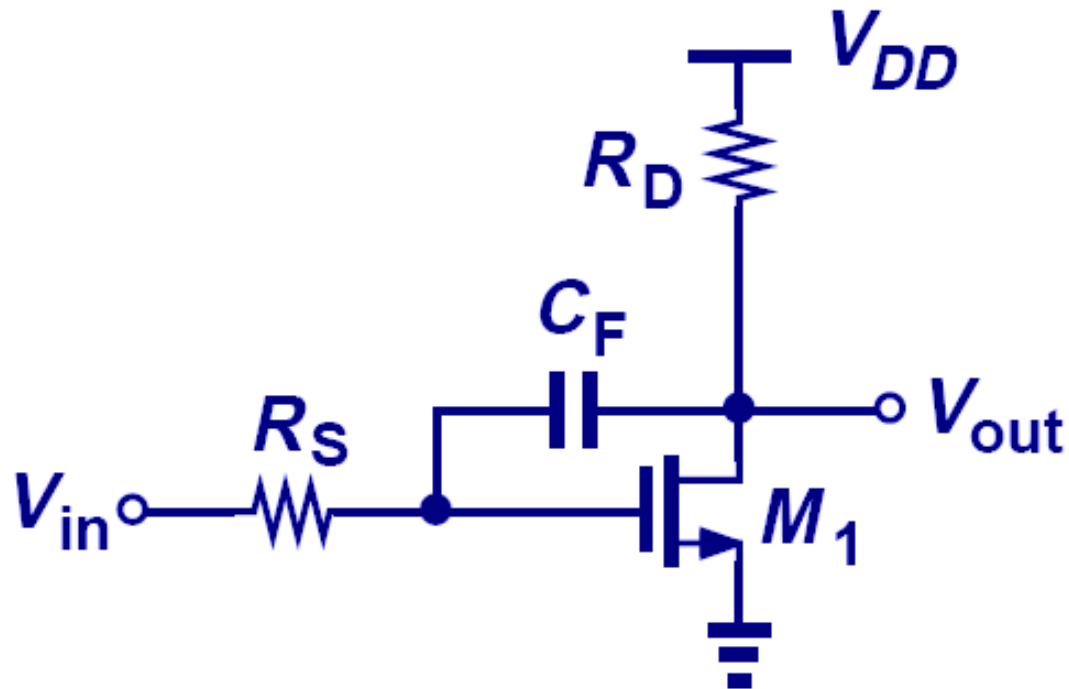
$$\left| \frac{V_{out}}{V_{in}} \right| = \frac{g_m R_D / (1 + g_m R_S)}{\sqrt{\left(1 + \omega^2 / \omega_{p1}^2\right) \left(1 + \omega^2 / \omega_{p2}^2\right)}}$$



$$\left| \omega_{p1} \right| = \frac{1}{\left(R_S \parallel \frac{1}{g_m} \right) C_{in}}$$

$$\left| \omega_{p2} \right| = \frac{1}{R_D C_L}$$

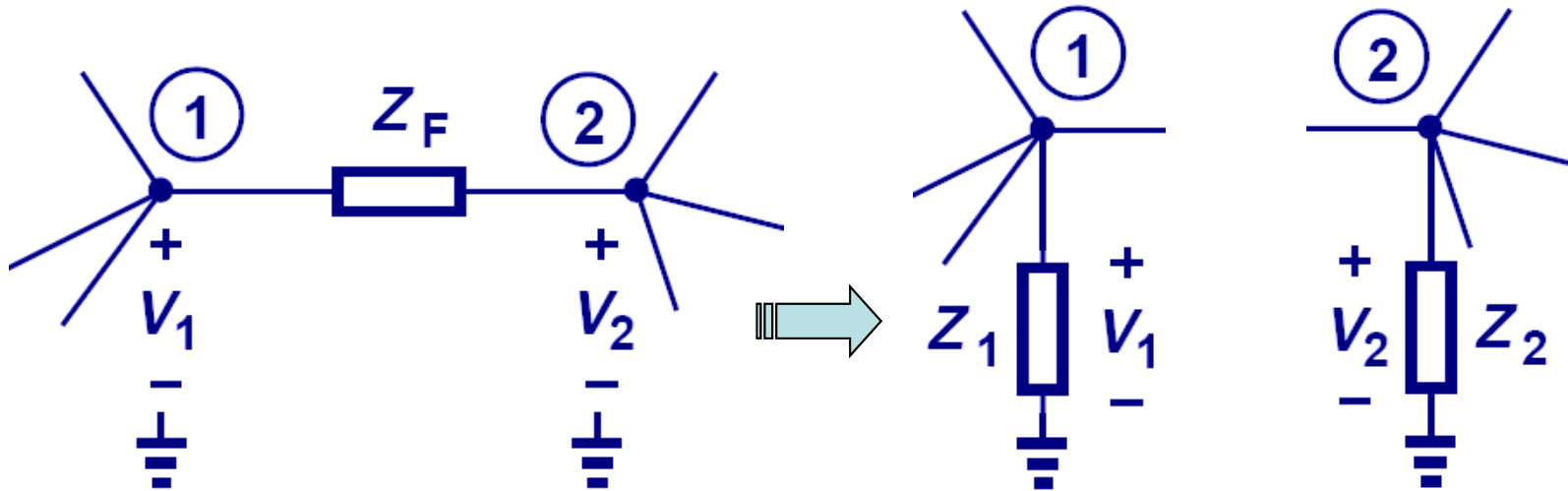
Circuit with Floating Capacitor



- The pole of a circuit is computed by finding the effective resistance and capacitance from a node to GROUND.
- The circuit above creates a problem since neither terminal of C_F is grounded.
- While we could always derive the transfer function from the small-signal model, there is a useful “Miller’s Theorem” which can be used to approximate the circuit’s poles

Miller's Theorem

➤ If A_v is the gain from node 1 to 2, then a floating impedance Z_F can be converted to two grounded impedances Z_1 and Z_2 .



I_1 should be the same in both circuits

$$I_1 = \frac{V_1 - V_2}{Z_F} = \frac{V_1}{Z_1}$$

$$Z_1 = \left(\frac{V_1}{V_1 - V_2} \right) Z_F = \left(\frac{1}{1 - \frac{V_2}{V_1}} \right) Z_F = \frac{Z_F}{1 - A_v}$$

where $A_v = \frac{V_2}{V_1}$

$$Z_1 = \frac{Z_F}{1 - A_v}$$

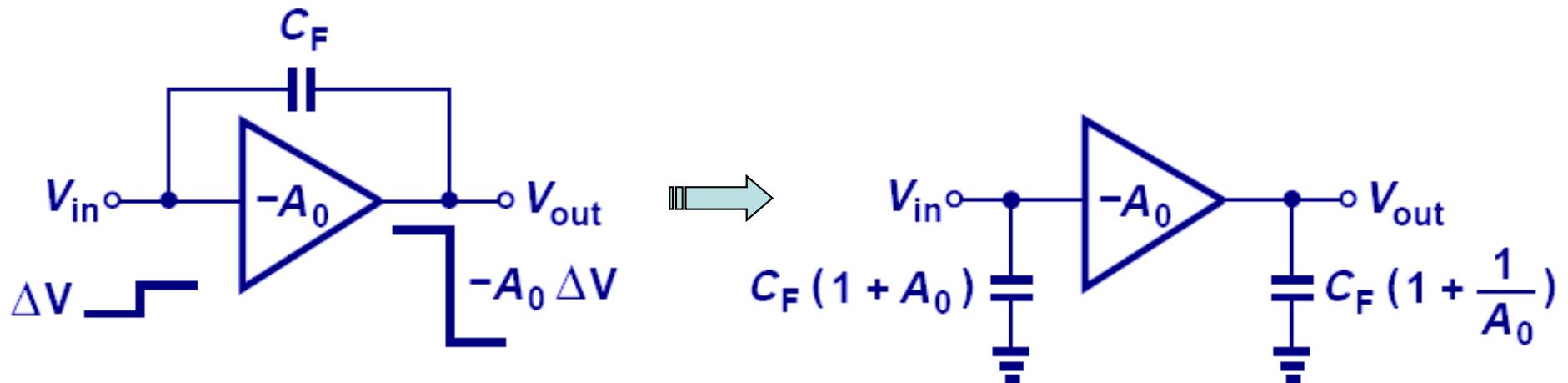
I_2 should be the same in both circuits

$$I_2 = \frac{V_2 - V_1}{Z_F} = \frac{V_2}{Z_2}$$

$$Z_2 = \left(\frac{V_2}{V_2 - V_1} \right) Z_F = \left(\frac{1}{1 - \frac{V_1}{V_2}} \right) Z_F = \frac{Z_F}{1 - \frac{1}{A_v}}$$

$$Z_2 = \frac{Z_F}{1 - 1/A_v}$$

Miller Multiplication



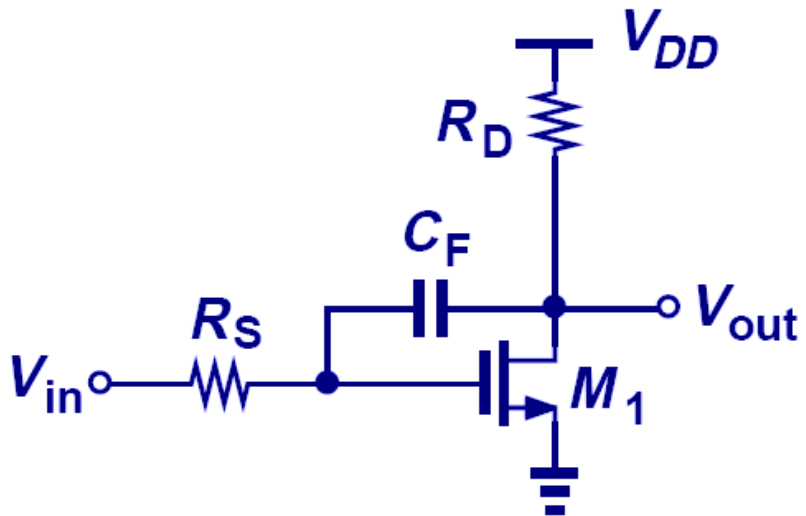
$$Z_{in} = \frac{1}{j\omega C_F (1 - A_v)} = \frac{1}{j\omega C_F (1 - (-A_o))} = \frac{1}{j\omega C_F (1 + A_o)}$$

Equivalent to an input cap that is the original C_F multiplied by $(1 + A_o)$

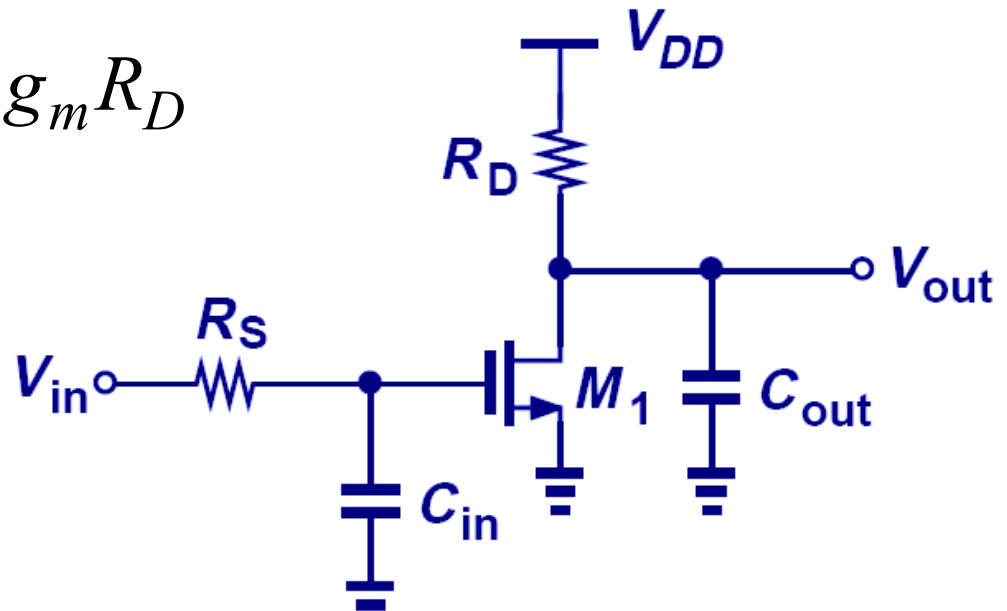
Following a similar procedure, the output cap is the original C_F multiplied by $\left(1 + \frac{1}{A_o}\right)$

➤ **With Miller's theorem, we can separate the floating capacitor. However, the input capacitor is larger than the original floating capacitor. We call this Miller multiplication.**

Example: Miller Theorem



$$A_v = -g_m R_D$$



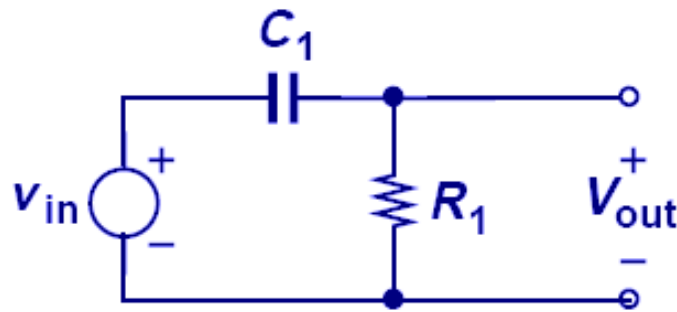
$$\omega_{in} = \frac{1}{R_S (1 + g_m R_D) C_F}$$

$$\omega_{out} = \frac{1}{R_D \left(1 + \frac{1}{g_m R_D} \right) C_F}$$

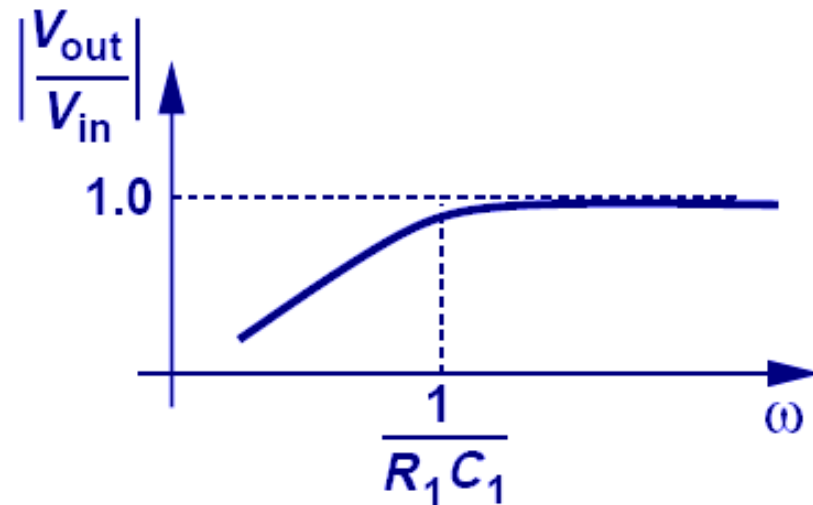
- Note, this is only a (often good) approximation of the transfer function
 - Uses only the low-frequency gain
 - Neglects a zero

$$\left| \frac{V_{out}}{V_{in}} \right| \approx \frac{g_m R_D}{\sqrt{\left(1 + \omega^2 / \omega_{in}^2 \right) \left(1 + \omega^2 / \omega_{out}^2 \right)}}$$

High-Pass Filter Response



(a)



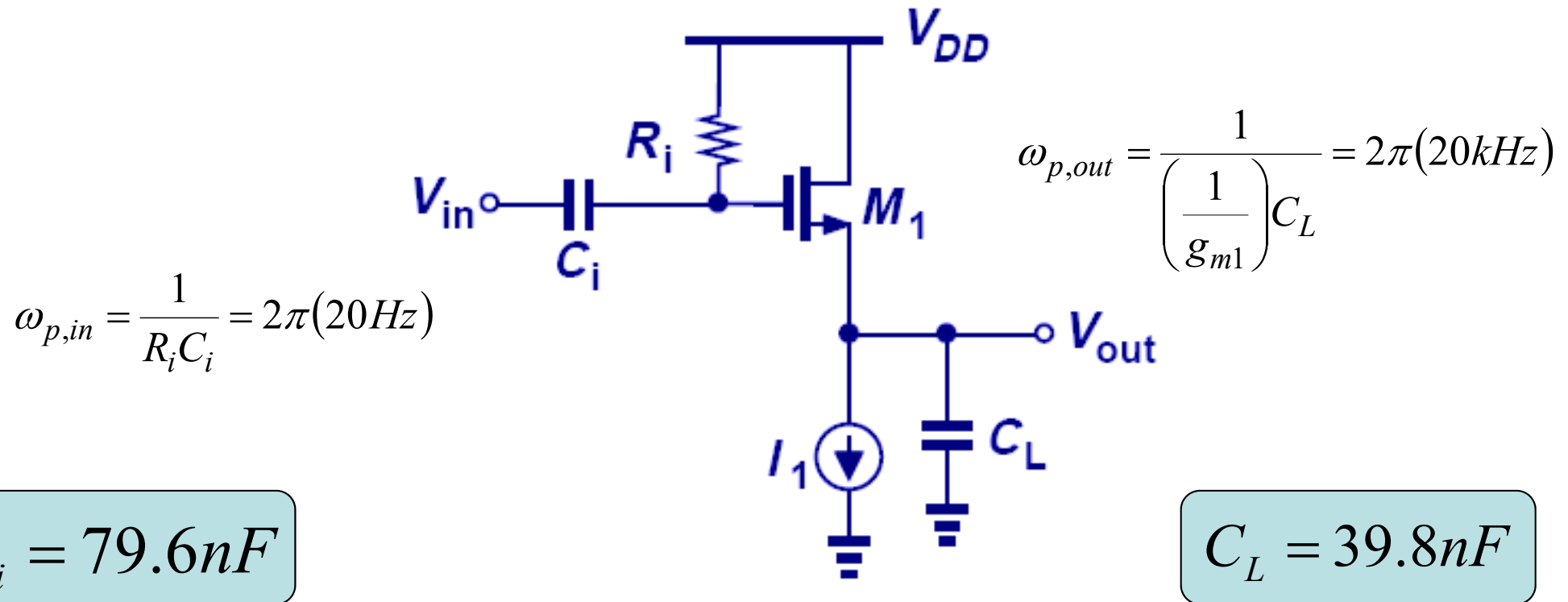
(b)

$$V_o(s) = \frac{Z_{R_1}}{Z_{R_1} + Z_{C_1}} V_{in}(s) = \frac{R_1}{R_1 + \frac{1}{sC_1}} V_{in}(s) = \frac{sR_1C_1}{1 + sR_1C_1} V_{in}(s)$$

$$\left| \frac{V_{out}}{V_{in}} \right| = \frac{R_1 C_1 \omega}{\sqrt{R_1^2 C_1^2 \omega^2 + 1}}$$

➤ The voltage division between a resistor and a capacitor can be configured such that the gain at low frequency is reduced.

Example: Audio Amplifier



$$R_i = 100\text{K}\Omega$$

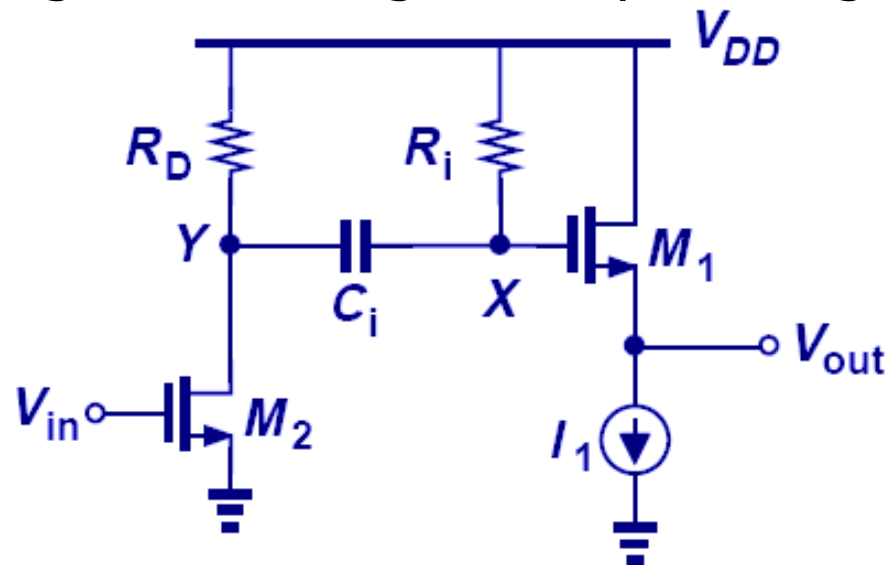
$$g_m = 1/200\Omega$$

- In order to successfully pass audio band frequencies (20 Hz-20 KHz), large input and output capacitances are needed.

Capacitive Coupling vs. Direct Coupling

- Capacitive coupling, also known as AC coupling, passes AC signals from Y to X while blocking DC contents.
- This technique allows independent bias conditions between stages. Direct coupling does not.

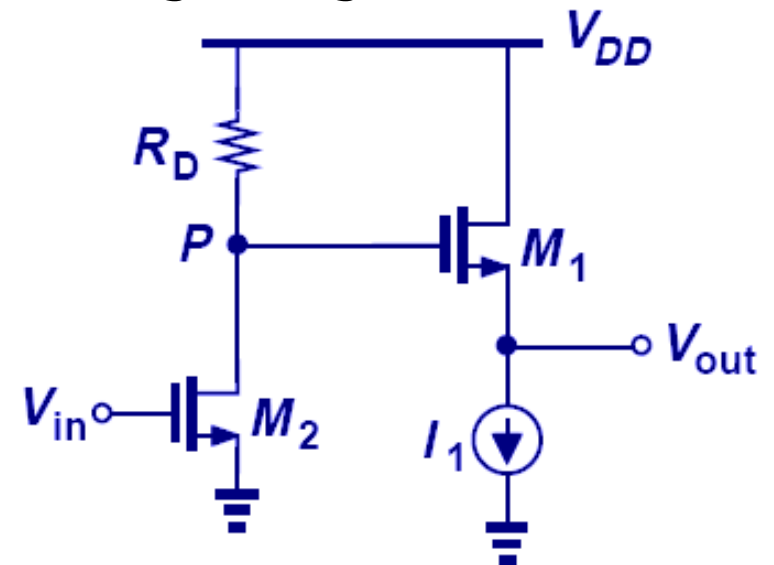
Allows for high $V(R_D)$ (gain), while also allowing a high output stage gate bias for good output swing



(a)

Capacitive Coupling

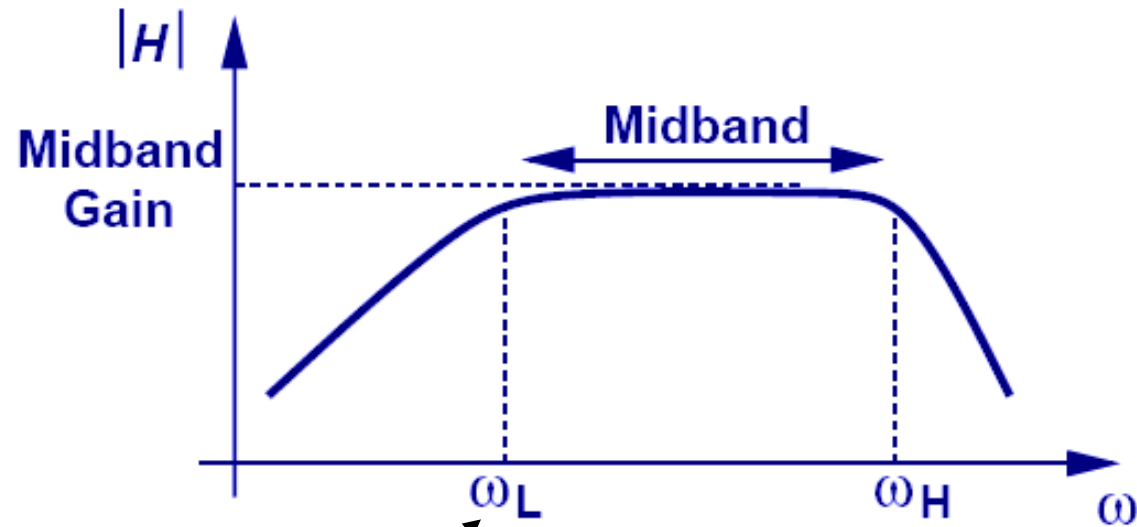
Due to direct coupling, must trade-off A_{V_1} for output stage biasing/swing



(b)

Direct Coupling

Typical Frequency Response



Lower Corner

Often due to
AC coupling

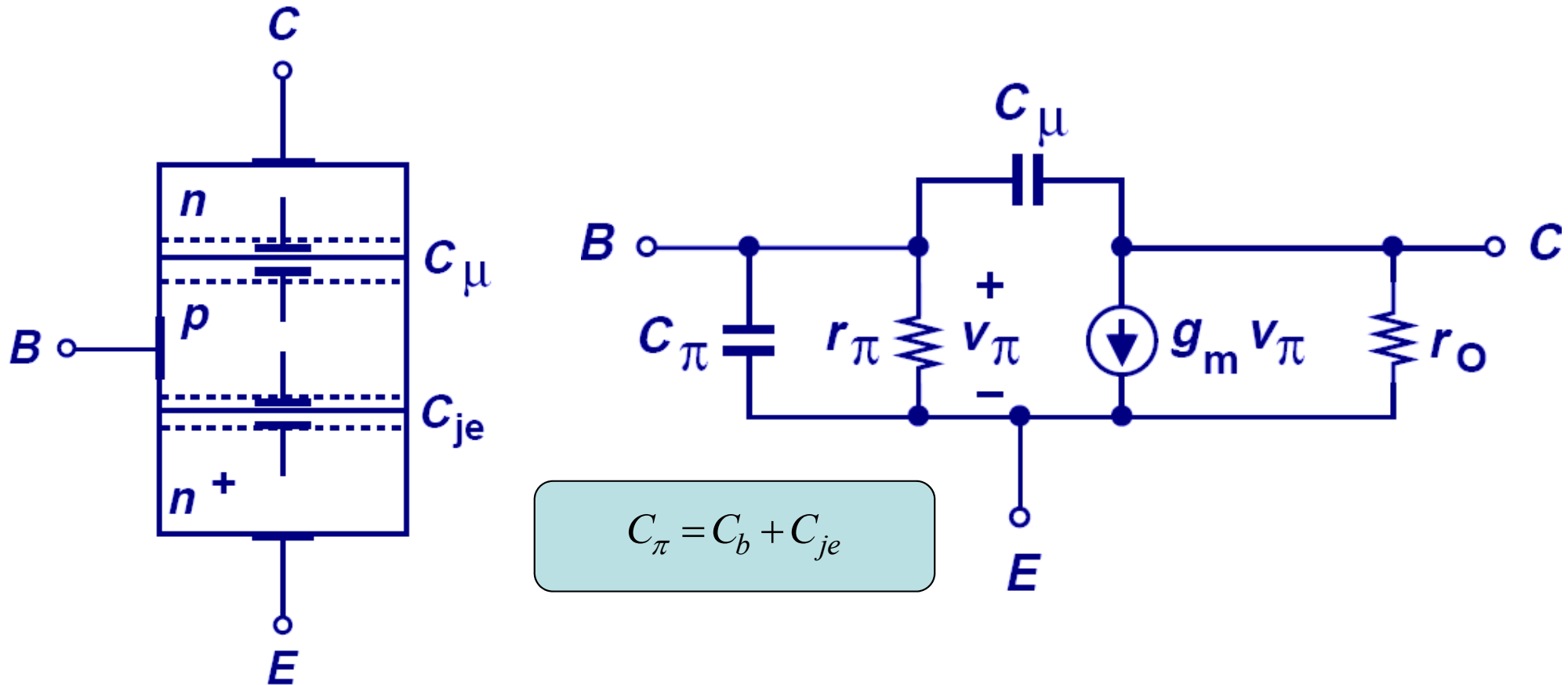
Upper Corner

Often due to
load/parasitic capacitors

Agenda

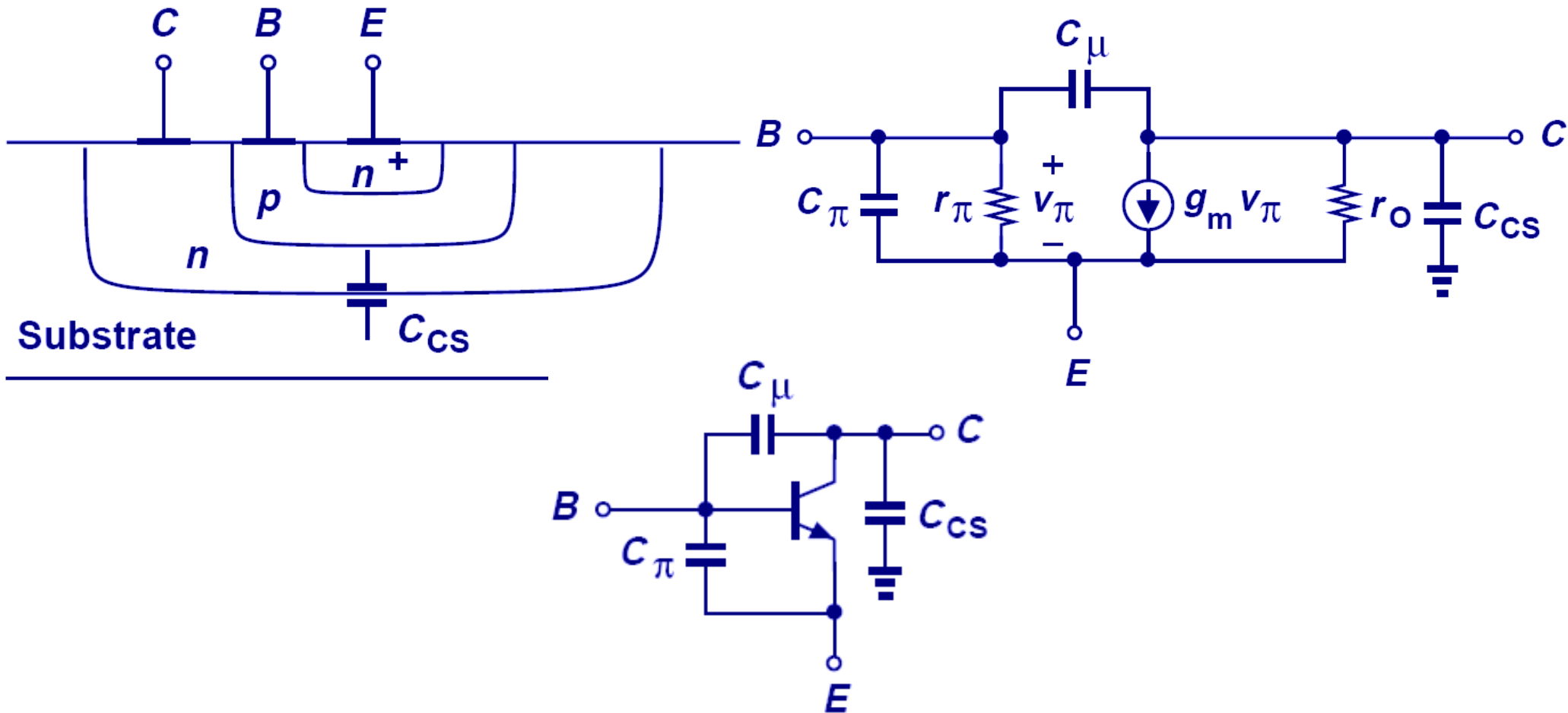
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High-Frequency Bipolar Model



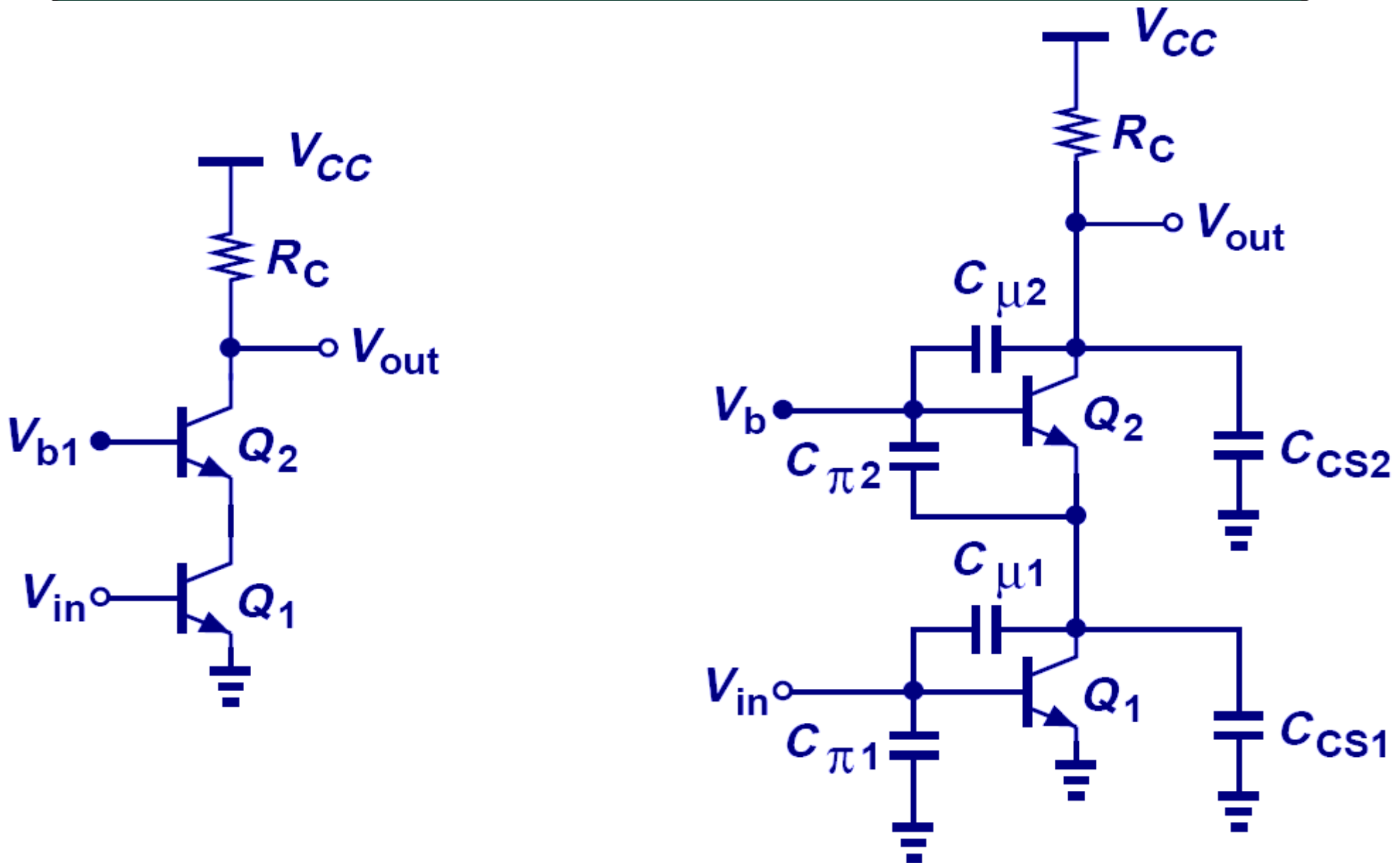
- At high frequency, capacitive effects come into play
- C_{μ} and C_{je} are the junction capacitances
- C_b represents the base charge to generate the non-uniform charge profile required for proper operation (Chapter 4)

High-Frequency Model of Integrated Bipolar Transistor

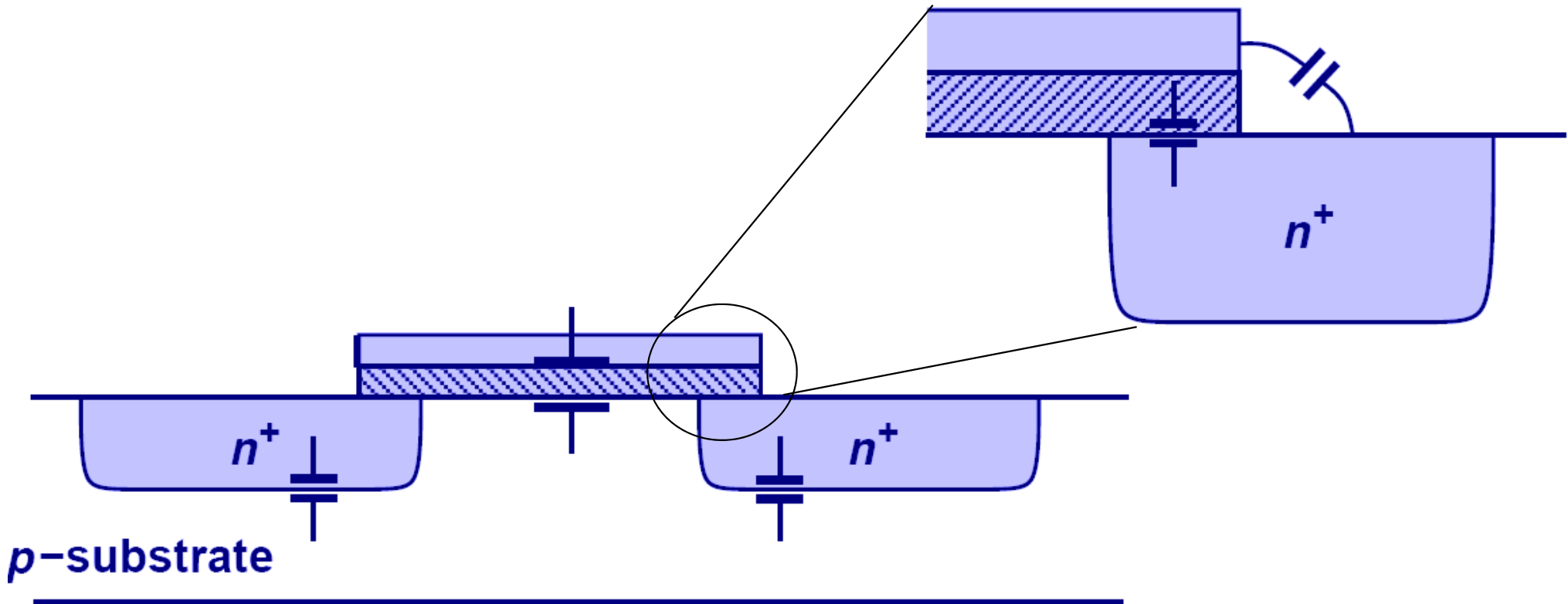


- Since an integrated bipolar circuit is fabricated on top of a substrate, another junction capacitance exists between the collector and substrate, namely C_{cs} .

Example: Capacitance Identification

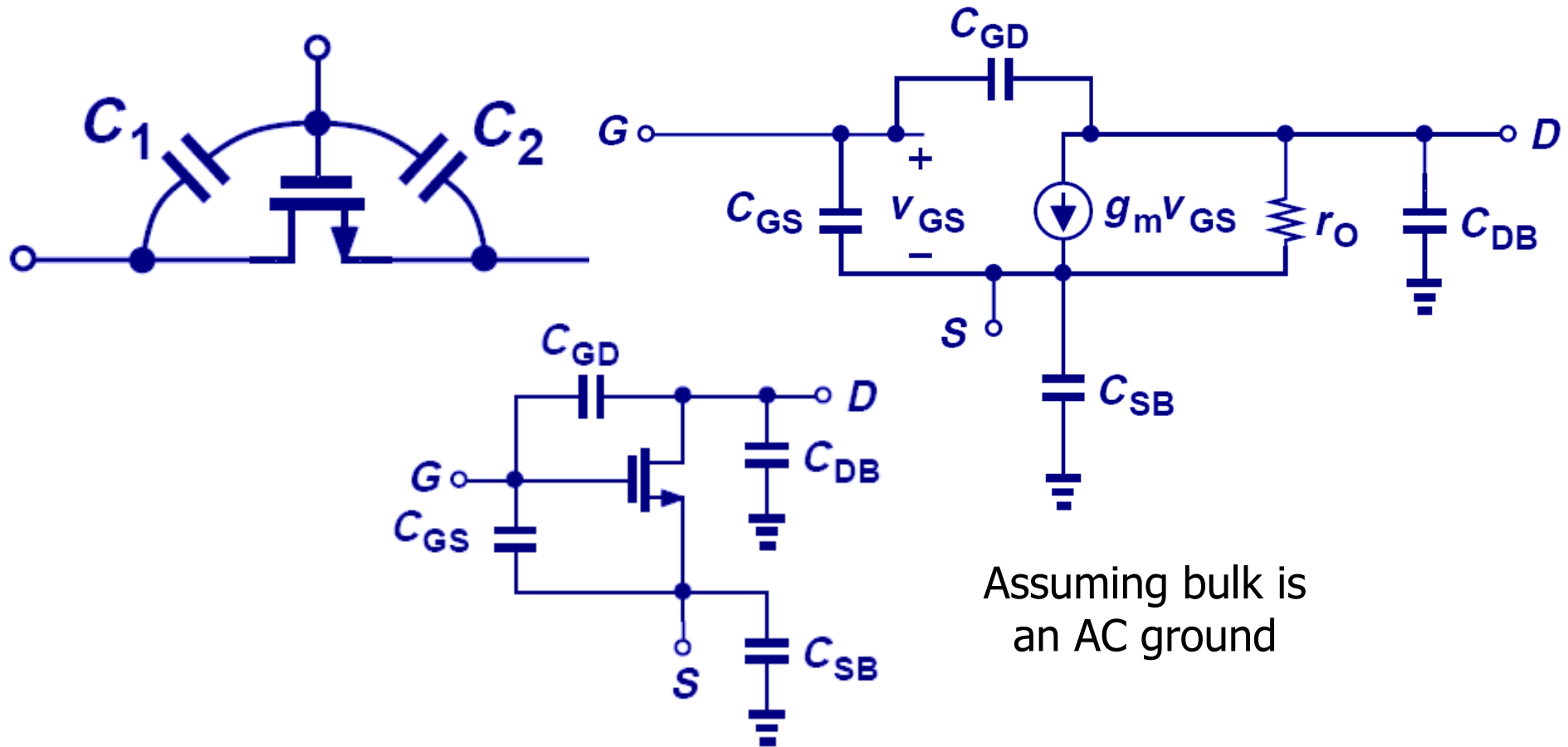


MOS Intrinsic Capacitances



- For a MOS, there exist oxide capacitance from gate to channel, junction capacitances from source/drain to substrate, and overlap capacitance from gate to source/drain.

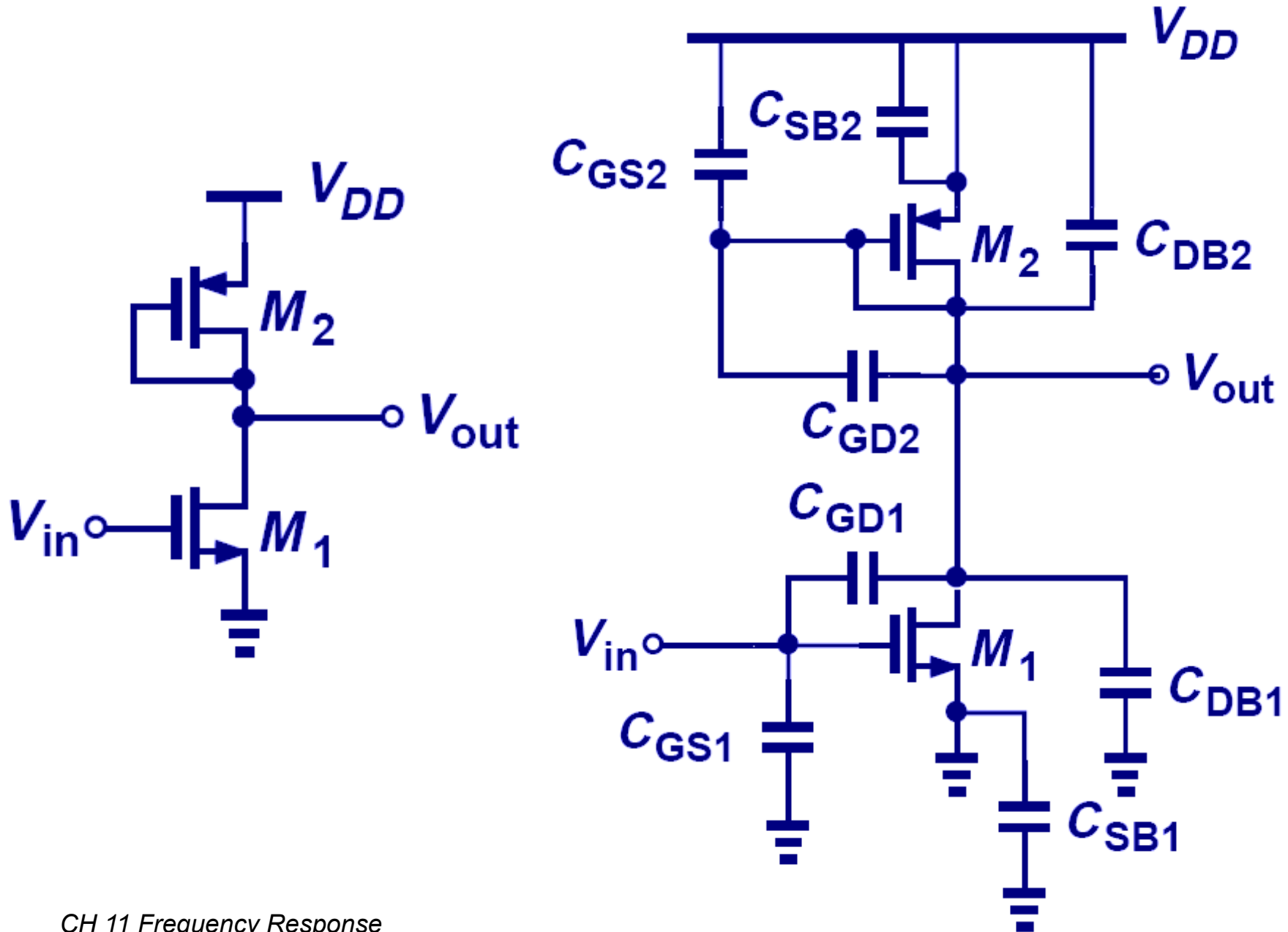
Gate Oxide Capacitance Partition and Full Model



Assuming bulk is an AC ground

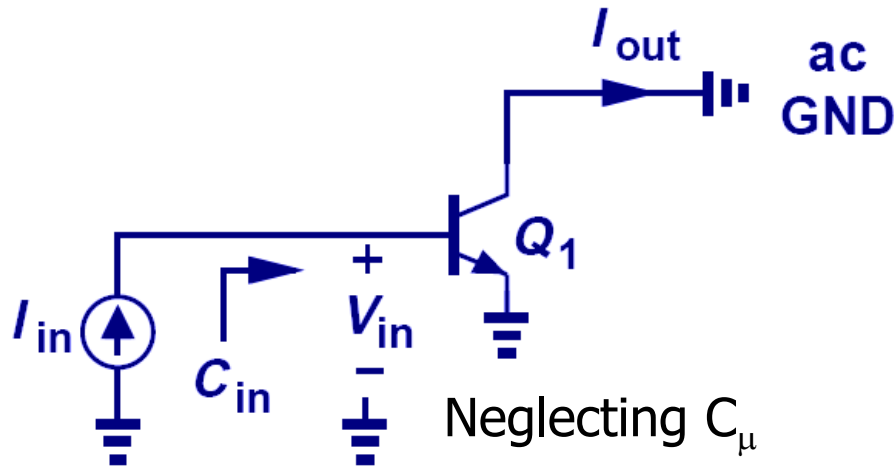
- The gate oxide capacitance is often partitioned between source and drain. In saturation, $C_2 \sim C_{\text{gate}}$, and $C_1 \sim 0$. They are in parallel with the overlap capacitance to form C_{GS} and C_{GD} .

Example: Capacitance Identification



Transit Frequency

- Transit frequency, f_T , is defined as the frequency where the current gain from input to output drops to 1.



$$I_{out} = g_m V_{in} = g_m I_{in} Z_{in}$$

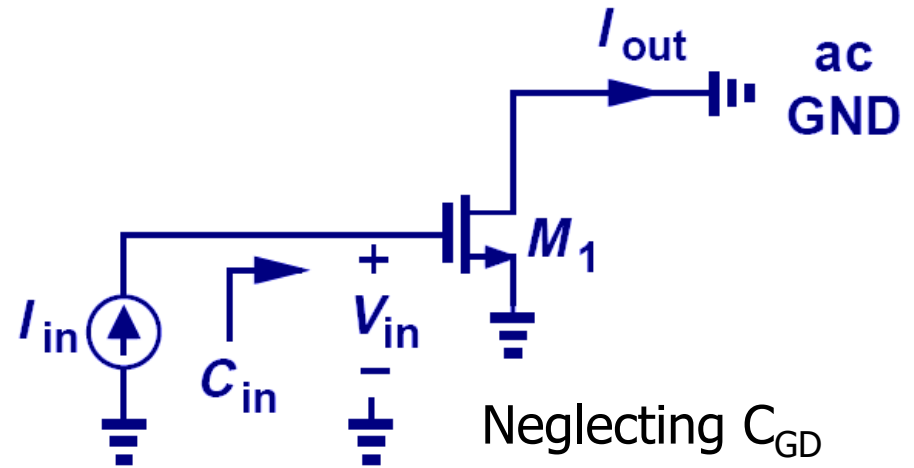
$$Z_{in} = \frac{1}{C_{\pi} s} \parallel r_{\pi}$$

$$\frac{I_{out}}{I_{in}} = \frac{g_m r_{\pi}}{r_{\pi} C_{\pi} s + 1} = \frac{\beta}{r_{\pi} C_{\pi} s + 1}$$

Setting the magnitude equal to 1 at ω_T yields

$$r_{\pi}^2 C_{\pi}^2 \omega_T^2 = \beta^2 - 1 \approx \beta^2$$

$$\omega_T \approx \frac{\beta}{r_{\pi} C_{\pi}} = \frac{g_m}{C_{\pi}}$$



$$I_{out} = g_m V_{in} = g_m I_{in} Z_{in}$$

$$Z_{in} = \frac{1}{C_{GS} s}$$

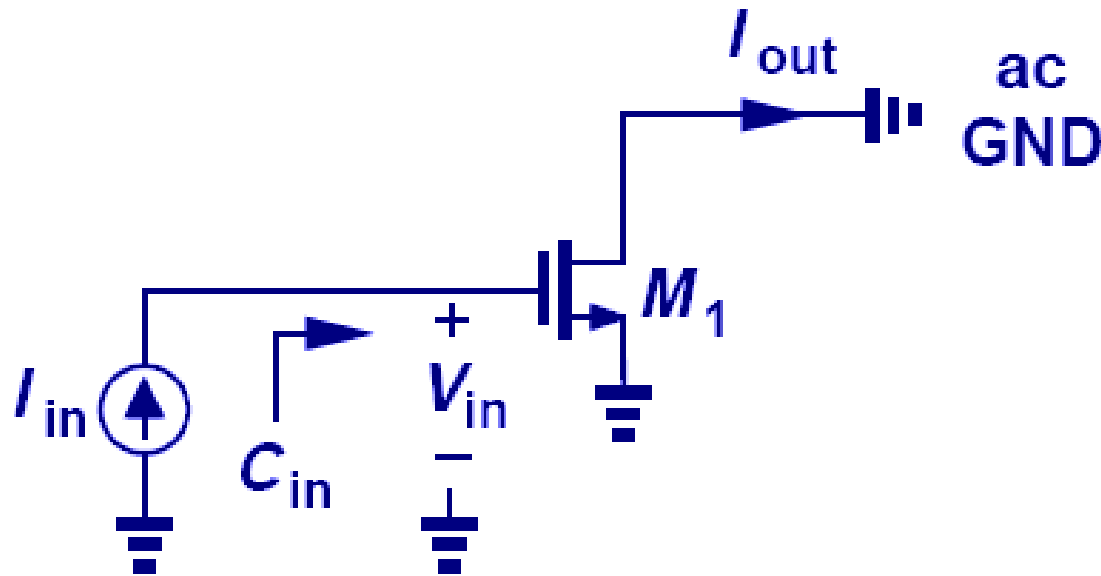
$$\frac{I_{out}}{I_{in}} = \frac{g_m}{C_{GS} s}$$

Setting the magnitude equal to 1 at ω_T yields

$$C_{GS}^2 \omega_T^2 = g_m^2$$

$$\omega_T = \frac{g_m}{C_{GS}}$$

Example: Transit Frequency Calculation



- The transit frequency increases dramatically as the channel length is shrunk, allowing for much faster transistors with CMOS scaling
- Note, this neglects some advanced device physics (carrier velocity saturation) which slows this rate of frequency increase

$$\omega_T = \frac{g_m}{C_{GS}}$$

$$g_m = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})$$

$$C_{GS} = \frac{2}{3} W L C_{ox} \quad (\text{talked about in 474})$$

$$\omega_T = 2\pi f_T = \frac{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})}{\frac{2}{3} W L C_{ox}}$$

$$f_T = \frac{3\mu_n (V_{GS} - V_{TH})}{4\pi L^2}$$

$$L = 65nm$$

$$V_{GS} - V_{TH} = 100mV$$

$$\mu_n = 400cm^2 / (V \cdot s)$$

$$f_T = 226GHz$$

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- **Frequency Response Analysis Procedure**
- CE and CS Stages
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Analysis Summary

- **The frequency response refers to the magnitude of the transfer function.**
- **Bode's approximation simplifies the plotting of the frequency response if poles and zeros are known.**
- **In general, it is possible to associate a pole with each node in the signal path.**
- **Miller's theorem helps to decompose floating capacitors into grounded elements.**
- **Bipolar and MOS devices exhibit various capacitances that limit the speed of circuits.**

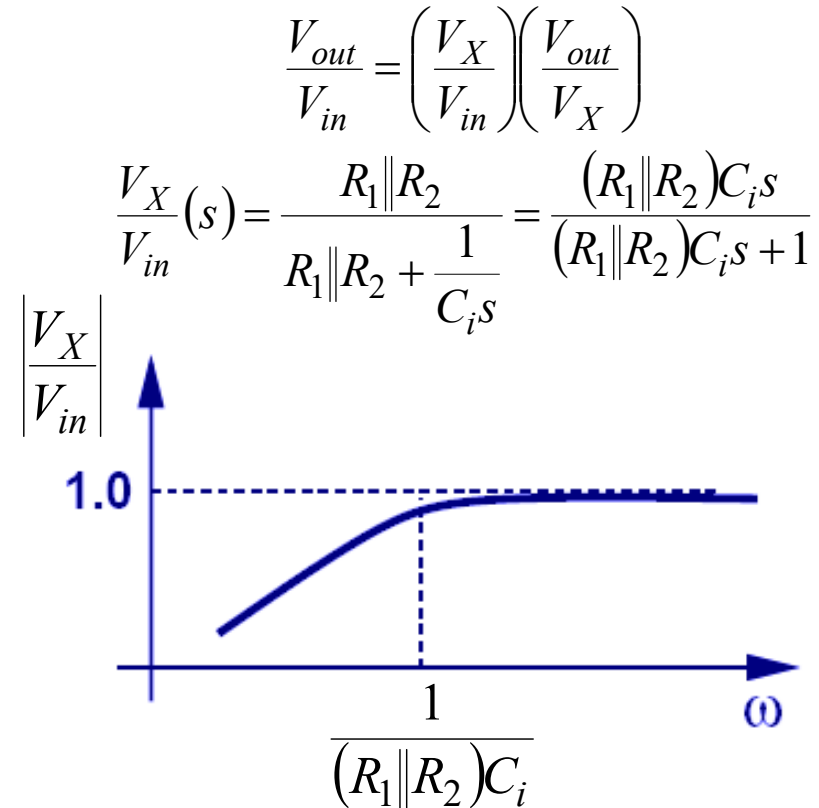
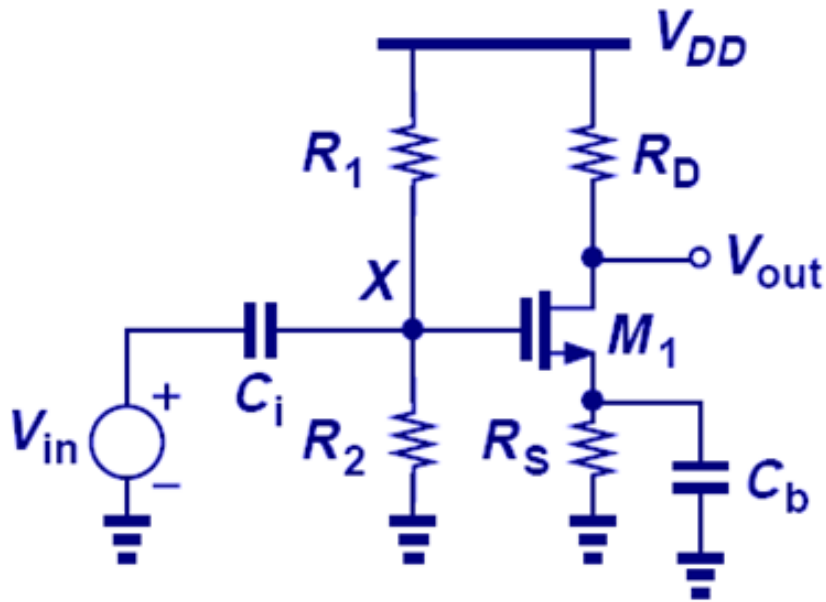
High Frequency Circuit Analysis Procedure

- Determine which capacitor impact the low-frequency region of the response and calculate the low-frequency pole (neglect transistor capacitance).
- Calculate the midband gain by replacing the capacitors with short circuits (neglect transistor capacitance).
- Include transistor capacitances.
- Merge capacitors connected to AC grounds and omit those that play no role in the circuit.
- Determine the high-frequency poles and zeros.
- Plot the frequency response using Bode's rules or exact analysis.

Agenda

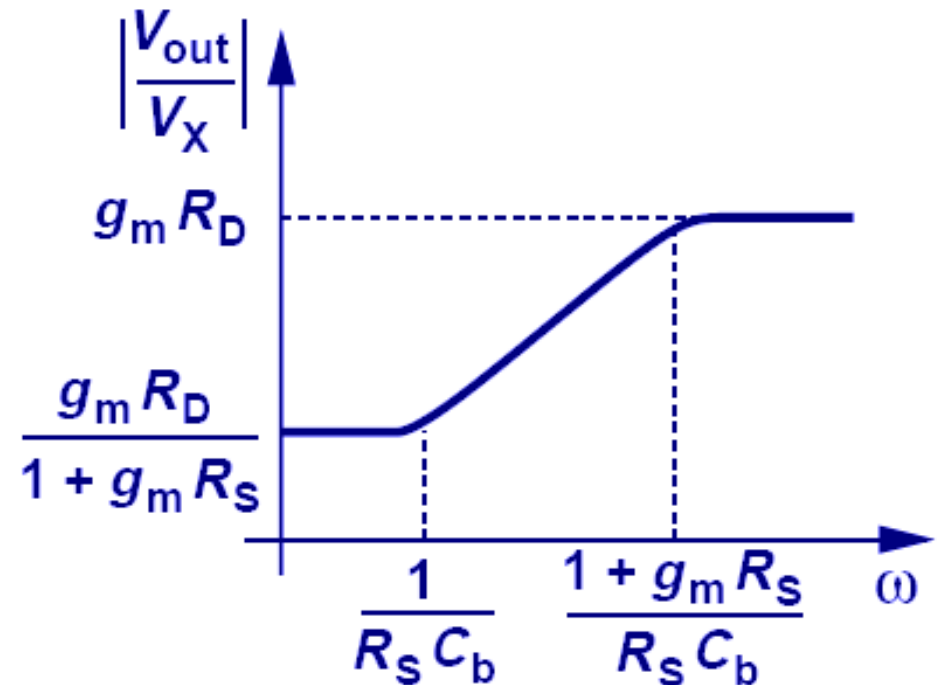
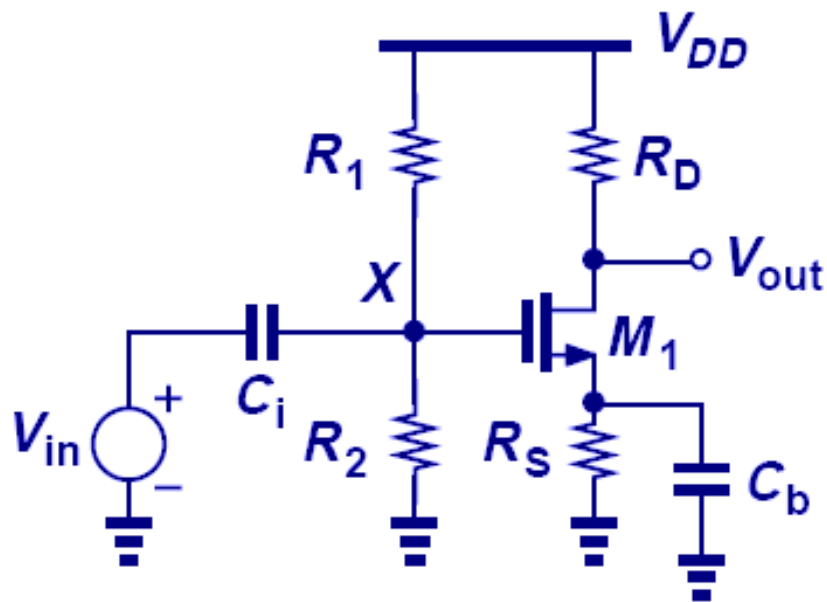
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Frequency Response of CS Stage with Bypassed Degeneration – Input AC Coupling



- The input AC coupling forms a high-pass filter which should be designed for a certain minimum cut-off frequency

Frequency Response of CS Stage with Bypassed Degeneration – Main Amplifier



➤ In order to increase the midband gain, a capacitor C_b is placed in parallel with R_S .

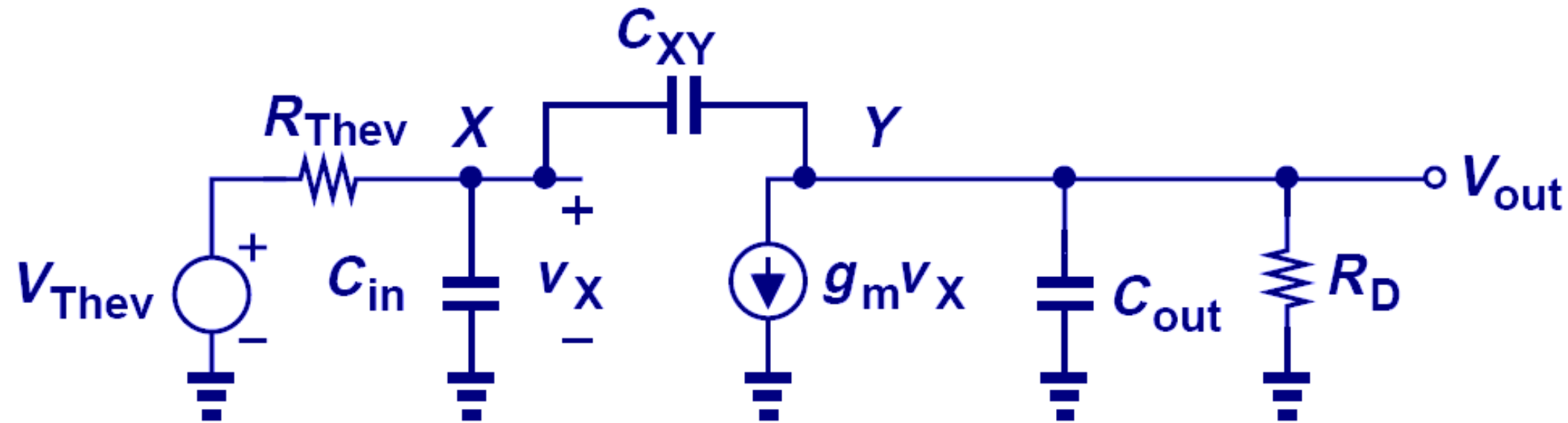
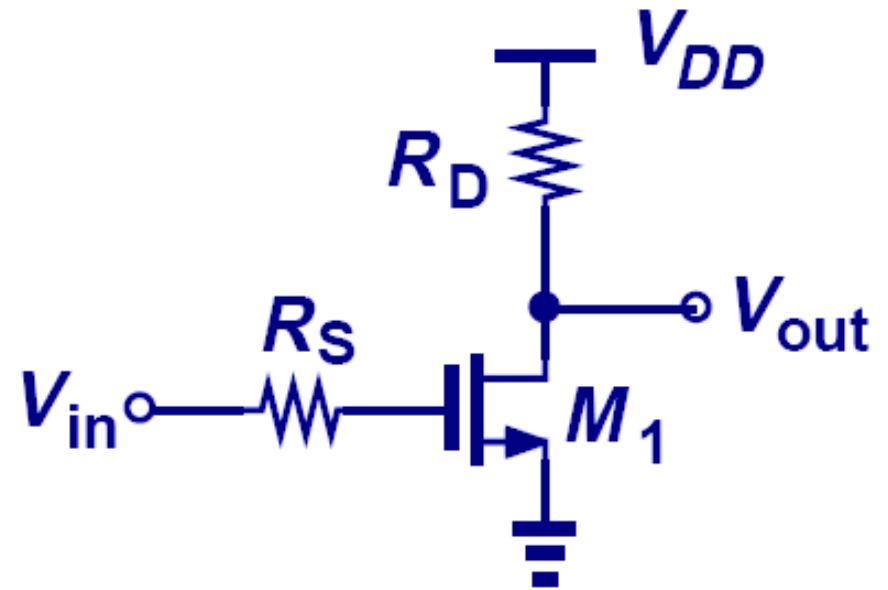
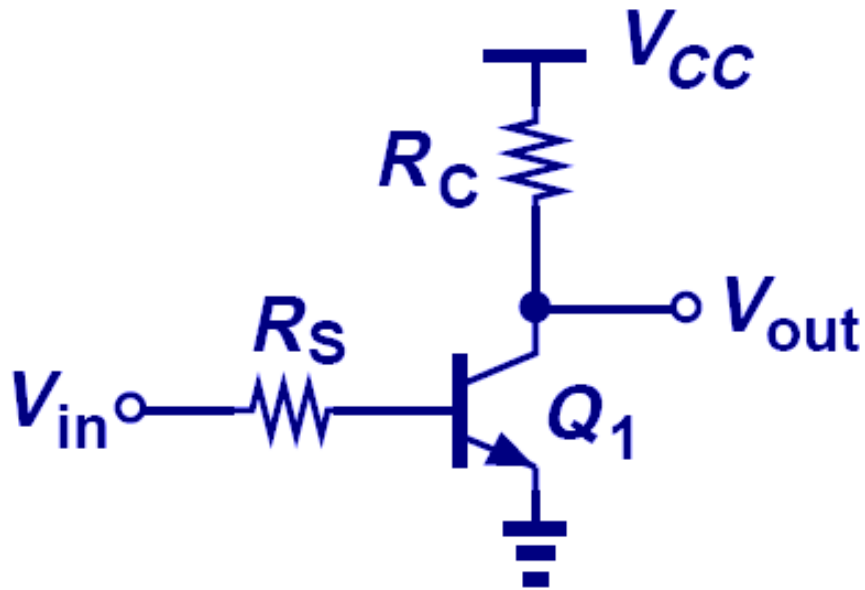
$$\frac{V_{out}}{V_X} = \frac{-R_D}{R_S \parallel \left(\frac{1}{C_b s} + \frac{1}{g_m} \right)} = \frac{-g_m R_D (R_S C_b s + 1)}{R_S C_b s + g_m R_S + 1}$$

The pole frequency

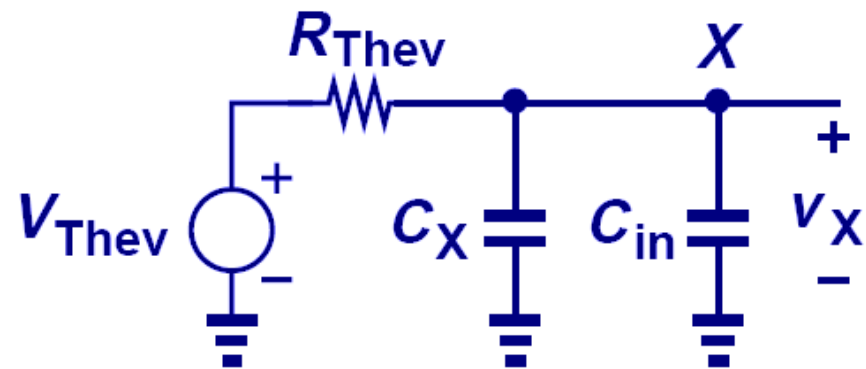
$$|\omega_p| = \frac{1 + g_m R_S}{R_S C_b}$$

should also be designed to set the minimum cut - off frequency

Unified Model for CE and CS Stages



Unified Model Using Miller's Theorem



CE Stage

$$V_{Thev} = V_{in} \frac{r_{\pi}}{r_{\pi} + R_S}$$

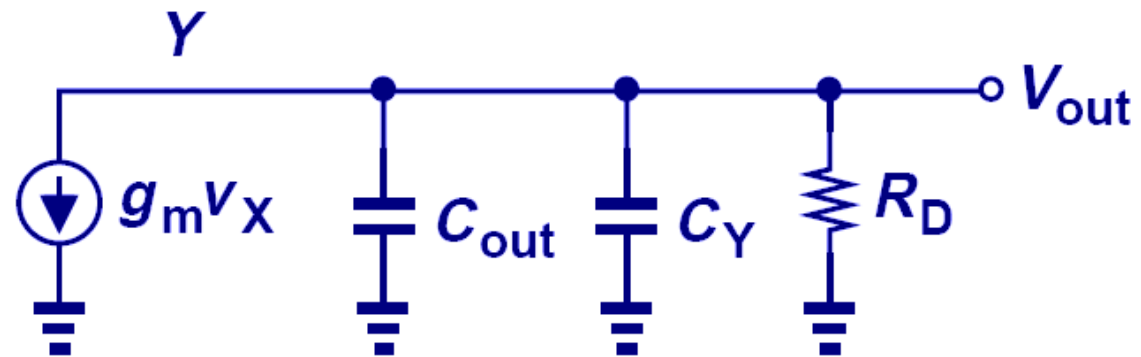
$$R_{Thev} = R_S \parallel r_{\pi}$$

$$C_X = C_{\mu} (1 + g_m R_C)$$

$$C_Y = C_{\mu} \left(1 + \frac{1}{g_m R_C} \right)$$

$$C_{in} = C_{\pi}$$

$$C_{out} = C_{CS}$$



CS Stage

$$V_{Thev} = V_{in}$$

$$R_{Thev} = R_S$$

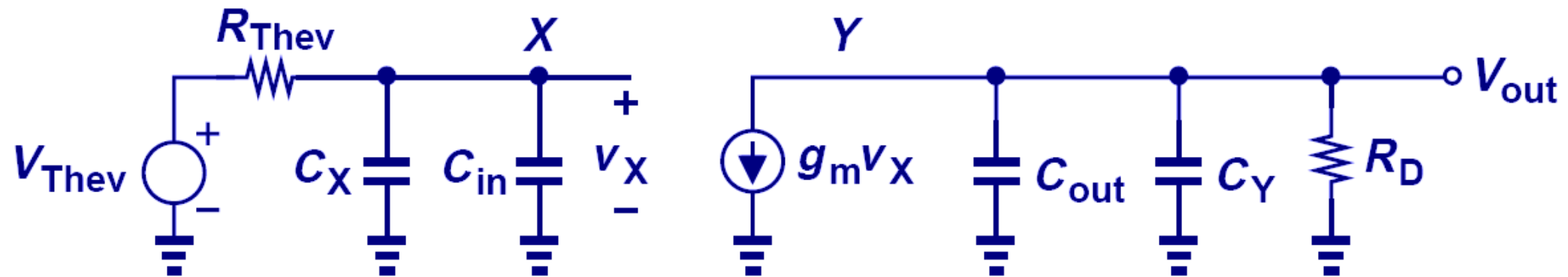
$$C_X = C_{GD} (1 + g_m R_D)$$

$$C_Y = C_{GD} \left(1 + \frac{1}{g_m R_D} \right)$$

$$C_{in} = C_{GS}$$

$$C_{out} = C_{DB}$$

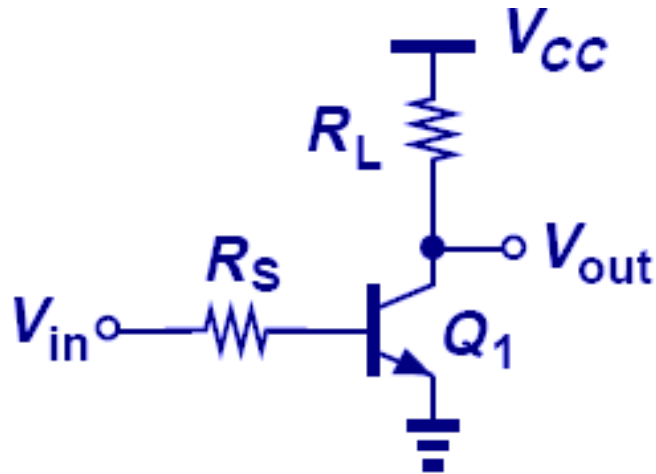
Unified Model Using Miller's Theorem



$$|\omega_{p,in}| = \frac{1}{R_{Thev} [C_{in} + (1 + g_m R_L) C_{XY}]}$$

$$|\omega_{p,out}| = \frac{1}{R_L \left[C_{out} + \left(1 + \frac{1}{g_m R_L} \right) C_{XY} \right]}$$

Example: CE Stage



$$R_L = 2\text{k}\Omega$$

$$R_S = 200\Omega$$

$$I_C = 1\text{mA}$$

$$\beta = 100$$

$$C_\pi = 100\text{fF}$$

$$C_\mu = 20\text{fF}$$

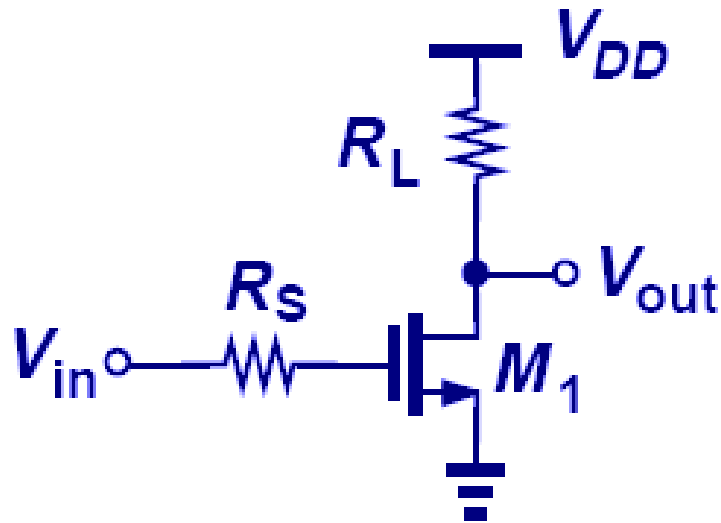
$$C_{CS} = 30\text{fF}$$

$$|\omega_{p,in}| = 2\pi \times (516\text{MHz})$$

$$|\omega_{p,out}| = 2\pi \times (1.59\text{GHz})$$

➤ The input pole is the bottleneck for speed.

Example: Half Width CS Stage



$$W \downarrow 2X$$

$$g_m = \mu C_{ox} \frac{W}{L} (V_{GS} - V_{TH})$$

In 474 we will learn that all MOS caps are $\propto W$

$$C_{GS} = \frac{2}{3} W L C_{ox} + W C_{ov}$$

$$C_{GD} = W C_{ov}$$

$$C_{DB} = A_D C_j + P_D C_{jsw} \propto W$$

$$|\omega_{p,in}| = \frac{1}{R_S \left[\frac{C_{in}}{2} + \left(1 + \frac{g_m R_L}{2} \right) \frac{C_{XY}}{2} \right]}$$

$$|\omega_{p,out}| = \frac{1}{R_L \left[\frac{C_{out}}{2} + \left(1 + \frac{2}{g_m R_L} \right) \frac{C_{XY}}{2} \right]}$$

- LF gain, $g_m R_L$ reduces by 1/2
- Assuming $g_m R_L$ is still high:
- The input pole increases by $\sim 4X$
- The output pole increases by $\sim 2x$
 - Constant gain-bandwidth product!

Direct Analysis of CE and CS Stages

- For a detailed direct small-signal analysis, see Razavi 11.4.4

$$\frac{V_{out}}{V_{Thev}}(s) = \frac{(C_{XY}s - g_m)R_L}{as^2 + bs + 1}$$

where

$$a = R_{Thev}R_L(C_{in}C_{XY} + C_{out}C_{XY} + C_{in}C_{out})$$

$$b = (1 + g_mR_L)C_{XY}R_{Thev} + R_{Thev}C_{in} + R_L(C_{XY} + C_{out})$$

To find the 2 poles, we can write

$$as^2 + bs + 1 = \left(\frac{s}{\omega_{p1}} + 1\right)\left(\frac{s}{\omega_{p2}} + 1\right) = \frac{s^2}{\omega_{p1}\omega_{p2}} + \left(\frac{1}{\omega_{p1}} + \frac{1}{\omega_{p2}}\right)s + 1$$

Using a "dominant pole" approximation $\omega_{p1} \ll \omega_{p2}$

$$as^2 + bs + 1 = \frac{s^2}{\omega_{p1}\omega_{p2}} + \frac{s}{\omega_{p1}} + 1$$

$$\omega_{p1} = \frac{1}{b} \quad \text{and} \quad \omega_{p2} = \frac{b}{a}$$

Exact
Expression

➤ **Direct analysis yields different pole locations and an extra zero.**

Direct Analysis of CE and CS Stages w/ Dominant Pole Approximation

$$|\omega_z| = \frac{g_m}{C_{XY}}$$

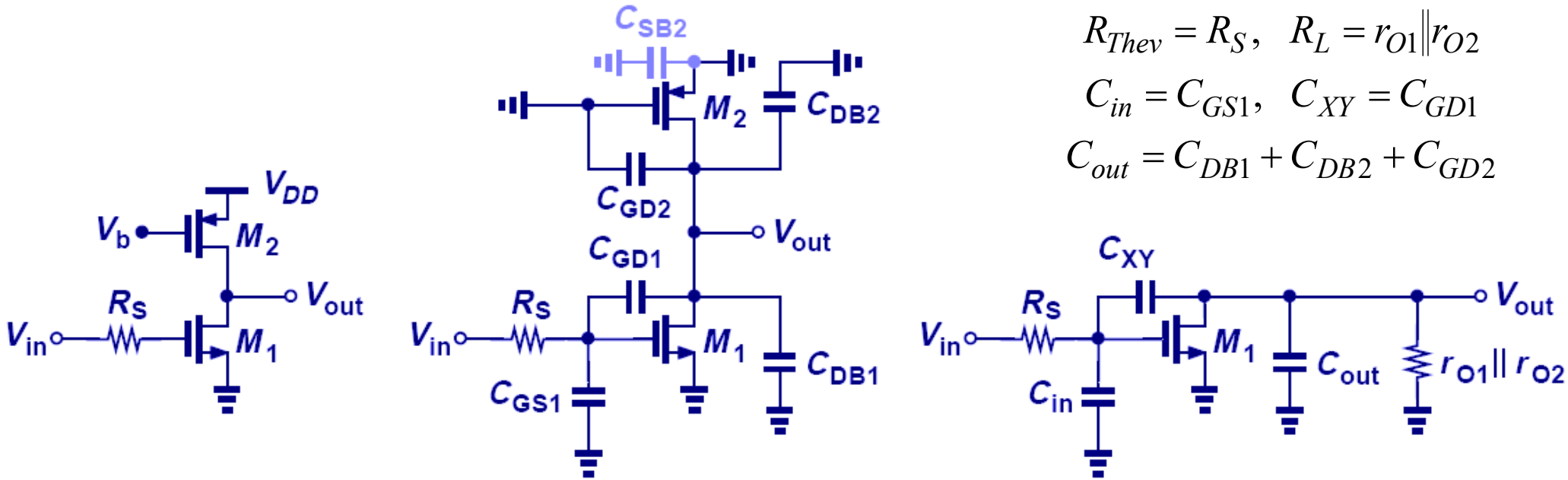
1

$$|\omega_{p1}| = \frac{1}{(1 + g_m R_L) C_{XY} R_{Thev} + R_{Thev} C_{in} + R_L (C_{XY} + C_{out})}$$

$$|\omega_{p2}| = \frac{(1 + g_m R_L) C_{XY} R_{Thev} + R_{Thev} C_{in} + R_L (C_{XY} + C_{out})}{R_{Thev} R_L (C_{in} C_{XY} + C_{out} C_{XY} + C_{in} C_{out})}$$

- ω_{p1} will be lower due to the additional term
- ω_{p2} is at a much higher frequency due to “pole splitting”
 - Discussed more when we talk about stability

Example: CE and CS Direct Analysis (Dominant Pole Approximation)



$$R_{Thev} = R_S, \quad R_L = r_{O1} \parallel r_{O2}$$

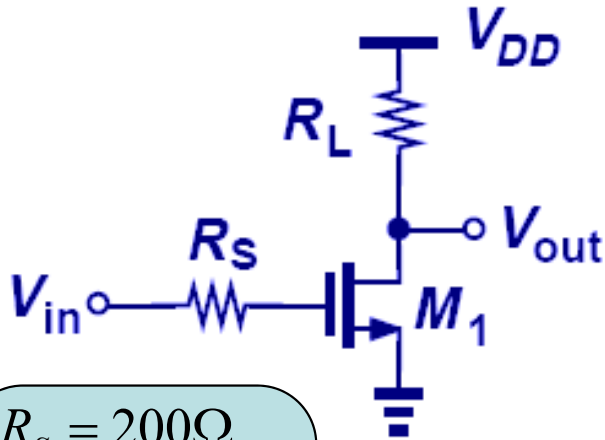
$$C_{in} = C_{GS1}, \quad C_{XY} = C_{GD1}$$

$$C_{out} = C_{DB1} + C_{DB2} + C_{GD2}$$

$$\omega_{p1} \approx \frac{1}{\left[1 + g_{m1}(r_{O1} \parallel r_{O2})\right]C_{XY}R_S + R_S C_{in} + (r_{O1} \parallel r_{O2})(C_{XY} + C_{out})}$$

$$\omega_{p2} \approx \frac{\left[1 + g_{m1}(r_{O1} \parallel r_{O2})\right]C_{XY}R_S + R_S C_{in} + (r_{O1} \parallel r_{O2})(C_{XY} + C_{out})}{R_S (r_{O1} \parallel r_{O2})(C_{in} C_{XY} + C_{out} C_{XY} + C_{in} C_{out})}$$

Example: Comparison Between Different Methods



$$R_S = 200\Omega$$

$$C_{GS} = 250\text{ fF}$$

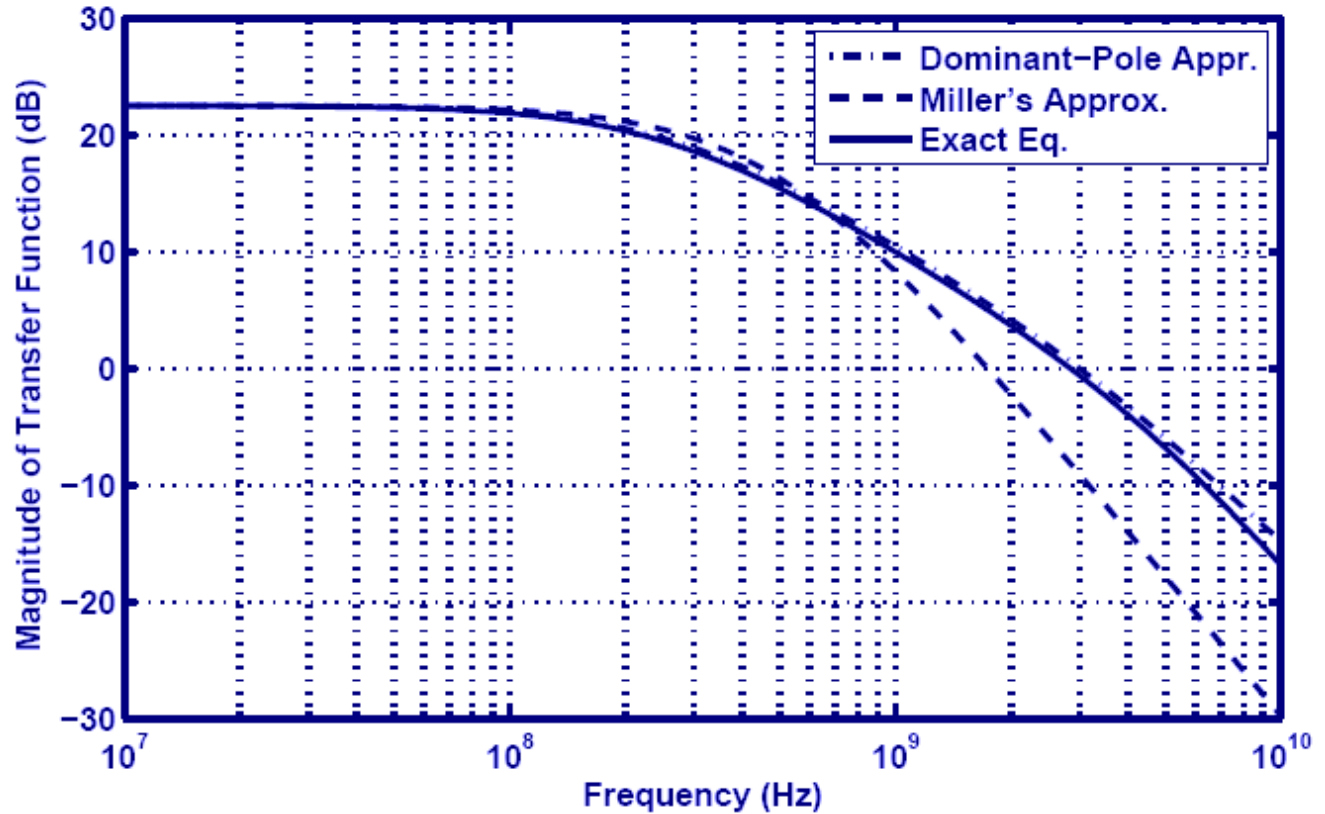
$$C_{GD} = 80\text{ fF}$$

$$C_{DB} = 100\text{ fF}$$

$$g_m = (150\Omega)^{-1}$$

$$\lambda = 0$$

$$R_L = 2\text{ K}\Omega$$



Simple Miller theorem analysis vastly overestimates the output pole at a lower frequency

Miller's

$$|\omega_{p,in}| = 2\pi \times (571\text{ MHz})$$

$$|\omega_{p,out}| = 2\pi \times (428\text{ MHz})$$

Exact

$$|\omega_{p,in}| = 2\pi \times (264\text{ MHz})$$

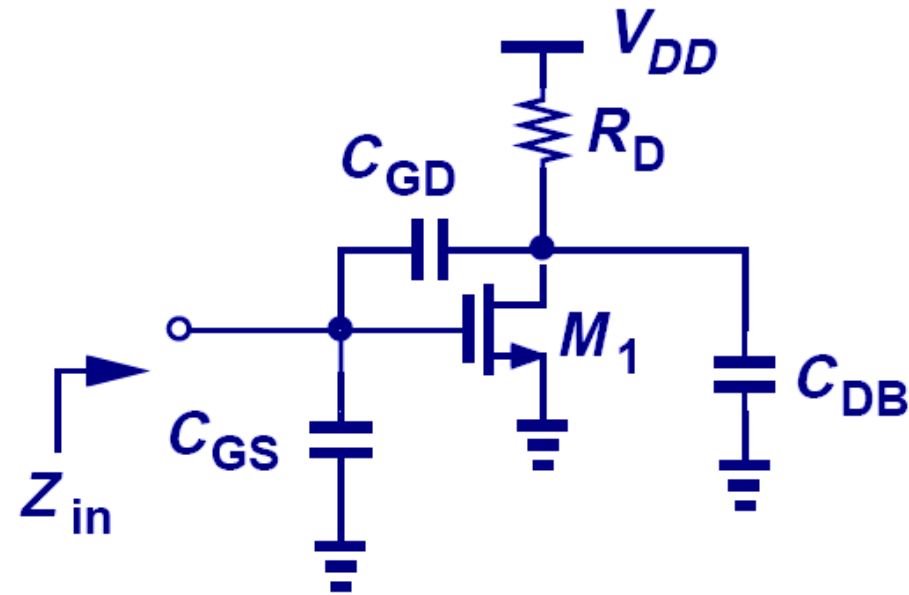
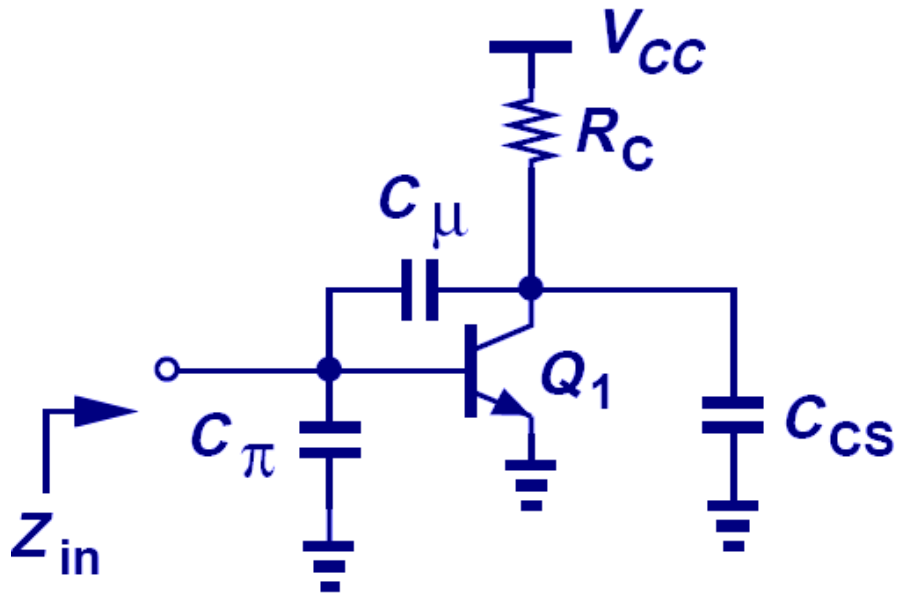
$$|\omega_{p,out}| = 2\pi \times (4.53\text{ GHz})$$

Dominant Pole

$$|\omega_{p,in}| = 2\pi \times (249\text{ MHz})$$

$$|\omega_{p,out}| = 2\pi \times (4.79\text{ GHz})$$

Input Impedance of CE and CS Stages



$$Z_{in} \approx \frac{1}{[C_{\pi} + (1 + g_m R_C)C_{\mu}]s} \parallel r_{\pi}$$

At low frequencies : r_{π}

Z_{in} has a pole at $\frac{1}{r_{\pi}(C_{\pi} + (1 + g_m R_C)C_{\mu})}$

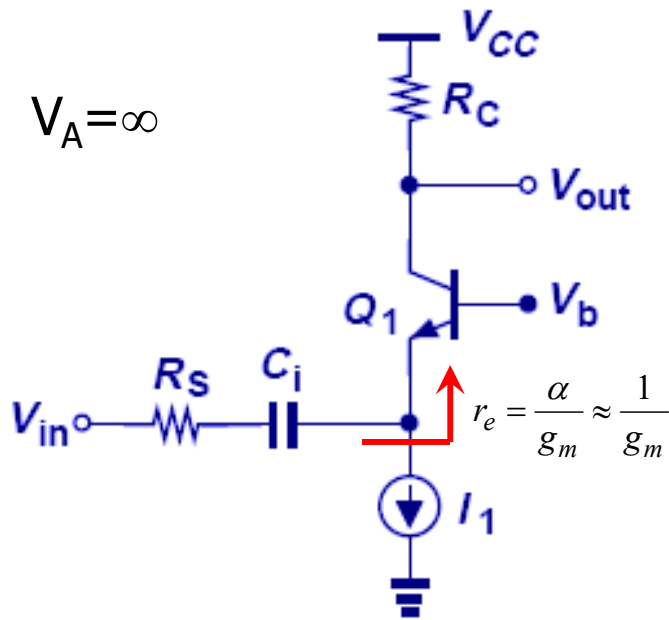
$$Z_{in} \approx \frac{1}{[C_{GS} + (1 + g_m R_D)C_{GD}]s}$$

Approximate as purely capacitive

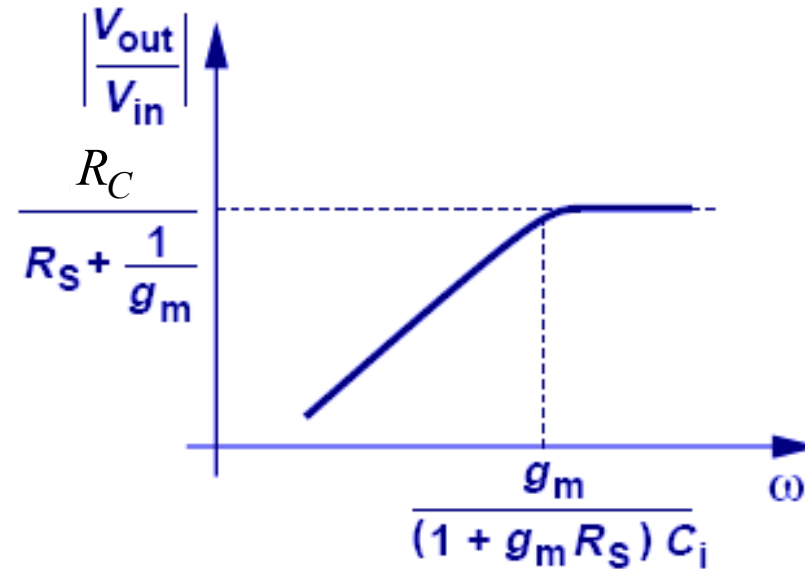
Agenda

- Frequency Response Concepts
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Low Frequency Response of CB and CG Stages



(a)

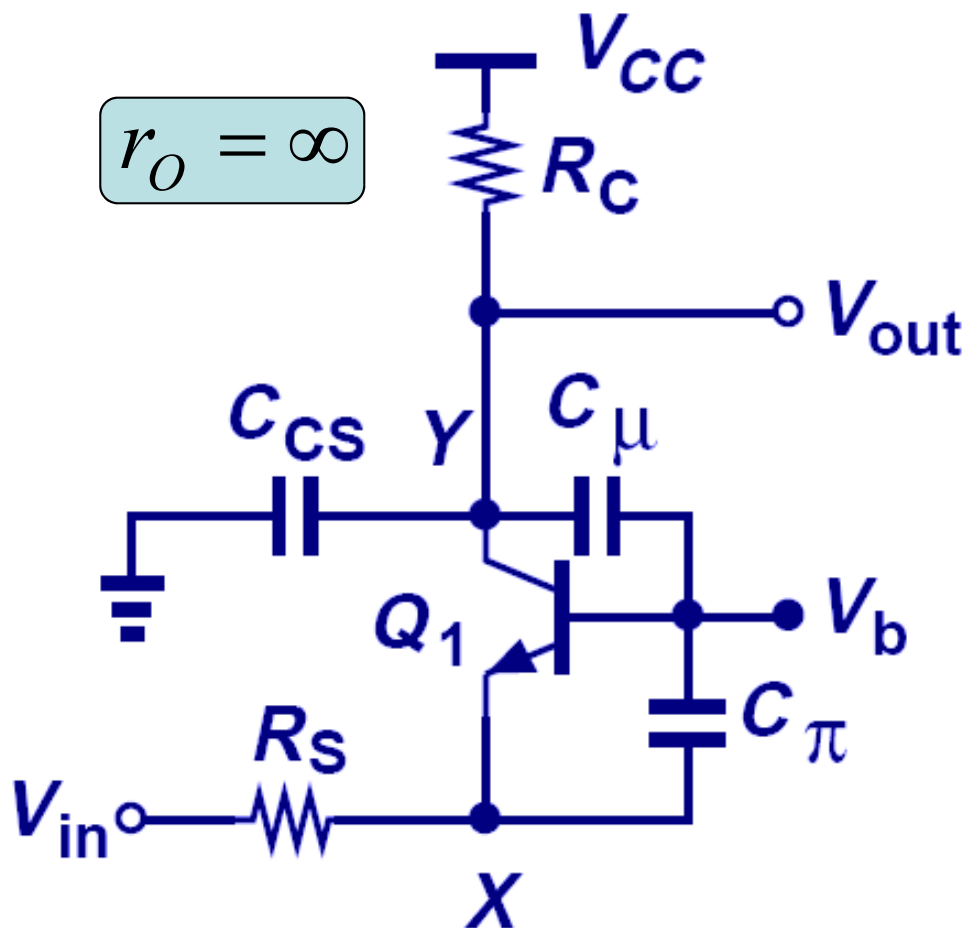


(b)

$$\frac{V_{out}}{V_{in}}(s) = \frac{g_m R_C C_i s}{(1 + g_m R_S) C_i s + g_m}$$

- As with CE and CS stages, the use of capacitive coupling leads to low-frequency roll-off in CB and CG stages (although a CB stage is shown above, a CG stage is similar).

Frequency Response of CB Stage



- No Miller effect
- Input pole is $\sim f_T$ (very high frequency)

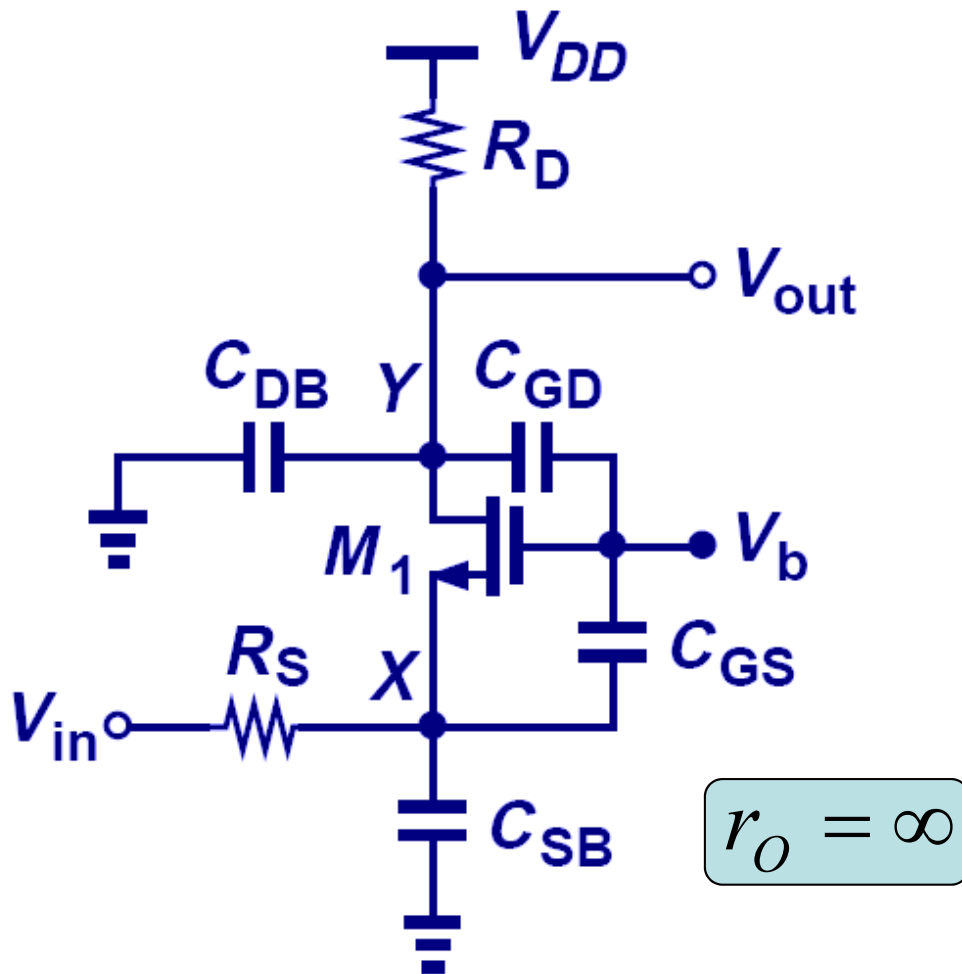
$$\omega_{p,X} = \frac{1}{\left(R_S \parallel \frac{1}{g_m} \right) C_X}$$

$$C_X = C_\pi$$

$$\omega_{p,Y} = \frac{1}{R_L C_Y}$$

$$C_Y = C_\mu + C_{CS}$$

Frequency Response of CG Stage



$$\omega_{p,X} = \frac{1}{\left(R_S \parallel \frac{1}{g_m} \right) C_X}$$

$$C_X = C_{GS} + C_{SB}$$

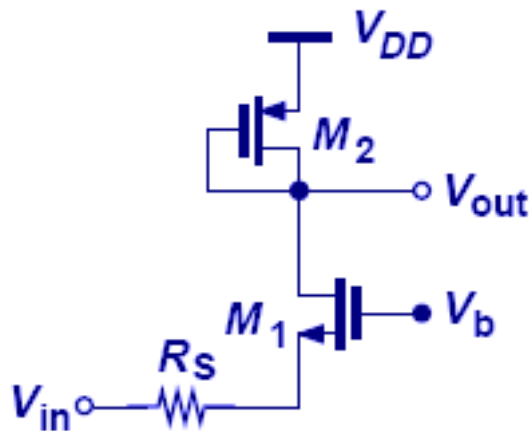
$$\omega_{p,Y} = \frac{1}{R_L C_Y}$$

$$C_Y = C_{GD} + C_{DB}$$

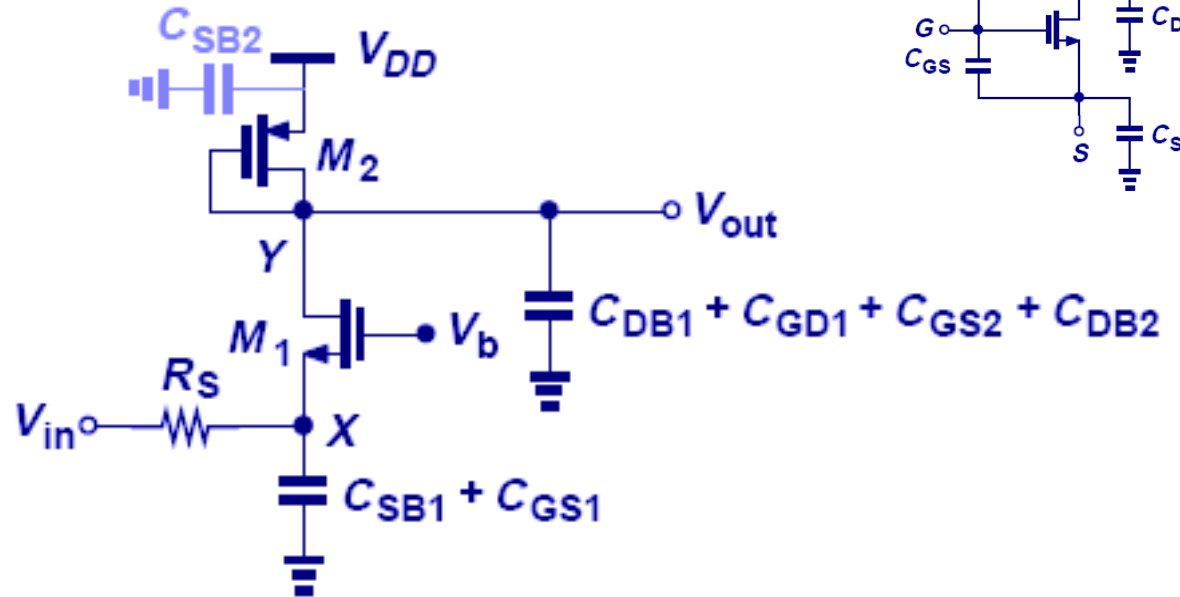
- Similar to a CB stage, the input pole is on the order of f_T , so rarely a speed bottleneck.

Example: CG Stage Pole Identification

$$r_O = \infty$$

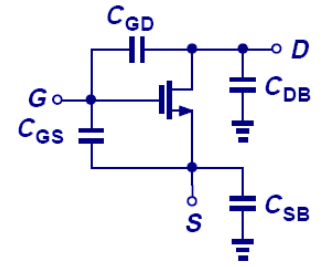


(a)



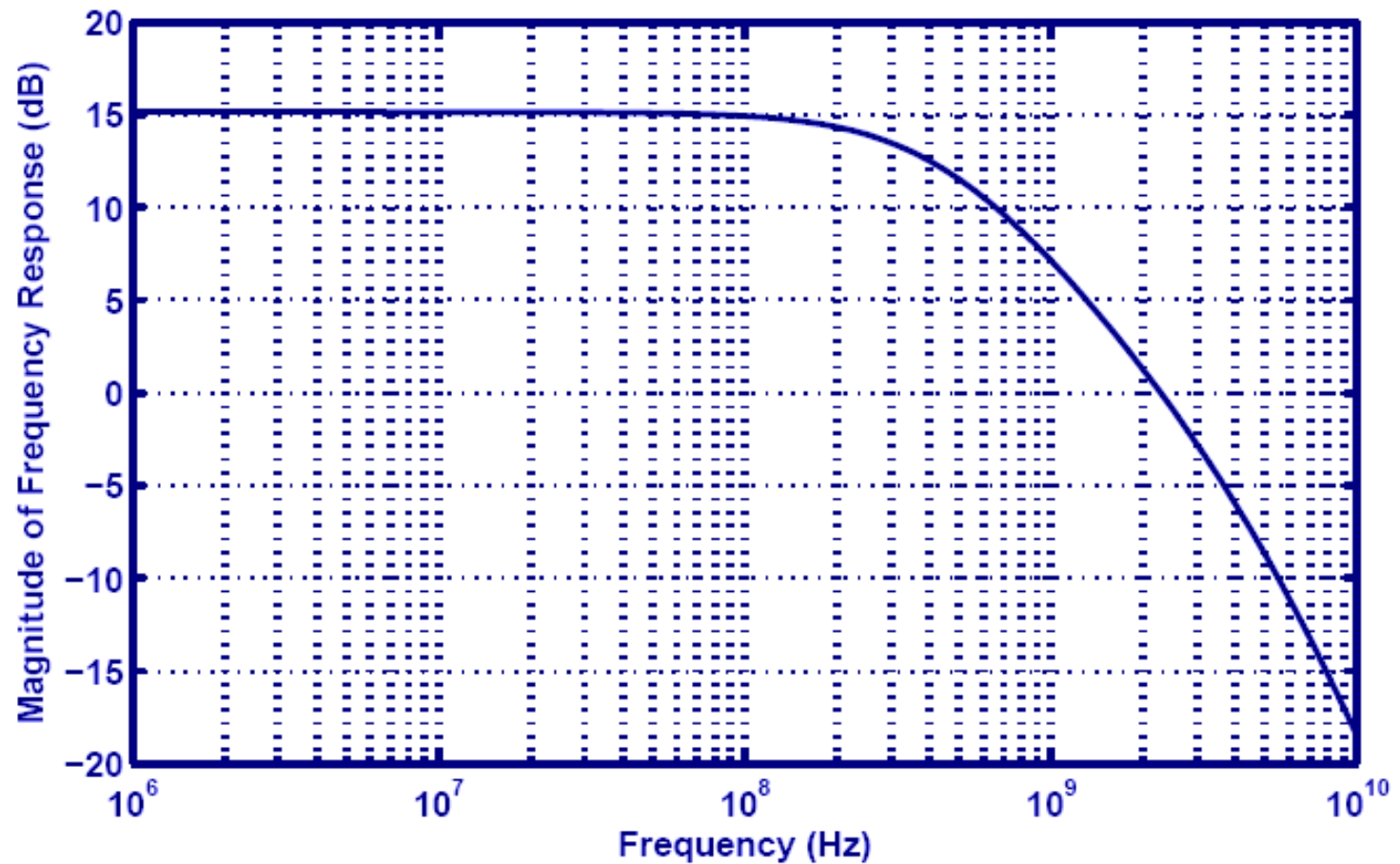
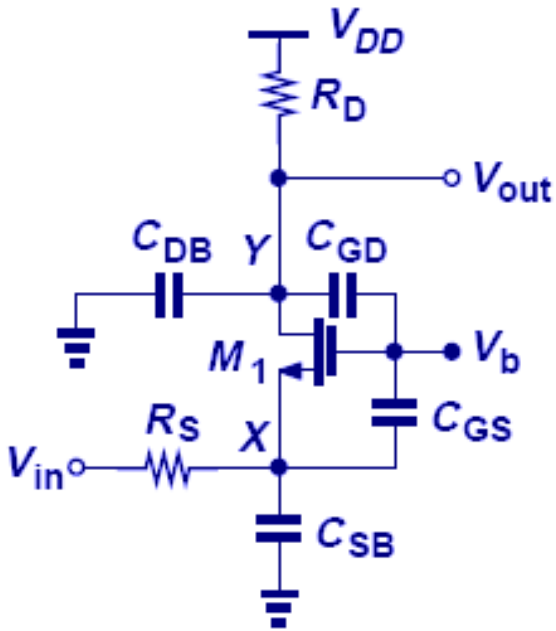
(b)

MOSFET Caps



$$\omega_{p,X} = \frac{1}{\left(R_S \parallel \frac{1}{g_{m1}} \right) (C_{SB1} + C_{GD1})} \quad \omega_{p,Y} = \frac{1}{g_{m2} (C_{DB1} + C_{GD1} + C_{GS2} + C_{DB2})}$$

Example: Frequency Response of CG Stage



$$R_S = 200\Omega$$

$$C_{GS} = 250\text{ fF}$$

$$C_{GD} = 80\text{ fF}$$

$$C_{SB} = C_{DB} = 100\text{ fF}$$

$$g_m = (150\Omega)^{-1}$$

$$\lambda = 0$$

$$R_d = 2\text{ K}\Omega$$

$$|\omega_{p,X}| = 2\pi \times (5.31\text{ GHz})$$

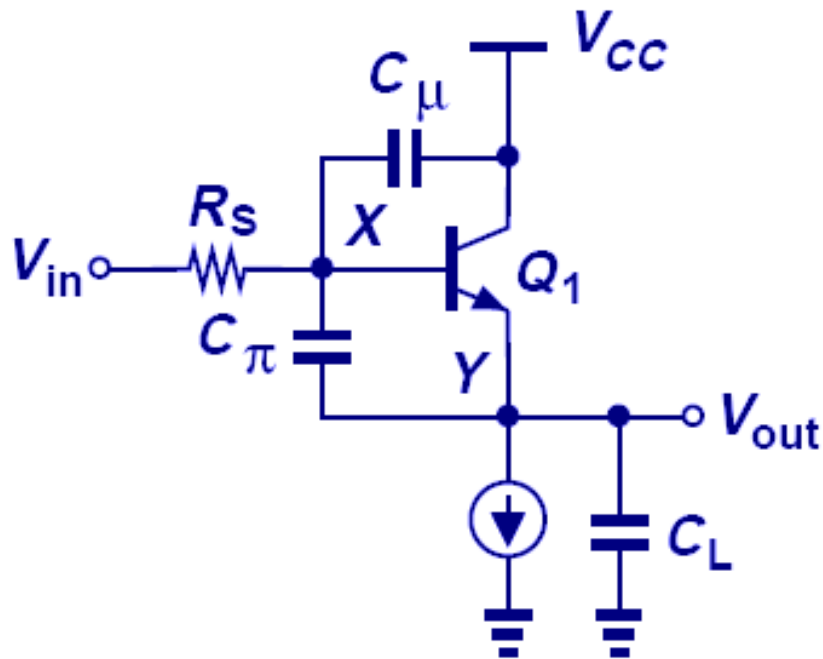
$$|\omega_{p,Y}| = 2\pi \times (442\text{ MHz})$$

- Input pole is $\sim f_T$
- Output pole limits bandwidth

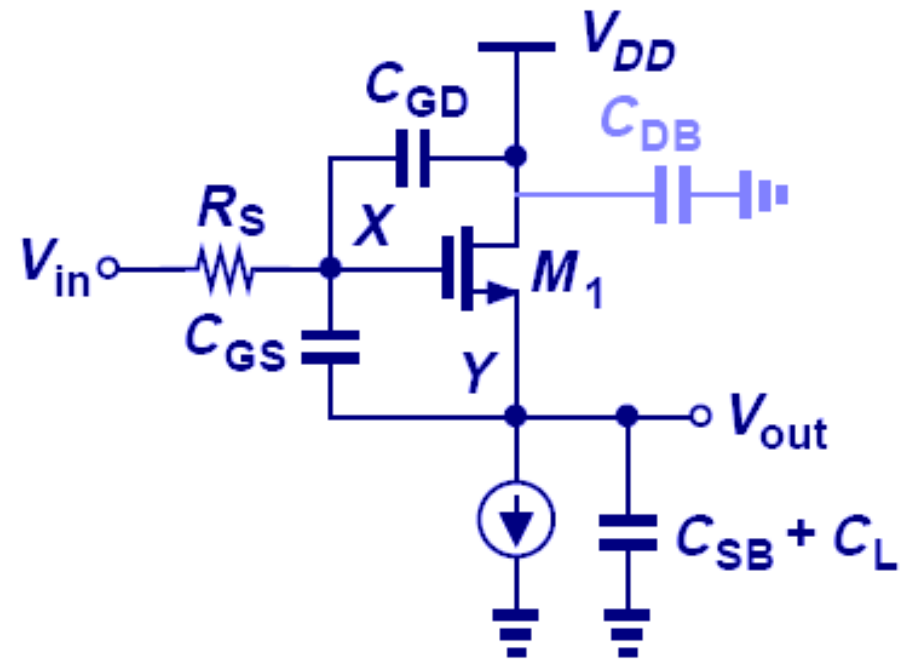
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- Differential Pairs
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Emitter and Source Followers



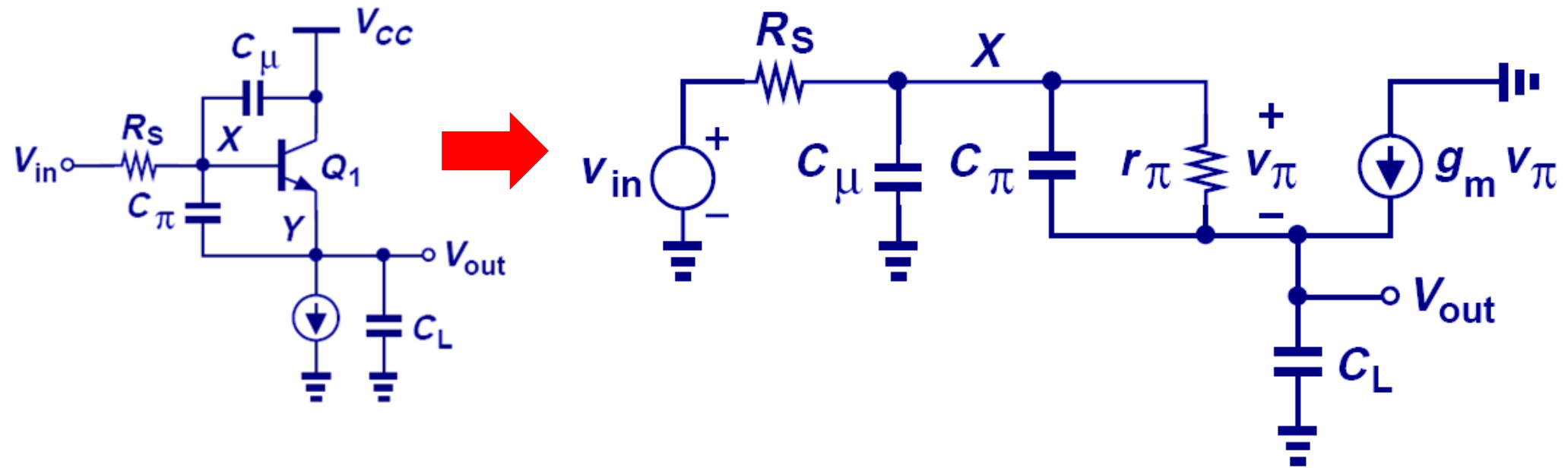
(a)



(b)

- The following will discuss the frequency response of emitter and source followers using direct analysis, as this circuit typically has 2 poles that are close together
- Emitter follower is treated first and source follower is derived easily by allowing r_π to go to infinity

Direct Analysis of Emitter Follower



For detailed analysis, see Razavi 11.6

Assuming that $r_{\pi} \gg \frac{1}{g_m}$

$$\frac{V_{out}}{V_{in}} = \frac{1 + \frac{C_{\pi}}{g_m} s}{as^2 + bs + 1}$$

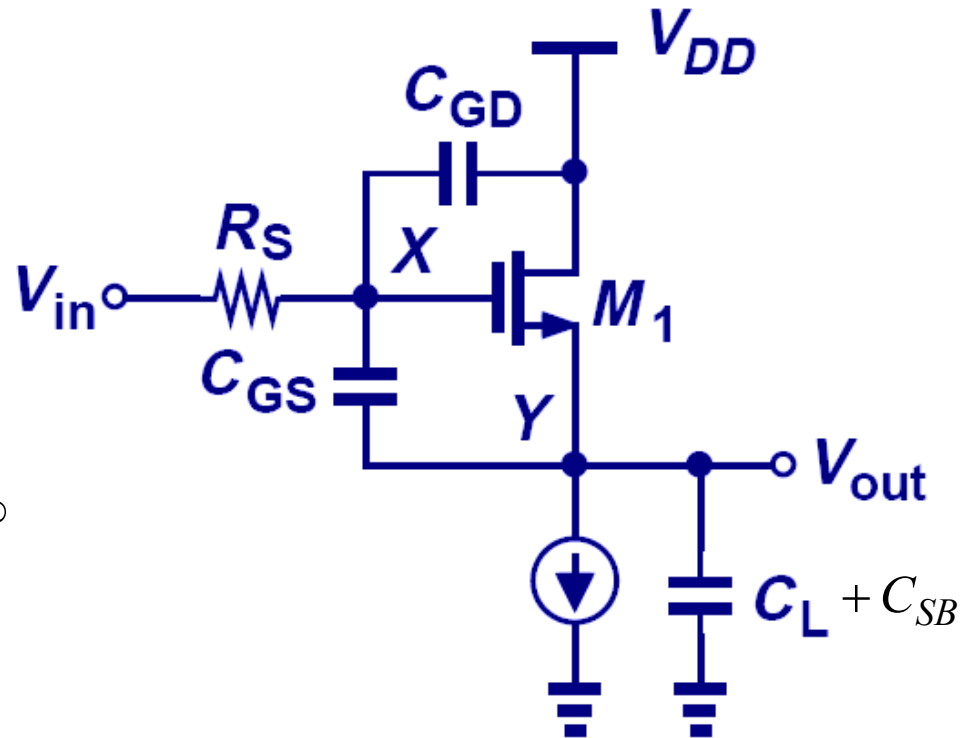
$$a = \frac{R_S}{g_m} (C_{\mu} C_{\pi} + C_{\mu} C_L + C_{\pi} C_L)$$

$$b = R_S C_{\mu} + \frac{C_{\pi}}{g_m} + \left(1 + \frac{R_S}{r_{\pi}}\right) \frac{C_L}{g_m}$$

$$|\omega_z| = \frac{g_m}{C_{\pi}}$$

Generally, this yields 2 close poles, necessitating a direct solution approach

Direct Analysis of Source Follower Stage



Taking $r_{\pi} \rightarrow \infty$

$$C_{\pi} \rightarrow C_{GS}$$

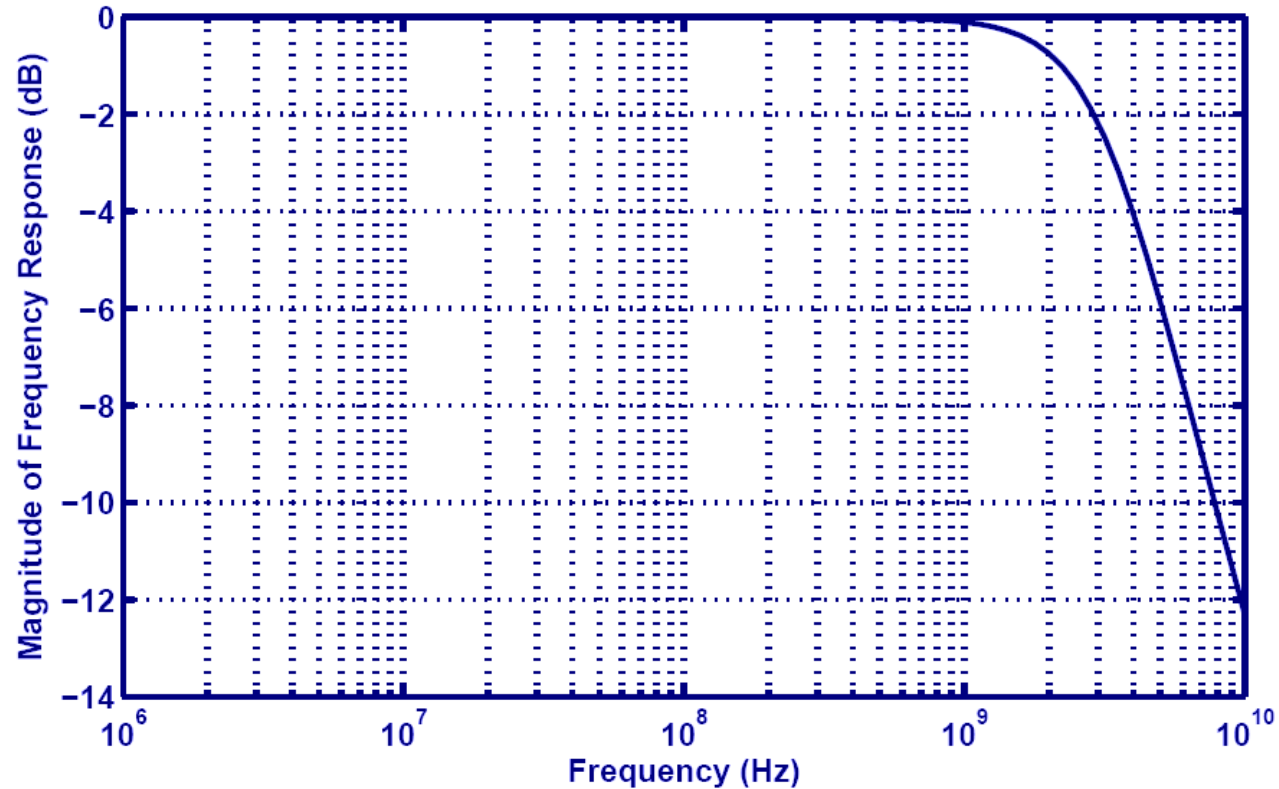
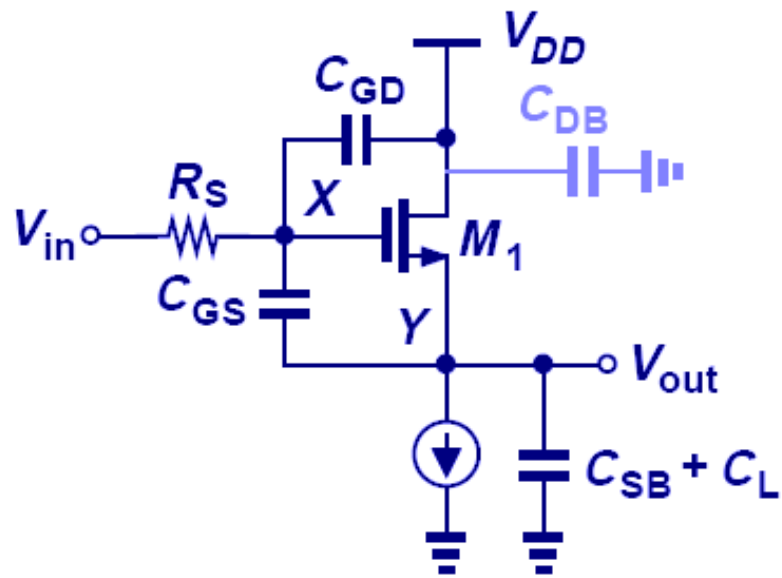
$$C_{\mu} \rightarrow C_{GD}$$

$$\frac{V_{out}}{V_{in}} = \frac{1 + \frac{C_{GS}}{g_m} s}{as^2 + bs + 1}$$

$$a = \frac{R_S}{g_m} (C_{GD}C_{GS} + C_{GD}(C_L + C_{SB}) + C_{GS}(C_L + C_{SB}))$$

$$b = R_S C_{GD} + \frac{C_{GD} + C_L + C_{SB}}{g_m}$$

Example: Frequency Response of Source Follower



$$R_S = 200\Omega$$

$$C_L = 100\text{ fF}$$

$$C_{GS} = 250\text{ fF}$$

$$C_{GD} = 80\text{ fF}$$

$$C_{DB} = 100\text{ fF}$$

$$g_m = (150\Omega)^{-1}$$

$$\lambda = 0$$

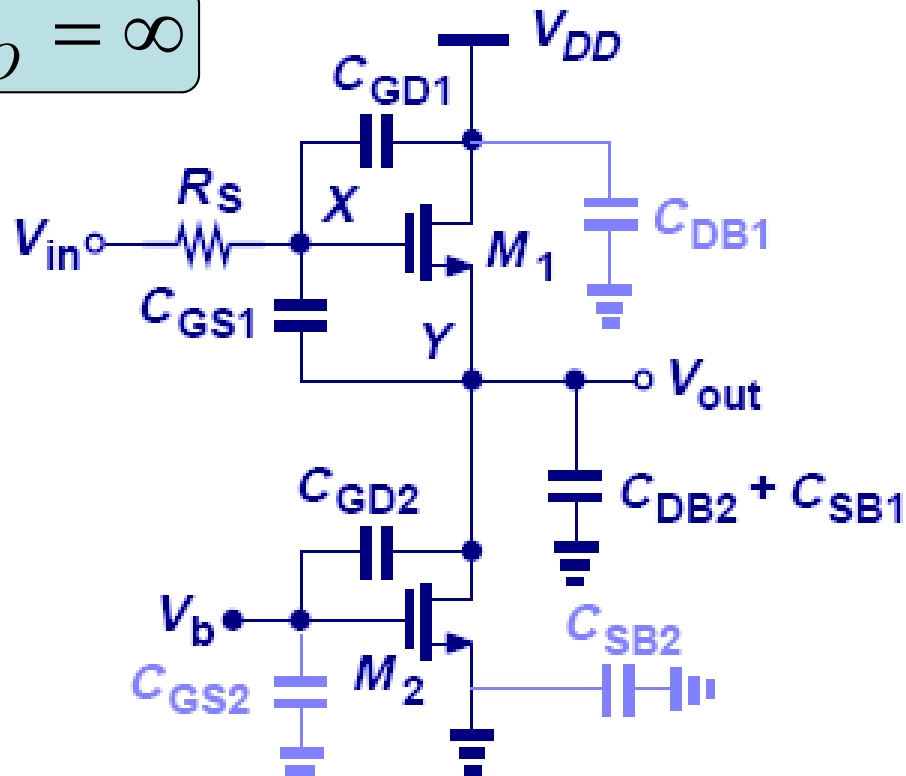
$$\omega_{p1} = 2\pi[-1.79\text{GHz} + j(2.57\text{GHz})]$$

$$\omega_{p2} = 2\pi[-1.79\text{GHz} - j(2.57\text{GHz})]$$

2 Complex Conjugate Poles

Example: Source Follower

$$r_O = \infty$$



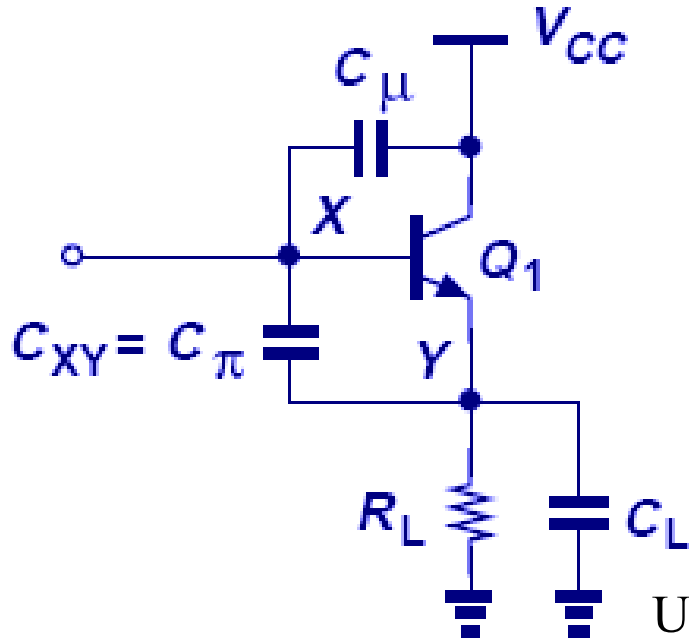
$$\frac{V_{out}}{V_{in}} = \frac{1 + \frac{C_{GS1}}{g_m} s}{as^2 + bs + 1}$$

$$a = \frac{R_S}{g_{m1}} \left[C_{GD1} C_{GS1} + (C_{GD1} + C_{GS1})(C_{SB1} + C_{GD2} + C_{DB2}) \right]$$

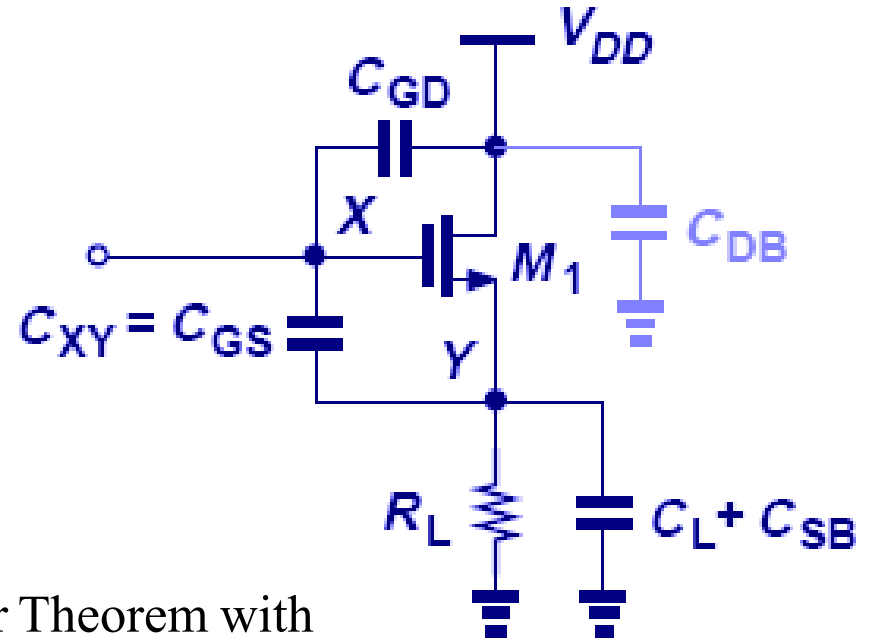
$$b = R_S C_{GD1} + \frac{C_{GD1} + C_{SB1} + C_{GD2} + C_{DB2}}{g_{m1}}$$

Input Capacitance of Emitter/Source Follower

$$r_O = \infty$$



(a)



(b)

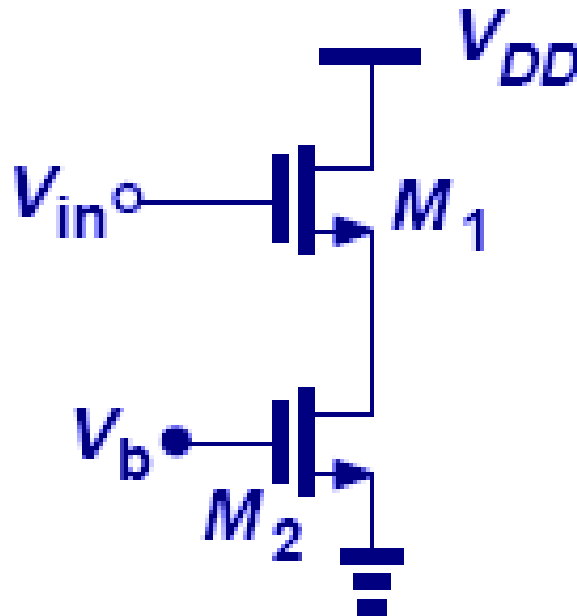
Using Miller Theorem with

$$A_v = \frac{g_m R_L}{1 + g_m R_L}$$

$$C_{in} = C_{\mu} + \frac{C_{\pi}}{1 + g_m R_L}$$

$$C_{in} = C_{GD} + \frac{C_{GS}}{1 + g_m R_L}$$

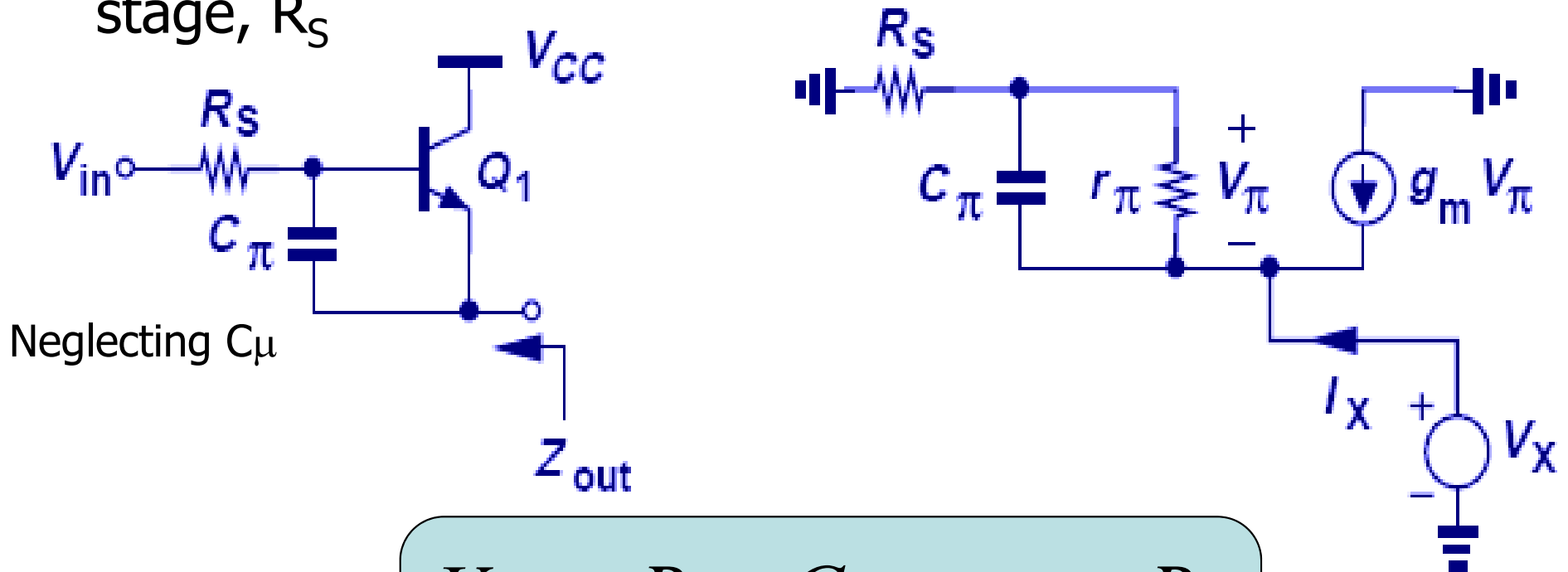
Example: Source Follower Input Capacitance



$$C_{in} = C_{GD1} + \frac{1}{1 + g_{m1}(r_{O1} \parallel r_{O2})} C_{GS1}$$

Output Impedance of Emitter Follower

- Need to consider the output resistance of the previous stage, R_S



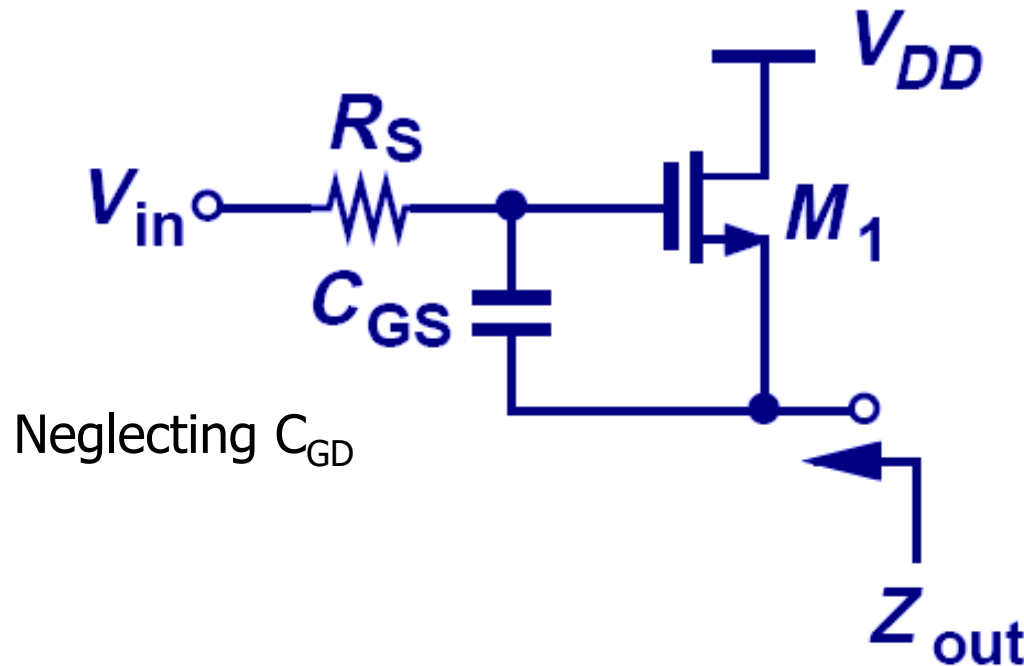
$$\frac{V_X}{I_X} = \frac{R_S r_\pi C_\pi s + r_\pi + R_S}{r_\pi C_\pi s + \beta + 1}$$

Low Frequency: $\frac{r_\pi + R_S}{\beta + 1} = r_e + \frac{R_S}{\beta + 1}$

High Frequency: R_S

Output impedance generally goes up w/ frequency!

Output Impedance of Source Follower



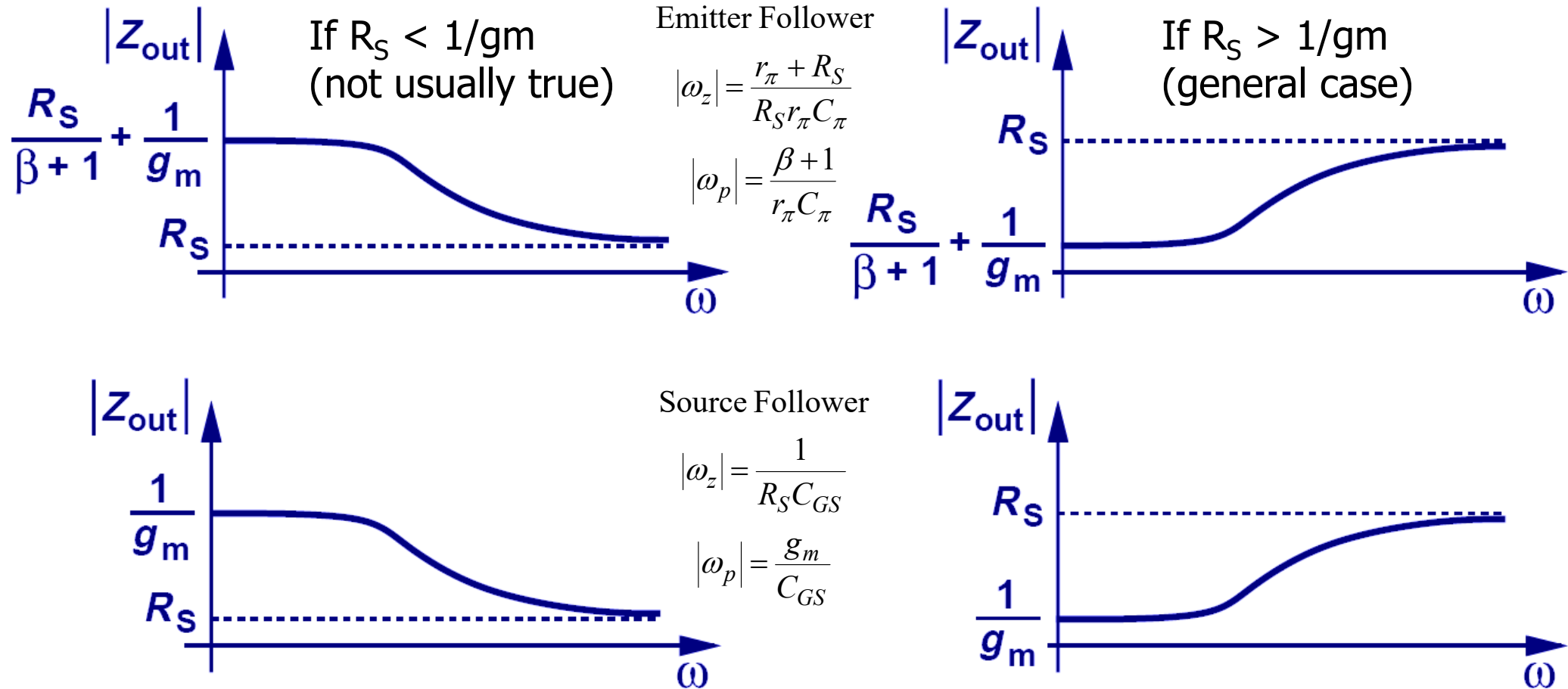
Output impedance generally goes up w/ frequency!

$$\frac{V_X}{I_X} = \frac{R_S C_{GS} s + 1}{C_{GS} s + g_m}$$

Low Frequency: $\frac{1}{g_m}$

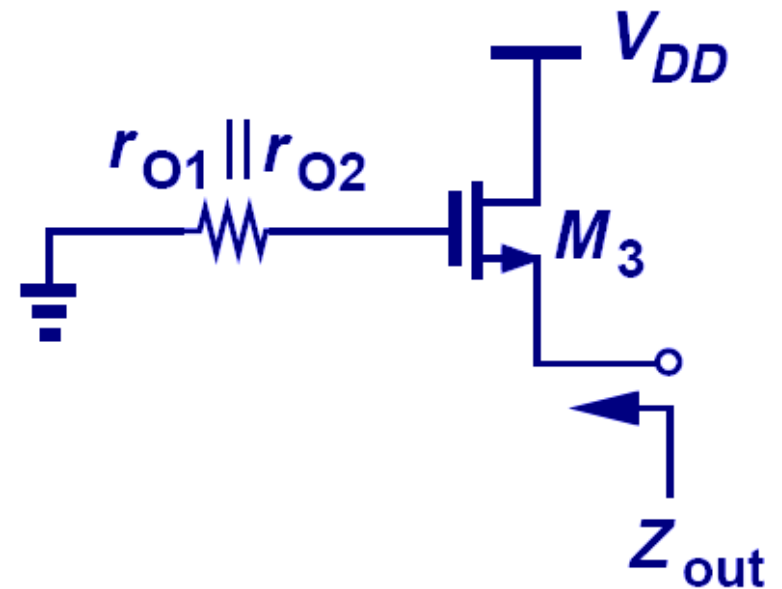
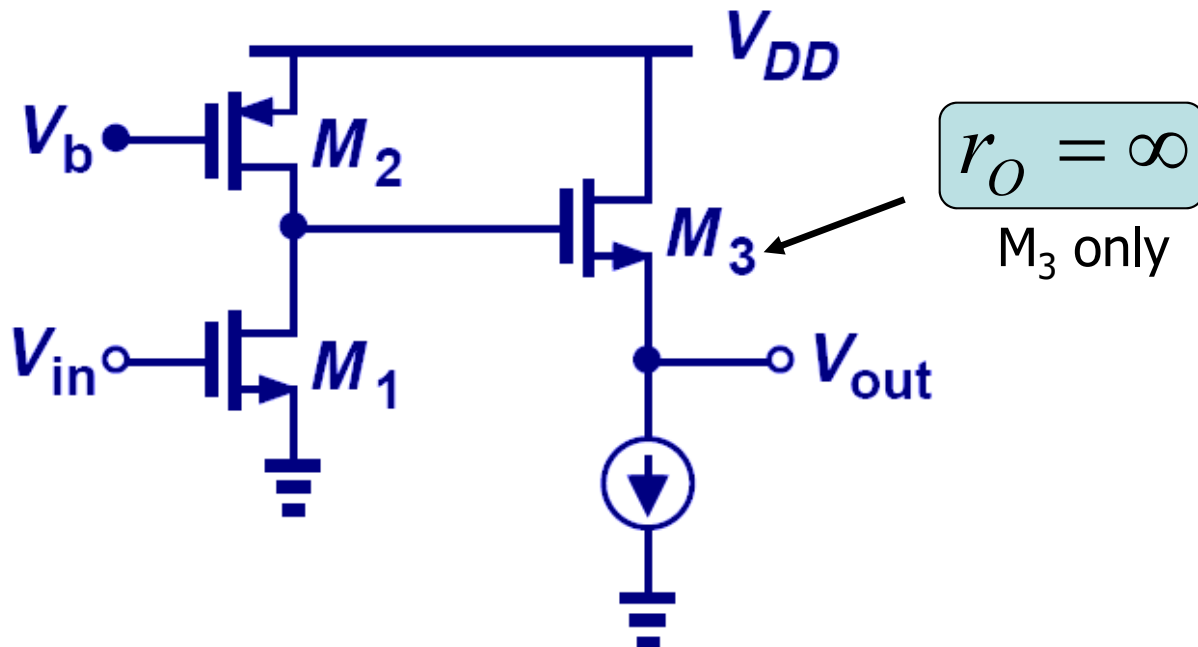
High Frequency: R_S

Active Inductor



➤ The plot above shows the output impedance of emitter and source followers. Since a follower's primary duty is to lower the driving impedance ($R_S > 1/g_m$), the "active inductor" characteristic on the right is usually observed.

Example: Output Impedance



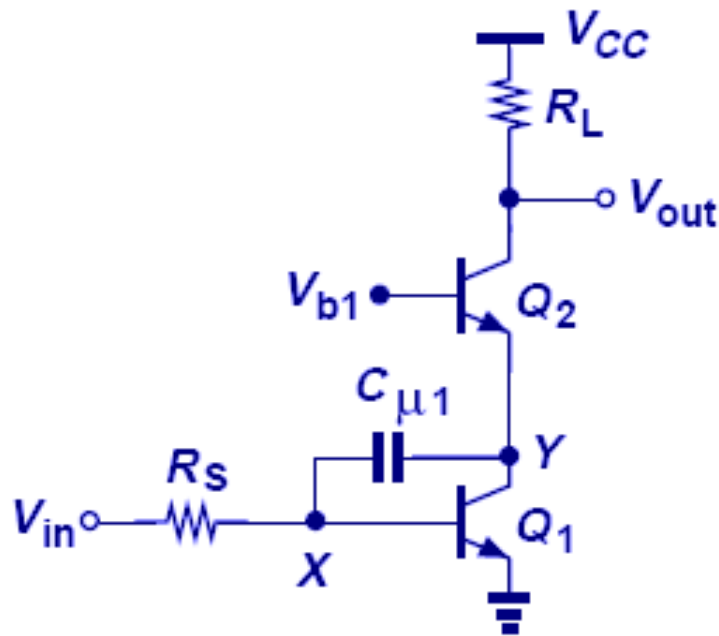
$$\frac{V_X}{I_X} = \frac{(r_{O1} \parallel r_{O2})C_{GS3}s + 1}{C_{GS3}s + g_{m3}}$$

Note: This neglects the capacitors from M_1 and M_2

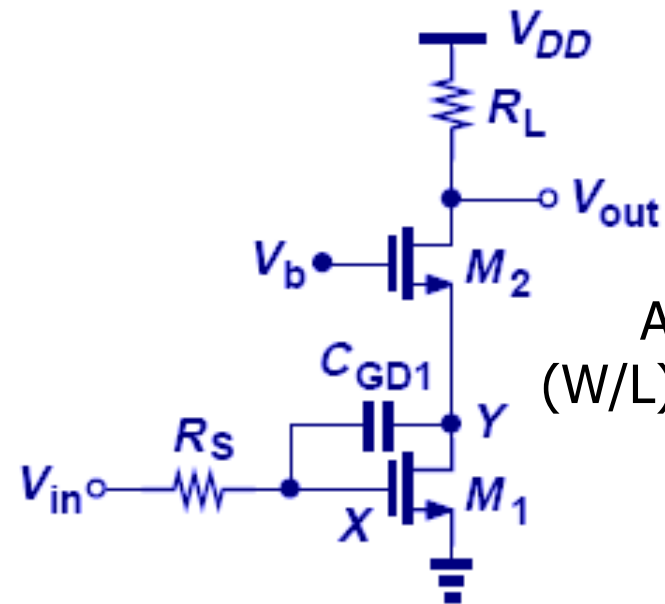
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Frequency Response of Cascode Stage



(a)



(b)

Assume
 $(W/L)_1 = (W/L)_2$

$$A_{v,XY} = \frac{-g_{m1}}{g_{m2}} \approx -1 \qquad C_x \approx 2C_{XY}$$

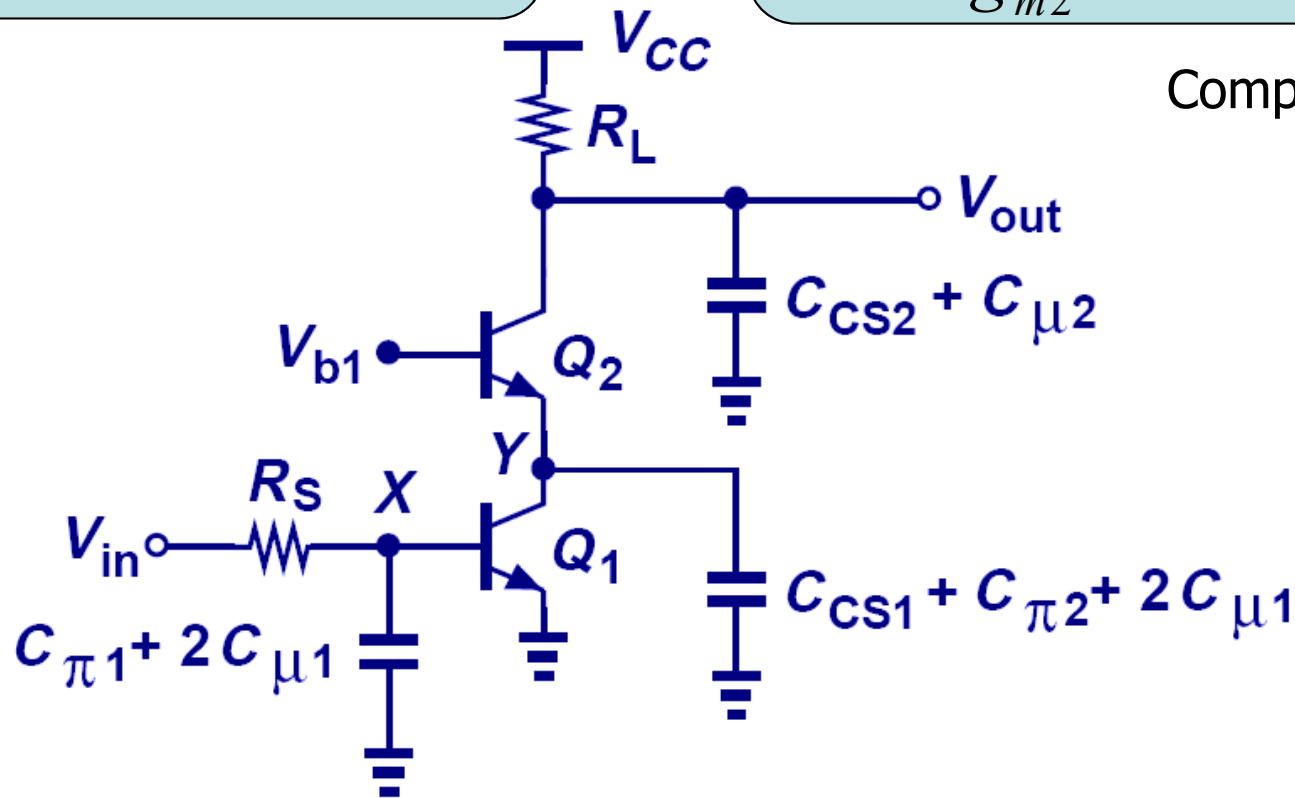
- For cascode stages, there are three poles and Miller multiplication is smaller than in the CE/CS stage.

Poles of Bipolar Cascode

$$\omega_{p,X} = \frac{1}{(R_S \parallel r_{\pi 1})(C_{\pi 1} + 2C_{\mu 1})}$$

$$\omega_{p,Y} = \frac{1}{\frac{1}{g_{m2}}(C_{CS1} + C_{\pi 2} + 2C_{\mu 1})}$$

Comparable to f_T

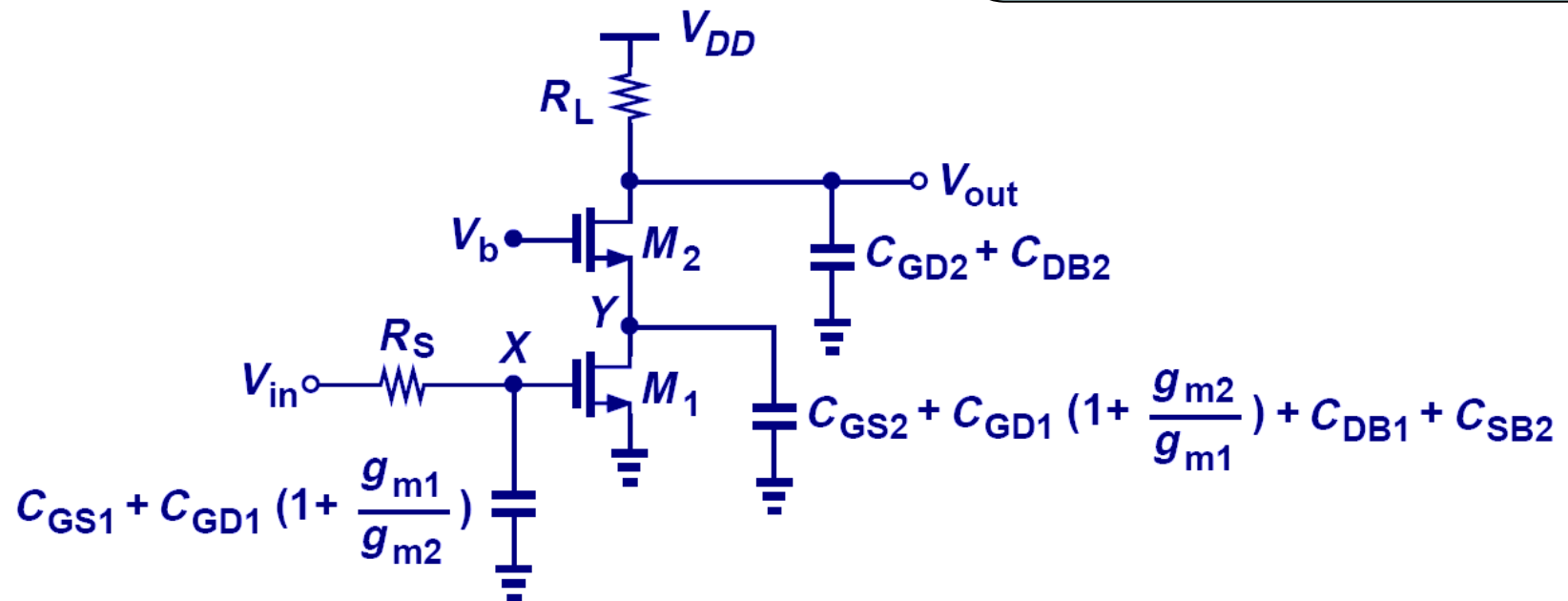


$$\omega_{p,out} = \frac{1}{R_L(C_{CS2} + C_{\mu 2})}$$

Poles of MOS Cascode

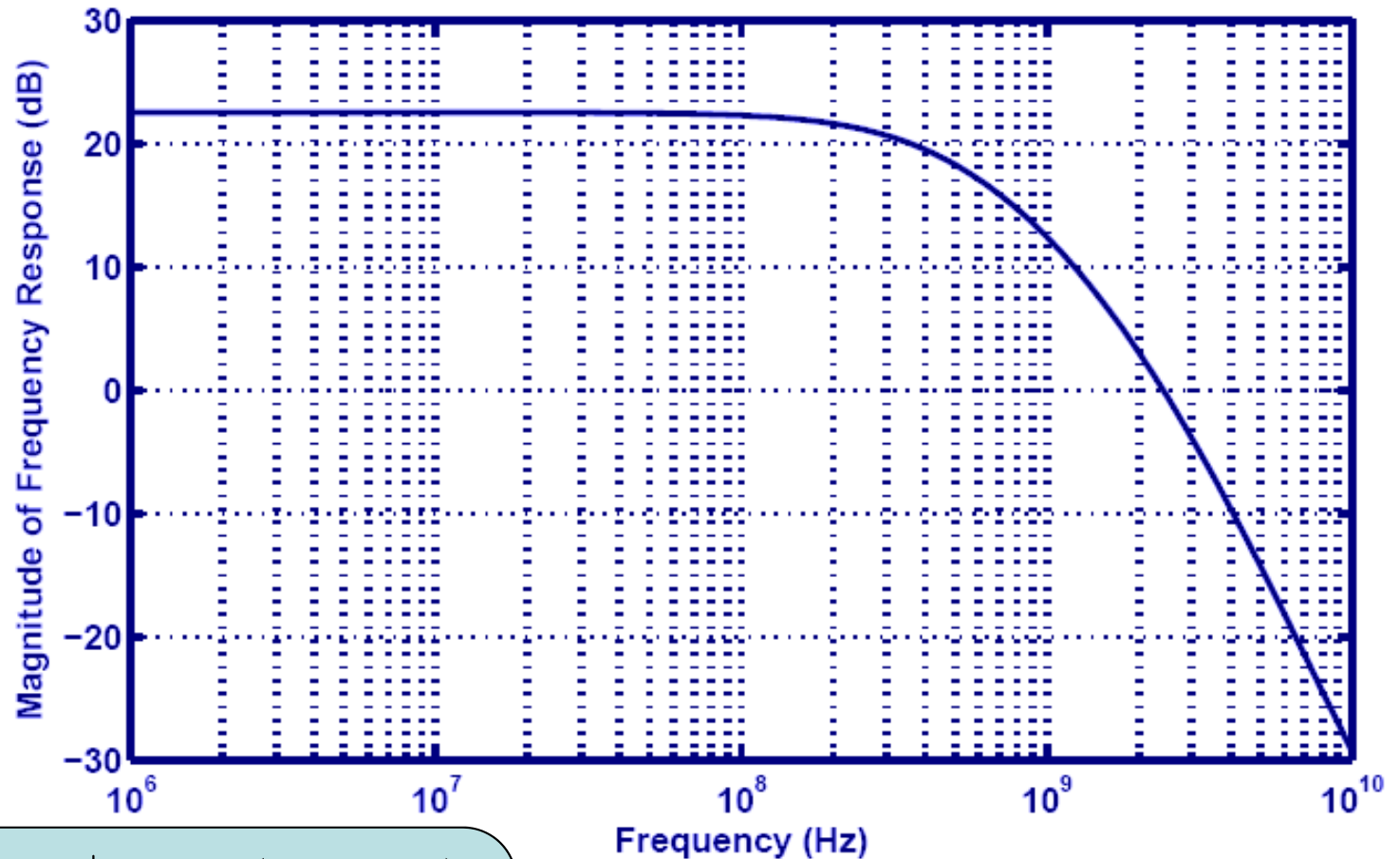
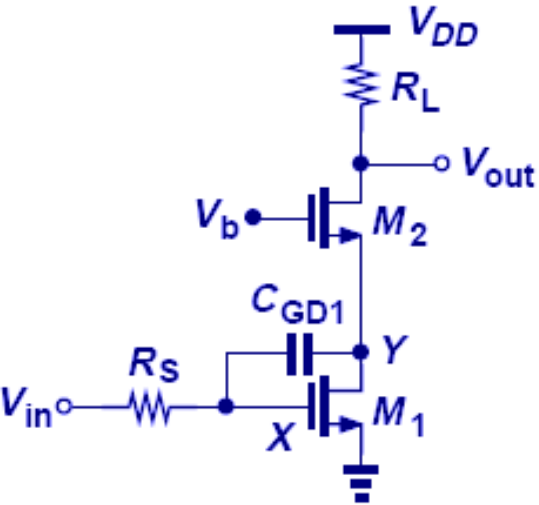
$$\omega_{p,X} = \frac{1}{R_S \left[C_{GS1} + \left(1 + \frac{g_{m1}}{g_{m2}} \right) C_{GD1} \right]}$$

$$\omega_{p,out} = \frac{1}{R_L (C_{DB2} + C_{GD2})}$$



$$\omega_{p,Y} = \frac{1}{\frac{1}{g_{m2}} \left[C_{DB1} + C_{GS2} + \left(1 + \frac{g_{m2}}{g_{m1}} \right) C_{GD1} + C_{SB2} \right]}$$

Example: Frequency Response of Cascode



$$R_S = 200 \Omega$$

$$C_{GS} = 250 \text{ fF}$$

$$C_{GD} = 80 \text{ fF}$$

$$C_{DB} = 100 \text{ fF}$$

$$g_m = (150 \Omega)^{-1}$$

$$\lambda = 0$$

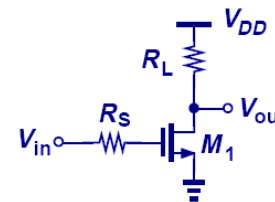
$$R_L = 2 \text{ K}\Omega$$

$$|\omega_{p,X}| = 2\pi \times (1.95 \text{ GHz})$$

$$|\omega_{p,Y}| = 2\pi \times (1.73 \text{ GHz})$$

$$|\omega_{p,out}| = 2\pi \times (442 \text{ MHz})$$

Compare to simple CS Exact



$$|\omega_{p,in}| = 2\pi \times (264 \text{ MHz})$$

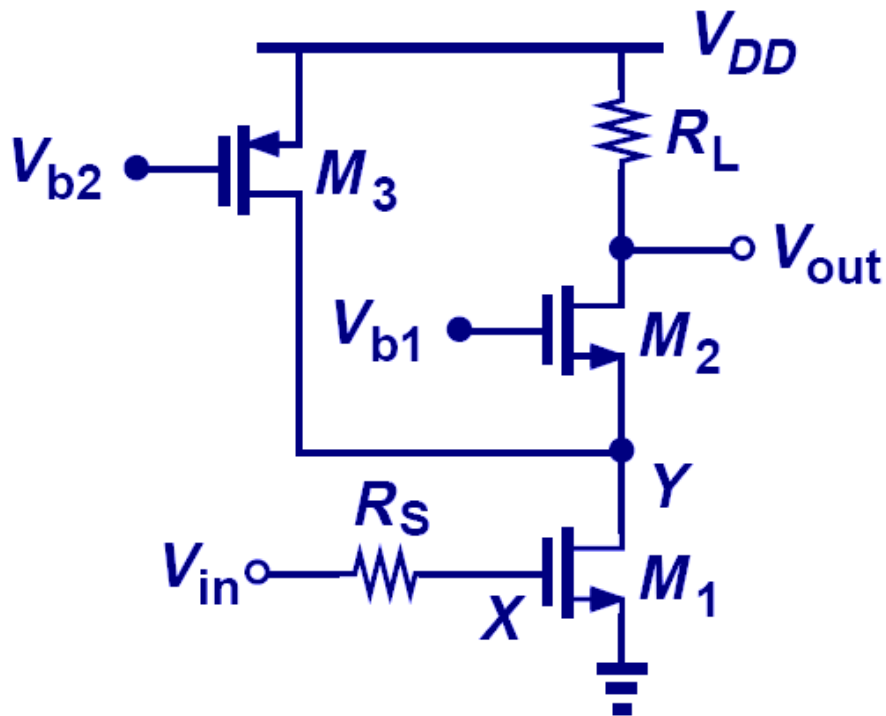
$$|\omega_{p,out}| = 2\pi \times (4.53 \text{ GHz})$$

Now output pole sets the bandwidth, and it has increased by 67%

MOS Cascode Example

$$\omega_{p,X} = \frac{1}{R_S \left[C_{GS1} + \left(1 + \frac{g_{m1}}{g_{m2}} \right) C_{GD1} \right]}$$

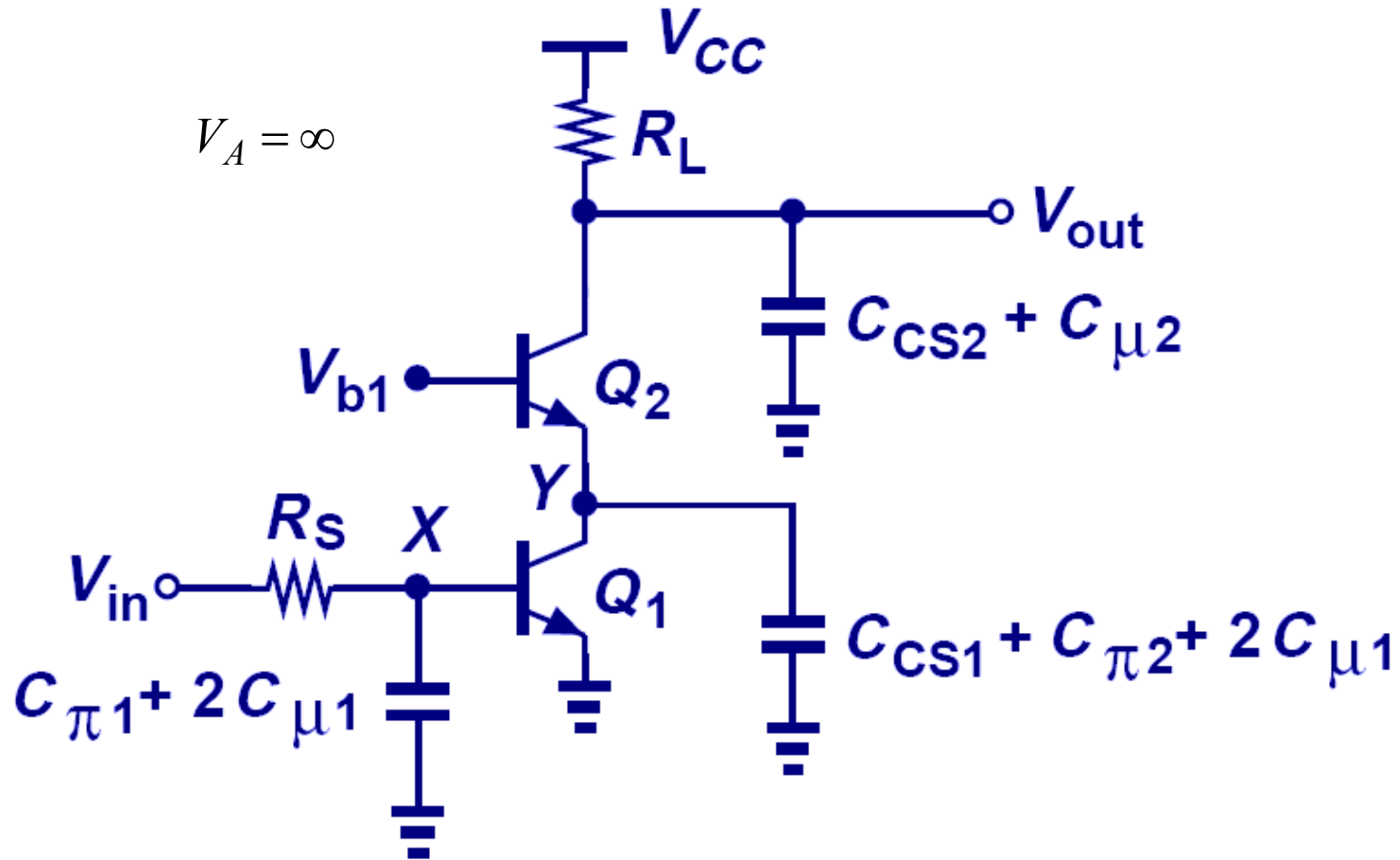
$$\omega_{p,out} = \frac{1}{R_L (C_{DB2} + C_{GD2})}$$



- Allows for a smaller M_2
 - Improves output pole
 - Lowers poles at nodes X and Y, but they should still be relatively high

$$\omega_{p,Y} = \frac{1}{\frac{1}{g_{m2}} \left[C_{DB1} + C_{GS2} + \left(1 + \frac{g_{m2}}{g_{m1}} \right) C_{GD1} + C_{GD3} + C_{DB3} \right]}$$

I/O Impedance of Bipolar Cascode

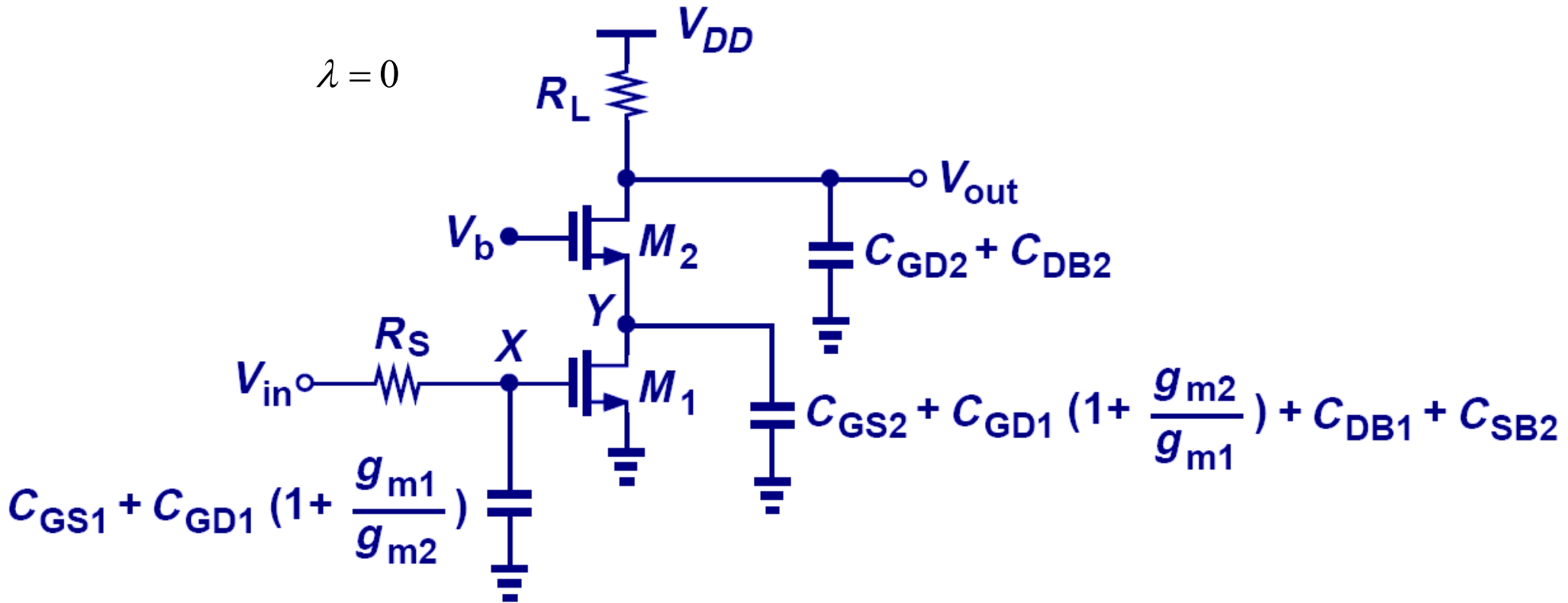


$$Z_{in} = r_{\pi 1} \parallel \frac{1}{(C_{\pi 1} + 2C_{\mu 1})s}$$

(Neglecting R_S)

$$Z_{out} = R_L \parallel \frac{1}{(C_{\mu 2} + C_{CS2})s}$$

I/O Impedance of MOS Cascode



$$Z_{in} = \frac{1}{\left[C_{GS1} + \left(1 + \frac{g_{m1}}{g_{m2}}\right) C_{GD1} \right] s}$$

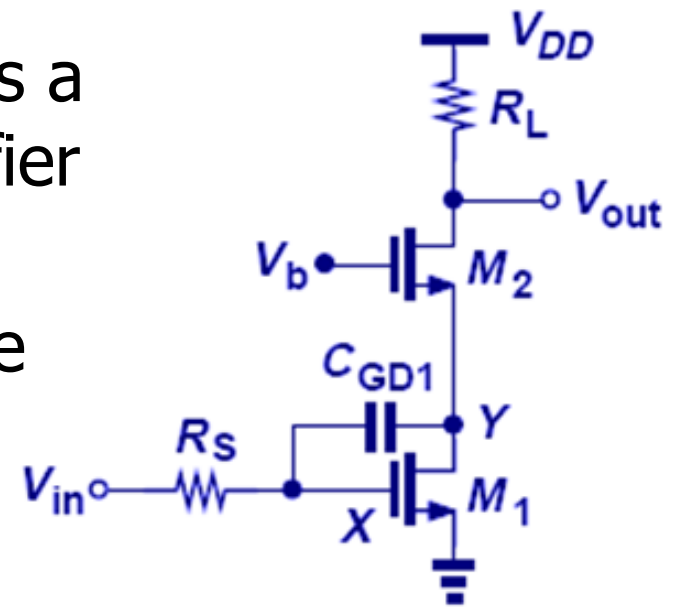
(Neglecting R_S)

$$Z_{out} = R_L \parallel \frac{1}{(C_{GD2} + C_{DB2})s}$$

Cascode Frequency Response

Take-Away Points

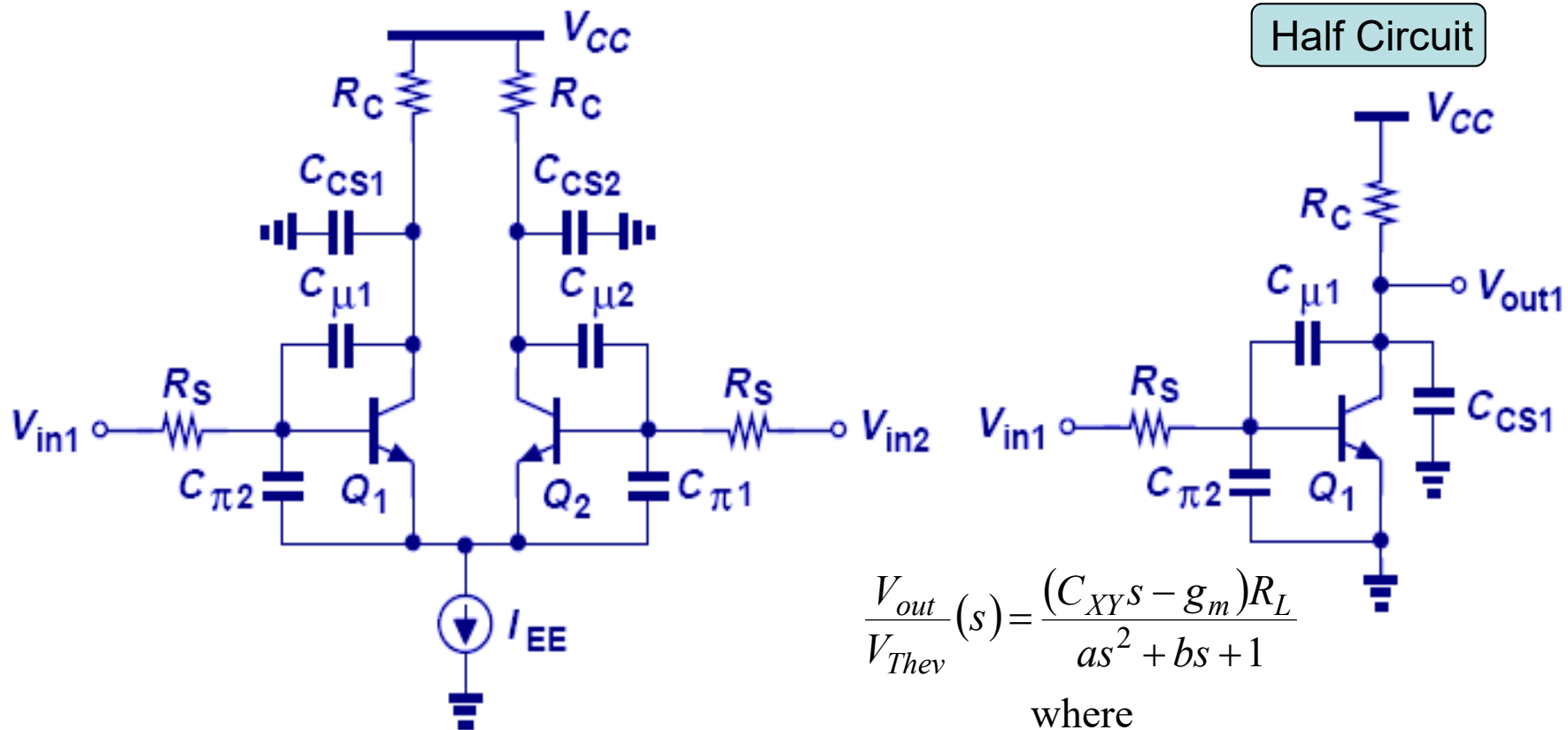
- Cascode amplifiers offer two good properties
 - High output impedance to serve as a good current source and/or amplifier
 - Reduction of the Miller effect and better high-frequency performance
- Main cost is higher voltage headroom to keep cascode transistor in saturation
 - Impacts maximum output swing and distortion performance



Agenda

- Frequency Response Concepts
- High-Frequency Models of Transistors
- Frequency Response Analysis Procedure
- CE and CS Stages
- CB and CG Stages
- CC and CD (Follower) Stages
- Cascode Stages
- **Differential Pairs**
- Additional Examples

Bipolar Differential Pair Frequency Response



$$\frac{V_{out}}{V_{Thev}}(s) = \frac{(C_{XY}s - g_m)R_L}{as^2 + bs + 1}$$

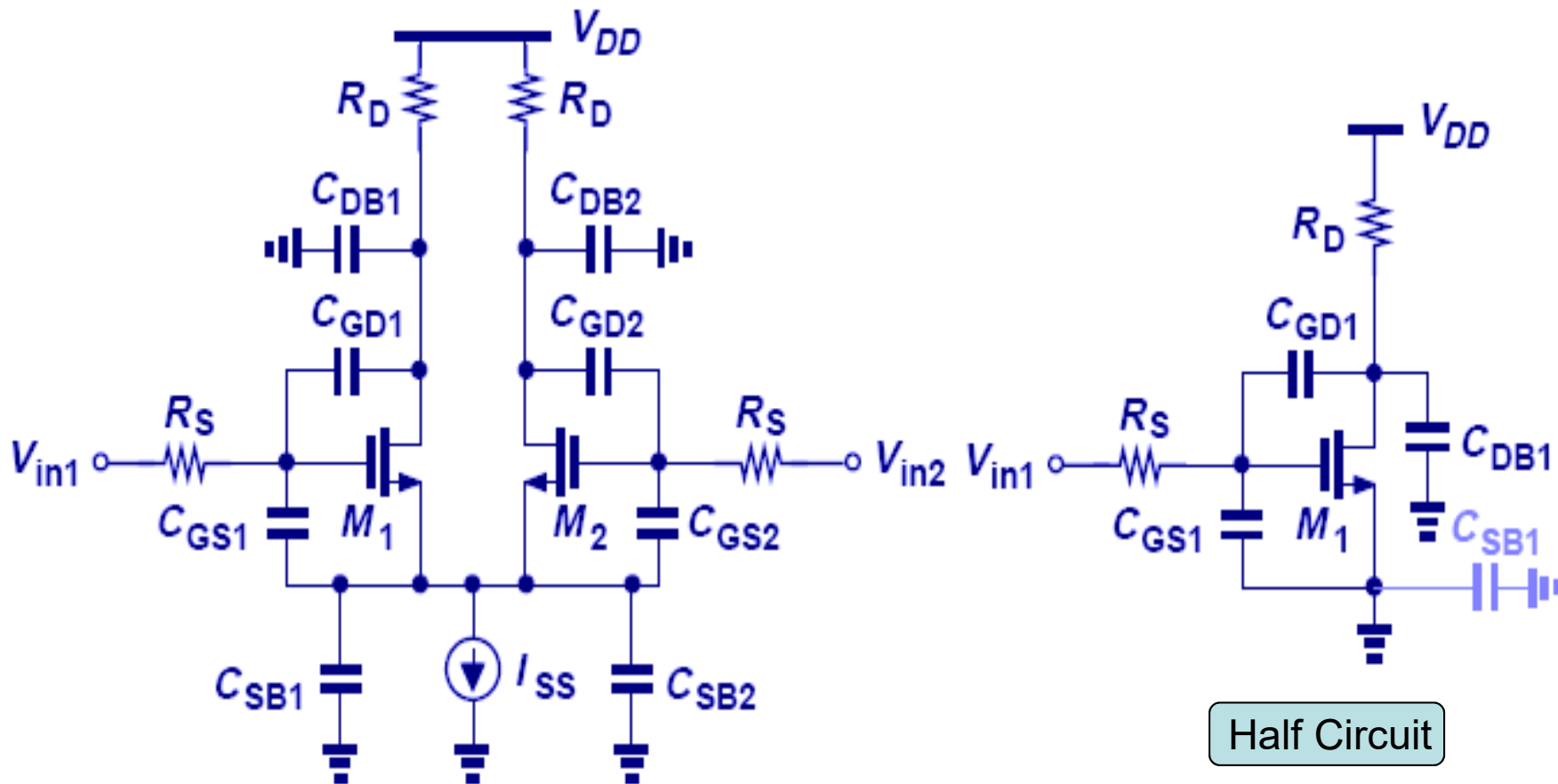
where

$$a = R_{Thev}R_L(C_{in}C_{XY} + C_{out}C_{XY} + C_{in}C_{out})$$

$$b = (1 + g_m R_L)C_{XY}R_{Thev} + R_{Thev}C_{in} + R_L(C_{XY} + C_{out})$$

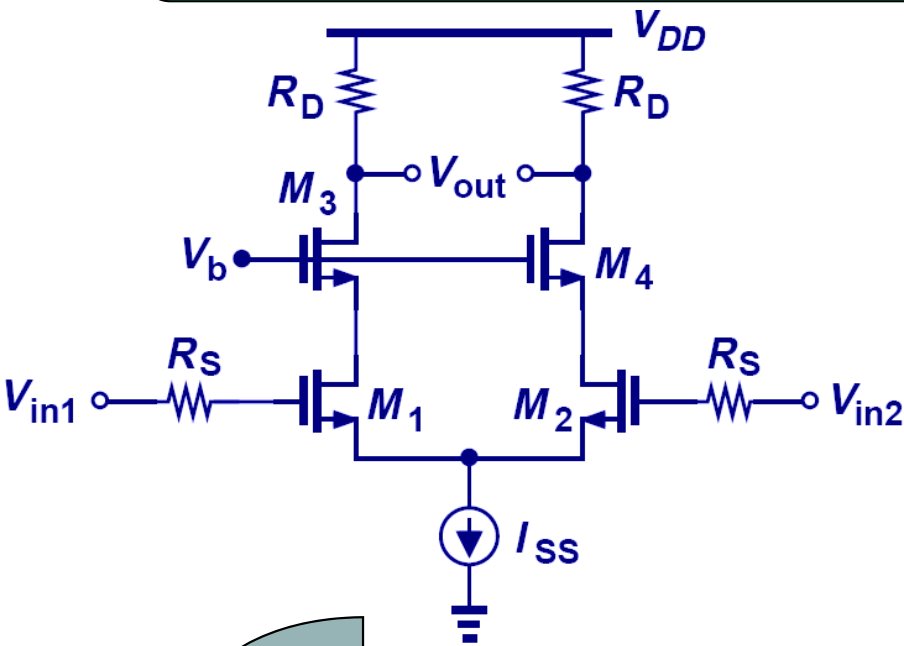
- Since bipolar differential pair can be analyzed using half-circuit, its transfer function, I/O impedances, locations of poles/zeros are the same as that of the half circuit's (Slide 43).

MOS Differential Pair Frequency Response



- Since MOS differential pair can be analyzed using half-circuit, its transfer function, I/O impedances, locations of poles/zeros are the same as that of the half circuit's (Slide 43).

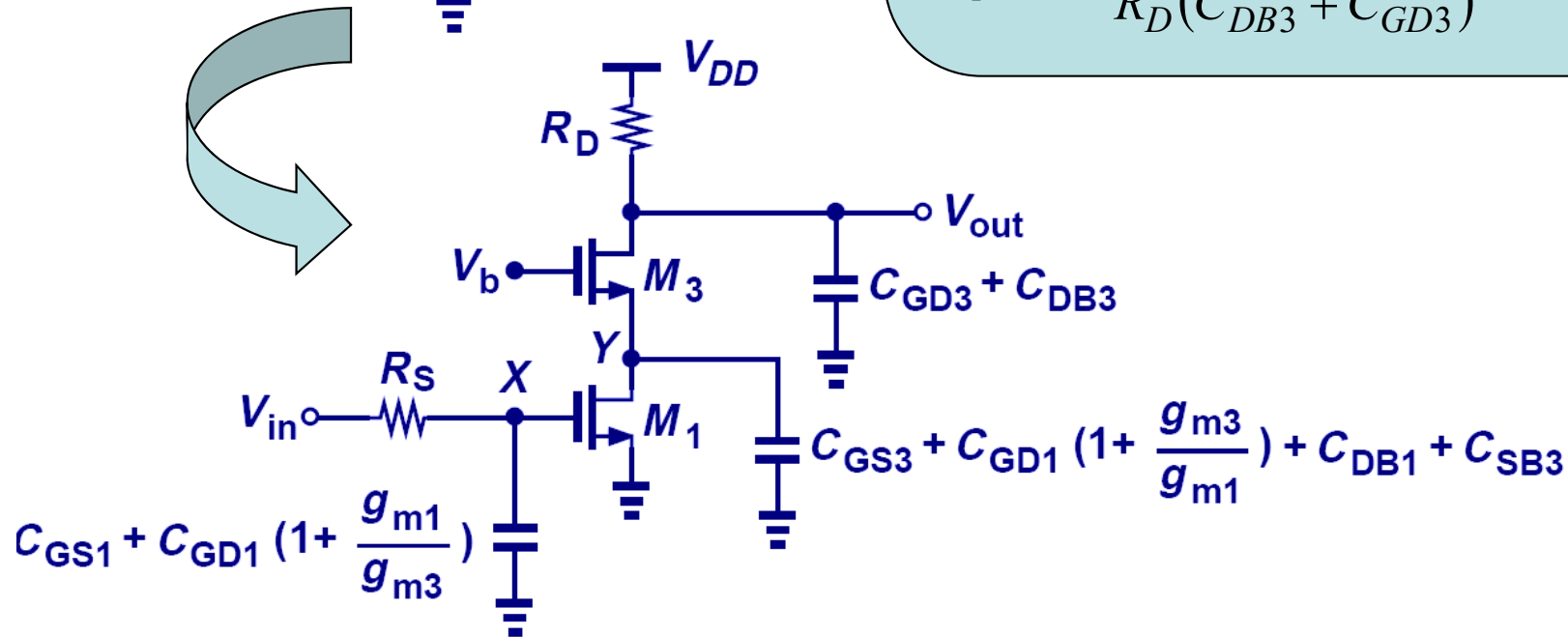
Example: MOS Differential Pair



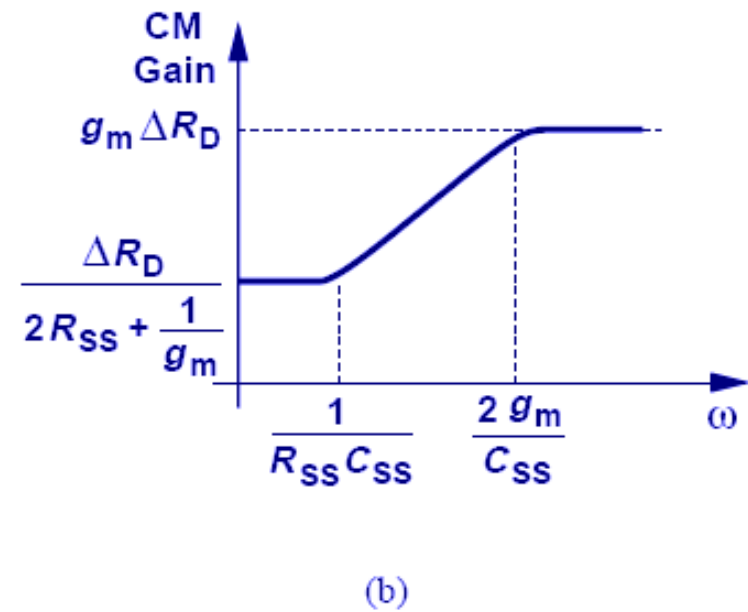
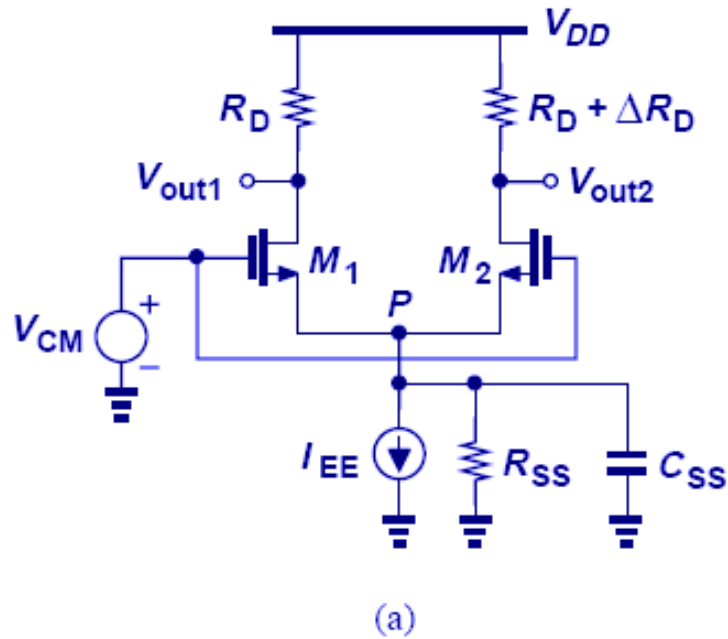
$$\omega_{p,X} = \frac{1}{R_S [C_{GS1} + (1 + g_{m1}/g_{m3})C_{GD1}]}$$

$$\omega_{p,Y} = \frac{1}{\frac{1}{g_{m3}} \left[C_{DB1} + C_{GS3} + \left(1 + \frac{g_{m3}}{g_{m1}} \right) C_{GD1} + C_{SB3} \right]}$$

$$\omega_{p,out} = \frac{1}{R_D (C_{DB3} + C_{GD3})}$$



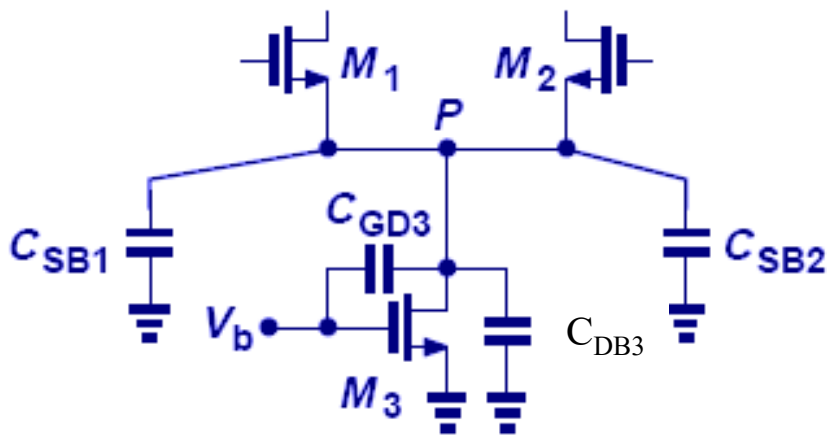
Common Mode Frequency Response



$$\left| \frac{\Delta V_{out}}{\Delta V_{CM}} \right| = \frac{\Delta R_D}{\frac{1}{g_m} + 2 \left(R_{SS} \parallel \frac{1}{C_{SS}s} \right)} = \frac{g_m \Delta R_D (R_{SS} C_{SS} s + 1)}{R_{SS} C_{SS} s + 2g_m R_{SS} + 1}$$

➤ C_{SS} will lower the total impedance between point P to ground at high frequency, leading to higher CM gain which degrades the CM rejection ratio.

Tail Node Capacitance Contribution



- Source-Body Capacitance of M_1, M_2
- Drain-Body Capacitance of M_3
- Gate-Drain Capacitance of M_3

- M_3 is often a large (wide) transistor in order to have a small compliance (V_{DS}) voltage
 - Watch out for degraded high-frequency CMRR!

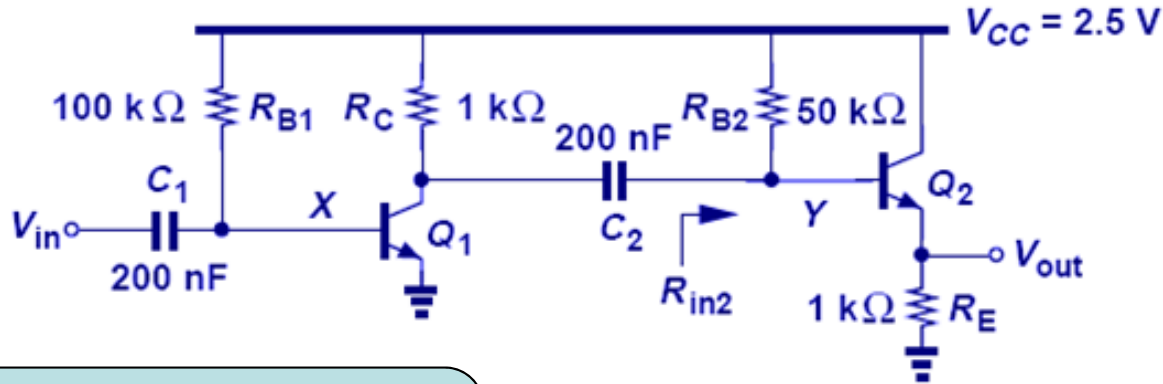
Agenda

- Frequency Response Concepts
- High-Frequency Models of Transistors
- Frequency Response Analysis Procedure
- CE and CS Stages
- CB and CG Stages
- CC and CD (Follower) Stages
- Cascode Stages
- Differential Pairs
- **Additional Examples**

Example: Capacitive Coupling (Low-Frequency Cut-Off)

$$I_{C1} = 1.75mA$$

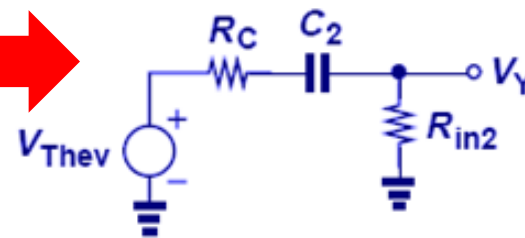
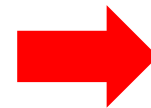
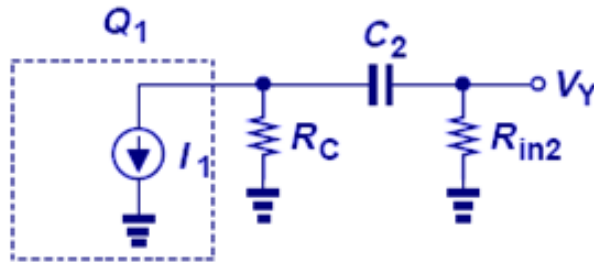
$$I_{C2} = 1.13mA$$



$$\omega_{L1} = \frac{1}{(r_{\pi1} \parallel R_{B1})C_1} = 2\pi \times (542Hz)$$

The "highest" low-frequency pole ($\omega_{L1} = 542Hz$) will set the low-frequency cut-off

To find ω_{L2} :



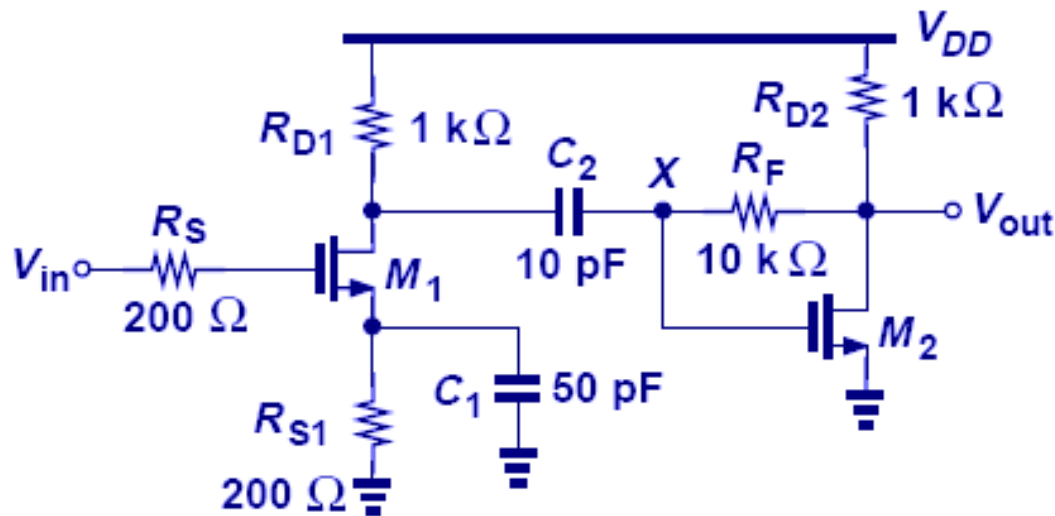
$$\frac{V_Y}{V_{Thev}}(s) = \frac{R_{in2}}{R_C + \frac{1}{sC_2} + R_{in2}} = \frac{sC_2 R_{in2}}{1 + sC_2(R_C + R_{in2})}$$

$$R_{in2} = R_{B2} \parallel [r_{\pi2} + (\beta + 1)R_E]$$

$$\omega_{L2} = \frac{1}{(R_C + R_{in2})C_2} = \pi \times (22.9Hz)$$

Example: IC Amplifier – Low Frequency Design

$$g_{m1} = g_{m2} = (150\Omega)^{-1}$$



$$\omega_{L2} = \frac{1}{(R_{D1} + R_{in2})C_2} = 2\pi \times (6.92\text{MHz})$$

$$R_{in2} = \frac{R_F}{1 - A_{v2}}$$

$$A_{v2} = -g_{m2}R_{D2} = -\frac{1\text{k}\Omega}{150\Omega} = -6.67$$

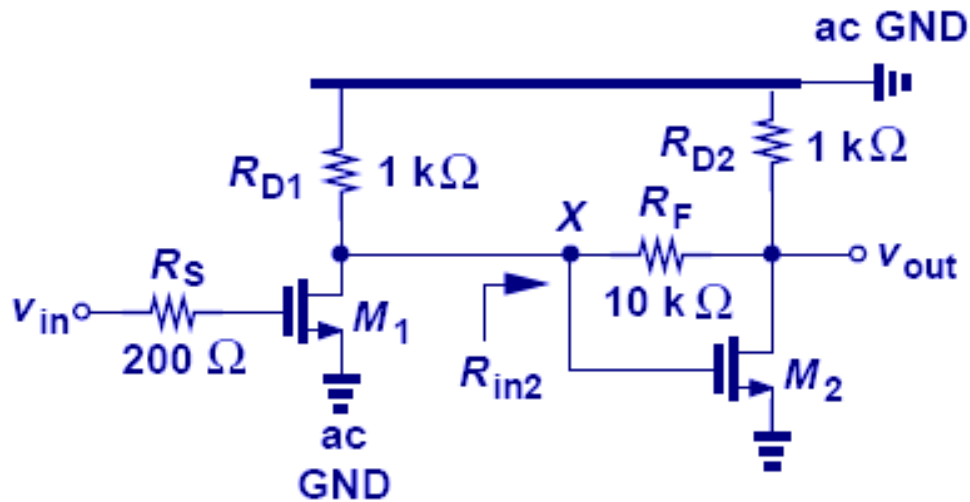
$$R_{in2} = \frac{10\text{k}\Omega}{7.67} = 1.30\text{k}\Omega$$

$$\omega_{L1} = \frac{1}{\left(\frac{1}{g_{m1}} \parallel R_{S1}\right)C_1} = \frac{g_{m1}R_{S1} + 1}{R_{S1}C_1} = 2\pi \times (37.2\text{MHz})$$

The "highest" low-frequency pole ($\omega_{L1} = 37.2\text{MHz}$) will set the low-frequency cut-off

Example: IC Amplifier – Midband Design

$$g_{m1} = g_{m2} = (150\Omega)^{-1}$$

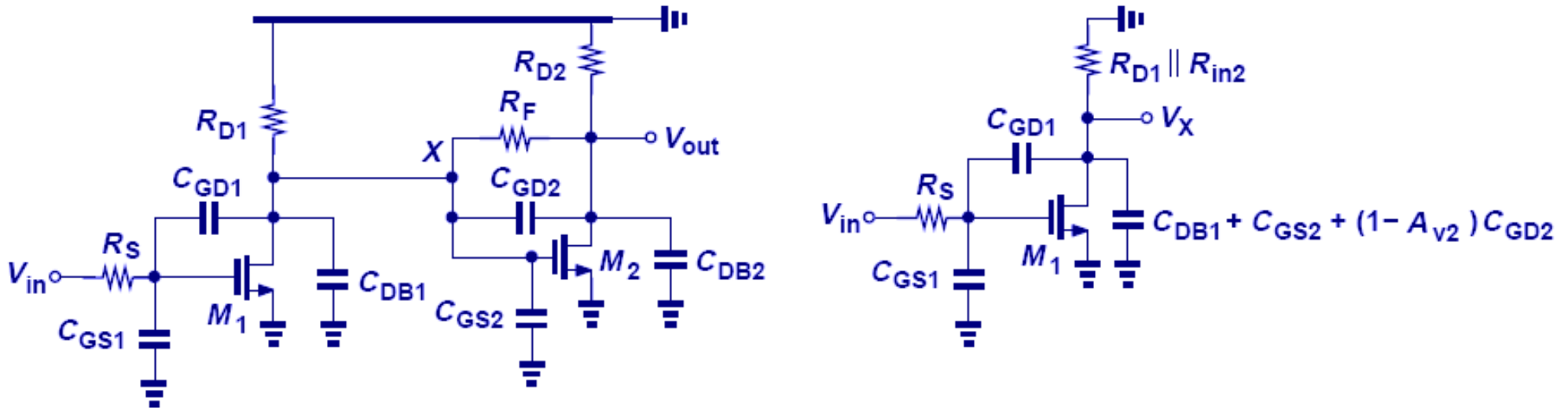


$$A_{v1} = \frac{v_X}{v_{in}} = -g_{m1}(R_{D1} \parallel R_{in2}) = -3.77$$

$$A_{v2} = -6.67$$

$$A_v = A_{v1}A_{v2} = 25.1 = 28.0dB$$

Example: IC Amplifier – High Frequency Design



To get an accurate estimate for ω_{p1} and ω_{p2} , use the dominant pole approximation expressions on Slide 44

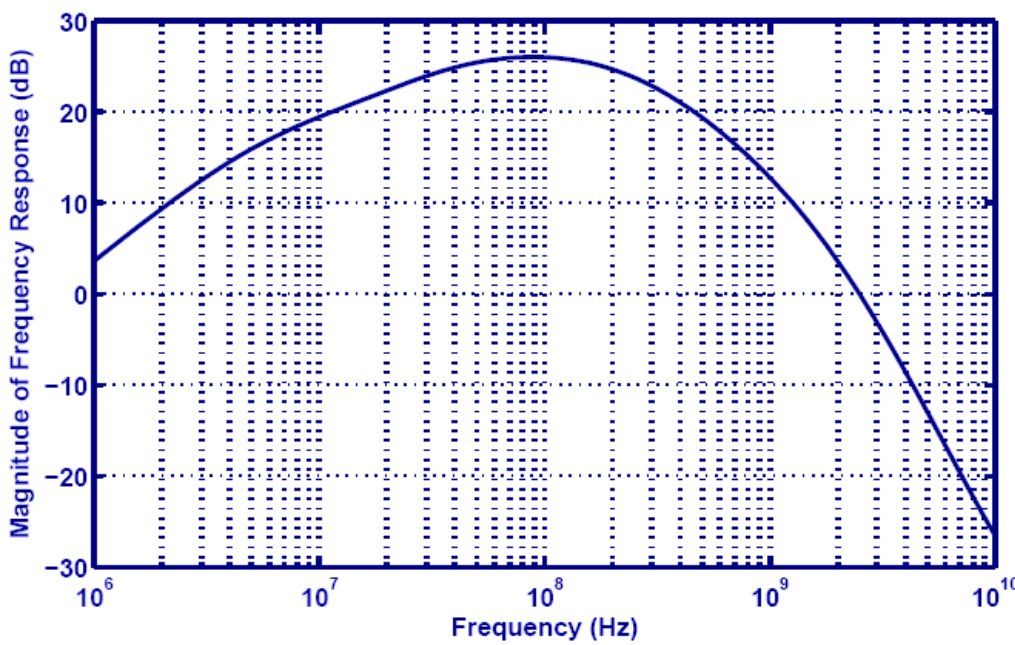
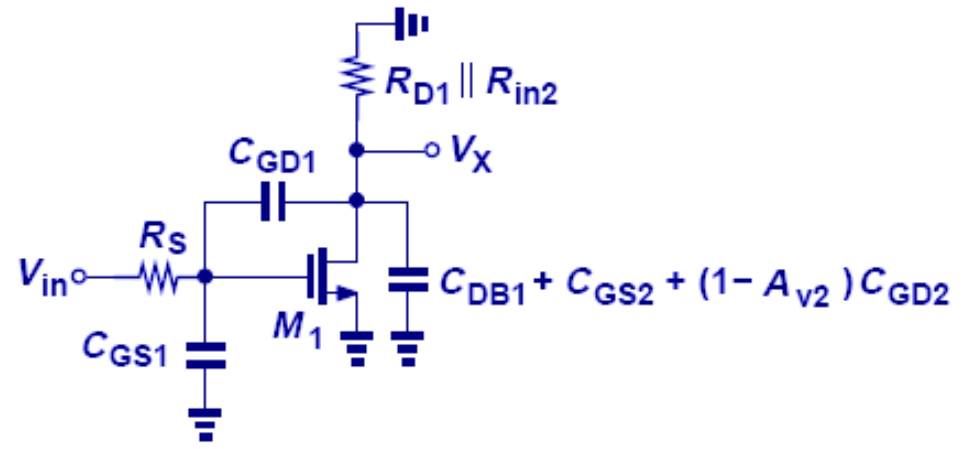
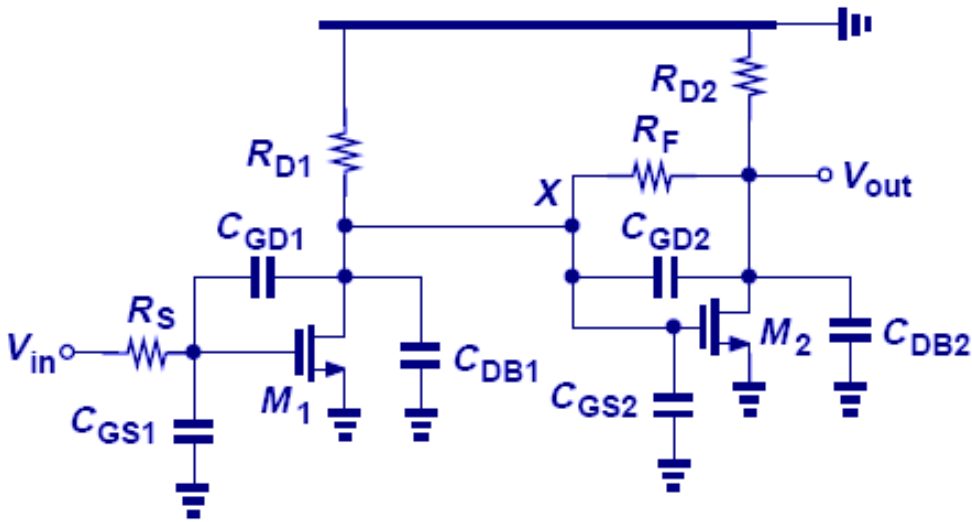
$$|\omega_{p1}| = \frac{1}{(1 - A_{v1})C_{GD1}R_S + R_S C_{GS1} + (R_{D1} \parallel R_{in2})(C_{GD1} + C_{out1})} = 2\pi(222\text{MHz})$$

$$|\omega_{p2}| = \frac{(1 - A_{v1})C_{GD1}R_S + R_S C_{GS1} + (R_{D1} \parallel R_{in2})(C_{GD1} + C_{out1})}{R_S(R_{D1} \parallel R_{in2})(C_{GS1}C_{GD1} + C_{GD1}C_{out1} + C_{GS1}C_{out1})} = 2\pi(2.99\text{GHz})$$

where

$$C_{out1} = C_{DB1} + C_{GS2} + C_{GD2}(1 - A_{v2})$$

Example: IC Amplifier – High Frequency Design



$$|\omega_{p1}| = 2\pi(222\text{MHz})$$

$$|\omega_{p2}| = 2\pi(2.99\text{GHz})$$

$$|\omega_{p3}| = \frac{1}{R_{D2} \left[C_{GD2} \left(1 - \frac{1}{A_{v2}} \right) + C_{DB2} \right]} = 2\pi(829\text{MHz})$$

Next Time

- Feedback
 - Razavi Chapter 12