ECEN326: Electronic Circuits
Spring 2022

Lecture 8: Output Stages and Power Amplifiers

Sam Palermo
Analog & Mixed-Signal Center
Texas A&M University

Announcements

- Homework 8 due Apr 28
- Exam 3 May 5
  - 12:30 – 2:30
  - Closed book w/ one standard note sheet
  - 8.5”x11” front & back
  - Bring your calculator
  - Emphasis will be on Lectures 7-8
  - Sample Exam3s posted on website
- Reading
  - Razavi Chapter 14

Agenda

- General Output Stage Considerations
- Emitter Follower as a Power Amplifier
- Push-Pull Stage
- Improved Push-Pull Stage
- Large-Signal Considerations
- Heat Dissipation
- Efficiency and Power Amplifier Classes

Why Special Output Stages or Power Amplifiers?

- Power amplifiers are necessary to efficiently drive a load with high power
- Examples
  - A cellphone may need 1W of power at the antenna
  - Audio systems require tens to hundreds of Watts
- As ordinary voltage/current amplifiers are not suited for efficiently supporting these power levels, specialized output stages are necessary

Power Amplifier Characteristics

- Can drive a small "heavy" load resistance
  - Example: Speaker resistance can be 4-16Ω
- Delivers large current levels
  - Often in the hundreds of mA
- Requires large voltage swings
- Draws a large amount of power from the supplies
- Dissipates a large amount of power, and thus can get **hot**

Example: Delivering 1W to an 8Ω speaker

$$\text{Sinusoidal } P_{out} = \left(\frac{V_P}{\sqrt{2}}\right)^2 \cdot \frac{1}{R_L} = 1W$$

This results in a peak voltage

$$V_P = 4V$$

and a peak current

$$I_P = \frac{V_P}{R_L} = \frac{4V}{8\Omega} = 500mA$$

Power Amplifier Performance Metrics

- Linearity or Distortion
  - Audio amplifiers must have low distortion to reproduce music with high fidelity
- Power Efficiency

$$\eta = \frac{\text{Power Delivered to Load}}{\text{Power Drawn from Supply}}$$

- Maximum Voltage Rating
  - May require high power supplies
  - Transistors must have sufficiently high breakdown voltages

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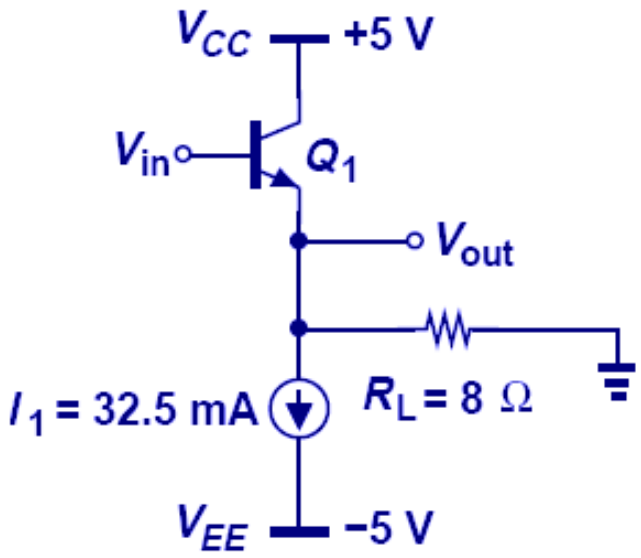
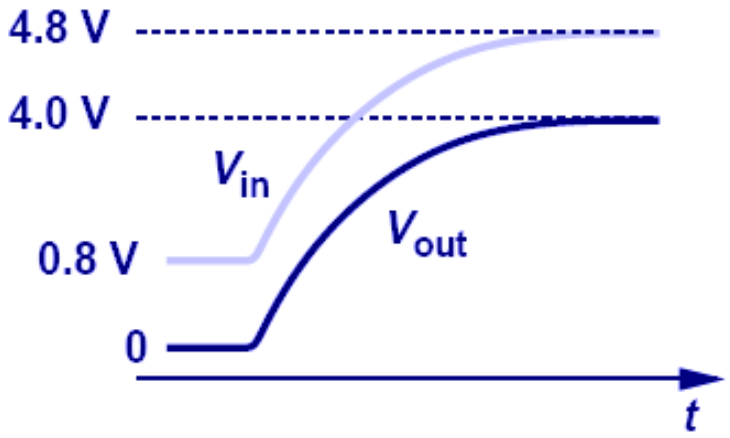
Emitter Follower Large-Signal Behavior: Positive Half-Cycle



(a)

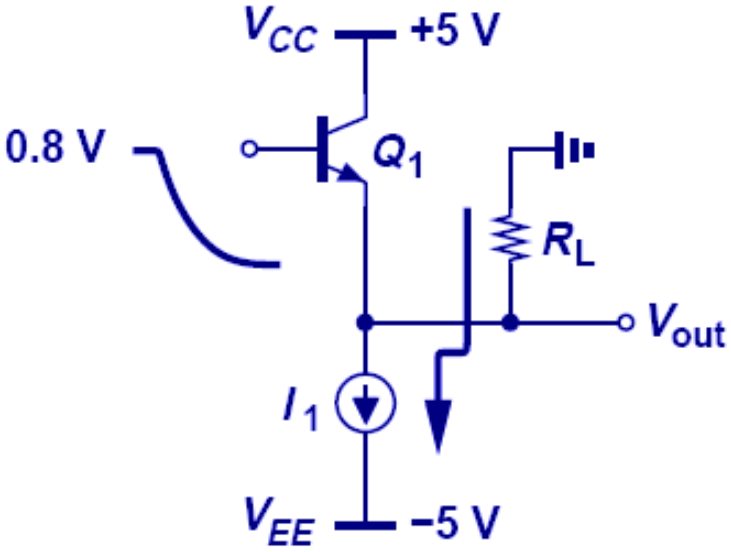
Here V_{BE} is assumed to be 0.8V due to the high current levels



(b)

- As V_{in} increases V_{out} also follows and Q_1 provides more current
- No major issue with the input signal positive half-cycle

Emitter Follower Large-Signal Behavior: Negative Half-Cycle



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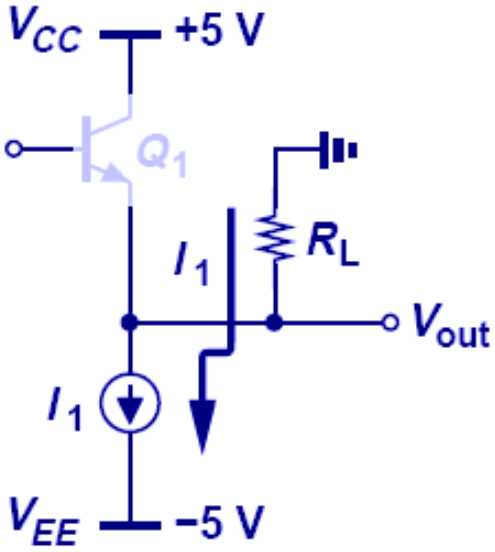
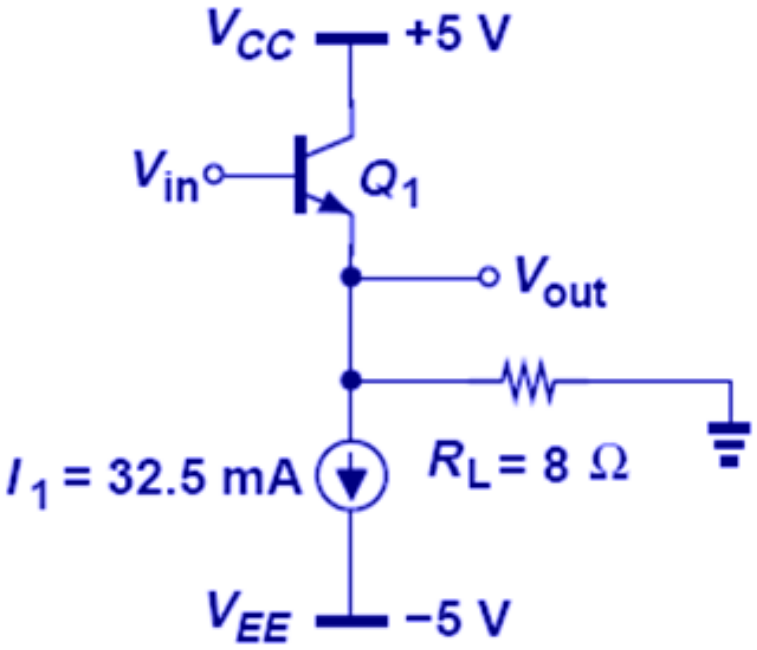


(d)

- However as V_{in} decreases, V_{out} also decreases, shutting off Q_1 and resulting in a constant V_{out}
- The output signal clips at a minimum value of $-I_1R_L$

Example: Emitter Follower

- What are the input and output voltages when I_{C1} drops to 1% of I_1?



$$\text{Assume } I_S = 5\times10^{-15}\,A$$

$$V_{in} - V_{BE} = V_{out}$$

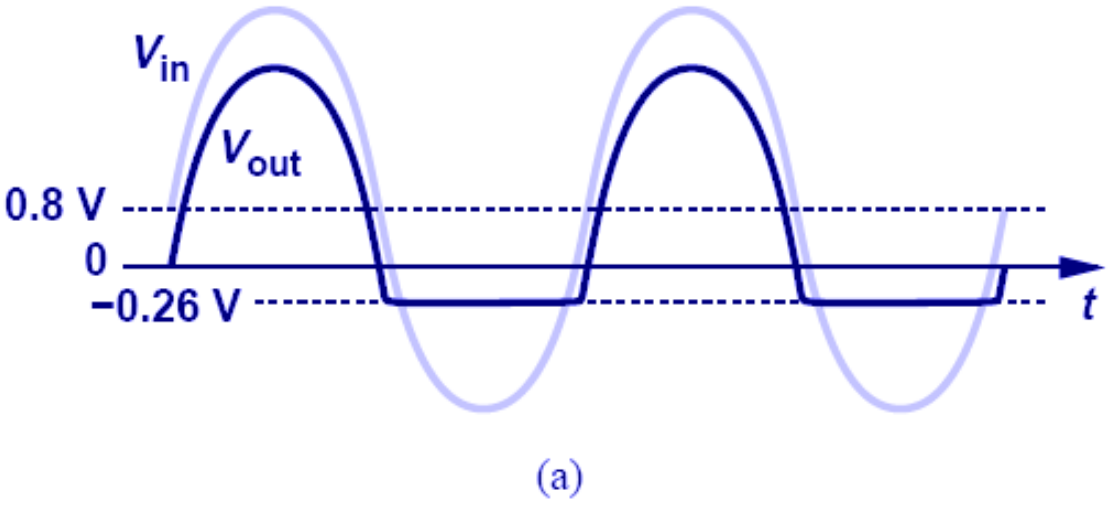
$$V_{in} - V_T \ln\left[\frac{I_{C1}}{I_S}\right] = (I_{C1} - I_1)R_L$$

$$V_{in} = 25.9mV \ln\left[\frac{0.325mA}{5\times10^{-15}\,A}\right] + (0.325mA - 32.5mA)8\Omega = 387mV$$

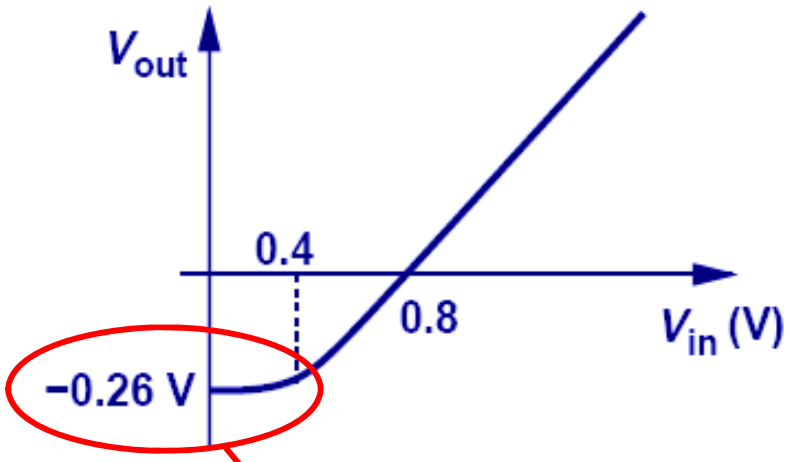
$$V_{out} = 387mV - 25.9mV \ln\left[\frac{0.325mA}{5\times10^{-15}\,A}\right] = -258mV$$

- At this current level, the V_{BE} has dropped to 645mV
- For voltage levels much below 400mV, the output will saturate at $-I_lR_L$ = -260mV

Linearity of an Emitter Follower

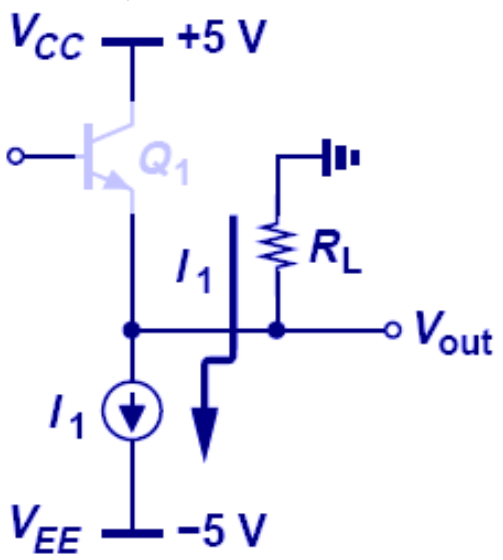


(a)



(b)

- As Vin decreases the output waveform will be clipped, introducing nonlinearity in I/O characteristics
- Overall, the fixed I_1 limits the output swing



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- General Output Stage Considerations
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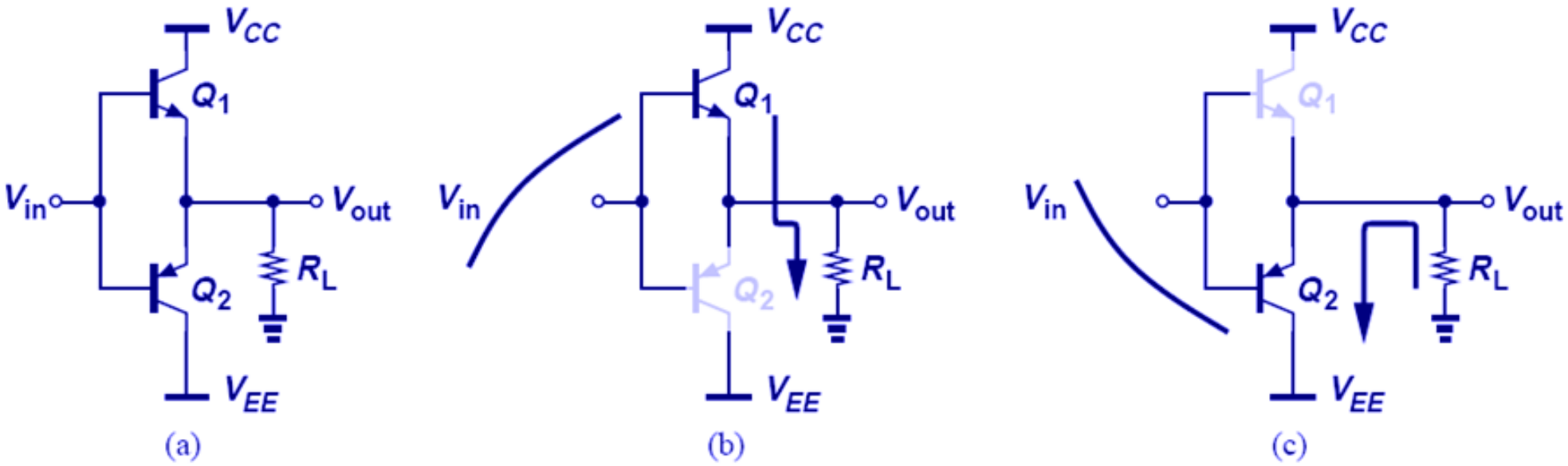
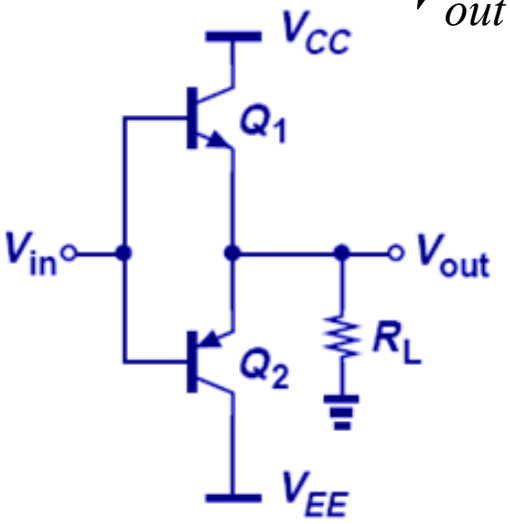
Push-Pull Stage

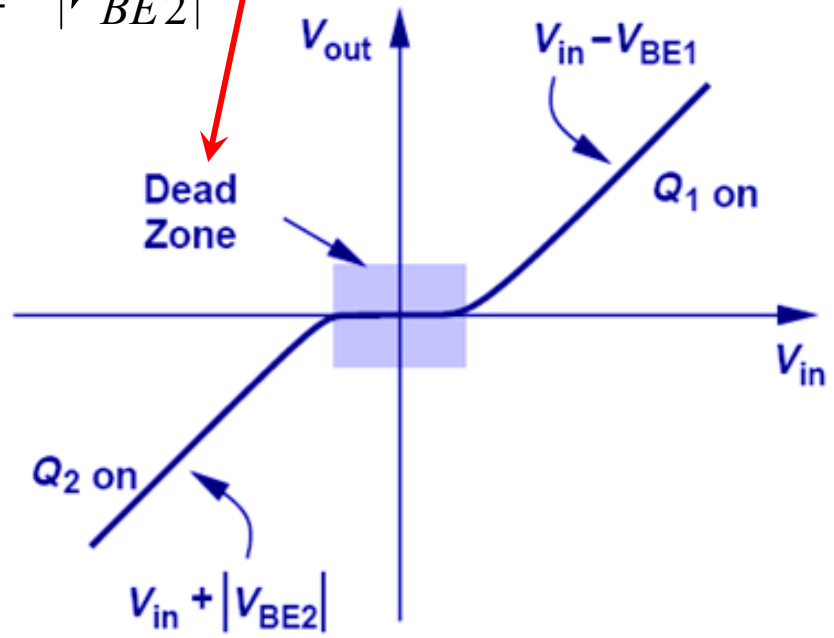


- As V_{in} increases, Q_1 is on and pushes a current into R_L.
- As V_{in} decreases, Q_2 is on and pulls a current out of R_L.
- For positive V_{in}, Q_1 shifts the output down and for negative V_{in}, Q_2 shifts the output up.

Overall I/O Characteristics of Push-Pull Stage

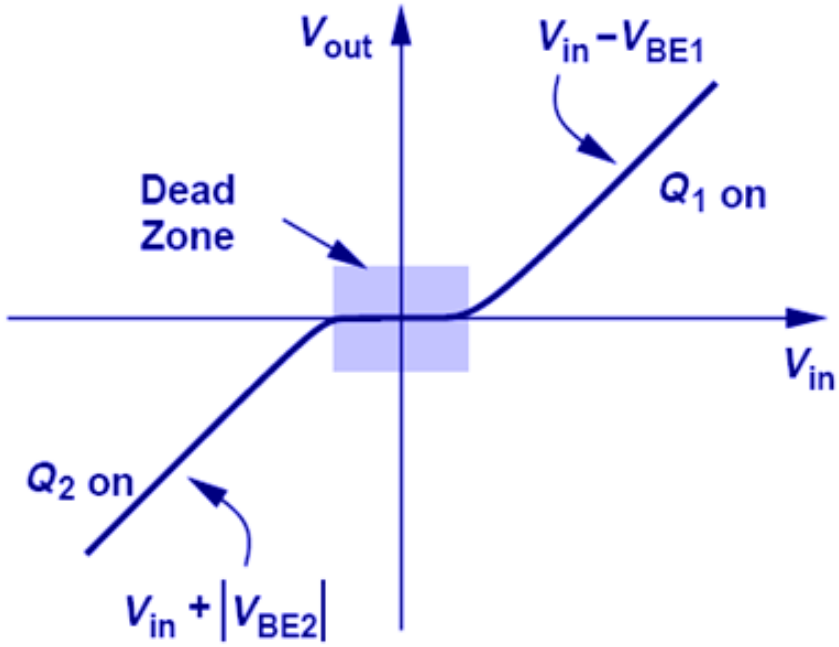
$$V_{out} = \begin{cases} V_{in} - V_{BE1}, & V_{in} \geq V_{BE1} \\ 0, & -|V_{BE2}| \leq V_{in} \leq V_{BE1} \\ V_{in} + |V_{BE2}|, & V_{in} \leq -|V_{BE2}| \end{cases}$$



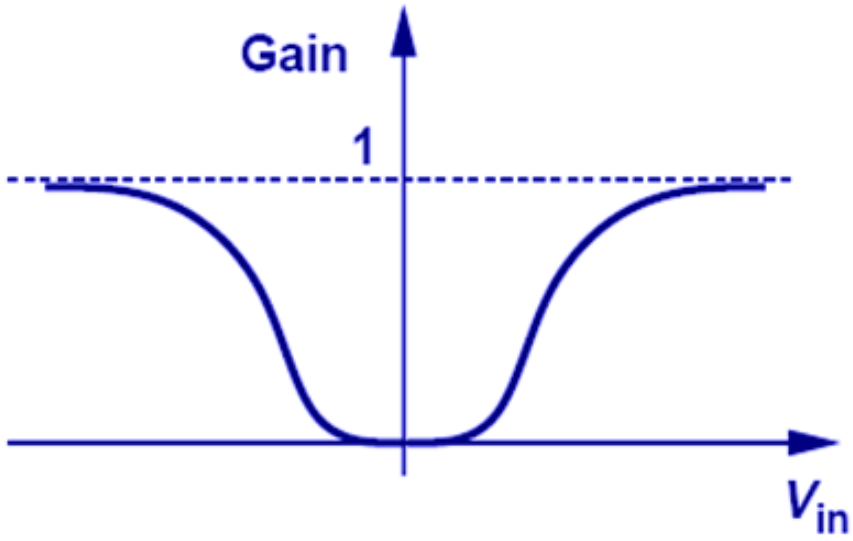


- However, for small V_{in}, there is a dead zone (both Q_1 and Q_2 are off) in the I/O characteristic, resulting in gross nonlinearity
- The dead zone is from $-|V_{BE2}| \leq V_{in} \leq V_{BE1}$

Small-Signal Gain of Push-Pull Stage

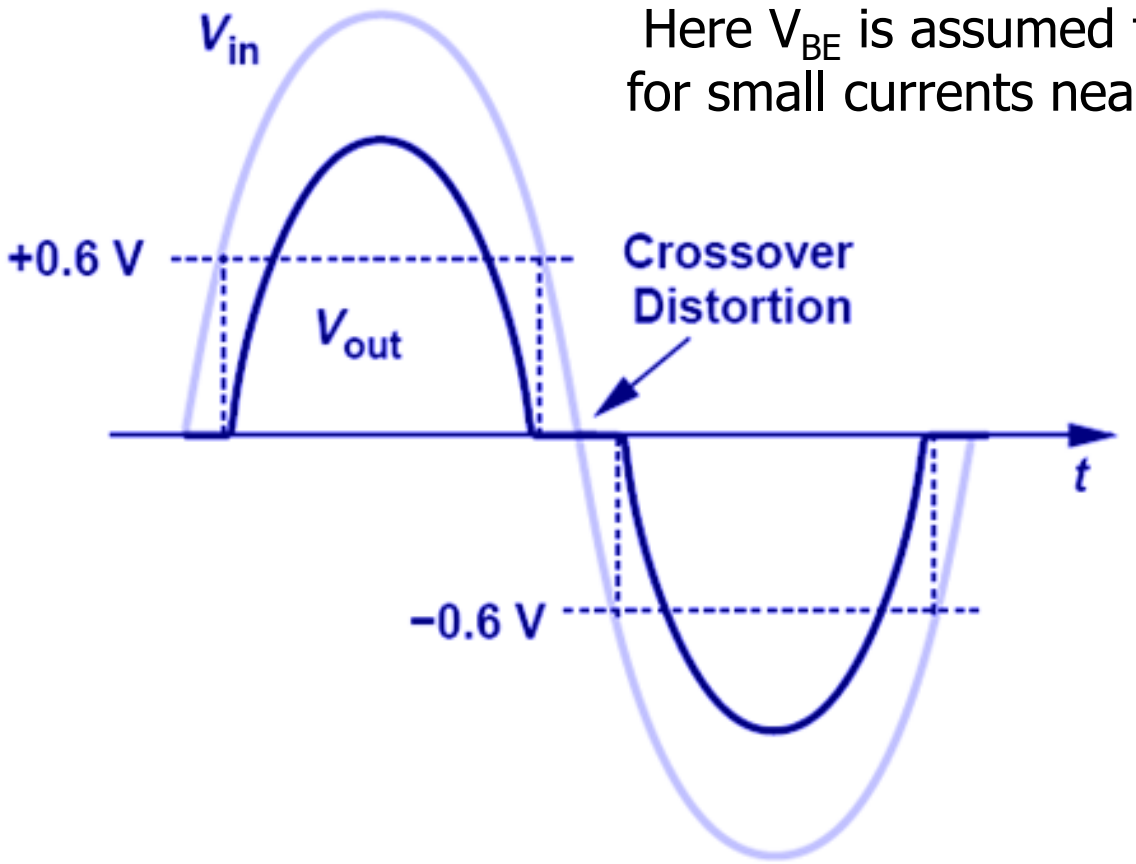


$$A_v = \frac{R_L}{R_L + r_e}$$



- The push-pull stage exhibits a gain that tends to unity when either Q1 or Q2 is on.
- When Vin is very small, the gain drops to zero.

Sinusoidal Response of Push-Pull Stage



Here V_{BE} is assumed to be 0.6V for small currents near crossover

- **For large Vin, the output follows the input with a fixed DC offset, however as Vin becomes small the output drops to zero and causes "Crossover Distortion."**

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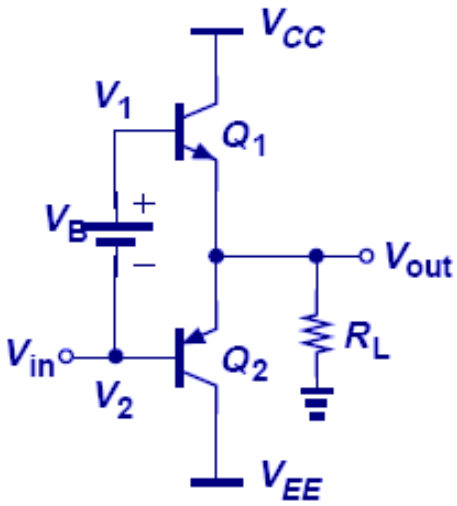
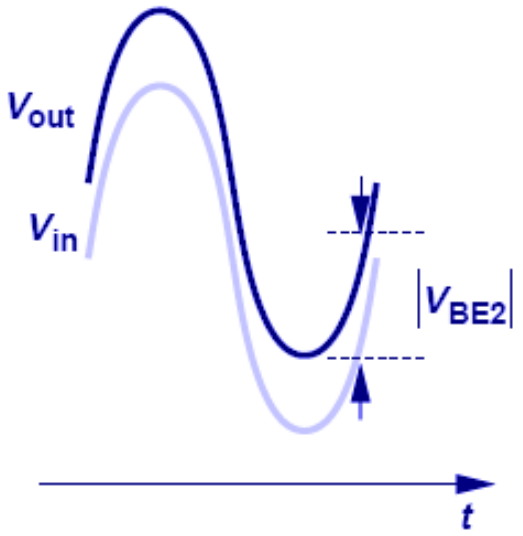
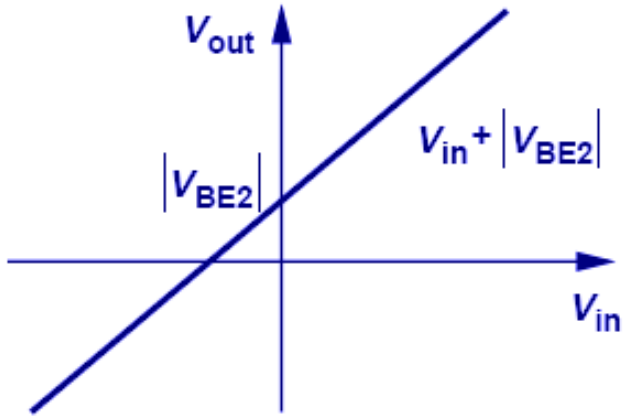
Improved Push-Pull Stage

- **With a battery of V_B inserted between the bases of Q_1 and Q_2, the dead zone is eliminated.**







What should V_B be so that at least one transistor is always on?

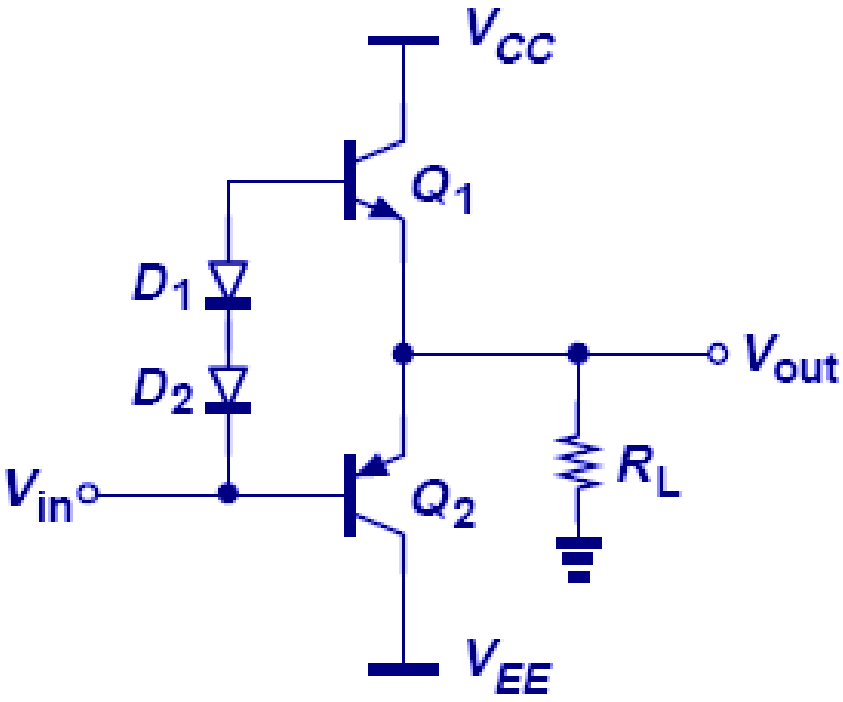
Q_2 turns off when $V_{in} = -|V_{BE2}|$

at this point we want Q_1 on, or $V_1 = V_{BE1}$

Thus, $V_B = V_1 - V_{in} = V_{BE1} - \left(-|V_{BE2}|\right)$

$$\boxed{V_B = V_{BE1} + |V_{BE2}|}$$

Implementation of V_B



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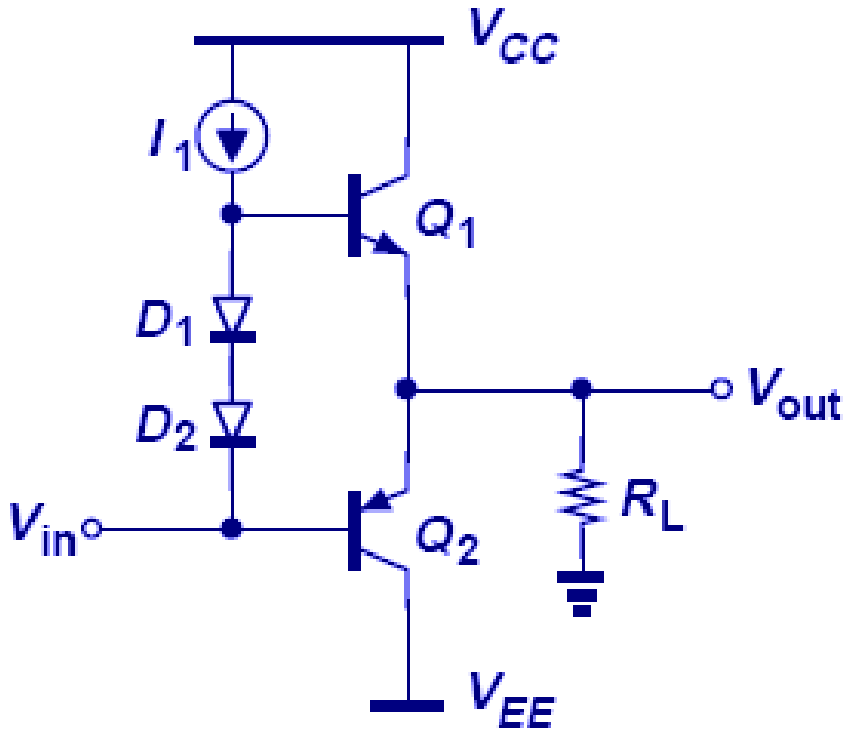
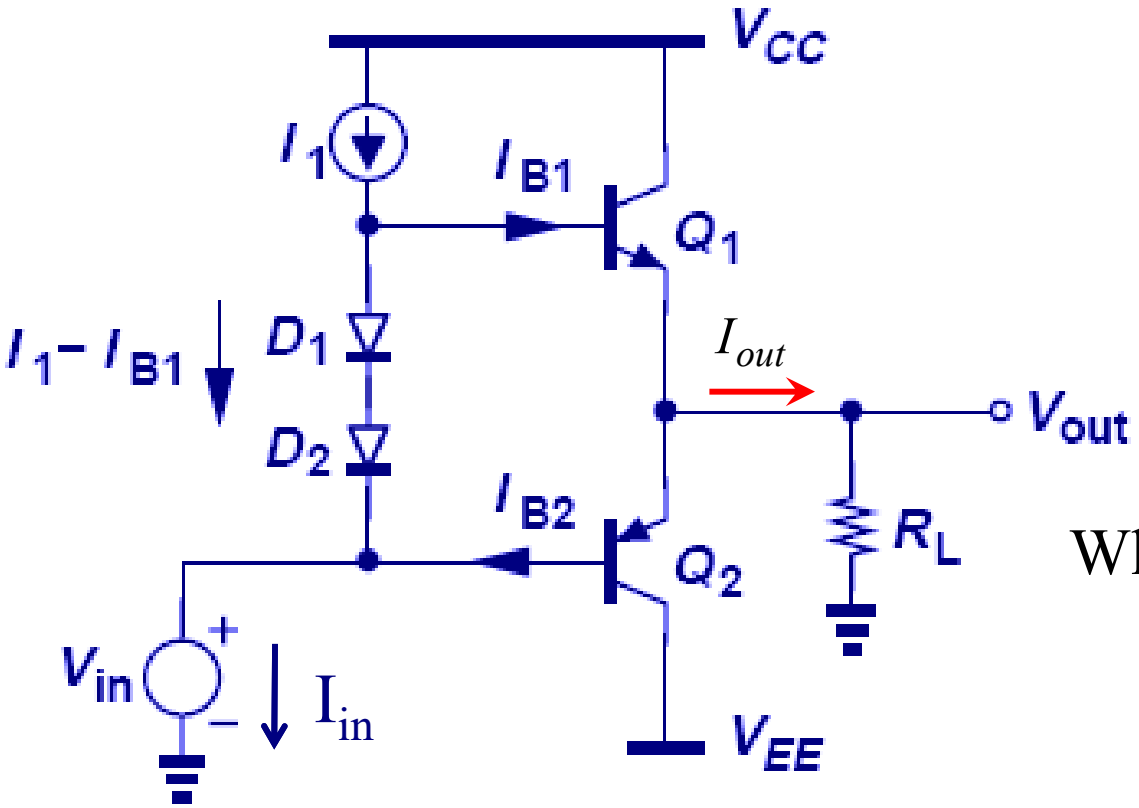


(b)

- Since $V_B=V_{BE1}+|V_{BE2}|$, a natural choice would be two series diodes
- I_1 in figure (b) is used to bias the diodes and Q_1.

Example: Current Flow I



$$I_{in} = I_1 - I_{B1} + I_{B2}$$

When is $I_{in} = I_1$, assuming $\beta_1 = \beta_2$?

This occurs when $I_{B1} = I_{B2}$,

which implies that $I_{C1} = I_{C2}$

and that $I_{out} = 0$

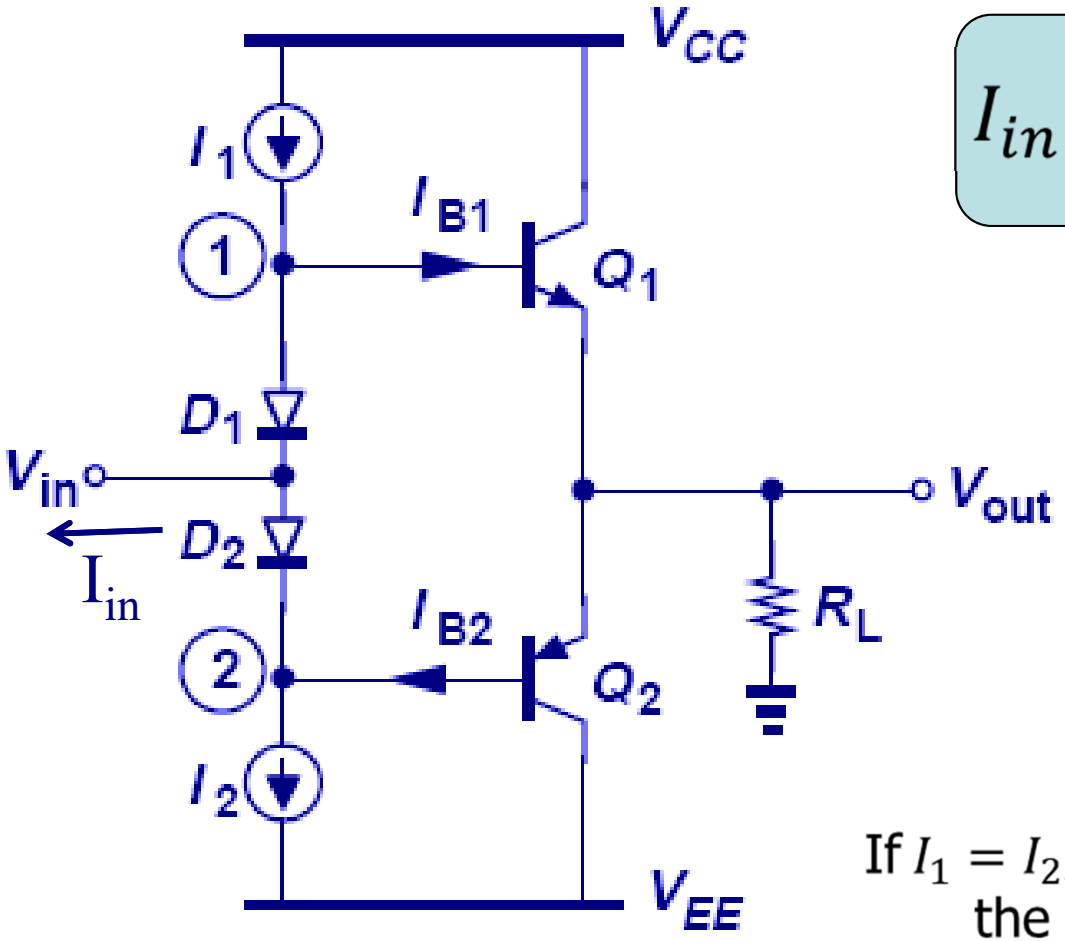
Thus, this occurs when

$$V_{out} = 0$$

The V_{in} source must support I_1 and the Q_1 and Q_2 base current difference, which can excessively load the source

Example: Current Flow II

- The offset between input and output is minimized when the input is in the middle of the diodes



$$I_{in} = (I_1 - I_2) + (I_{B2} - I_{B1})$$

If $V_{D1} \approx V_{BE1}$ and $V_{D2} \approx |V_{BE2}|$,

then $V_{out} \approx V_{in}$

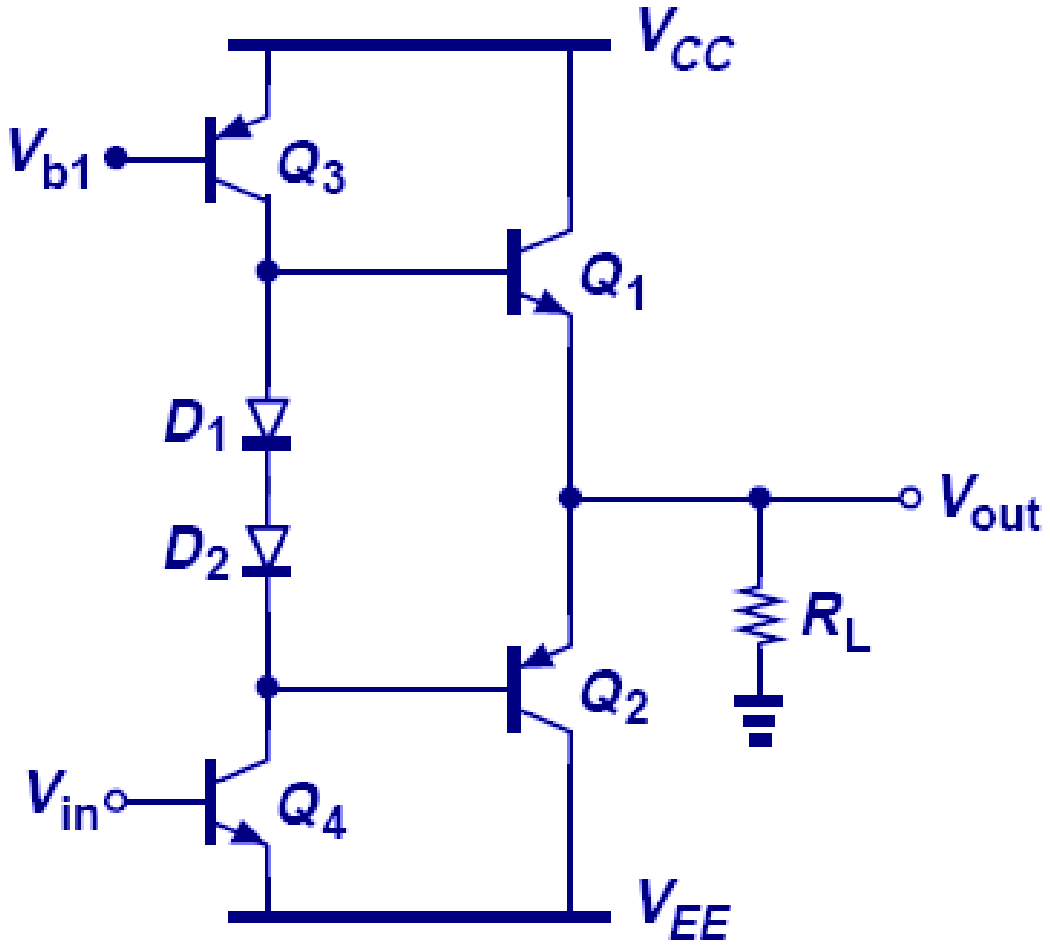
Assuming a balanced design with

$I_1 = I_2$ and $I_{B1} \approx I_{B2}$,

then $I_{in} = 0$ when $V_{out} = 0$

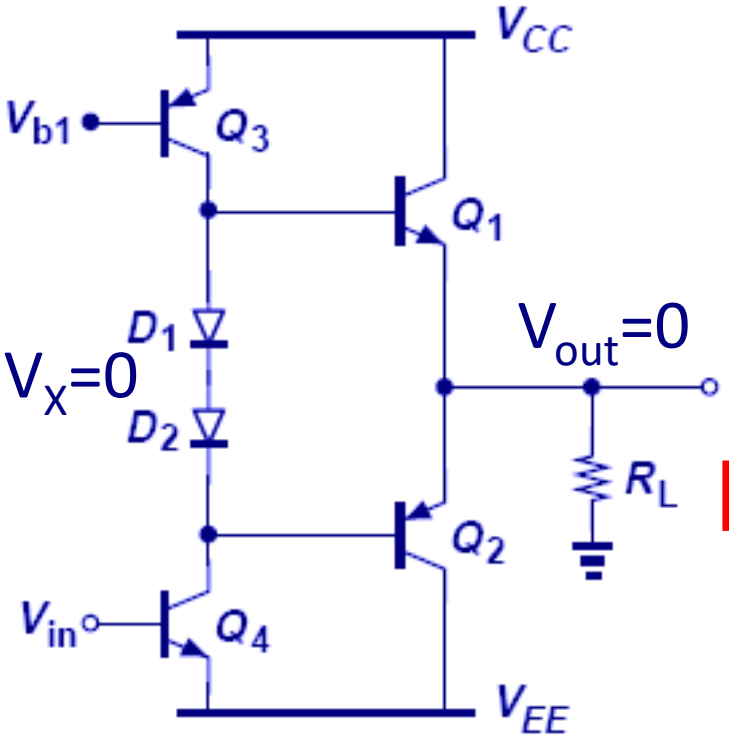
If $I_1 = I_2$, then the V_{in} source must only support the Q_1 and Q_2 base current difference

Addition of CE Stage



- A CE stage (Q_4) is added to provide voltage gain from the input to the bases of Q_1 and Q_2
- This push-pull circuit is often used in high-power output stages

Bias Point Analysis

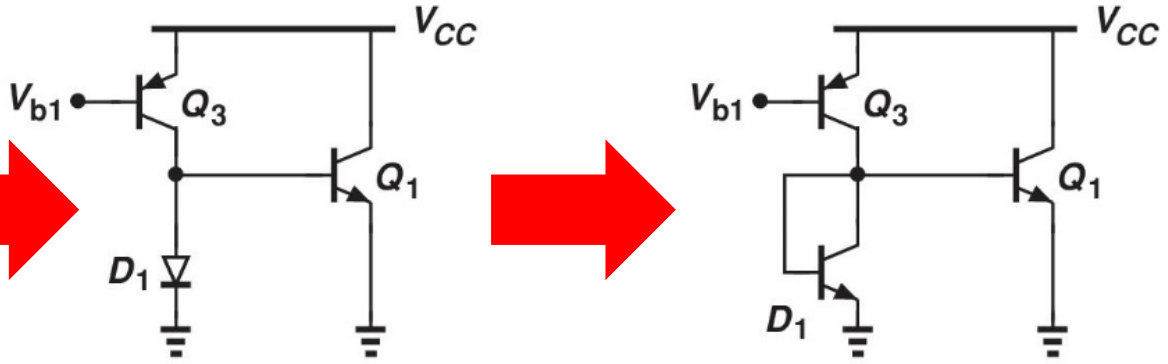


With $V_{out} = 0$ and assuming that

$$I_{C3} = I_{C4}, V_{D1} = V_{BE1}, \text{and } V_{D2} = |V_{BE2}|$$

then the voltage in the middle of the diodes

$V_X = 0$, and we can redraw the top half of the circuit



$$V_{D1} = V_T \ln\left(\frac{|I_{C3}|}{I_{S,D1}}\right) = V_{BE1} = V_T \ln\left(\frac{I_{C1}}{I_{S,Q1}}\right)$$

$$I_{C1} = \left(\frac{I_{S,Q1}}{I_{S,D1}}\right)|I_{C3}|$$

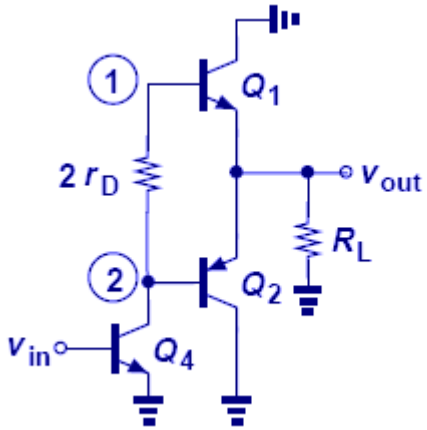
- **For bias point analysis, the circuit can be simplified to the one on the right, which resembles a current mirror**
- **For a well-defined I_S ratio, D_1 can be realized as a diode-connected transistor**

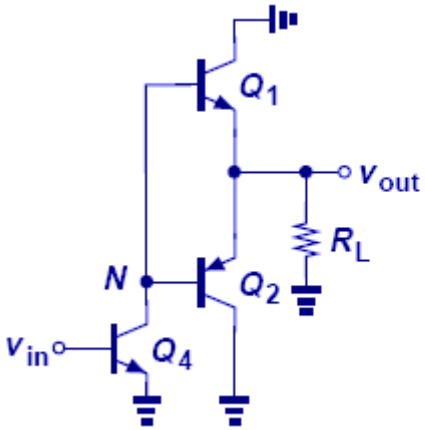
Small-Signal Analysis - I

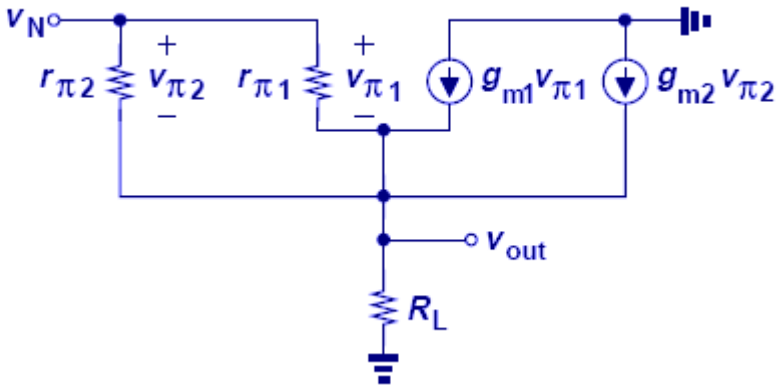
In order to derive the gain of the circuit, we can treat it as a two-stage amplifier

$$\frac{v_{out}}{v_{in}} = \frac{v_N}{v_{in}} \cdot \frac{v_{out}}{v_N}$$

Assuming $V_A = \infty$ and $r_D = 0$, the second stage can be viewed as 2 parallel emitter followers







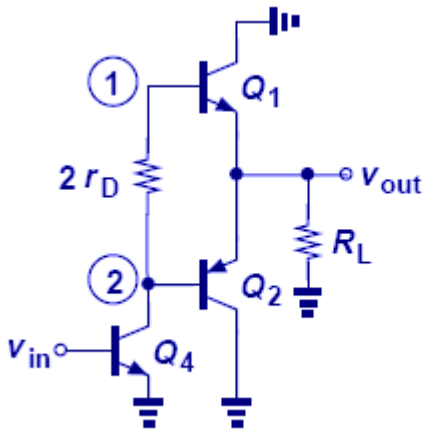
$$\frac{v_{out}}{v_N} = \frac{R_L}{R_L + r_{e1} \| r_{e2}} \approx \frac{R_L}{R_L + \dfrac{1}{g_{m1} + g_{m2}}}$$

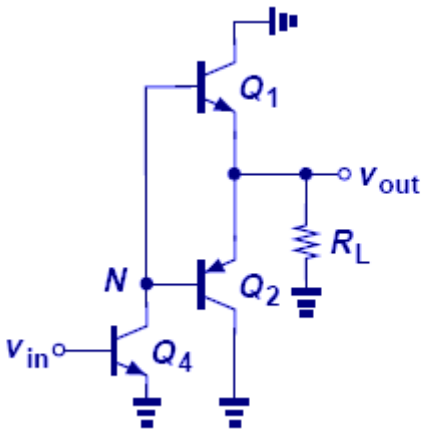
Small-Signal Analysis - II

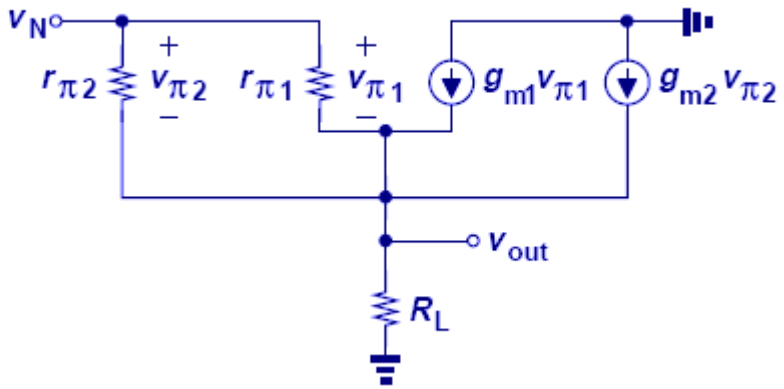
The gain of the first stage can be expressed as

$$\frac{v_N}{v_{in}} = -g_{m4}R_N \quad \text{where}$$

$$R_N = r_{\pi 1} \| r_{\pi 2} + (g_{m1} + g_{m2})(r_{\pi 1} \| r_{\pi 2})R_L$$







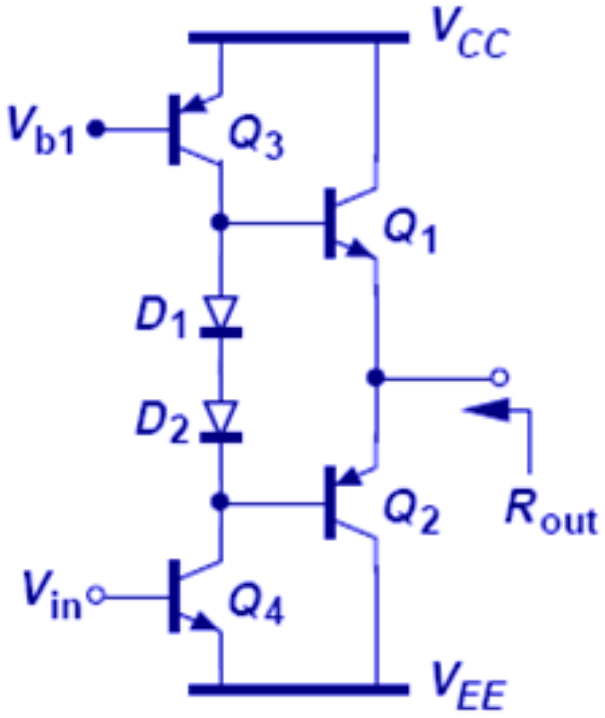
The overall gain is

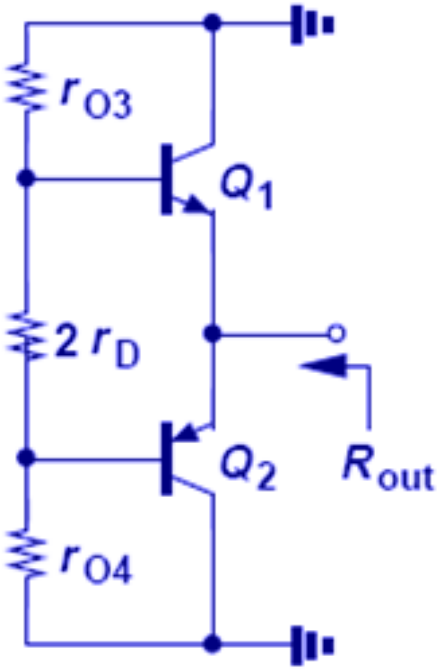
$$\frac{v_{out}}{v_{in}} = \frac{v_N}{v_{in}} \cdot \frac{v_{out}}{v_N} = -g_{m4}\left[r_{\pi 1} \| r_{\pi 2} + (g_{m1} + g_{m2})(r_{\pi 1} \| r_{\pi 2})R_L\right]\left(\frac{R_L}{R_L + \frac{1}{g_{m1} + g_{m2}}}\right)$$

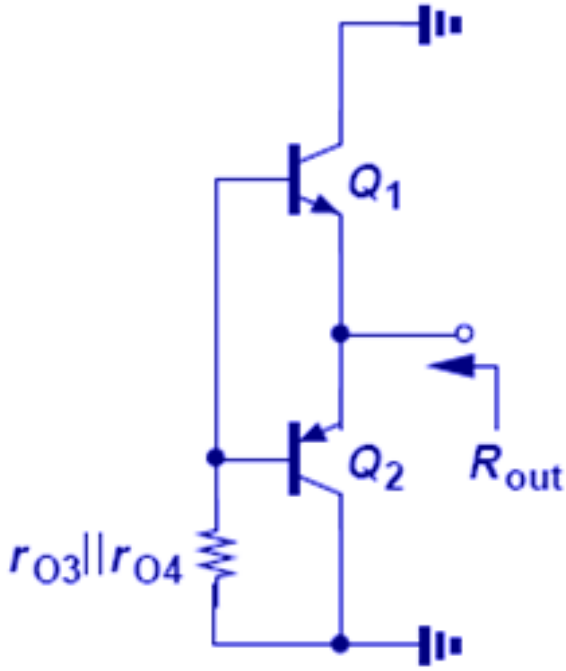
$$\boxed{\frac{v_{out}}{v_{in}} = -g_{m4}(r_{\pi 1} \| r_{\pi 2})(g_{m1} + g_{m2})R_L}$$

Output Resistance Analysis

- For the output resistance, we do need to consider the finite r_O of Q_3 & Q_4







$$R_{out} \approx \frac{1}{g_{m1}+g_{m2}} + \frac{r_{O3} \| r_{O4}}{(g_{m1}+g_{m2})(r_{\pi 1} \| r_{\pi 2})}$$

- **If β is low, the second term of the output resistance will rise, which will be problematic when driving a small resistance.**

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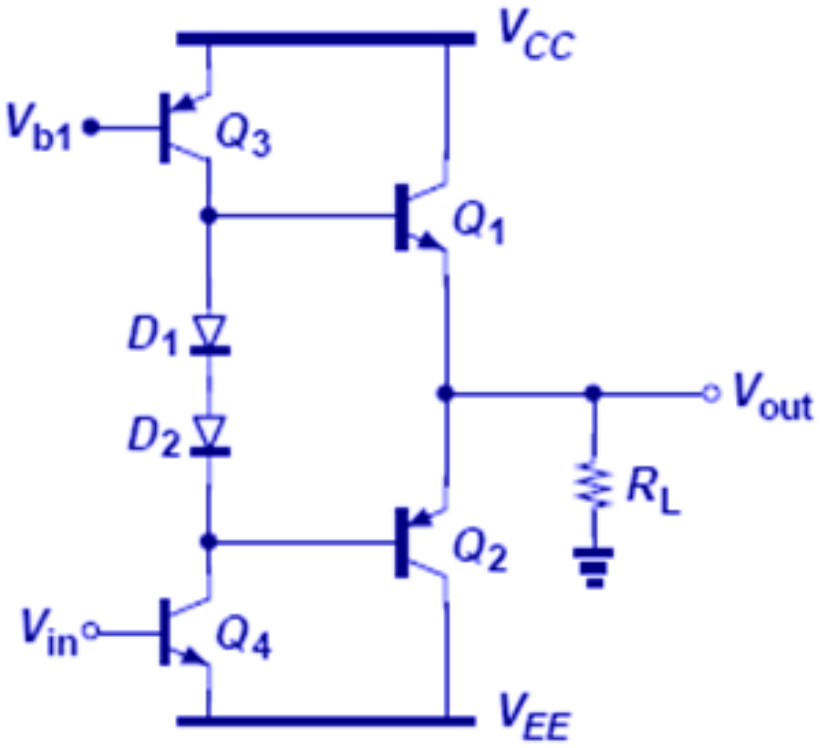
Example: Biasing



Design Specs :

Common Emitter $A_v = 5$

Output Stage $A_v = 0.8$

with $R_L = 8\Omega, \beta_{npn} = 2\beta_{pnp} = 100$

and assume $I_{C1} \approx I_{C2}$

1. From the output stage gain and $I_{C1,2}$ conditions we can find $g_{m1,2}$ and $I_{C1,2}$

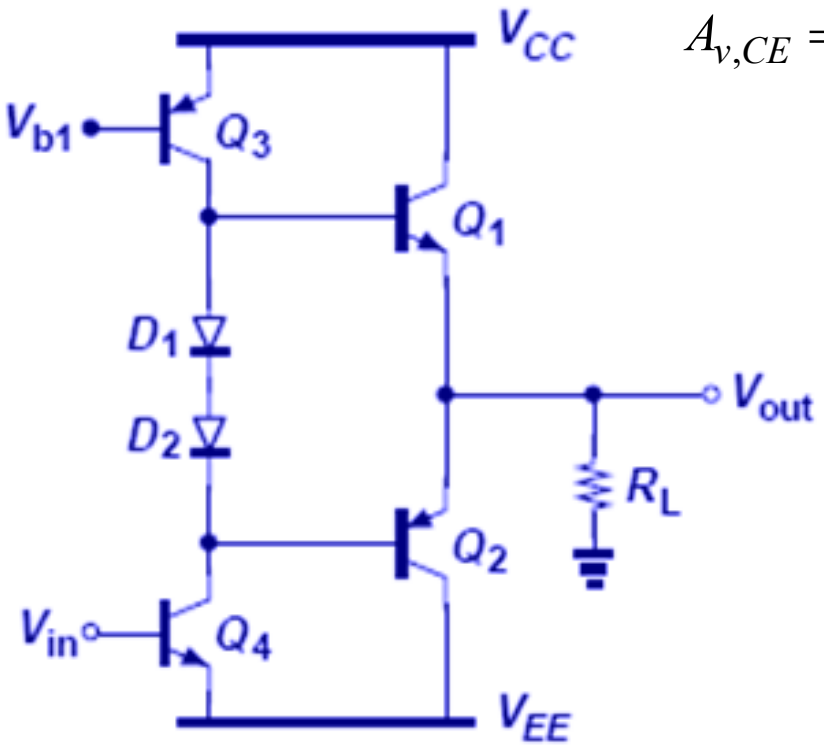
$$A_{v,OS} = \frac{v_{out}}{v_N} = \frac{R_L}{R_L + \dfrac{1}{g_{m1} + g_{m2}}} = 0.8$$

$$g_{m1} + g_{m2} = \frac{1}{2\Omega}$$

with $I_{C1} = I_{C2} \Rightarrow g_{m1} = g_{m2} = \frac{1}{4}\left(\Omega^{-1}\right) = 250\,mA/V$

and $I_{C1} = I_{C2} = 6.5mA$

Example: Biasing



2. From the Common Emitter gain condition we can find I_{C4}

$$A_{v,CE} = -g_{m4}R_N = -g_{m4}\left[r_{\pi 1} \| r_{\pi 2} + (g_{m1} + g_{m2})(r_{\pi 1} \| r_{\pi 2})R_L\right]$$

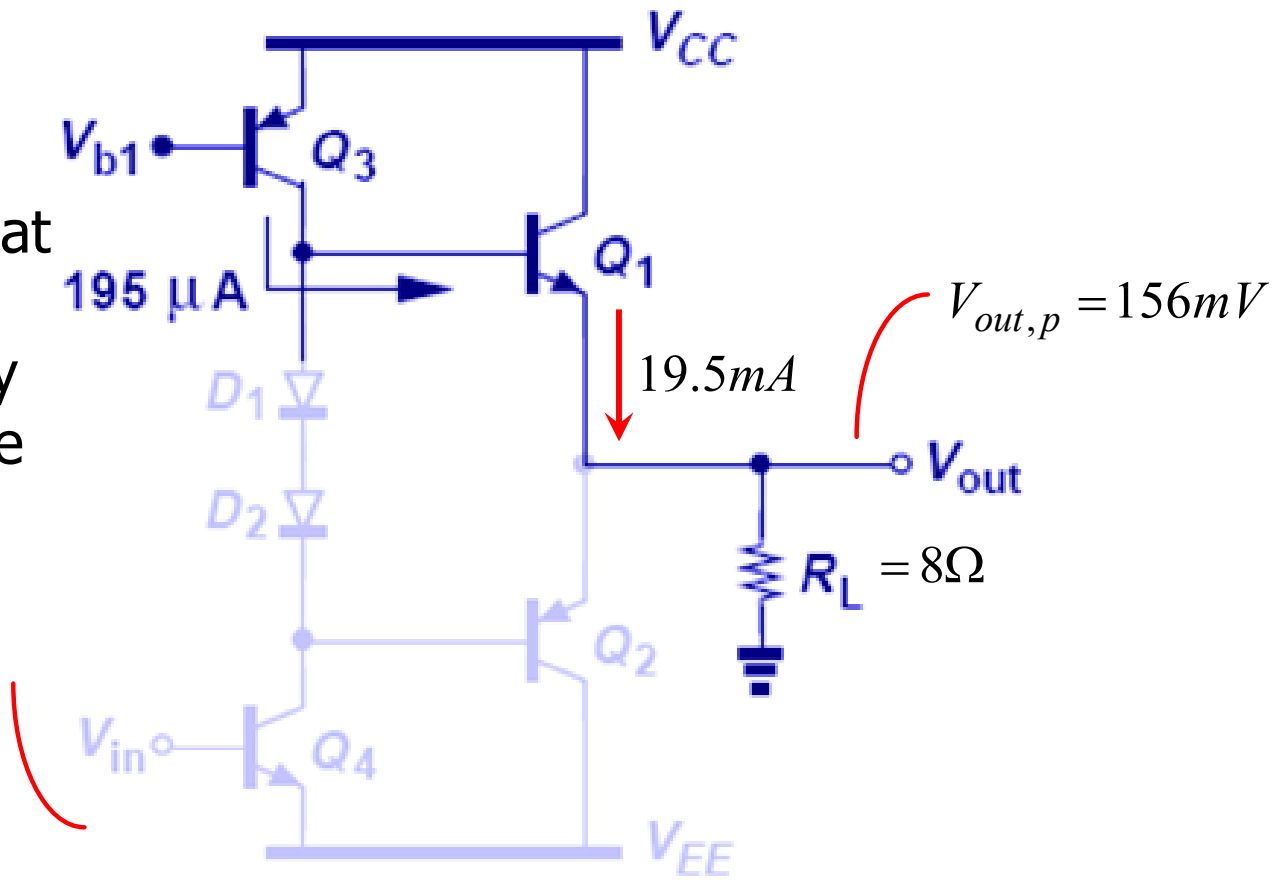
$$\text{Using } r_{\pi 1} = 398\Omega,\ r_{\pi 2} = 199\Omega, \text{ and } R_L = 8\Omega$$

$$g_{m4} = 7.52\,mA/V \Rightarrow I_{C4} = 195\,\mu A$$

However, this design procedure neglects any output swing specification!

Problem of Base Current

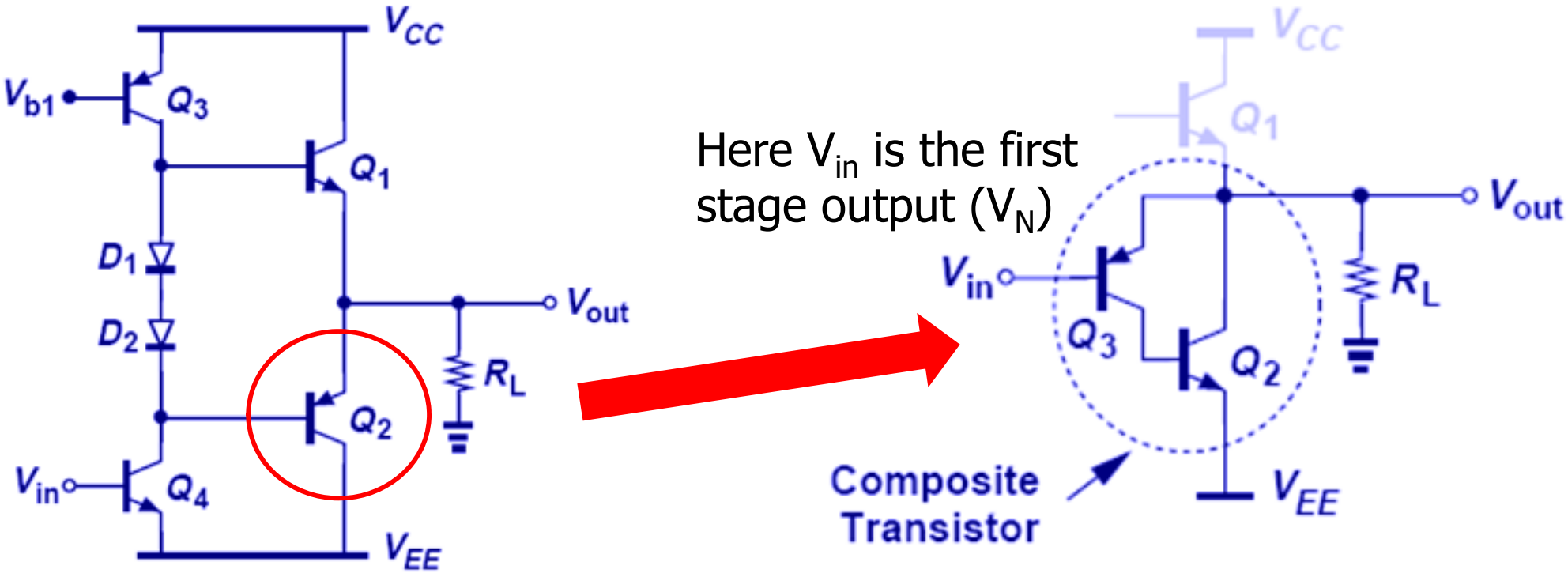
Note, this assumes that I_{C3} is the same as I_{C4}, which may not exactly be the case due to the different $\beta_{1,2}$



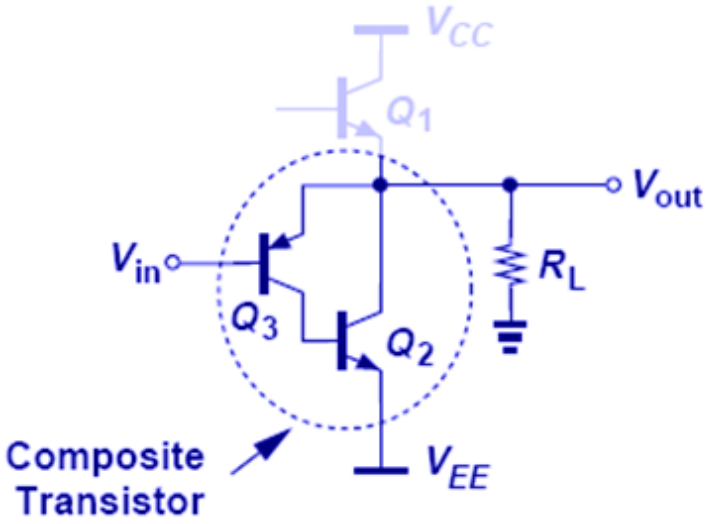
- **195 μA of base current in Q_1 can only support 19.5 mA of collector current, insufficient for high current operation (hundreds of mA).**

Modification of the PNP Emitter Follower

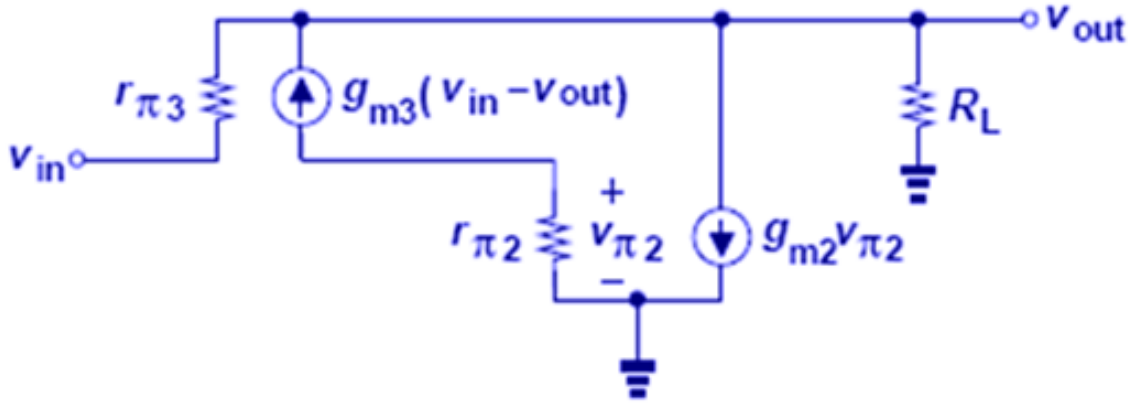
- Another output stage issue is that the Q_2 PNP transistor typically have low current gain (β) and low f_T
- Using a composite transistor consisting of an emitter follower PNP (Q_3) and a common emitter NPN (Q_2) allows for improved performance



Modified PNP Emitter Follower
Gain & Output Resistance



Small-Signal Model



Writing a KCL at the output node

$$\frac{v_{out}-v_{in}}{r_{\pi 3}}-g_{m3}(v_{in}-v_{out})+g_{m2}(-g_{m3})(v_{in}-v_{out})r_{\pi 2}+\frac{v_{out}}{R_L}=0$$

As the Q_3 collector current forms the Q_2 base current

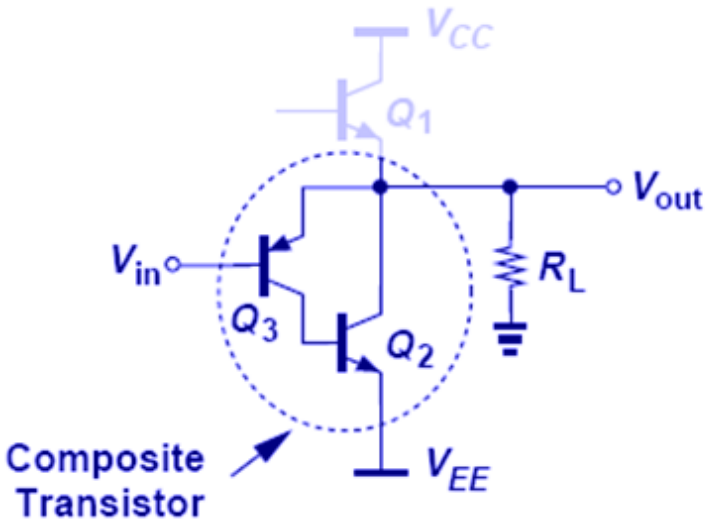
$$g_{m2}=\beta_2 g_{m3}$$

$$\frac{v_{out}}{v_{in}}=\frac{R_L}{R_L+\dfrac{1}{(\beta_2+1)g_{m3}+\dfrac{1}{r_{\pi 3}}}}$$

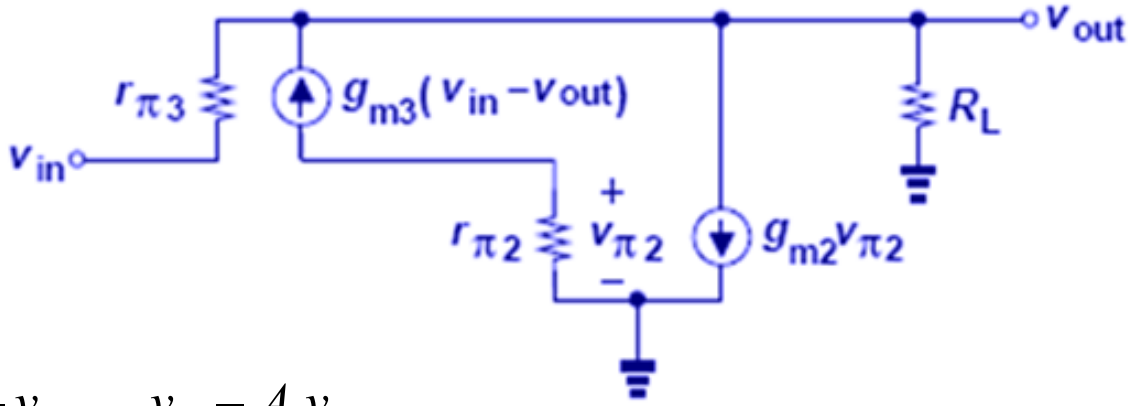
$$R_{out}=\frac{1}{(\beta_2+1)g_{m3}+\dfrac{1}{r_{\pi 3}}}\approx\frac{1}{(\beta_2+1)g_{m3}}$$

Output resistance has been reduced by β_2+1 factor

Modified PNP Emitter Follower
Input Resistance



Small-Signal Model



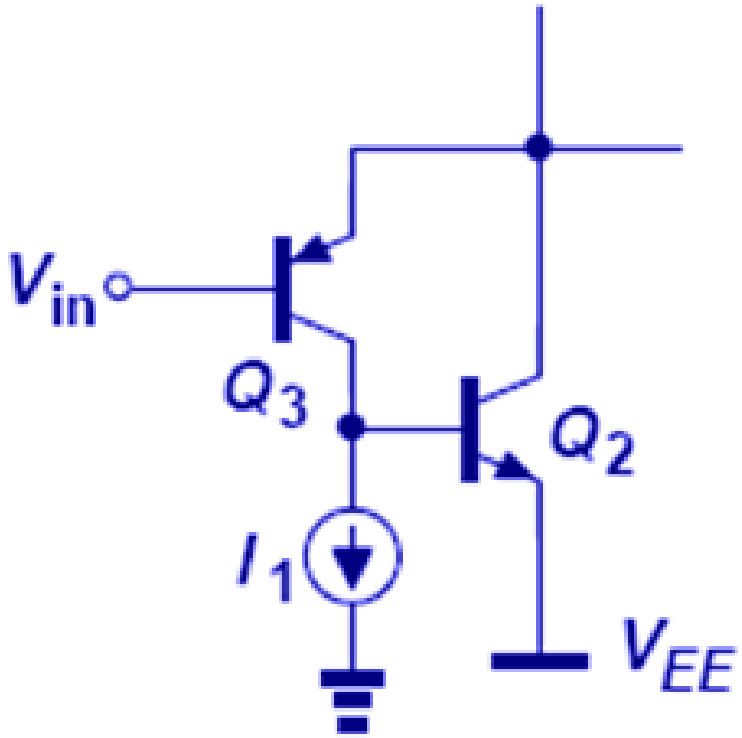
$$i_{in} = \frac{v_{in} - v_{out}}{r_{\pi 3}} = \frac{v_{in} - A_v v_{in}}{r_{\pi 3}}$$

$$R_{in} = \frac{v_{in}}{i_{in}} = \frac{r_{\pi 3}}{1 - A_v} = \frac{r_{\pi 3}}{1 - \dfrac{R_L}{R_L + \dfrac{1}{(\beta_2 + 1) g_{m3}}}}$$

$$\boxed{R_{in} = r_{\pi 3} + \beta_3 (\beta_2 + 1) R_L}$$

Input resistance has been increased by ~(β_2+1) factor

Additional Bias Current

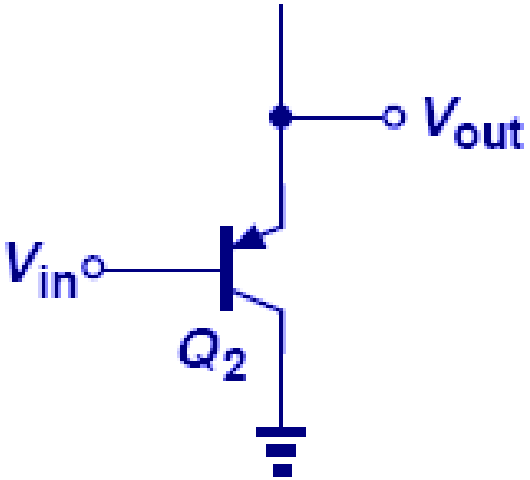


- Q_2 is often a large transistor to support the output current levels, resulting in large base capacitance
- I_1 is added to the base of Q_2 to provide an additional bias current to Q_3 so the capacitance at the base of Q_2 can be charged/discharged quickly

Example: Minimum V_{in}

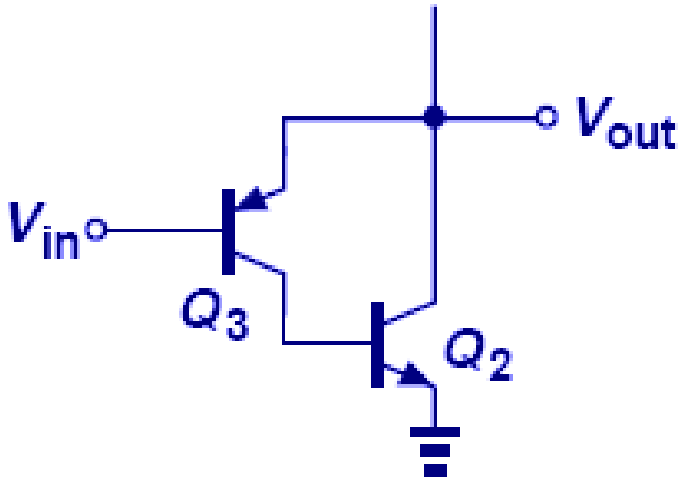
- There is a minimum Vin for which the effective emitter follower transistors remain in active mode
- Here we conservatively assume for active mode we need a min. V_{BC}=0V

Simple PNP Emitter Follower



Min $V_{in} \approx 0$
$V_{out} \approx |V_{EB2}|$

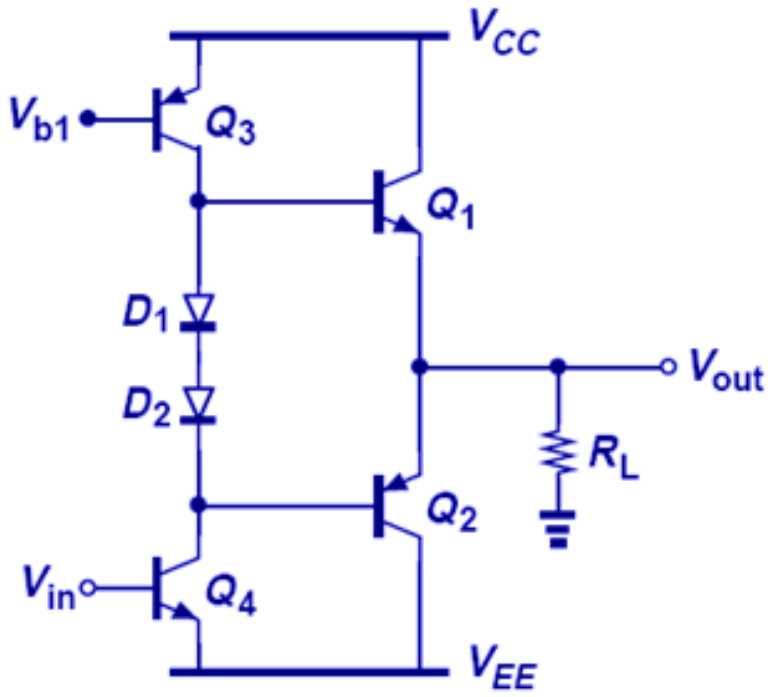
Modified PNP Emitter Follower

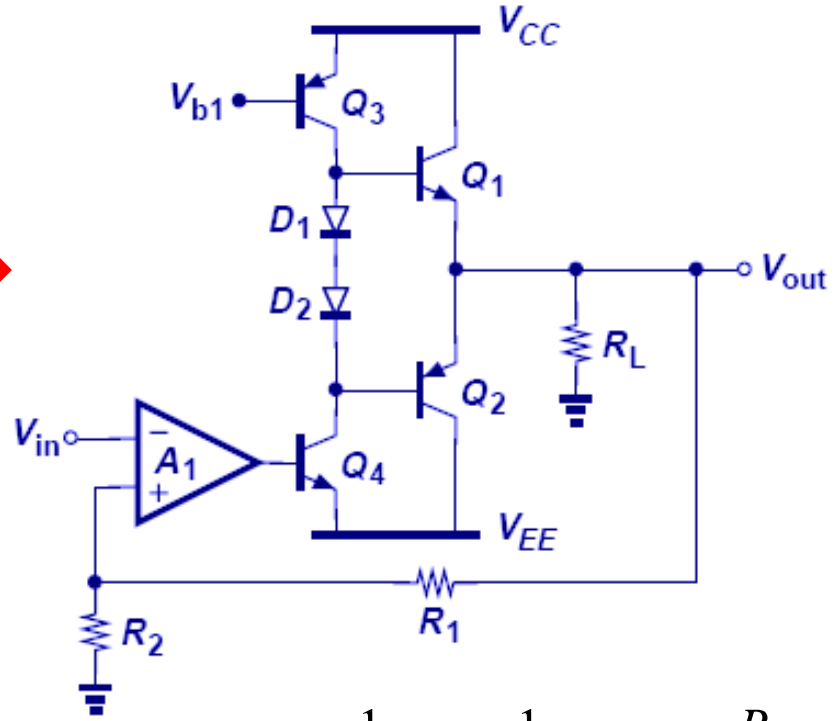


Min $V_{in} \approx V_{BE2}$
$V_{out} \approx |V_{EB3}| + V_{BE2}$

- The modified PNP emitter follower has a reduced input range by V_{BE2}

HiFi Design





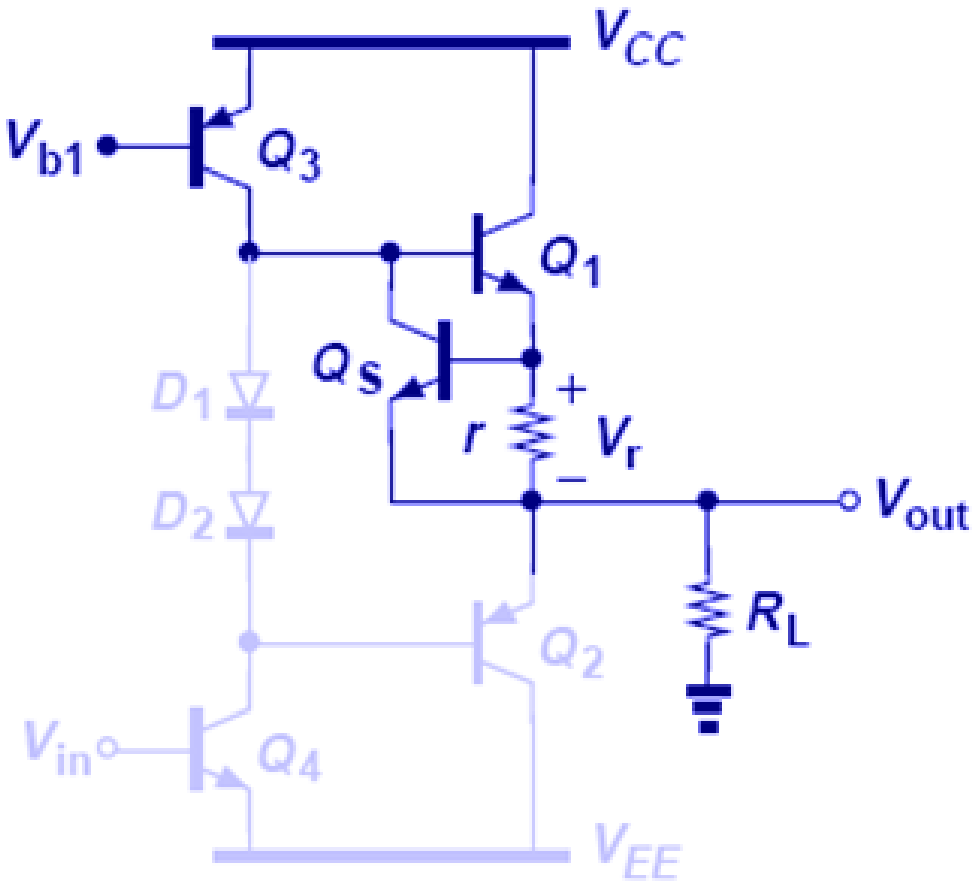
$$\frac{v_{out}}{v_{in}} = -g_{m4}\left(r_{\pi 1} \| r_{\pi 2}\right)\left(g_{m1} + g_{m2}\right)R_L$$

$$\frac{v_{out}}{v_{in}} \approx \frac{1}{K} = \frac{1}{\frac{R_2}{R_1 + R_2}} = 1 + \frac{R_1}{R_2}$$

- As g_{m1} and g_{m2} vary dramatically during large signal operation, the circuit displays nonlinear distortion
- Placing the output stage in a negative feedback loop allows for a more constant gain, and thus better linearity

Short-Circuit Protection

- Excessive output stage current can result if the output is shorted to ground, damaging the circuit
- Q_s and r are used to "steal" some base current away from Q_1 when the output is accidentally shorted to ground, preventing short-circuit damage
- Drawbacks
  - r increases output resistance
  - Voltage drop across r reduces maximum output swing

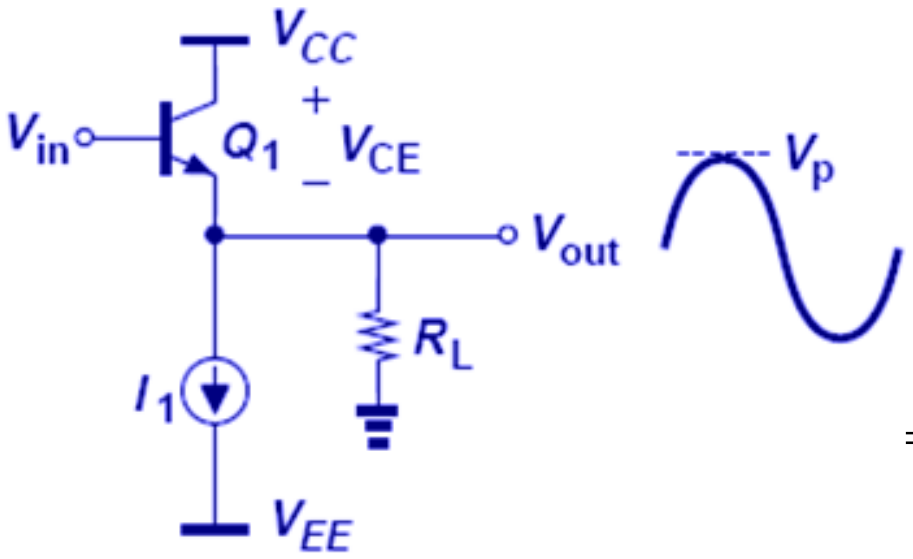


Agenda

- General Output Stage Considerations
- Emitter Follower as a Power Amplifier
- Push-Pull Stage
- Improved Push-Pull Stage
- Large-Signal Considerations
- Heat Dissipation
- Efficiency and Power Amplifier Classes

Emitter Follower Power Rating

The average power dissipated by Q_1 can be calculated by integrated the current - voltage product over a complete period and dividing by the period time.



$$P_{av} = I_1\left(V_{CC} - \frac{V_P}{2}\right)$$

$$P_{av,\max} = I_1 V_{CC}$$

$$P_{av} = \frac{1}{T}\int_0^T I_C V_{CE}\,dt$$

$$P_{av} = \frac{1}{T}\int_0^T \left(I_1 + \frac{V_P \sin\omega t}{R_L}\right)(V_{CC} - V_P \sin\omega t)\,dt$$

$$= \frac{1}{T}\int_0^T I_1 V_{CC} - I_1 V_P \sin\omega t + \frac{V_{CC} V_P \sin\omega t}{R_L} - \frac{V_P^2 \sin^2\omega t}{R_L}\,dt$$

($I_1 V_P \sin\omega t$ → 0; $\frac{V_{CC} V_P \sin\omega t}{R_L}$ → 0)

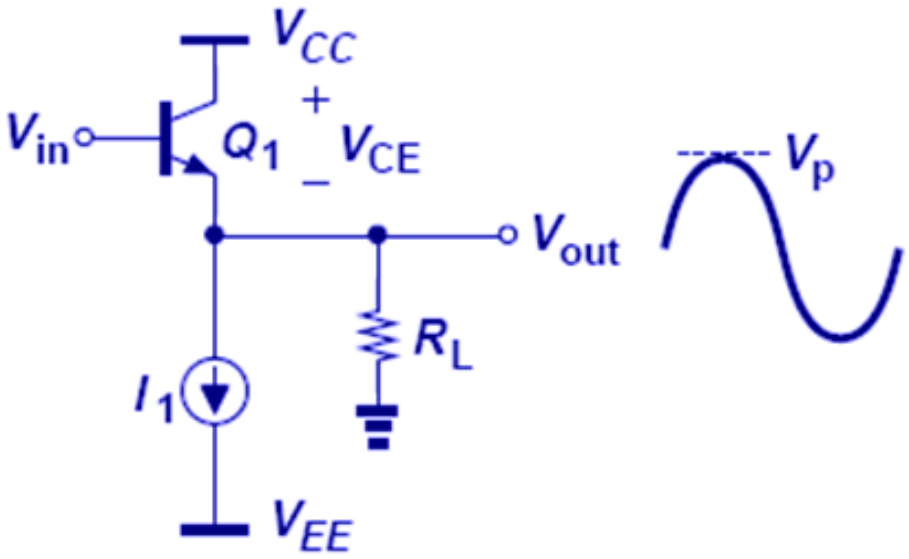
$$= \frac{1}{T}\int_0^T I_1 V_{CC} - \frac{V_P^2}{2R_L}(1 - \cos 2\omega t)$$

$$= I_1 V_{CC} - \frac{V_P^2}{2R_L} \xrightarrow{I_1 = \frac{V_P}{R_L}} I_1\left(V_{CC} - \frac{V_P}{2}\right)$$

- **Maximum power dissipated across Q_1 occurs in the *absence* of a signal.**

Example: Current Source Power Dissipation

- The power dissipated by the I_1 current source is also important, as it will ultimately need to be realized at the transistor level also



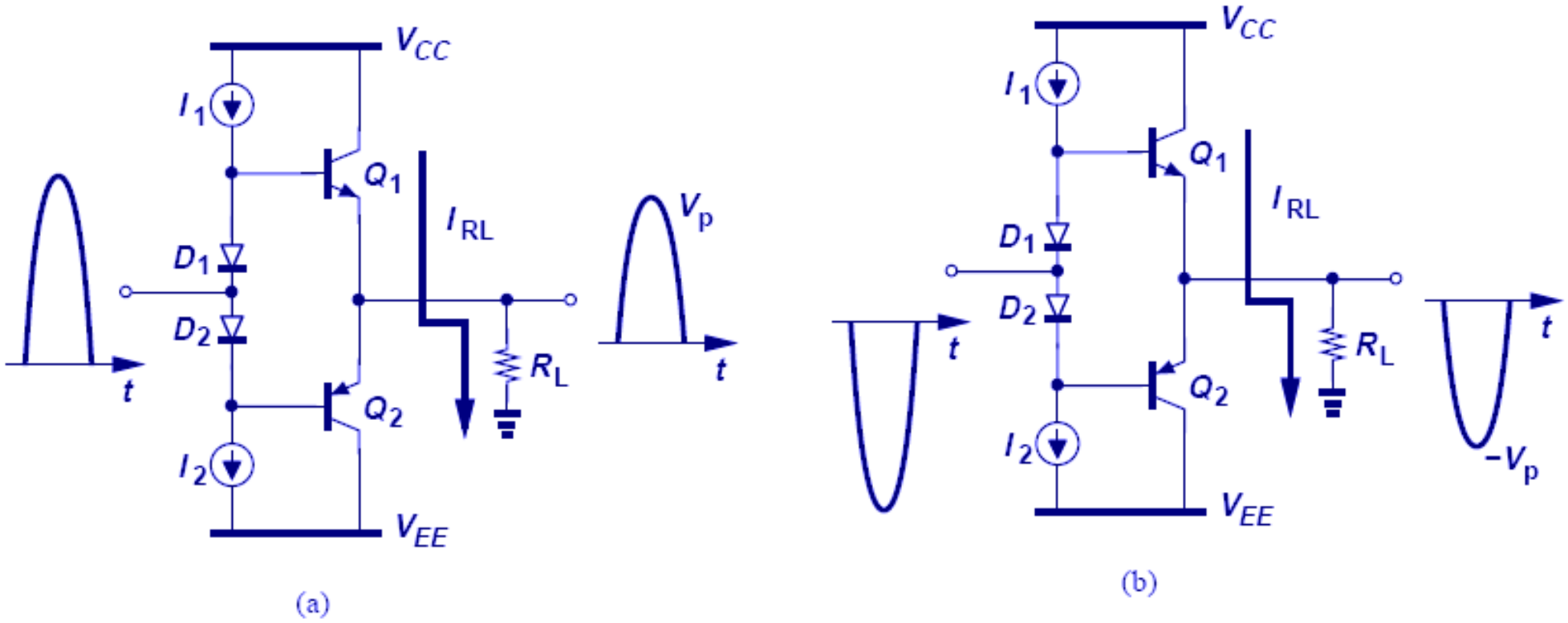
$$P_{I_1} = \frac{1}{T}\int_0^T I_1(V_{out} - V_{EE})dt = \frac{1}{T}\int_0^T I_1(V_P \sin\omega t - V_{EE})dt$$

$$= \frac{1}{T}\int_0^T I_1 V_P \underbrace{\sin\omega t}_{0} - I_1 V_{EE} dt$$

$$\boxed{P_{I_1} = -I_1 V_{EE}}$$

- Note that the I_1 power is positive, as V_{EE} is a negative supply

Push-Pull Stage Power Rating



- Assuming a symmetric design, the power ratings of Q1 and Q2 are the same and can be computed by integrating over a half-period.

Push-Pull Stage Power Rating

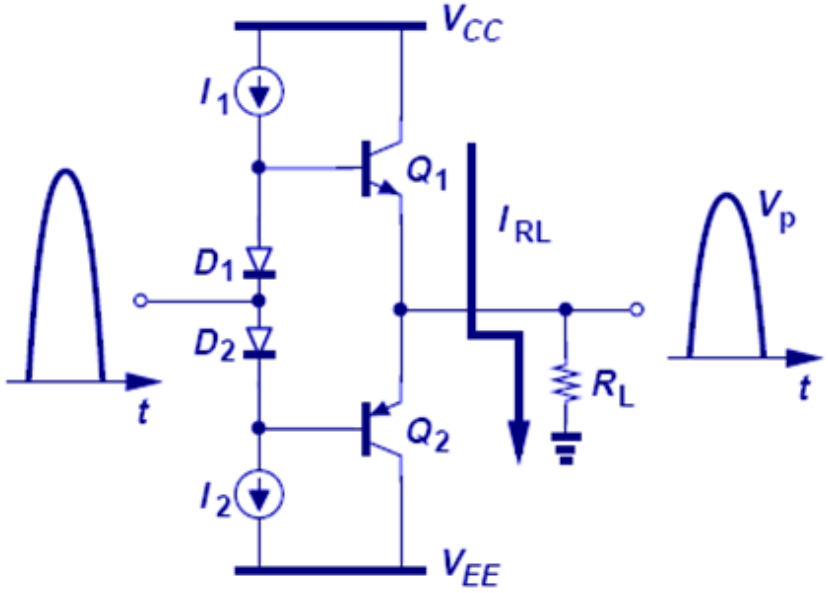
$$P_{av} = \frac{1}{T}\int_0^{T/2} V_{CE} I_C dt = \frac{1}{T}\int_0^{T/2} (V_{CC} - V_P \sin\omega t)\left(\frac{V_P}{R_L}\sin\omega t\right) dt$$

$$= \frac{1}{T}\int_0^{T/2} \frac{V_{CC}V_P}{R_L}\sin\omega t - \frac{V_P^2}{R_L}\sin^2\omega t dt$$

$$= \frac{1}{T}\int_0^{T/2} \frac{V_{CC}V_P}{R_L}\sin\omega t dt - \frac{1}{T}\int_0^{T/2} \frac{V_P^2}{2R_L}(1 - \cos 2\omega t) dt \quad (\cos 2\omega t \to 0)$$

$$= \frac{V_{CC}V_P}{\pi R_L} - \frac{V_P^2}{4R_L}$$

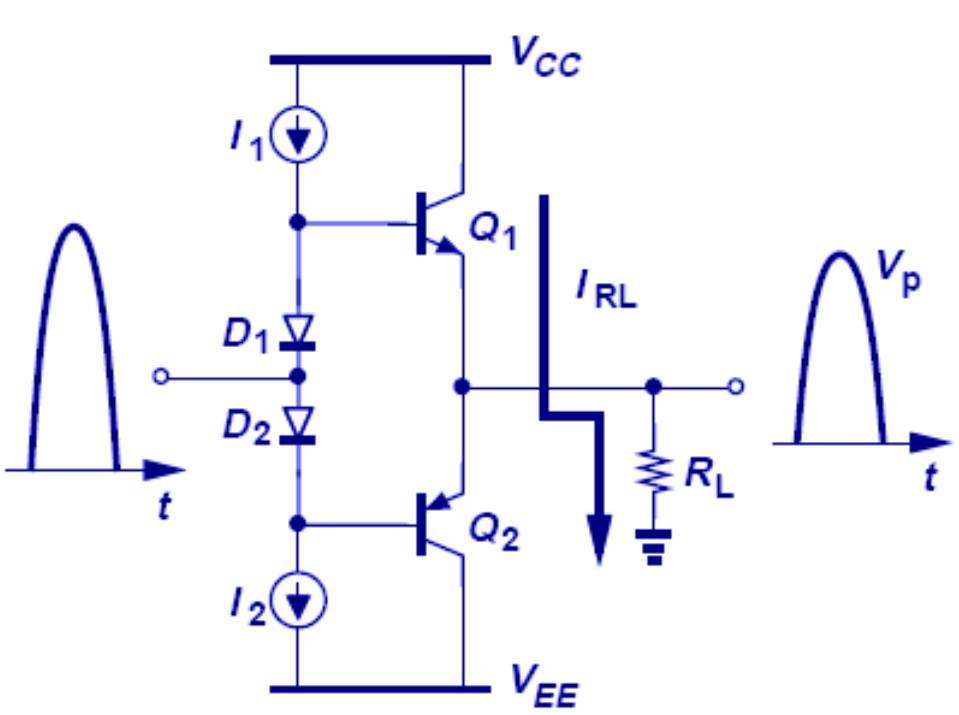
$$P_{av} = \frac{V_P}{R_L}\left(\frac{V_{CC}}{\pi} - \frac{V_P}{4}\right)$$



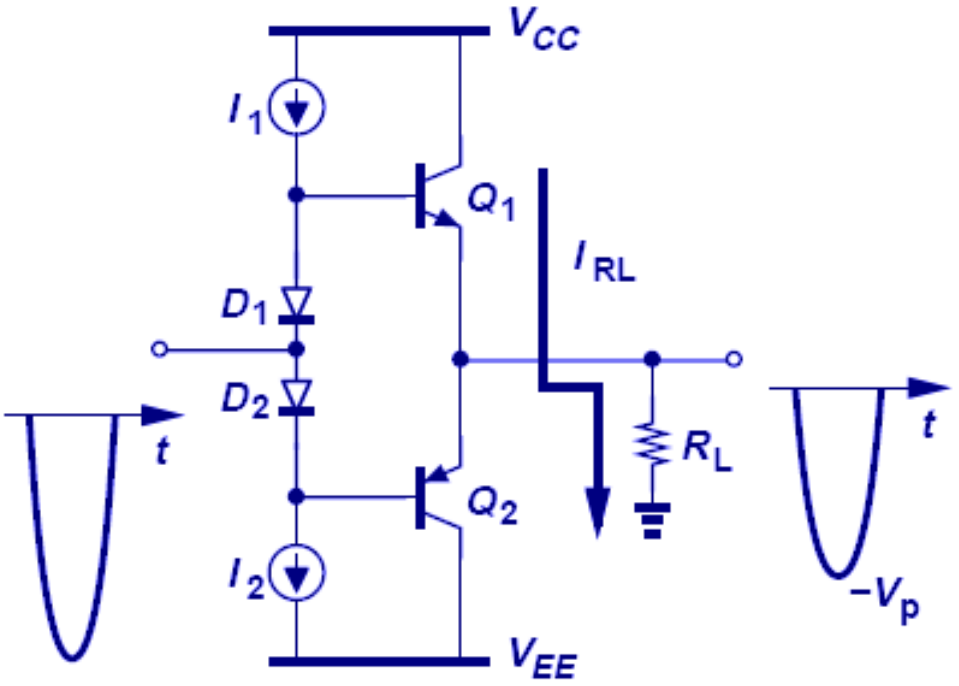
Maximum power occurs with $V_P = \frac{2V_{CC}}{\pi}$

$$P_{av,\max} = \frac{V_{CC}^2}{\pi^2 R_L}$$

Example: Push-Pull P_{av}



(a)



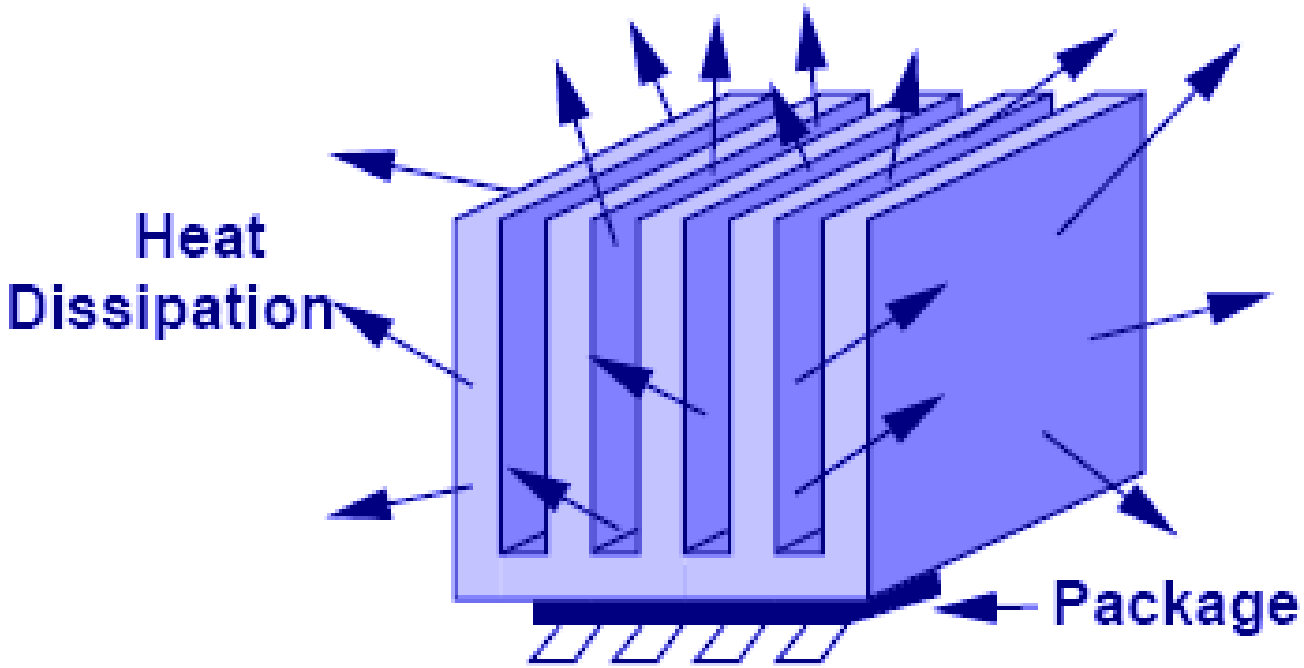
(b)

$$P_{av} = \frac{V_P}{R_L}\left(\frac{V_{CC}}{\pi} - \frac{V_P}{4}\right)$$

If $V_p = 4V_{CC}/\pi \rightarrow P_{av}=0$

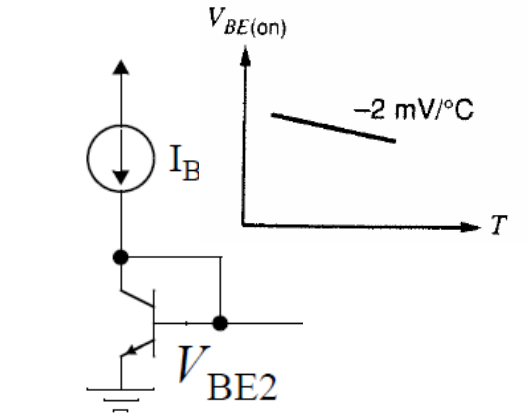
Impossible since V_p cannot go above supply (V_{CC})

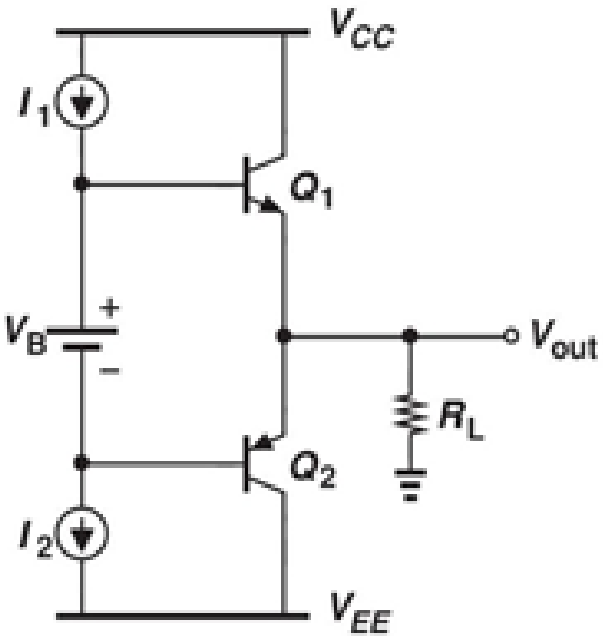
Heat Sink



- **Heat sink, provides large surface area to dissipate heat from the chip.**

Thermal Runaway

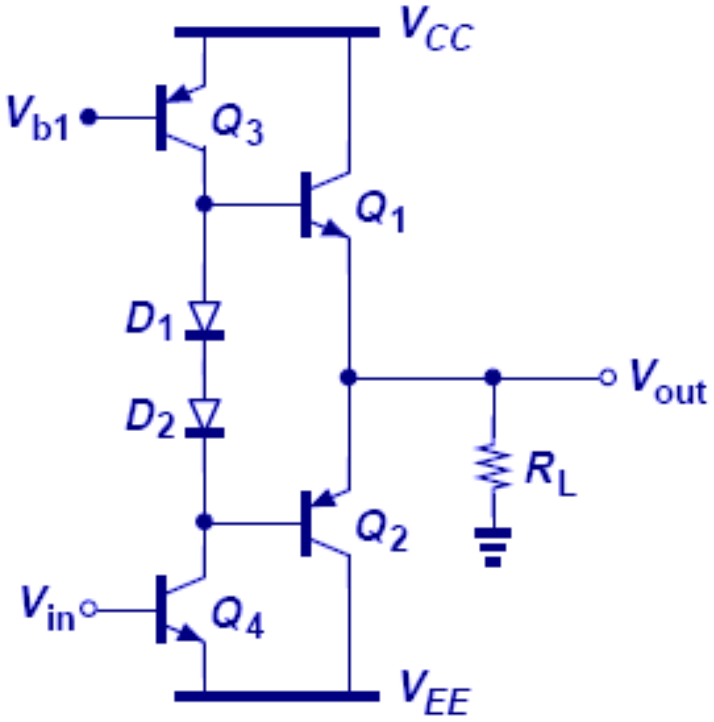




- For a constant I_C, V_{BE} has a **negative-to-absolute-temperature (NTAT)** coefficient of approximately -2mV/°K
- Conversely, if the push-pull output stage is biased with a constant voltage, the current will increase with temperature
- This increased current results in more heat (higher temperature), and thus more current
- This positive feedback loop is called **thermal runaway** and can result in transistor damage

Thermal Runaway Mitigation

- Assuming that Q_3 and Q_4 have relatively constant bias currents with temperature (using good current mirror techniques), the diode voltages drop with temperature



Diode Voltages

$$V_{D1} + V_{D2} = V_T \ln \frac{I_{D1}}{I_{S,D1}} + V_T \ln \frac{I_{D2}}{I_{S,D2}} = V_T \ln \frac{I_{D1} I_{D2}}{I_{S,D1} I_{S,D2}}$$

Transistor V_{BE} Voltages

$$V_{BE1} + V_{BE2} = V_T \ln \frac{I_{C1}}{I_{S,Q1}} + V_T \ln \frac{I_{C2}}{I_{S,Q2}} = V_T \ln \frac{I_{C1} I_{C2}}{I_{S,Q1} I_{S,Q2}}$$

From a KVL, these voltage pairs are the same

$$V_T \ln \frac{I_{D1} I_{D2}}{I_{S,D1} I_{S,D2}} = V_T \ln \frac{I_{C1} I_{C2}}{I_{S,Q1} I_{S,Q2}}$$

$$\boxed{\frac{I_{D1} I_{D2}}{I_{S,D1} I_{S,D2}} = \frac{I_{C1} I_{C2}}{I_{S,Q1} I_{S,Q2}}}$$

- **Using diode biasing prevents thermal runaway since the currents in Q_1 and Q_2 will track those of D_1 and D_2 as long as their I_s's track with temperature.**

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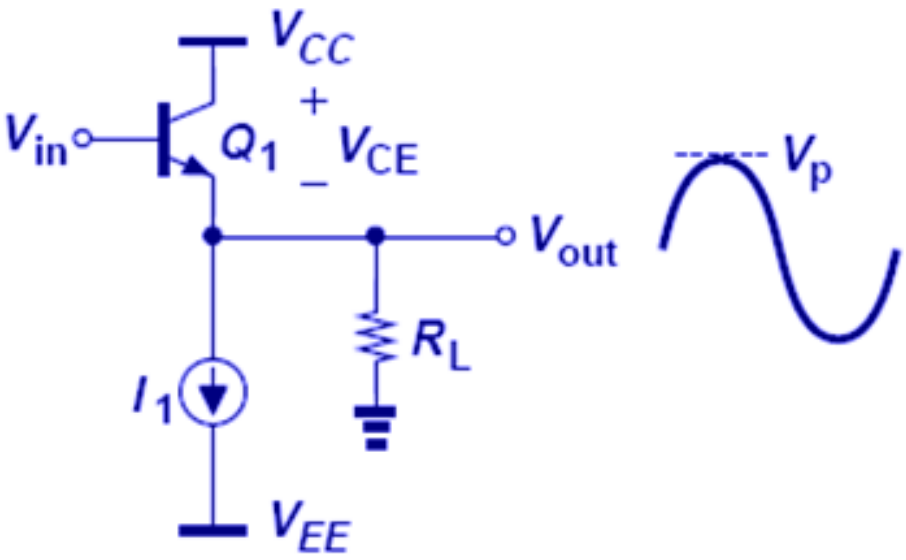
Power Amplifier Efficiency

- Power amplifier efficiency is critical because PAs draw a significant amount of power from the supply voltages

- Power amplifier efficiency is the ratio of the average power delivered to the load over the total power consumed from the supplies

$$\eta = \frac{\text{Power Delivered to Load}}{\text{Power Drawn from Supply}} = \frac{P_{out}}{P_{out} + P_{ckt}}$$

Emitter Follower Efficiency



The average power delivered to the load is

$$P_{out} = \frac{V_P^2}{2R_L}$$

The average power consumed by Q_1 is

$$P_{Q_1} = I_1\left(V_{CC} - \frac{V_P}{2}\right)$$

The average power consumed by I_1 is

$$P_{I_1} = -I_1 V_{EE} = I_1 V_{CC} \quad \text{with} \quad V_{EE} = -V_{CC}$$

Thus the total average circuit power is

$$P_{ckt} = I_1\left(V_{CC} - \frac{V_P}{2}\right) + I_1 V_{CC} = I_1\left(2V_{CC} - \frac{V_P}{2}\right)$$

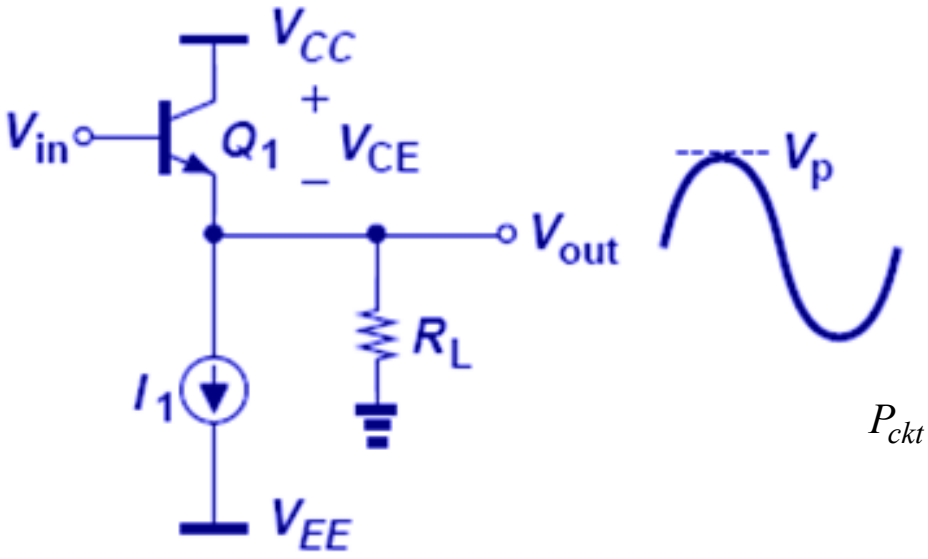
The Emitter Follower Efficiency is $\eta_{EF} = \dfrac{\dfrac{V_P^2}{2R_L}}{\dfrac{V_P^2}{2R_L} + I_1\left(2V_{CC} - \dfrac{V_P}{2}\right)}$

with $I_1 = \dfrac{V_P}{R_L} \quad \Rightarrow \quad \boxed{\eta_{EF} = \dfrac{V_P}{4V_{CC}}}$

- The emitter follower output stage only has a peak efficiency of 25% as V_P goes to V_{CC}
- Note, this can't actually be achieved, as we need some V_{CE} and voltage across I_1

Emitter Follower Efficiency Example

- What if the emitter follower is designed to deliver V_p, but only operates with $V_p = V_{CC}/2$?



Now the average power delivered to the load is

$$P_{out} = \frac{\left(\frac{V_P}{2}\right)^2}{2R_L} = \frac{V_P^2}{8R_L}$$

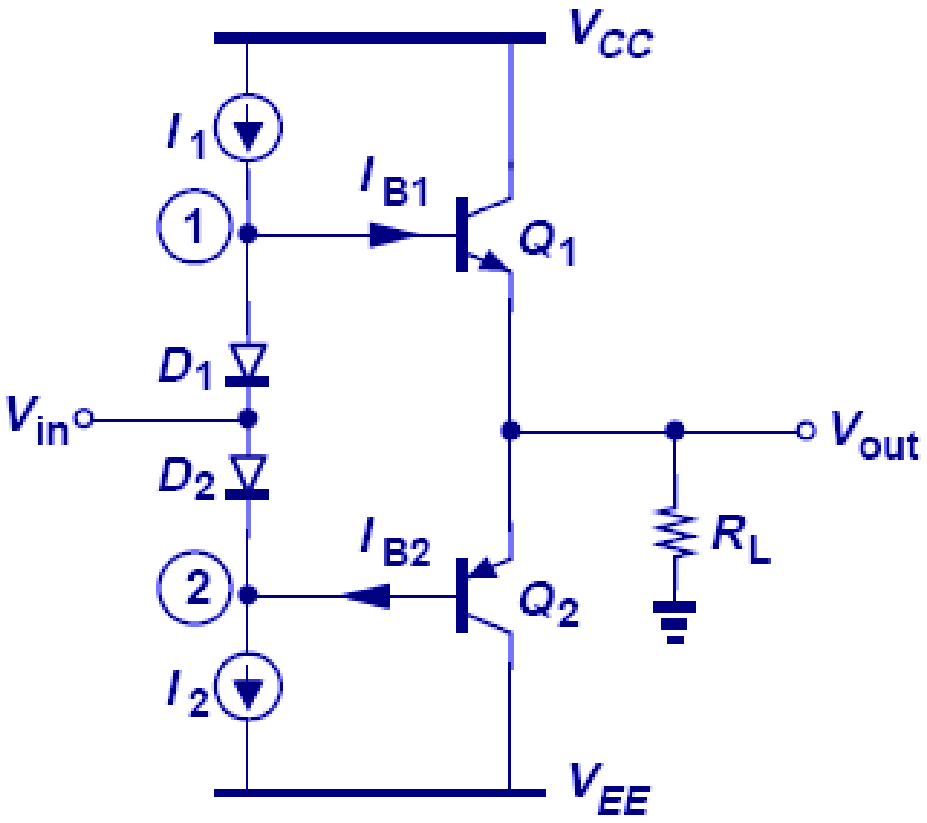
The total average circuit power becomes

$$P_{ckt} = I_1\left(2V_{CC} - \frac{V_P}{4}\right) = \frac{2V_P^2}{R_L} - \frac{V_P^2}{4R_L} \quad \text{with} \quad I_1 = \frac{V_P}{R_L} \quad \text{and} \quad V_{CC} = V_P$$

$$\eta_{EF} = \frac{\frac{V_P^2}{8R_L}}{\frac{V_P^2}{8R_L} + \frac{2V_P^2}{R_L} - \frac{V_P^2}{4R_L}} = \frac{1}{15}$$

- Now the efficiency drops to only 6.7%

Push-Pull Stage Efficiency



The average power delivered to the load is

$$P_{out} = \frac{V_P^2}{2R_L}$$

Both Q_1 and Q_2 consume an average power of

$$P_{Q_{1,2}} = \frac{V_P}{R_L}\left(\frac{V_{CC}}{\pi} - \frac{V_P}{4}\right)$$

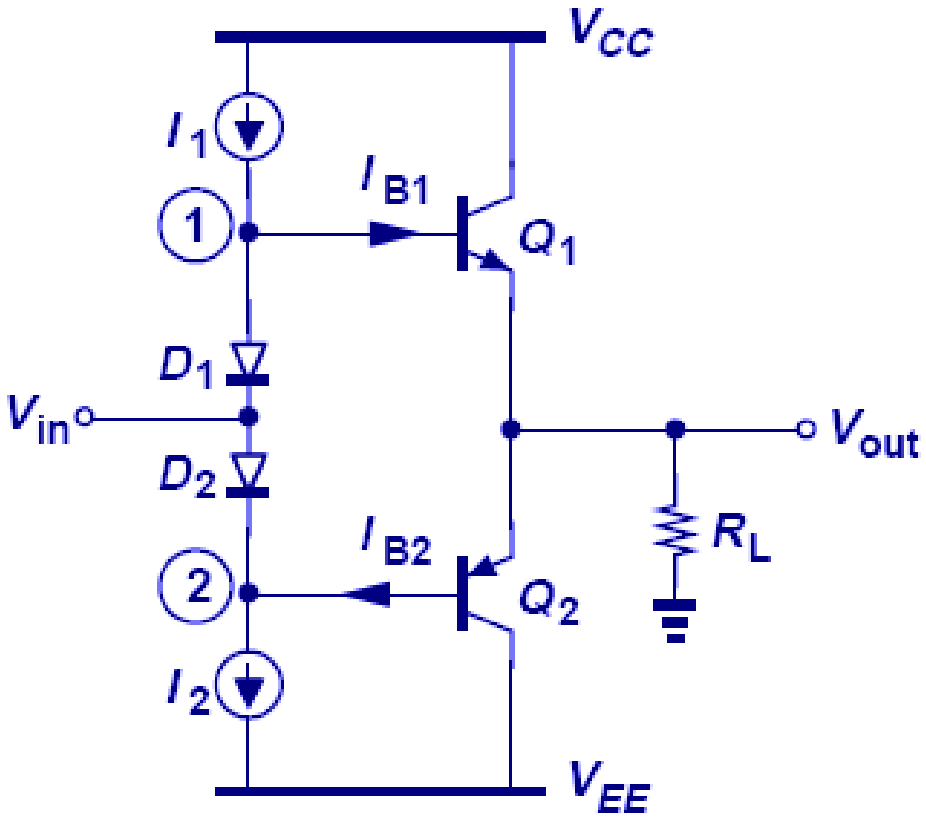
The Push - Pull Stage Efficiency is $\eta_{PP} = \dfrac{\frac{V_P^2}{2R_L}}{\frac{V_P^2}{2R_L} + \frac{2V_P}{R_L}\left(\frac{V_{CC}}{\pi} - \frac{V_P}{4}\right)}$

$$\eta_{PP} = \frac{\pi V_P}{4V_{CC}}$$

- The push-pull output stage has a peak efficiency of 78.5% as V_P goes to V_{CC}
- Note, this can't actually be achieved, as we need some V_{CE} across both Q_1 and Q_2
- Also, we are excluding the input bias stage

Total Push-Pull Stage Efficiency

- Assume that $I_1=I_2$ and that they are chosen to allow a peak swing of V_P



In order to support a peak swing of V_P

$$I_1 = \frac{V_P}{\beta R_L}$$

The input bias stage power is

$$\frac{2V_{CC}V_P}{\beta R_L}$$

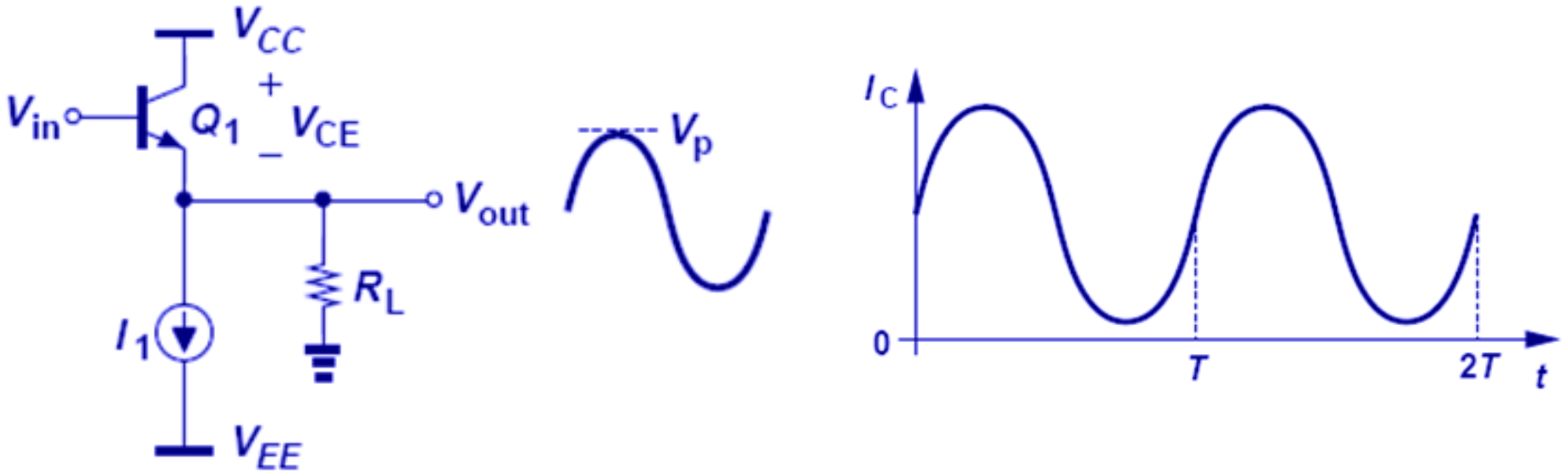
Thus the total push - pull stage efficiency is

$$\eta_{PP} = \frac{\frac{V_P^2}{2R_L}}{\frac{2V_PV_{CC}}{\pi R_L} + \frac{2V_{CC}V_P}{\beta R_L}}$$

$$\eta_{PP} = \frac{1}{4}\left(\frac{V_P}{\frac{V_{CC}}{\pi} + \frac{V_P}{\beta}}\right)$$

Class A Power Amplifiers

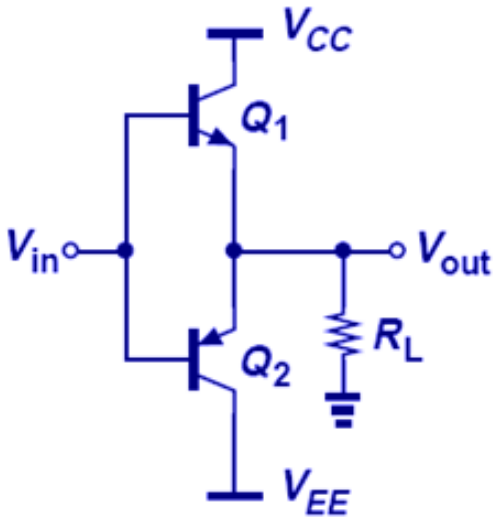
- Each transistor is on for the entire cycle
- Emitter follower is a Class A power amplifier

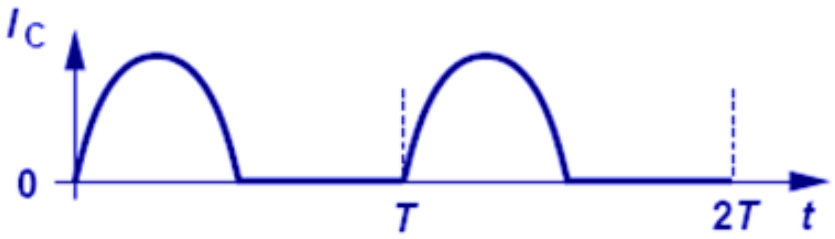


- Display high linearity, but low efficiency (25% maximum)

Class B Power Amplifiers

- Each transistor conducts for half the cycle
- Simple push-pull stage is a Class B power amp

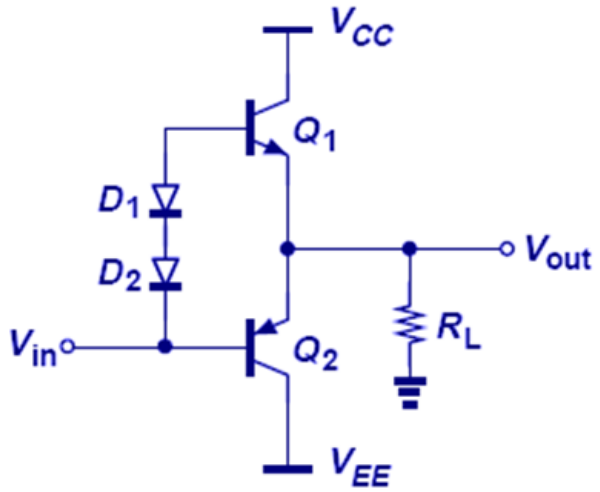


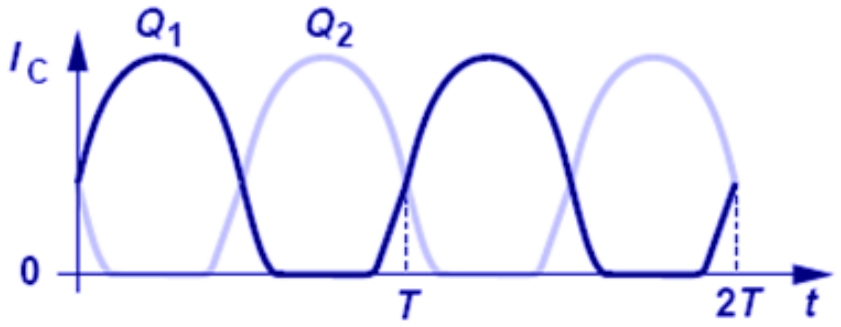


- Display high efficiency, but low linearity
  - Bad crossover distortion

Class AB Power Amplifiers

- Each transistor conducts for slightly more than a half-cycle
- Improved push-pull stage is a Class AB power amp





- Compromise between Class A and B
  - Good distortion at slightly degraded efficiency
- Many other PA classes exist (C, D, E, …) and are often studied in grad-level RF circuit design classes

Thanks for the fun semester!!!