

ECEN 474/704 Lab: Cadence Layout, DRC, LVS, and PEX

Preparing the Schematic for Layout and Post-Layout Steps

The simulation performed in the previous Lab 1 was to obtain preliminary results for the inverter functionality. To complete the full design cycle, any cell schematic should be complete with input and output pins to allow creation of its symbol view. Then, the symbol should be inserted into a test bench to simulate the schematic view, as well as the extracted view after layout.

To prepare the schematic for further steps, the sources need to be deleted and pins need to be added to take their place in the circuit. To place a pin go to *Add*→*Pin* or use the "p" hotkey to pull up the pin editor. Pin names and directions need to be consistent within the schematic, layout and symbol views. Using the inputOutput direction is recommended for power supplies. Also an important thing to note is that all uppercase letters need to be used when naming pins. When complete, the schematic should resemble Figure 1-10.

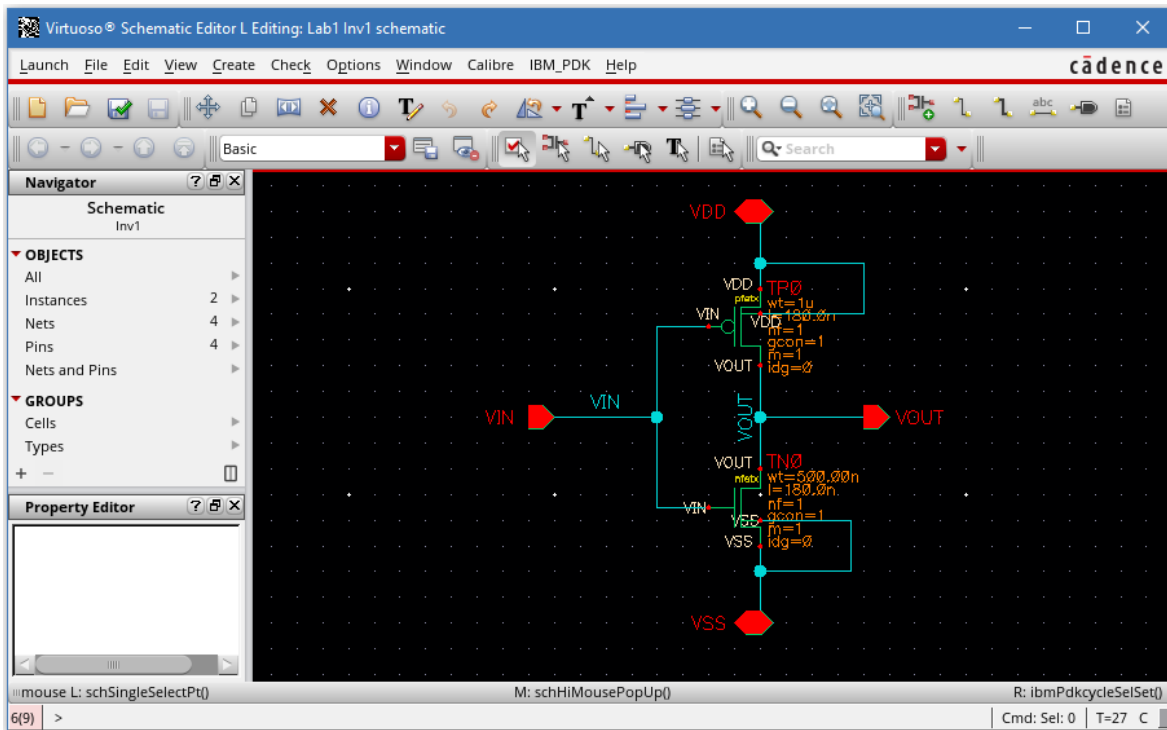


Figure 1-10: Complete Inverter Schematic with Input and Output pins

Creating a Layout

After the schematic has been updated, it is time to move on to the layout of the circuit. From the library manager select *File*→*New*→*Cell View*. Select Layout as the Type (Figure 1-11). After clicking OK (and OK again for the following two popup windows), Virtuoso Layout Suite should open as shown in Figure 1-12.

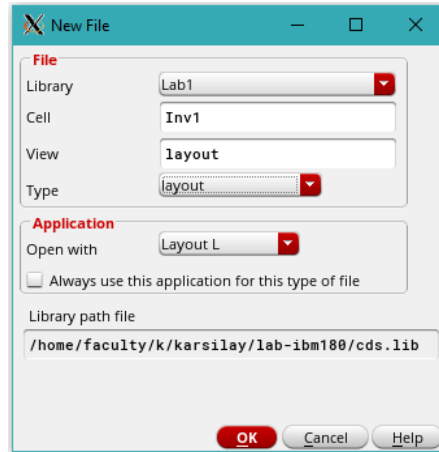


Figure 1-11: Creating a Layout Cell View

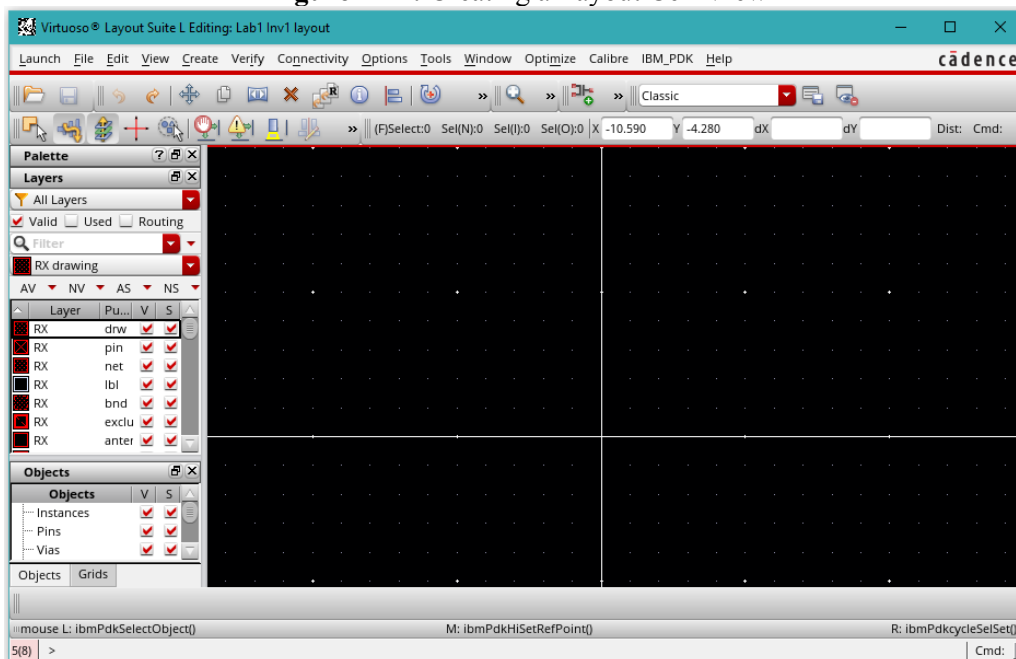


Figure 1-12: The Virtuoso Layout Suite

The Gravity Option

Gravity enables the cursor to only move to critical points on the layout design. For our purposes it is suggested that the student work with Gravity both on and off, and figure out which style is more practical. To toggle gravity on or off, go to *Options*→*Editor*, then disable (or enable) "Gravity On" (Figure 1-13).

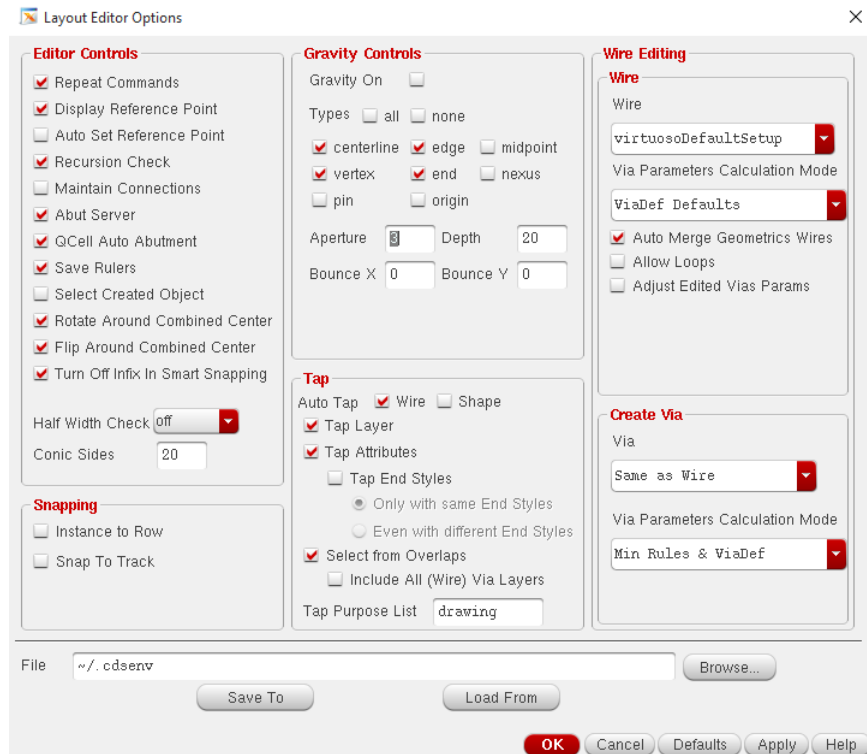


Figure 1-13: Window to Toggle Gravity Option

Creating the Inverter Layout to Match the Schematic

As the first step, place the NFET on the layout. Hit "i" and then "Browse", then make sure under "Library" cmhv7sf is highlighted. Under the "Cell" field scroll down to **nfetx** and then make sure that under "View" the word "layout" is highlighted. After placement, the transistor will first appear as a red box with its name on it, so Shift+f needs to be pressed to change the view to show the layers (Figure 1-14).

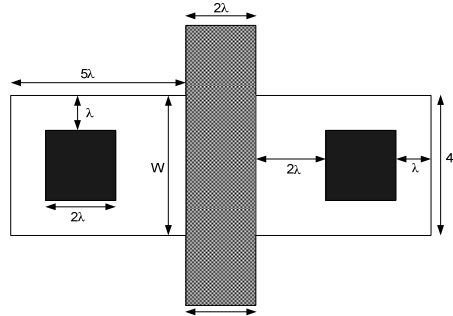


Figure 1-14: A View of the Transistor

Next, the PFET needs to be placed above the NFET. Repeat the process except selecting **pfetx** instead of **nfetx**, and when the parameter window pops up be sure to change the width from 500 nm to 1 μm . PFET and NFET should be repositioned such that the centers of the two are vertically aligned. To do this, select a device and press "q", then change the "Origin" X and Y such that both devices are aligned. Be sure to **deselect a device once you are done editing it by using ctrl-d**.

Next, we need to add substrate contacts (i.e. vias between RX and M1 layers) using the hotkey "o" (or *Create*→*Via*). The "Via Definition" field will be "RX_M1" for substrate contacts. Set Rows as 2 and Columns as 5, then place the vias above and below the transistors. The RX layer defines the active areas, which are heavily doped regions. When placed in an N-Well, RX defines n+ regions, whereas RX and BP layer combination (or overlap) defines p+ regions on the common p- substrate. Therefore, N-Well should cover the entire RX_M1 contacts, as well as PMOS transistors, for the substrate connection of PMOS devices. For NMOS devices, BP layer covering the RX_M1 contacts provide substrate connection.

To draw such layers, look to the left of the screen, it should have a list of layers and purposes. Now, in the search bar above type "NW" to query the list for the N-well material. Find the one with the purpose field "drw" (drawing) and select it. Now, we are ready to draw a rectangle by pressing the "r" hotkey and click and drag the N-well to encompass the RX_M1 vias and the PMOS transistor. Next, a BP layer will be needed to encompass RX_M1 vias of the NMOS (not including the NMOS though). Draw such a rectangle on BP drawing layer using the same procedure.

Next, we will need to wire the transistors and power sources together. Under that same search bar, find "M1 drw" and wire the transistor sources and drains either using "p" or "r" hotkeys. If you draw a trace that is too thin or too thick, you may stretch it by using the "s" hotkey. Then, find "PC drw" for the gate layers and wire the two gates together. Finally, a layer of GRLOGIC "GR" will encompass the entire layout. To check the widths of the traces you can use the hotkey "k" for the ruler tool (Shift-k to clear), if a trace is too thin it will not pass the DRC.

The last step to completing our layout is to add labels for the pins. Go to *Create*→*Label*→<give the pin the same name as the one in the schematic>→<select the "Select Layer" option under the label layer/purpose field and adjust it accordingly>. For VDD, VSS and VOUT the field "label layer/purpose" needs to be "M1 label", and for VIN it needs to be "PC label". When the process is complete the layout should resemble Figure 1-15. Be sure that the GRLOGIC layer surrounds everything including the letters on the labels.

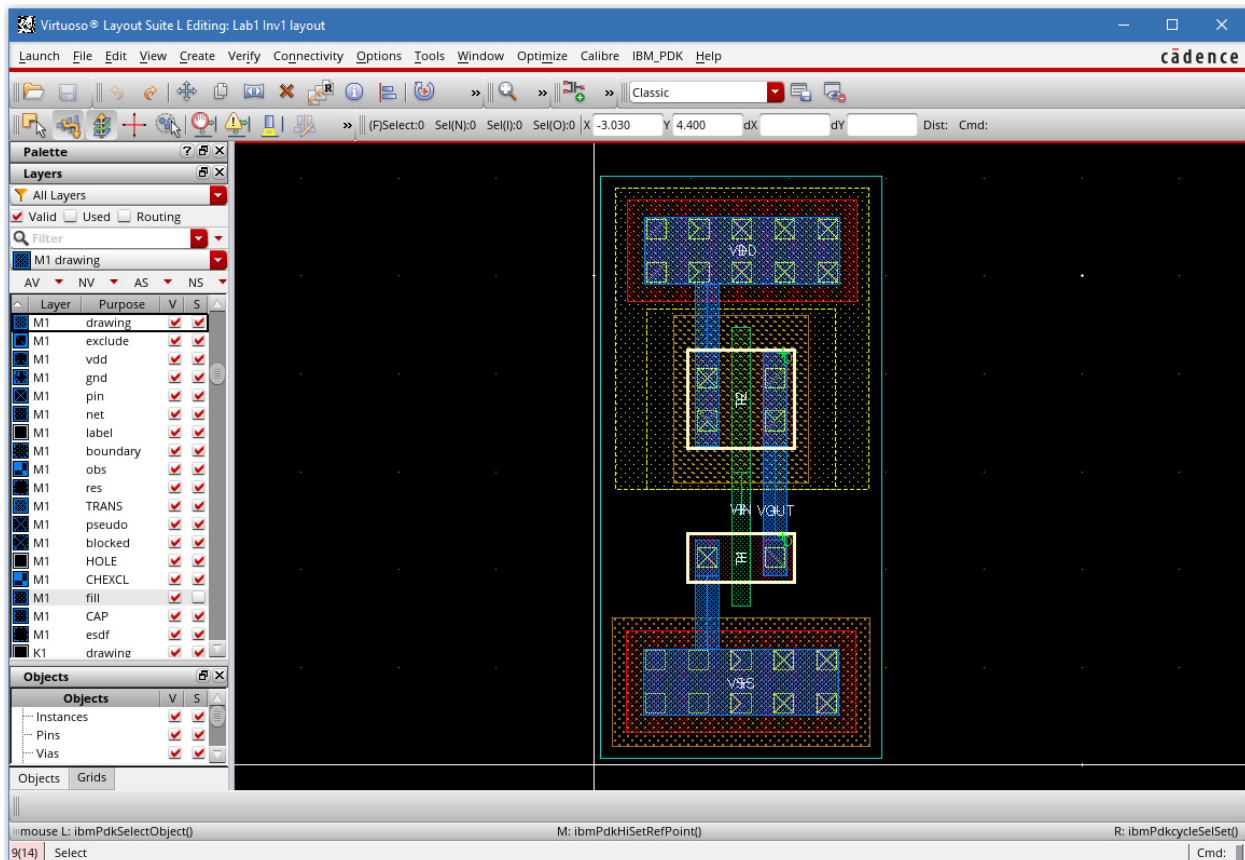


Figure 1-15: Inverter Layout

Post Layout Steps

To simulate the layout with parasitic elements included, the following post-layout steps must be completed:

1. Design Rule Check (DRC) should be run to check the physical layout data against any fabrication specific rules. Typical checks are for spacing, enclosure and overlap.
2. Layout Versus Schematic (LVS) check must be done to ensure the schematic net matches the layout net.
3. Device parameters from the layout need to be extracted by running PEX.

DRC

The first step is to run a clean DRC. DRCs should be run not just at the end of the layout construction, but during it as well. Go to *Calibre* → *Run DRC* at the popup window nothing needs to be changed so just click "Run DRC" and wait for the RVE window (Figure 1-16) to pop up (it is the third window to pop up in this process and it may take a while). Once the RVE window pops up you will see all the checks given, there are way too many to scroll through, so if you click the word "Results" on the left side of the RVE window you may filter the checks and errors. To have Cadence tell you where the error was detected, double click on the number shown to the right after highlighting the error. Run DRC until no errors appear (with the exception of density violations, which do not need to be corrected unless you plan on physically manufacturing your layout on a chip).

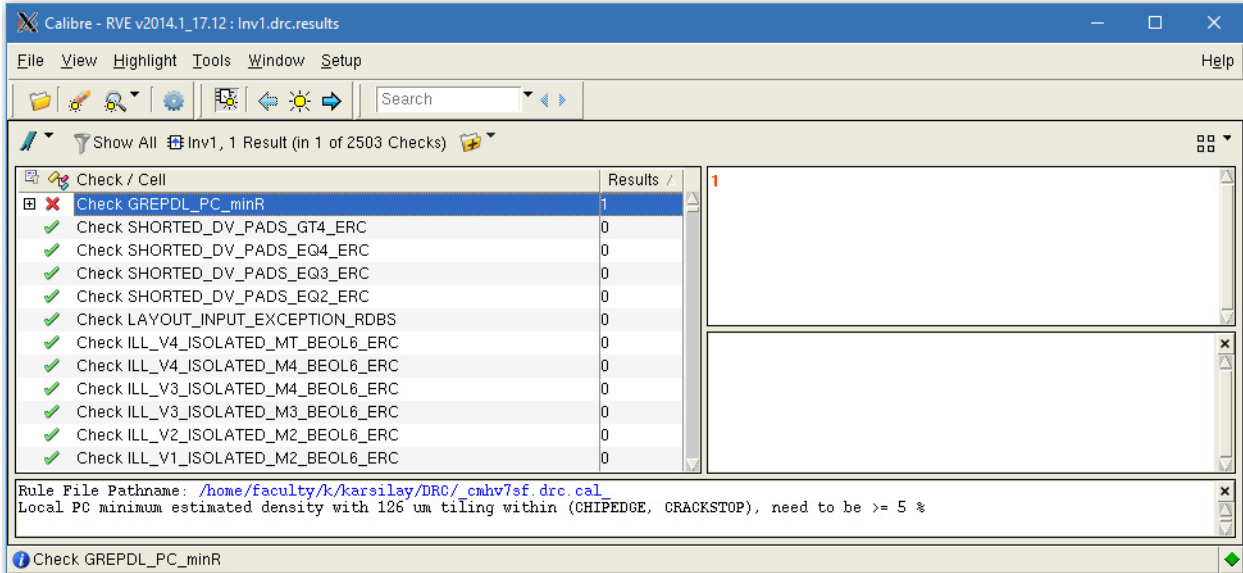


Figure 1-16: Calibre RVE Window Showing the DRC Results

LVS

From the schematic window, select *IBM_PDK*→*Netlist*→*Create CDL Netlist*. In the next window, type "~/LVS" for the "Run Directory", then click OK (see Figure). To confirm, you will receive "Analysis Job Succeeded" message. Next, select *IBM_PDK*→*Netlist*→*CDL pre_Process for LVS*. Change the "Run Directory" to "~/LVS" and click on "Refresh File List", then click to highlight the "Inv1.netlist" file and click the "<<" button to move it from the right column to the left column (Figure 1-17). Finally, click OK and the file "Inv1.netlist.lvs" will be generated.

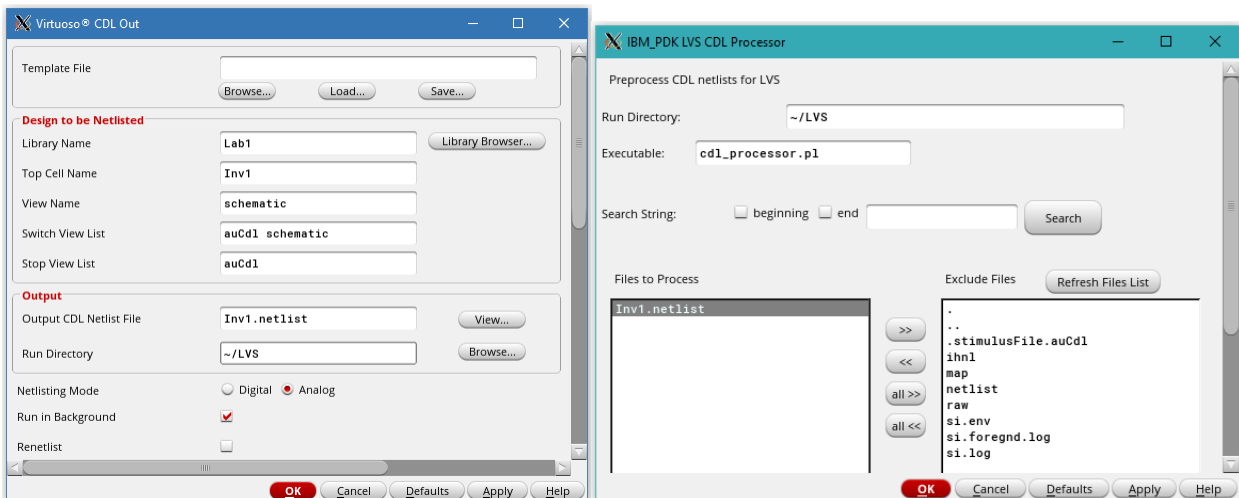


Figure 1-17: Netlist Generation from Schematic for LVS

Go back to the layout window and select *Calibre*→*Run LVS*. In the Calibre LVS window (Figure 1-18) click on the "Inputs" tab on the left side, then click on the "Netlist" tab. Make sure the "Export from schematic viewer" box has been unchecked. Next, find the "Inv1.netlist.lvs" file in "~/LVS" directory after clicking on the "..." button, then click on "Run LVS".

Two windows should pop up when LVS is complete, the one that you want to take a screen capture of is the window that shows your NetID and a time stamp (Figure 1-19). **No credit will be given if the LVS report is missing either the NetID or the time stamp.** If there are errors, select "Error Display" to find out what they are. Adjust the layout to match, rerun DRC and LVS until the netlists match.

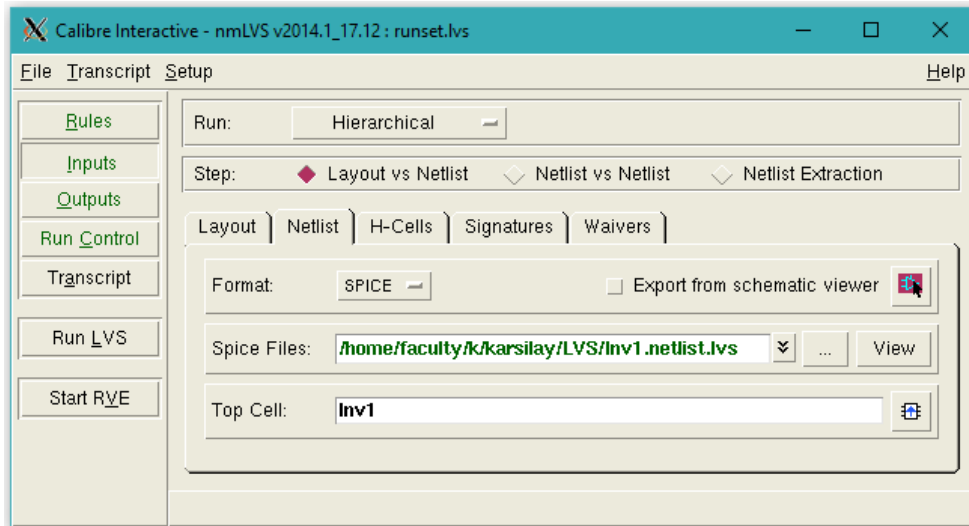


Figure 1-18: Calibre Interactive LVS Window

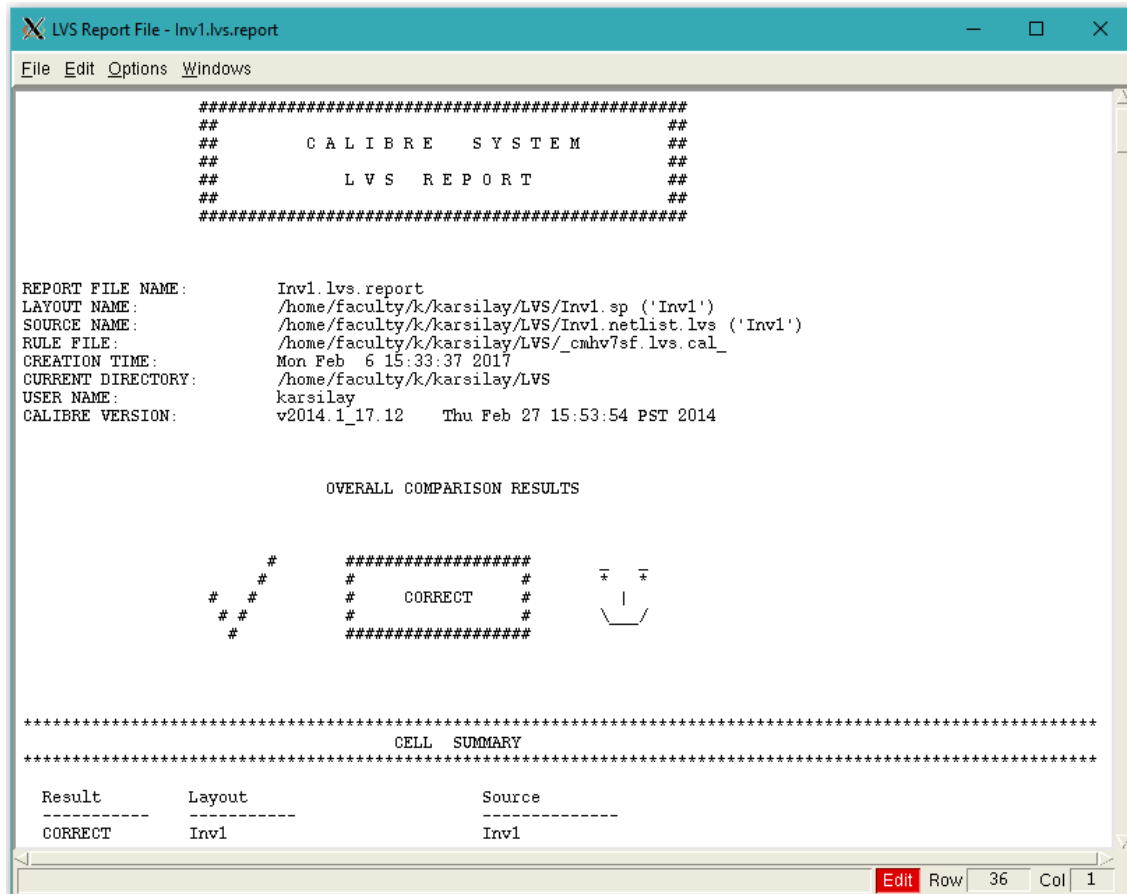


Figure 1-19: Calibre LVS Report Showing NetID and Time Stamp

PEX

Once DRC and LVS are successful, you can now extract the layout for post-layout simulation using PEX. From the layout window select *Calibre*→*Run PEX*. In the Calibre interactive PEX window, click on "Inputs" and then "Netlist", and find the "Inv1.netlist.lvs" file in ~/LVS directory after clicking on the "..." button (Figure 1-20), then click on "Run PEX".

In the middle of the extraction process, the Calibre View Setup window will pop up (Figure 1-21), just click OK to continue. PEX should run to completion, click "close" when the final window pops up with the number of errors and warnings.

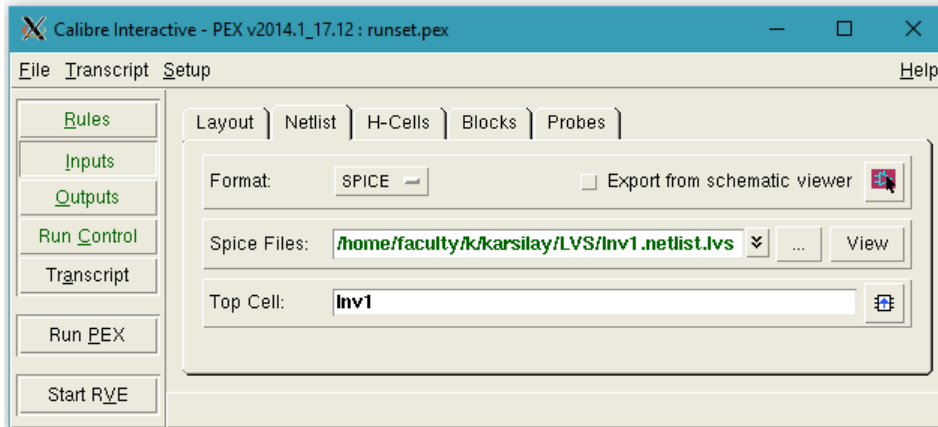


Figure 1-20: Calibre Interactive PEX Window

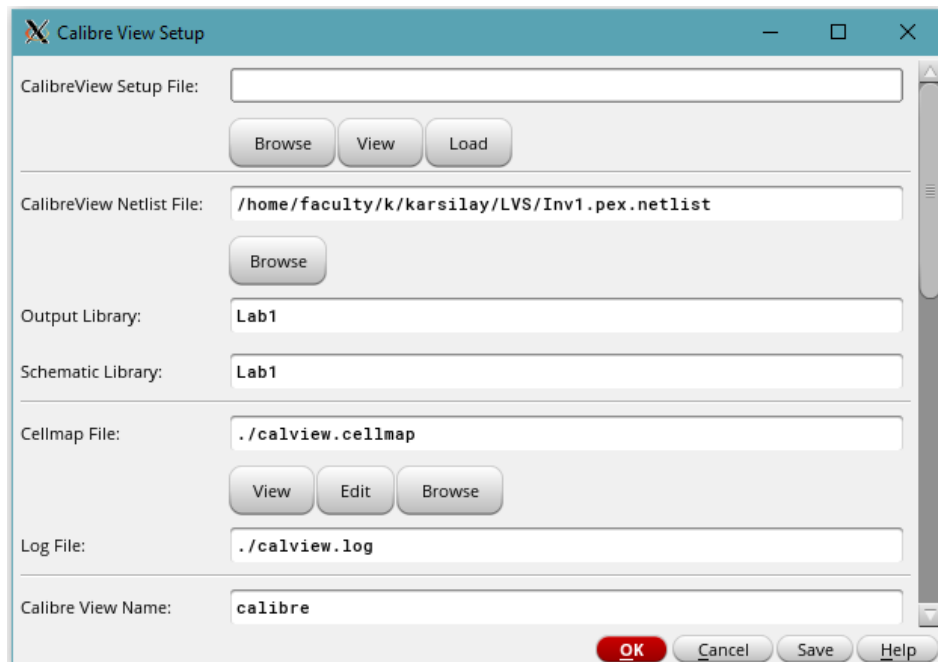


Figure 1-21: Calibre View Setup Window

Creating a Symbol

Creating a symbol is required for post-layout simulation, but may be done before the layout if you prefer using the symbol for schematic simulations as well. Going back to the schematic window, select *Create*→*Cellview*→*From Cellview* and click OK (Figure 1-22). In the next window arrange the pin specifications and click OK. Note that when listing pins from right to left they will appear from right to left on the top and bottom and when listed from right to left on the "Left Pins" and "Right Pins" fields they will appear from top to bottom in that order. Next, the symbol editor will appear with the default symbol, which is a box with inputs and outputs. Edit the symbol using the drawing tools such that it resembles the one in Figure 1-23. Finally, save and exit this window.

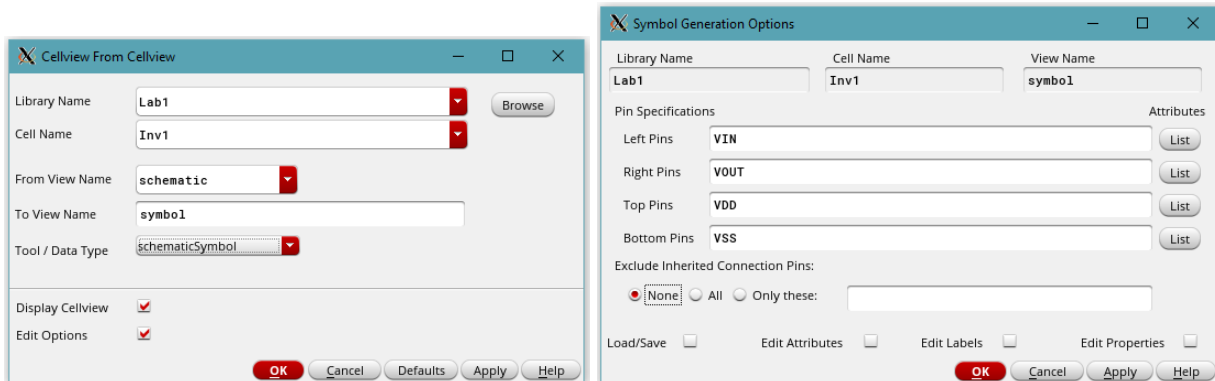


Figure 1-22: Creating a Symbol from a Schematic

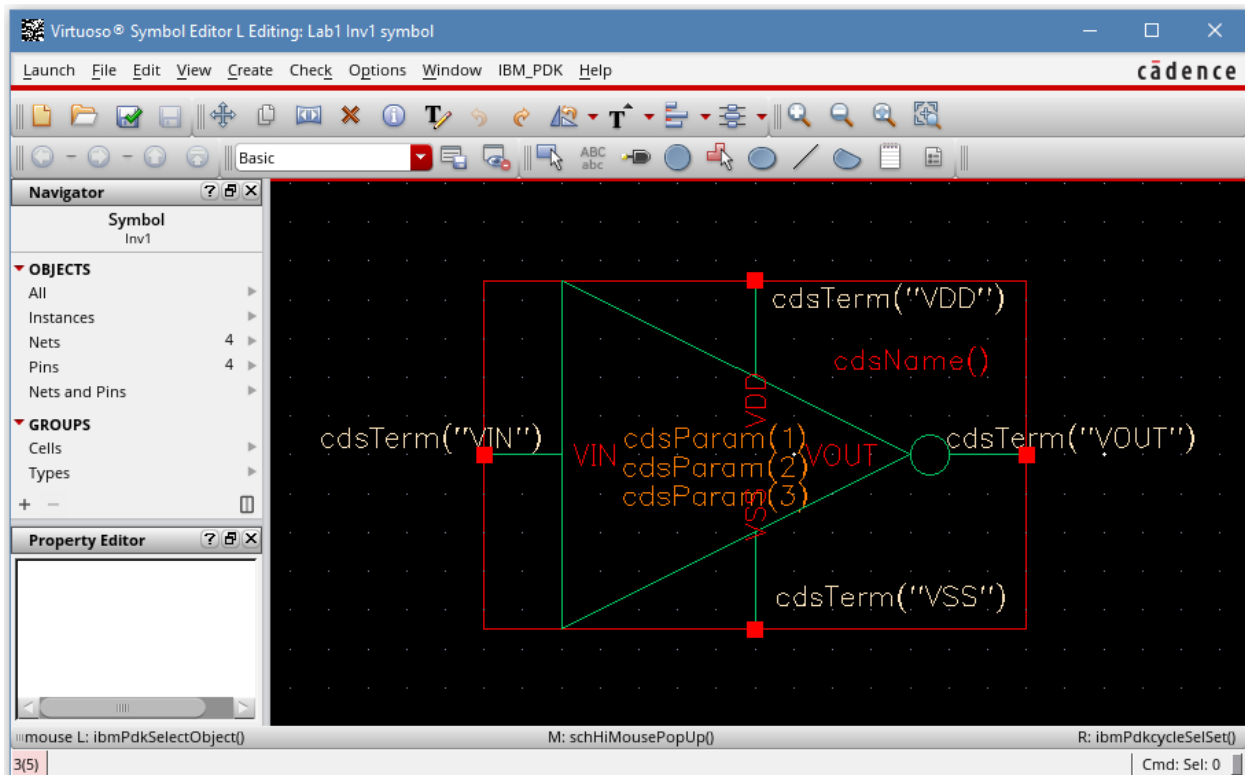


Figure 1-23: Final Inverter Symbol

Schematic and Post-Layout Simulation

To run simulations using the newly created symbol, we need to create a "test bench" or another schematic plane under the "Cell" field in the "Library Manager". To do this go to the "Library Manager" window and make sure that "Lab1" is highlighted. Next go to *File*→*New*→*Cell View* and title the new cell as "Inv1test" then click OK. A new schematic plane should pop up and when an instance is added (remember press "i") the symbol will appear under the "Inv1" cell when it is highlighted. Next create the configuration shown in Figure 1-24. Note the resistor has a value of 100k, and the values of the DC voltage sources should be 1.8V and "Vdc".

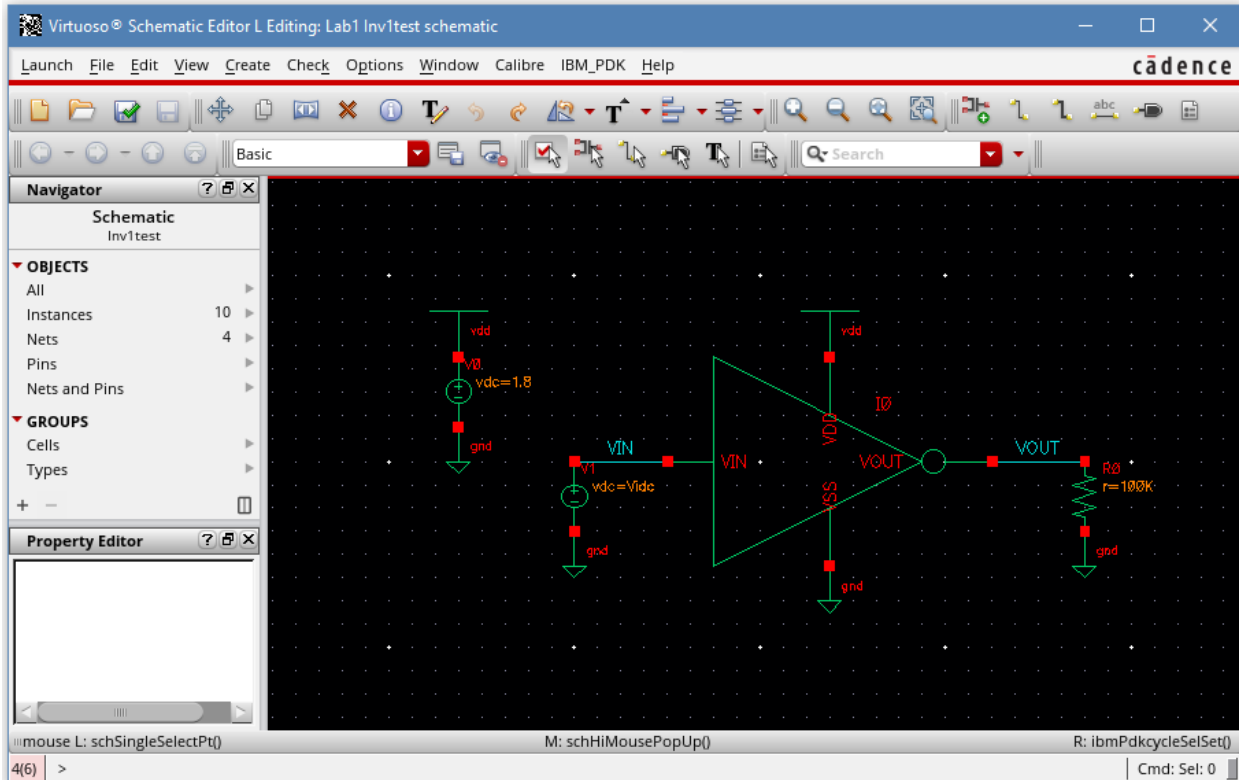


Figure 1-24: Inverter Test Bench Schematic

Next, start the simulator by *Launch*→*ADE L* and follow the steps previously given in the section "**Simulating a Schematic**". With the default setup, simulation will use the schematic (ideal components) instead of the layout (components with routing parasitics), so the simulation results should be identical to those obtained earlier (Figure 1-9).

To simulate the layout, go to *Setup*→*Environment* in the ADE L window and in the field labeled "Switch View List", add "calibre" between "cmos.sch" and "schematic" (see Figure 1-25), then click OK. Now, if you run the simulation, you will still obtain a plot that resembles Figure 1-9, but it may be slightly different due to added parasitics, and the fact that the extracted netlist from the layout will be different from the schematic netlist. If the "calibre" view of the cell is deleted or the Switch View List is modified back to its original, "schematic" view can still be used for simulation.

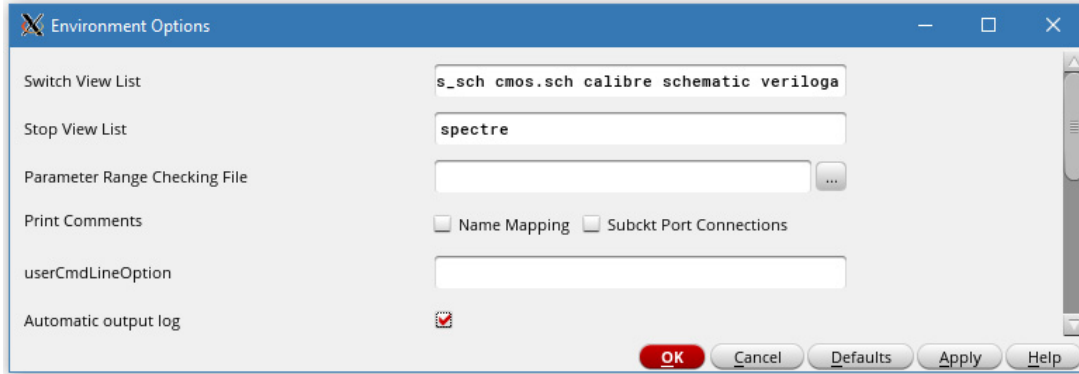


Figure 1-25: Switch View List in Environment Options

A Note about Locks and How to Remove Them

Locks may occur on schematics or layouts if Cadence crashes or the user terminates a session from the terminal window without properly saving all data or shutting down Cadence properly. If at any time the user encounters a lock on a schematic or layout the user will be unable to edit said schematic or layout. To remove locks, exit Cadence and issue the following commands:

```
cd ~/lab-ibm180  
/disk/amsc/bin/clearcdslck
```